Module – 2 FET and SCR

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2.1 Introduction

A *transistor* is a semiconductor device that controls current with the application of a small electrical signal. Transistors may be roughly grouped into two major families: *bipolar* and *field-effect*. BJT utilize a small current to control a large current. But, FET utilizing a small *voltage* to control current.

FETs are *unipolar* rather than *bipolar* devices. That is, the main current through them is comprised either of electrons through an N-type semiconductor (N-channel FET) or holes through a P-type semiconductor (P-channel FET). In a JFET, the controlled current passes from Source to Drain, or from Drain to Source as the case may be. The controlling voltage is applied between the Gate and Source. Current flowing through this channel widely depends on the input voltage applied to its Gate terminal.

FET can be made much smaller than an equivalent BJT transistor and along with their low power consumption and power dissipation makes them ideal for use in integrated circuits such as the CMOS range of digital logic chips.

The FET has one major advantage over BJT, in that their input impedance, (Rin) is very high, (kilo Ohms), while the BJT is comparatively low. This very high input impedance makes them very sensitive to input voltage signals, but the price of this high sensitivity also means that they can be easily damaged by static electricity.

FETs generally of two types :

1) JFET (Junction Field Effect Transistors) and
2) MOSFET (Metal Oxide Semiconductor Field Effect Transistors).

On a MOSFET, the metallic or poly silicon Gate is isolated from the channel by a thin layer of silicon dioxide (SiO_2). Some fundamental performance differences are there between MOSFETs and JFETS. JFETs, by nature, operate only in the depletion mode. That is, a reverse gate bias depletes, or pinches off the flow of channel current. A MOSFET, by virtue of its electrically-insulated gate, can be fabricated to perform as either a depletion mode or enhancement-mode FET.

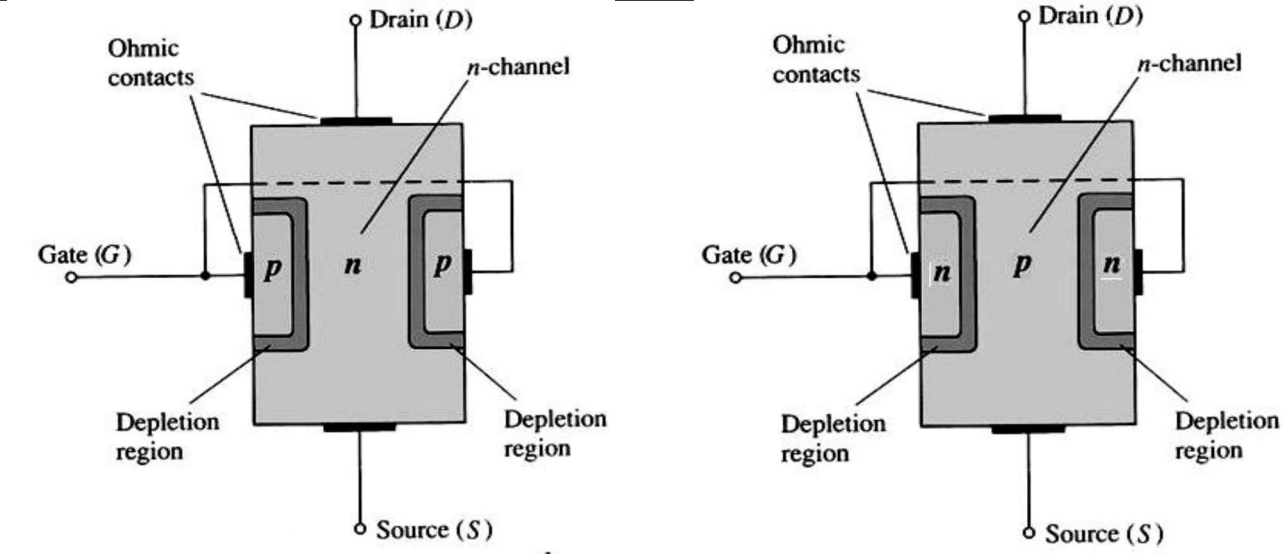
2.2 Junction Field Effect Transistor (JFET)

JFET is a voltage controlled three terminal uni-polar semiconductor device. The three terminals namely, Source (S), Gate (G) and Drain (D). As the voltage applied to the Gate with respect to the Source (V_{GS}), controls the current flowing between the Drain and the Source terminals. See fig.2.1.

JFETs can be classified into two types **(i)** n-channel JFET and (ii) p-channel JFET, depending on whether the current flow is due to electrons or holes, respectively.

Components of FET

1. **Channel:** This is the area in which majority charge carriers flow. When the majority charge carriers are entered in FET, then with the help of this channel only they flow from source to drain.
2. **Source:** Source is the terminal through which the majority charge carriers are introduced in the FET.
3. **Drain:** Drain is the collecting terminal in which the majority charge carriers enter and thus contribute in the conduction procedure.
4. **Gate:** Gate terminal is formed by diffusion of a type of semiconductor with another type of semiconductor. It basically creates high impurity region which controls the flow of carrier from source to drain.



(a) **(b)**

Fig. 2.1Constructional details of (a) N-channel JFET (b) P-channel JFET

Working of n-channel JFET

Case I: *No voltage is applied to the device (V_{DS} = 0 and V_{GS} = 0).*
At this state, the device will be idle and no current flows through it (I_{DS} = 0).

Case-II: *When V_{DS} is applied and V_{GS} = 0*
As shown in fig.2.2 (a), the two PN junctions at the sides of the N channel establish depletion layers. The electrons will flow from Source to Drain through a channel between the depletion layers.
The size of the depletion layers determines the width of the channel and hence current I_{DS}, conduction through the bar.

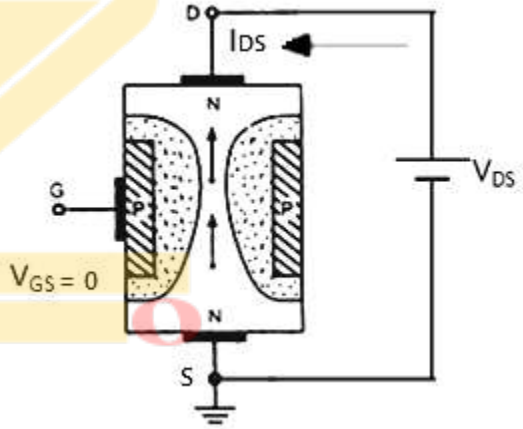


Fig.2.2(a)

Case-III: *When V_{DS} is applied and V_{GS} = - ve*
The depletion region width increases, which results in reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from Source to Drain is decreased.
If more ($-V_{GS}$) is applied, further reduces the channel width until no current flows through the channel. At this condition the JFET is said to be "pinched-off". The applied voltage at which the JFET channel is called as *pinched-off voltage*, V_P. At this state, the I_{DS} current is restricted only by the channel-resistance. However, once the pinch-off occurs ($V_{DS} = V_P$), the current I_{DS} saturates at a particular level I_{DSS}.

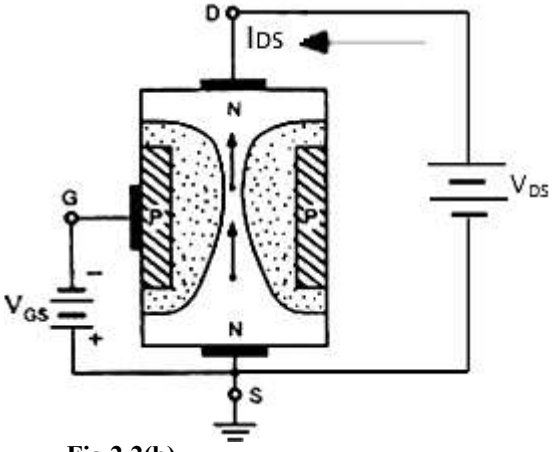


Fig.2.2(b)

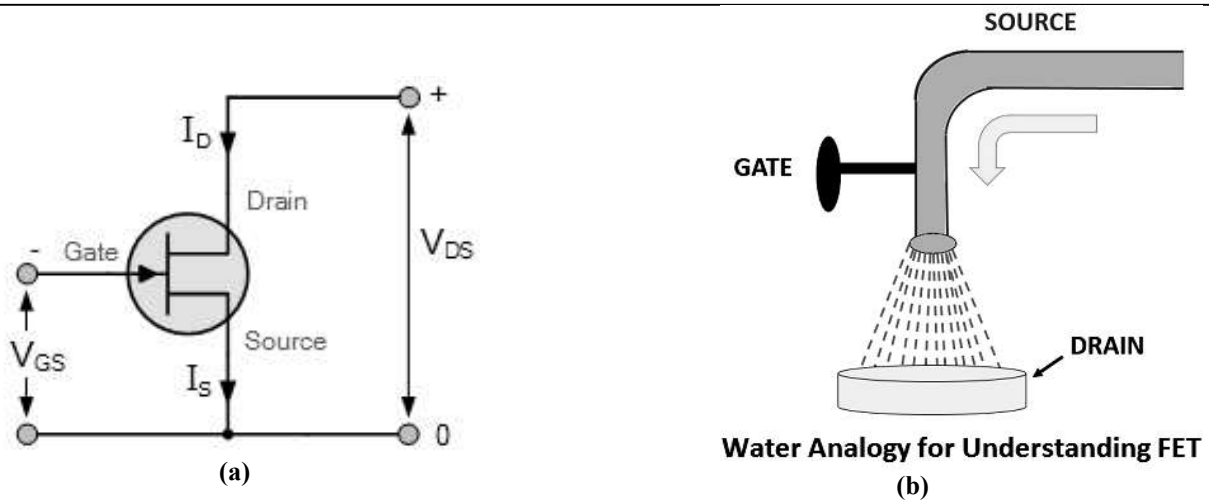


Fig. 2.3. circuit diagram of (a) N-channel JFET (b) water analogy for understanding the FET working principle

2.3 Output characteristic (Drain) V-I curves of JFET

The characteristics curves of a JFET shown in the fig.2.4, reveals four different regions of operation are given as:

- *Ohmic Region* – When V_{GS} = 0 the depletion region of the channel is very small and the JFET acts like a voltage controlled resistor.
- *Cut-off Region* – This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- *Saturation or Active Region* – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.
- *Breakdown Region* – The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to break down and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current I_D decreases with an increasing positive Gate-Source voltage, V_{GS}.

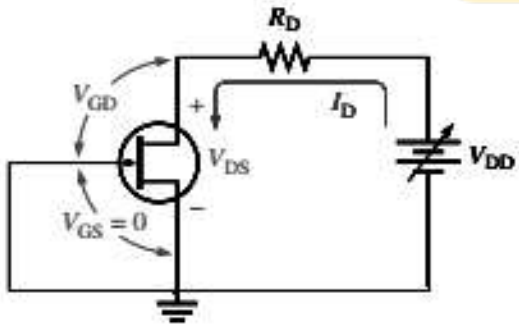
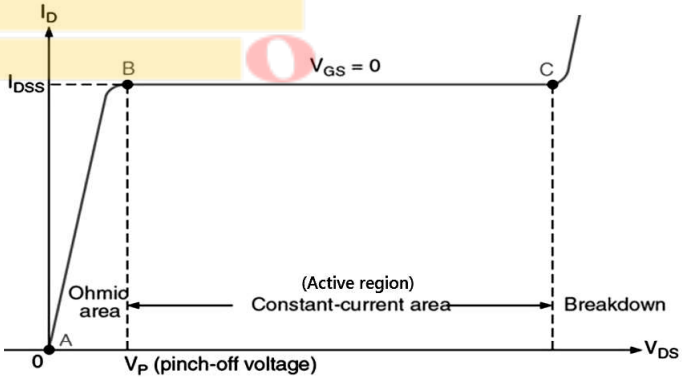


Fig.2.4 (a) JFET with *V*GS = 0 V and a variable V_{DS} (V_{DD})



(b) The drain characteristic curve for *V*GS = 0 showing pinch-off voltage.

The Drain current I_{DS} is zero when $V_{GS} = V_P$. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. Then we can calculate the Drain current, I_D for any given bias point in the saturation or active region as follows:

1. Drain current in the active region

Drain current (I_D) at the active region can be calculated as follows: I_D lies between (pinch-off) zero to I_{DSS}.

$$I_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2$$

2. Drain-Source channel resistance (R_{DS})

Similarly, if we know drain source voltage Vds and drain current Id, we can calculate the **drain-source channel resistance**.

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Where: g_m is the "trans-conductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the I_D with respect to the change in V_{GS}.

3. Amplification factor (μ)

It is given by

$$\mu = \frac{\text{change in } V_{DS}}{\text{change in } V_{GS}} \text{ at } I_D \text{ constant}$$

Relation among JFET parameters

It can be proved from above that $\mu = R_{DS} * g_m$

$$\mu = \left(\frac{\Delta V_{DS}}{\Delta I_D}\right) * \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) = \frac{\Delta V_{DS}}{\Delta V_{GS}} = R_{DS} * g_m$$

Inference:

1. As the gate to source voltage (**V_{GS}**) is increased above zero, pinch off voltage is increased at a smaller value of drain current as compared to that when **V_{GS} = 0V**.
2. The value of drain to source voltage (**V_{DS}**) is decreased as compared to that when **V_{GS} = 0V**.

Salient Features of JFET

1. A JFET is a three-terminal voltage-controlled semiconductor device.
2. JFET is always operated with gate-source PN junction reverse biased.
3. In a JFET, the gate current is zero i.e. $I_G = 0$.
4. Since there is no gate current, $I_D = I_S$.
5. JFET must be operated between V_{GS} and $V_{GS\,(off)}$. For this range of Gate-to-Source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.
6. Because the two gates are at the same potential, both depletion layers widen or narrow down by an equal amount.
7. JFET is not subjected to thermal runaway when the temperature of the device increases.
8. The drain current I_D is controlled by changing the channel width.

2.4 Transfer characteristics

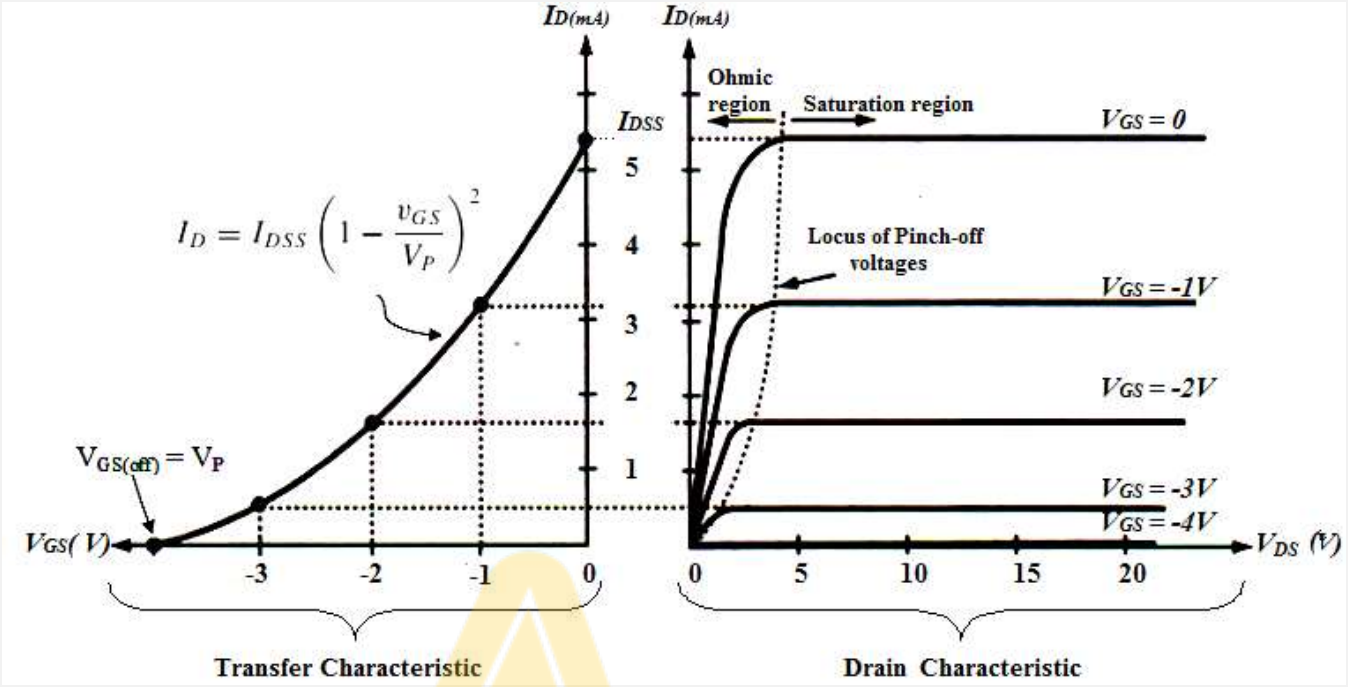


Fig.2.5 Characteristics of JFET

The transfer characteristics can be determined by observing different values of I_D with variation in V_{GS} provided that the V_{DS} should be constant as shown in the fig.2.5.

Notice that the bottom end of the *transfer characteristic* curve is at a point on the V_{GS} axis equal to V_{GS}(off), and the top end of the curve is at a point on the I_D axis equal to I_{DSS}.

This curve shows that

i) $\boldsymbol{I_D = 0}$; when $\boldsymbol{V_{GS} = V_{GS}(off)}$

ii) $\boldsymbol{I_D = I_{DSS}}$ when $\boldsymbol{V_{GS} = 0}$

iii) The transfer characteristic curve is expressed approximately as

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Hence, JFETs are often referred to as *square-law devices.*

Applications of JFET

- constant current source, buffer amplifier, electronic switch, phase shift oscillator, voltage variable resistor (VVR) and chopper.

Comparision between BJT and JFET

BJT	JFET
Bipolar device	*Uni junction transistor*
Input impedance is very less	Input impedance is very large
Current control device, preferred for low current applications	Voltage controlled device, preferred for low voltage applications
More noisy	Less noisy

Frequency variations effect its performance	High frequency response
Temperature dependent device	Better heat stability
Cheaper than FET	Costly than BJT
Bigger in size than FET	Smaller in size than BJT
More gain	Less gain
High output impedance because of high gain	Low output impedance because of less gain
High voltage gain	Low voltage gain
Low current gain	High current gain
Switching time is medium	Switching time is fast
Consumes more power	Consumes less power

2.5 Metal Oxide Semiconductor Field-Effect Transistor (MOSFET)

The MOSFET, different from the JFET, has no *pn* junction structure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO2) layer shown in the fig.2.6. The MOSFET is widely used for switching and amplifying electronic signals. Also, it is a core of ICs and it can be designed and fabricated in a single chip because of smaller silicon chip area.

The two basic types of MOSFETs

1. Enhancement MOSFET (E-MOSFET) and
2. Depletion MOSFET (D-MOSFET). Of the two types, the enhancement MOSFET is more widely used.

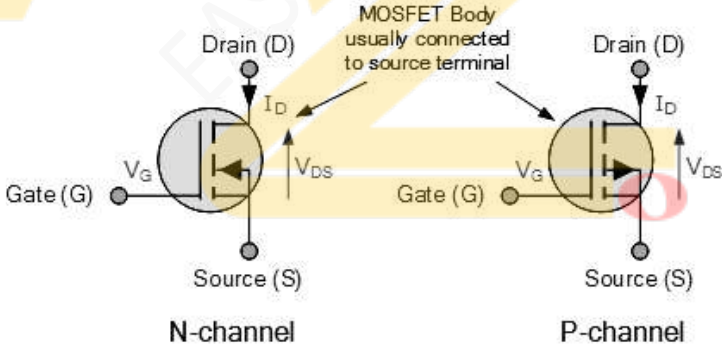


Fig.2.6 MOSFET circuit symbols

2.5.1 Depletion Mode

The depletion mode MOSFETs are generally ON at (V_{GS} = 0V). The conductivity of the channel in depletion MOSFETs is less compared to the enhancement type of MOSFETs. See fig. 2.7.

Case I: When there is no Gate voltage (V_{GS} = 0), as in fig. 2.7, maximum current flows ($I_D = I_S = I_{DSS}$).

Case II: When V_{GS} = -ve with respect to the substrate, the Gate repels some of the electrons out of the N-channel. This creates a *depletion region* in the channel, as illustrated in fig.2.8, and, therefore, increases the channel resistance and reduces the Drain current, I_D. The more negative the gate, the less the Drain current. In this mode of operation the device is referred to as a *depletion-mode MOSFET.* Here too much negative Gate voltage can pinch-off the channel.

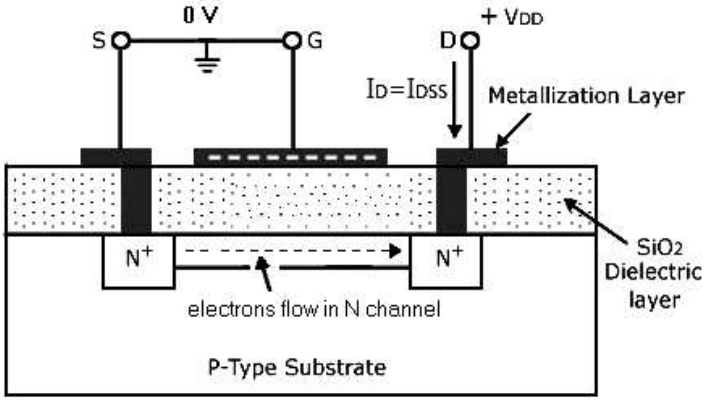


Fig.2.7 MOSFET in depletion mode with gate voltage zero

Case II: When V_{GS} = -ve with respect to the substrate, the Gate repels some of the electrons out of the N-channel. This creates a *depletion region* in the channel, as illustrated in fig.2.8, and, therefore, increases the channel resistance and reduces the Drain current, I_D. The more negative the gate, the less the Drain current. In this mode of operation the device is referred to as a *depletion-mode MOSFET.* Here too much negative Gate voltage can pinch-off the channel. Then device is said to be OFF.

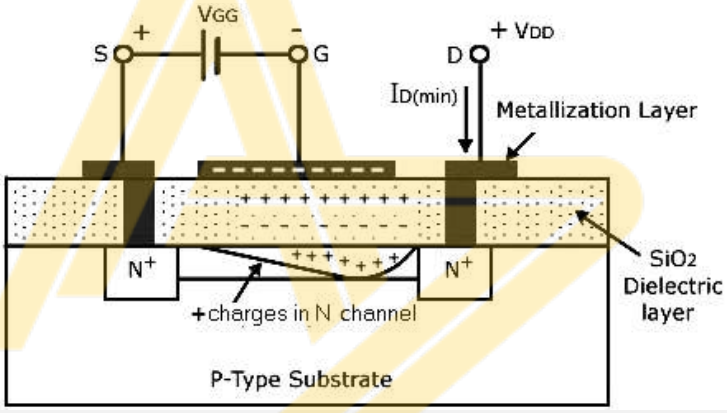


Fig.2.8 MOSFET in depletion mode with gate voltage negative

Case III: When V_{GS} = +ve, Gate attracts the negative charge carriers from the P-substrate to the N-channel and thus reduces the channel resistance and increases the drain current, I_D. The more positive the Gate is made, the more Drain current flows. In this mode of operation the device is referred to as a *enhancement-mode MOSFET.* This is depicted in the fig. 2.9.

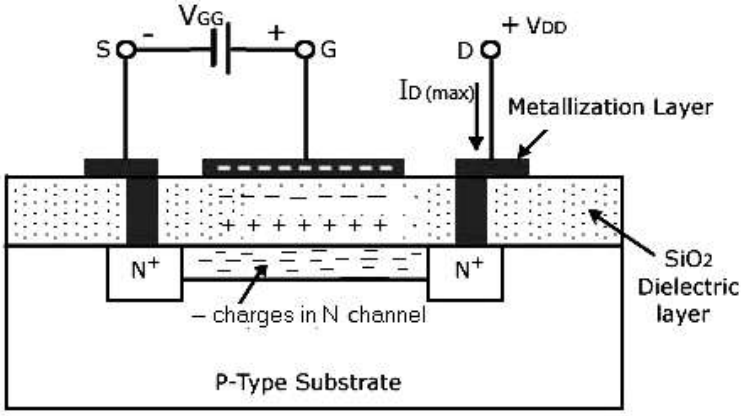


Fig.2.9 MOSFET in depletion mode with gate voltage positive

Transfer and Drain characteristic of depletion MOSFET is shown in the fig.2.10.

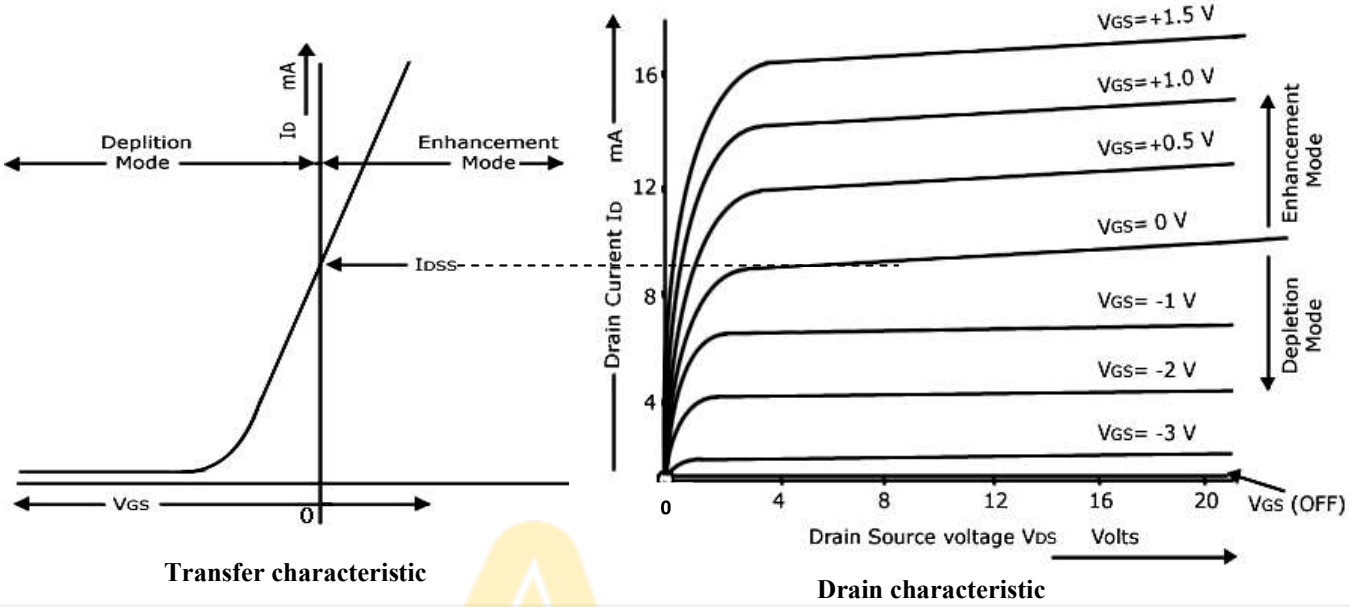


Fig. 2.10 Transfer characteristic and Drain characteristic of depletion MOSFET

2.5.2 Enhancement mode

The construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of an N-channel between the drain and source terminals.
The minimum value of V_{GS} is required to form the induced N-channel, that turns the E-MOSFET ON is called threshold voltage [$V_{GS\,(th)}$]. For V_{GS} below $V_{GS\,(th)}$, the drain current $I_D = 0$.

(i) **When V_{GS} = 0 V, V_{DS} = +ve :** There is no channel induced between Source and Drain. The p-substrate has only a few thermally produced free electrons (minority carriers) so that drain current is almost zero. For this reason, E-MOSFET is normally OFF when $V_{GS} = 0V$.

(ii) **When $V_{GS} = V_{GS(th)} = +$ ve**, and **$V_{DS} = +$ ve:** The free electrons developed next to the SiO_2 layer and induced an N channel, as shown in the fig.2.11. Now a Drain current I_D starts flowing. E-MOSFET is turned ON. Beyond $V_{GS\,(th)}$, if the value of V_{GS} is increased, the induced N channel becomes wider, resulting large I_D. If the value of V_{GS} decreases not less than $V_{GS\,(th)}$, the channel becomes narrower and I_D will decrease.

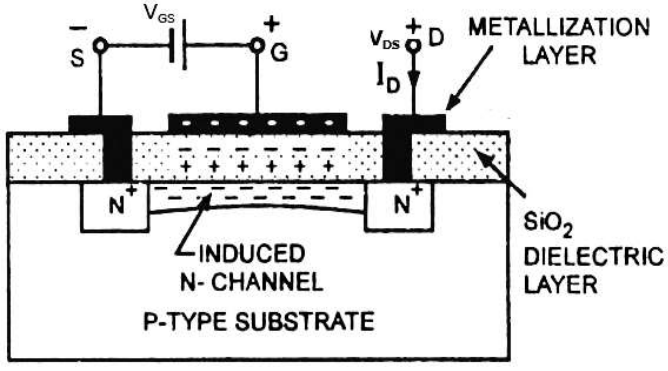


Fig. 2.11 MOSFET in enhancement mode with gate voltage positive

Since the conductivity of the channel is enhanced by the *positive bias* on the Gate, so this device is also called the *enhancement MOSFET* or E- MOSFET.

2.6 Characteristics of E-MOSFET

Drain characteristic curves: (shown in the fig.2.12 (b)), have almost vertical and almost horizontal parts. The vertical components of the curves correspond to the *ohmic region*, and the horizontal components correspond to the *saturation region* (constant current). Note the following worthy points:

- I_D depends on different values of V_{GS} (from 0V to + $V_{GS\,(max)}$).
- When $V_{GS} = 0$, even for large increase in V_{DS}, $I_D = 0$. This is said to be cut-off region. (MOSFET *off state*).

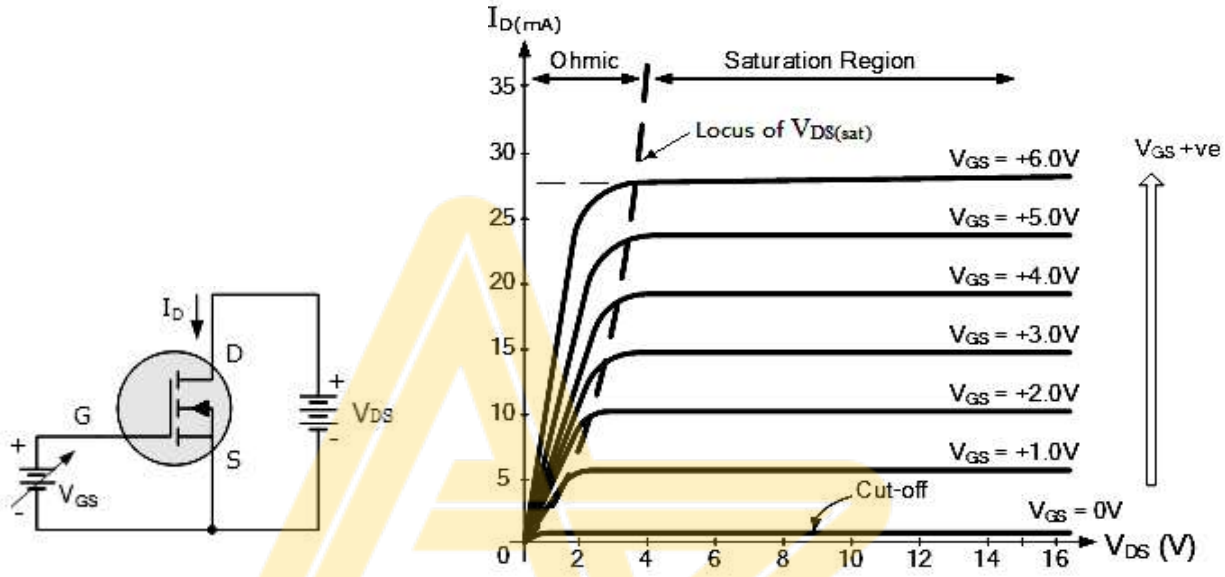


Fig. 2.12 (a) E – MOSFET circuit **(b) Drain characteristic of E - MOSFET**

Transfer Characteristic Curves

i) When $V_{GS} < V_{GS(th)}$, then $I_D = 0$. This is because under this state, the channel will not be connecting between the drain and the source terminals. This is called as *cut-off region*. (MOSFET off state). The tranfer curves of MOSFET is shown in the fig.2.13.

ii) When $V_{GS} > V_{GS(th)}$,. then I_D flows through the device, initially (Ohmic region) and then saturates to a value (*saturation region*). That means, I_D is controlled by the Gate voltage, V_{GS}.

iii) I_D can be obtained by analytical expression:

$$I_D = k\,(V_{GS} - V_{GS(th)})^2$$

where $$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \quad A/V^2$$

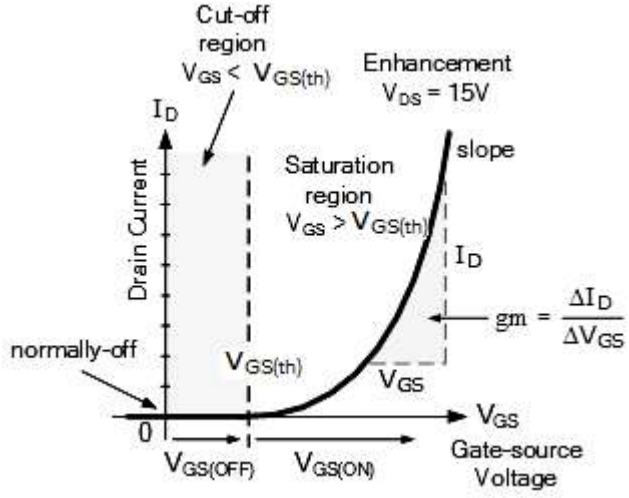


Fig.2.13 Transfer characteristic of E - MOSFET

2.8 CMOS Circuits

The CMOS circuit consists of a combination of P-type (PMOS) and N-type (NMOS) complementary MOSFETs. In NMOS, the majority carriers are electrons. When a high voltage is applied to the gate, ~~the~~ NMOS will conduct. Similarly, when a low voltage is applied to the gate, NMOS will not conduct.
In PMOS the majority carriers are holes. When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct.
Fig.2.14(a) and (b) illustrate the basic operation of CMOS inverter and it can be studied by using simple switch models.
NMOS source (S) is grounded. PMOS source (S) is connected to V_{DD} (= +5V)
PMOS and NMOS gates (G) are shorted and taken as input (V_{IN}).
PMOS and NMOS drain (D) are shorted and taken as output (V_{out}).

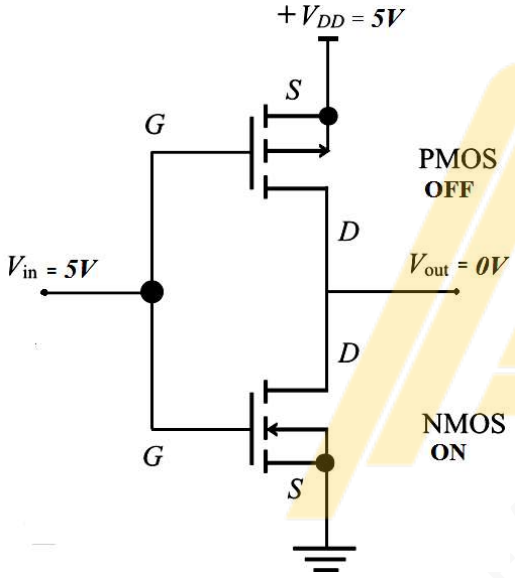
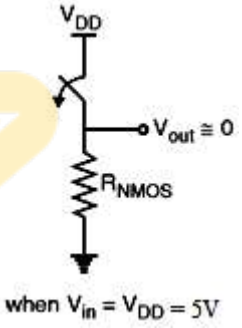


Fig.2.14(a) Circuit for input logic 1

i) When *Vin* = V_{DD} = 5V (Logic - 1):

NMOS transistor is ON, while the PMOS is OFF.
A direct path exists between *Vout* and the ground node, resulting in *Vout* = 0 V.
This yields the equivalent circuit shown below.



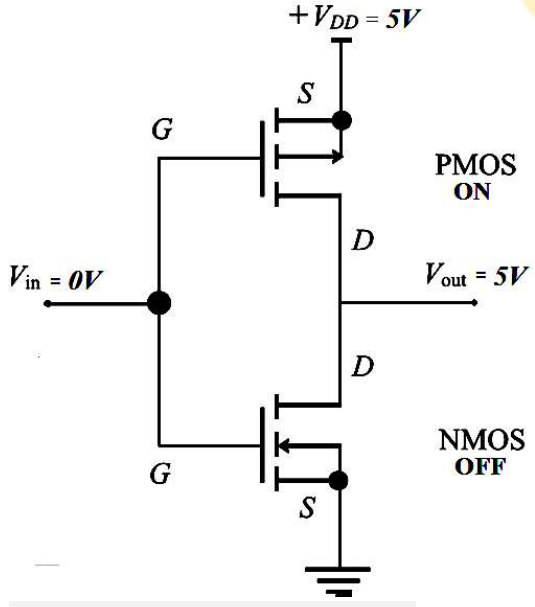
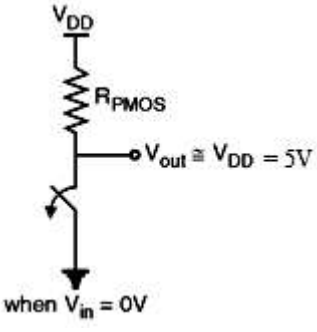


Fig.2.14 (b) Circuit for input logic 0

ii) When *Vin* = 0V, (Logic - 0) V_{DD} = 5V:

PMOS transistor is ON, while the NMOS is OFF.
A direct path exists between V_{DD} and the *Vout*, resulting in *Vout* = 5 V.
This yields the equivalent circuit shown below.



CMOS Functional Table

V_{in}	PMOS	NMOS	V_{out}
V_{DD} = 5V (logic 1)	OFF	NO	0V (logic 0)
0V (logic 0)	ON	OFF	V_{DD} = 5V (logic 1)

CMOS Advantages

High switching speed (50ns),
Low power dissipation (2.5nW),
Occupies lower packing density in IC fabrication,

CMOS Applications

Computer memories, CPUs
Microprocessor designs
Flash memory chip designing
To design application specific integrated circuits (ASICs). Ex: ALU circuits, Microcontrollers, etc.

2.9 Silicon Controlled Rectifier (SCR)

An SCR is a 4-layer *PNPN* with three terminals: Anode, Cathode, and Gate. The upper *PNP* layers act as a transistor T_1, and the lower *NPN* layers act as a transistor T_2.
The schematic symbol and basic structure of an SCR is shown in Fig.2.15.

CASE-1: Gate current is zero or the Gate terminal is open

i) When the Anode voltage is positive with respect to the Cathode, junctions J_1 and J_3 are forward biased and J_2 is reverse biased. The device offers high resistance. Hence, only a small leakage current (I_{CO}) flows from Anode to Cathode. Then the Anode current is $I_A = I_{CO}$. SCR is said to be in ***OFF state***.
ii) If Anode to Cathode voltage V_{AK} is increased to a sufficiently large value, the reverse biased junction J_2 will break. This is known as *avalanche breakdown* and corresponding voltage is called as *forward break over voltage* V_{BO}. Since J_1 and J_3 are already in forward biased, resulting in large forward current. The device is in ***ON state***. In this state I_A is limited by an external resistance R.
iii) When Cathode voltage is larger than Anode voltage J_1 and J_3 are reverse biased and J_2 will be forward biased. So, SCR will be in OFF state and only leakage current flows.

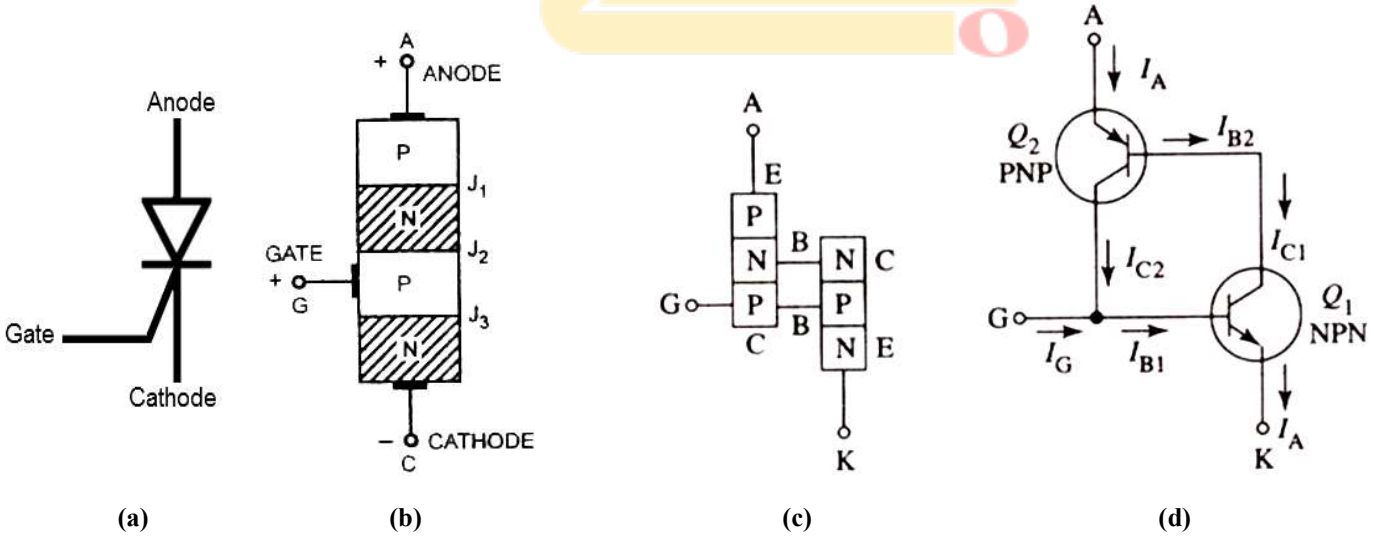


Fig. 2.15 SCR (a) Symbol (b) Basic Layout (c) Cross-sectional view and (d) Two transistor Model

CASE-2: Transistor Logic: When positive current pulse is applied to the Gate: *Switching Action*

The two transistor equivalent circuit shows (see fig. 2.15 (d)) that the collector current I_{C1} of the NPN transistor Q_1 feeds directly into the base I_{B2} of the PNP transistor Q_2, while the collector current I_{C2} of Q_2 feeds into the base $I_{B1}$of Q_1. In this case both transistors Q_1 and Q_2 turn ON (the Anode must be more positive than the Cathode).

When a sufficient positive pulse is applied to the Gate, at first, I_{B1} turns on Q_1, providing a conduction path for Q_2 via I_{B2}, thus turning on Q_2. The collector current I_{C2} of Q_2 provides an additional base current for Q_1 so that Q_1 stays in conduction even after the Gate pulse is removed. This regenerative action continues until both, Q_1 and Q_2 drive into saturation – acts like *closed switch* between Anode and Cathode. In this case, I_A is limited by an external resistance R.

Turning OFF SCR (commutation)

The turn OFF process of an SCR is called commutation. The term commutation means the transfer of currents from one path to another. So the commutation circuit does this job by reducing the forward current to zero so as to turn OFF the SCR.

To turn OFF the conducting SCR the below conditions must be satisfied.

- The anode or forward current of SCR must be reduced to zero or below the level of holding current,
- A sufficient reverse voltage must be applied across the SCR to regain its forward blocking state.

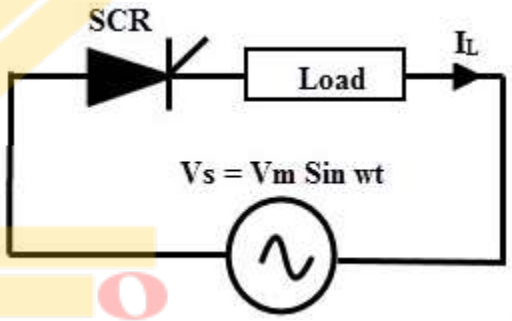
Types of Commutation:

1) Natural commutation and 2) Forced commutation

1. Natural Commutation

In AC circuit, the current always passes through zero for every half cycle. (Analyze one AC cycle).

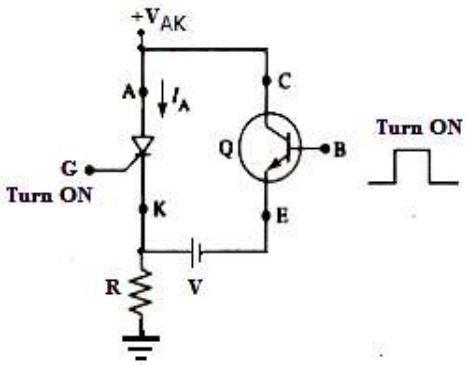
If the SCR is connected to an AC supply V_s, as shown in the fig. SCR turns off when negative voltage appears across it. This process is called as *natural commutation*, since no external circuit is required for this purpose.



2. Forced Commutation

In case of DC circuits, there is no natural current zero to turn OFF the SCR. In such circuits, forward current or Anode current must be forced to zero to turn OFF the SCR, with an external circuit. Hence, named as *forced commutation*.

This commutation circuit consist a transistor, Q and a DC supply (V) connecting in series to the SCR as shown in the fig. When SCR is ON, transistor is made OFF. To turn OFF the SCR, a + ve pulse is applied to the Base of transistor to drive it into saturation. Now, transistor acts like a closed switch. When $I_A < I_H$, SCR turns OFF. Transistor is *held ON* just long enough to turn OFF the SCR. *Turn-off time* of an SCR is typically 5 - 30μs.



V-I Characteristics of SCR

The typical VI characteristic of SCR is as shown in the fig.2.16. The three basic modes of operation of SCR are:

1. Forward Blocking mode, 2. Forward conduction mode and 3. Reverse Blocking mode

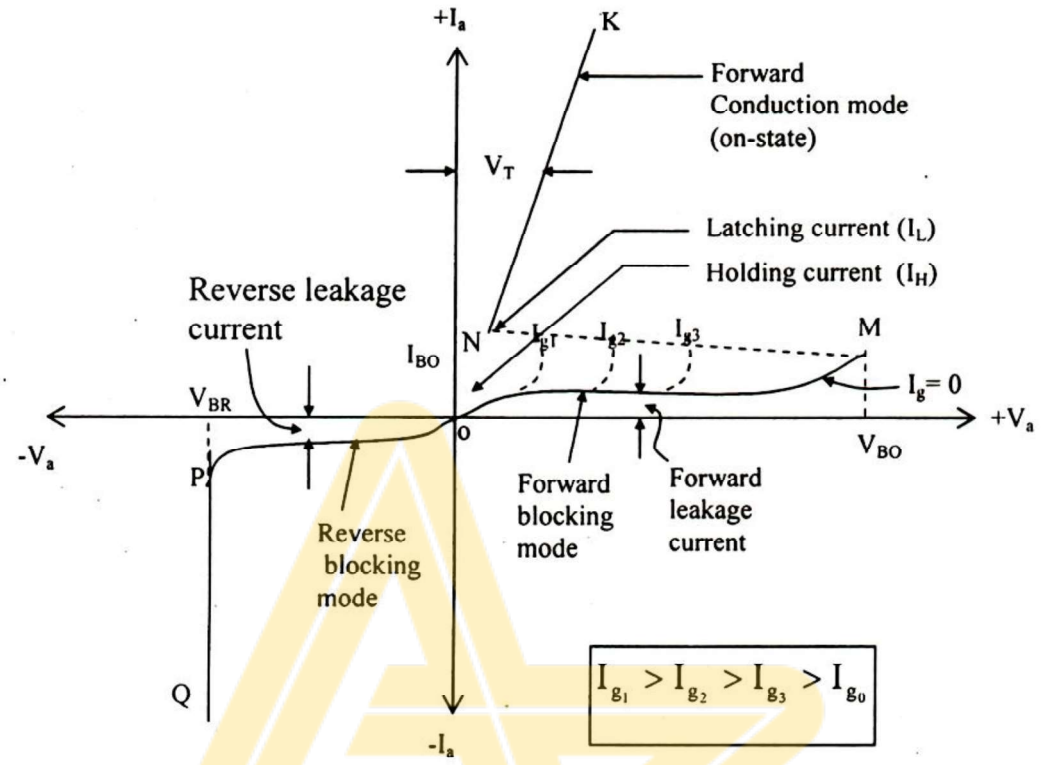


Fig. 2.16 VI Characteristics of SCR

1. Forward Blocking mode:

- When Anode is at a higher potential than Cathode, SCR is said to be forward biased,
- In this mode, a small current called *forward leakage current* flows from Anode to Cathode.
- From the graph, OM represents the forward blocking mode.
- SCR is treated as an open switch in the forward blocking mode.

2. Forward Conduction mode:

- When Anode to Cathode forward voltage is increased with Gate circuit open, reverse biased junction J_2 will breakdown at a voltage called *forward break over voltage,* V_{BO}.
- After this breakdown, SCR gets turned ON with point 'M' at once shifting to N. Here, NK represents the forward conduction mode.

Latching Current (I_H): It is the minimum value of Anode current required to keep SCR in conducting state even after removal of Gate pulse.

Holding Current (I_L): It is defined as the minimum value of Anode current below which the SCR gets turned off. $I_L > I_H$.

3. Reverse Blocking mode:

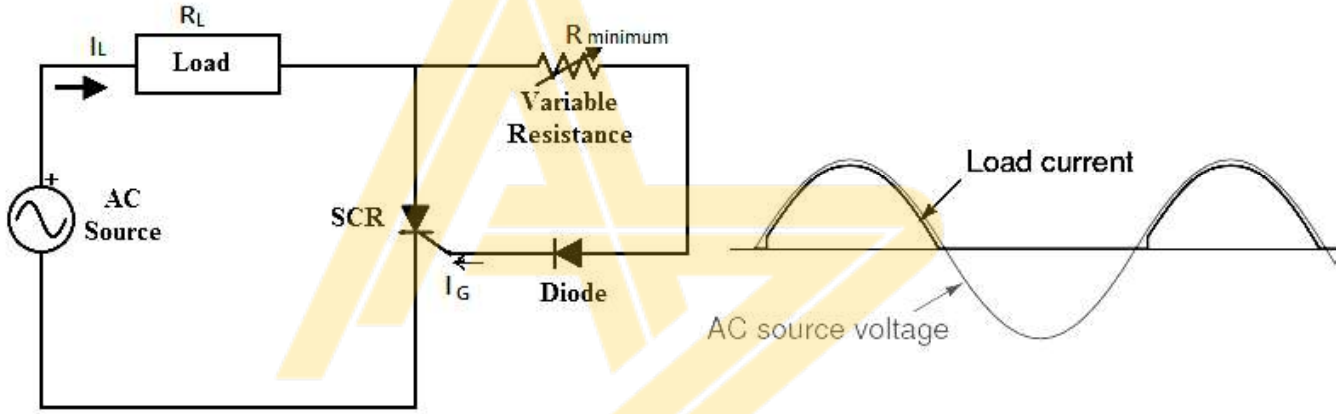
- When Cathode is made high potential with respect to Anode with Gate open, then the SCR is said to be reverse biased.
- J_1 and J_3 are reverse biased and J_2 is forward biased.
- A small current flow through the SCR, called as *reverse leakage current*.

- If the reverse voltage increased, then at reverse breakdown voltage V_{BR}, an avalanche breakdown occurs at J1 and J3 and the reverse current increases rapidly (see in the graph points PQ).
- The SCR in the reverse blocking mode may therefore be treated as (OFF) an *open switch*.

2.10 Phase Control Application of SCR

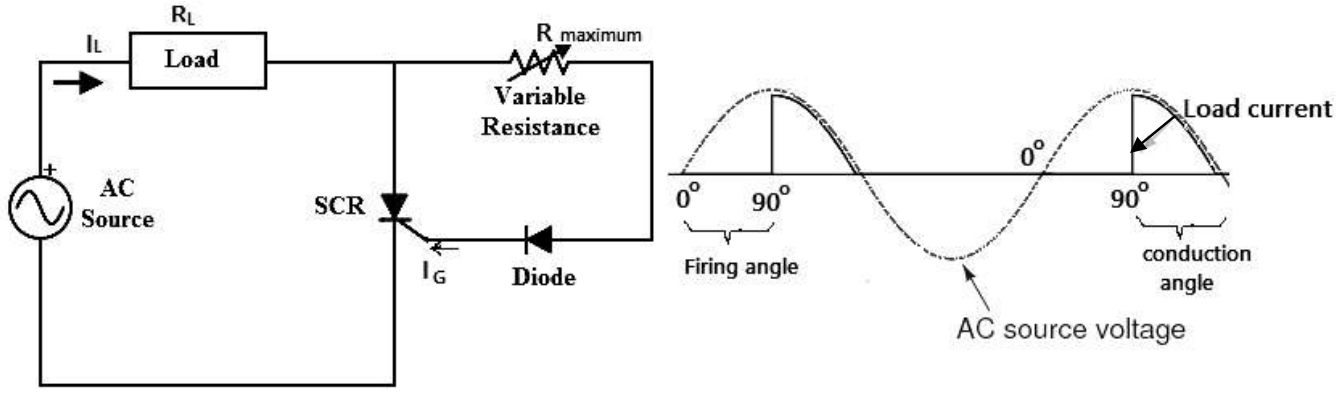
SCR is turned ON by applying a short pulse to the Gate at any angle is called firing angle (α). When load power is controlled by varying firing angle is known as phase control. The fig.2.17 shows the single phase half wave phase control circuit using SCR. A diode D in series with the variable resistor R is connected to the gate which prevents reverse bias being applied to the Gate.

- During the negative half cycle of the AC input signal, SCR is reverse biased and does not conduct. Hence, no current flows through the load R_L.
- During the positive half cycle of the AC input, SCR is forward biased. But for $I_G = 0$ (i.e, absence of Gate signal), SCR remains OFF.
- I_G is derived from AC supply and it is controlled by the variable resistance R. If the resistance R is set to minimum value, triggering current is applied to the gate, then immediately at the beginning of positive half cycle of input voltage the SCR is turned ON (see fig.2.17(a)). Hence the current starts flowing to the load R_L.



2.17 (a) Fig. Phase control circuit for R minimum

- If the resistance R is set to maximum value, the SCR will not turned ON until the peak value of positive half cycle of the input voltage is reached. (see fig.2.17(b)).



2.17 (a) Fig. Phase control circuit for R minimum

- For this rectifier circuit, firing angle can be varied during the positive half cycle only.

- Therefore, by varying the firing angle or gate current (by changing the resistance R value), it is possible to make the SCR conduct part or full positive half cycle so that the average power fed to the load get varied.
- That means, increasing the resistance R, causing less power to be delivered to the load R_L. Decreasing the resistance R, causing more power to be delivered to the load R_L.

Exercise

1. Draw the structure of JFET and discuss its working.
2. What is 'pinch off' voltage? How to get its value experimentally?
3. An n-JFET is operated with negative gate voltage and not with positive one. Give reasons.
4. Give the structure of depletion MOSFET (D - MOSFET). How is D - MOSFET different from enhancement MOSFET (E - MOSFET)?
5. Draw and discuss drain characteristics for a D-MOSFET.
6. Discuss the formation of channel in E-MOSFET emphasizing the role of inversion layer.
7. How are D-MOSFET and E-MOSFET connected in a circuit to work as resistors?
8. Explain a CMOS inverter circuit.

SCR

9. Define Holding current and Latching current?

Ans. *Holding current* is the minimum value of anode current below which the device stops conducting and return to its OFF state. The value is usually in millimeters.
Latching current is the minimum anode current that must flow through SCR to keep it in ON state after the triggering pulse has been removed. Latching current is 2-3 times the holding current.

10. What is the Turn ON processes of SCR?

Ans. Following are the Turn ON processes of SCR:

a. Forward Voltage Triggering
b. Thermal Triggering or Temperature Triggering
c. dv/dt Triggering
d. Radiation or Light Triggering
e. Gate Triggering

11. What are the Gate control methods?

Ans. For gate control, a signal is applied between gate terminal and cathode terminal of the device. There are three types of signals used for this purpose and they are as follows:

DC Signals

- A DC voltage of proper magnitude and polarity is applied between the gate and cathode terminal in such a way that the gate becomes positive with respect to cathode
- When the applied voltage is sufficient to produce the required gate current, the device starts conducting.
- The drawback of this scheme is that both power and control circuit is DC and there is no isolation between them; also a continuous DC signal has to be applied to the gate causing more gate power loss.

AC Signals

- AC source is commonly used for the gate signal in all applications of Thyristor control. This scheme provides proper isolation between the power and control circuit. The firing angle control is obtained easily by changing the phase angle of the control system.
- However, the gate drive is maintained for one and a half cycle after the device is turned ON and reverse voltage is applied between the gate and cathode terminal during the negative half cycle.
- The drawback is that a separate transformer is required to step down the AC supply which adds to the cost.

Pulse Signals

- In this method, the gate drive consists of a single pulse appearing periodically or a sequence of high-frequency pulses. This is also known as 'carrier frequency gating'.
- A pulse transformer is used for isolation between main drive supply and gating signal. The main advantage is that there is no need of applying continuous signals and hence the gate losses are reduced.

12. What are the advantages of Gate Turn ON process?

Ans. Following are the advantages of Gate Turn ON process:

- Less Power consumption.
- It is possible to turn ON the SCR precisely at the desired value of anode to cathode voltage $V_{AK.}$
- If the supply voltage is AC then it is possible to adjust the firing angle to the desired value.
- Triggering circuit is easy to design.
- Turn ON gain is very high.
- Pulse triggering circuit provides greater flexibility.

13. What are operating modes or operating regions of SCR? Explain with neat VI characteristics.

Solved Examples

2.1 The device parameters for an n-Channel JFET are: Maximum current I_{DSS} = 10mA, Pinch off voltage, V_p = - 4V. Calculate the drain current for (a) V_{GS} = 0, (b) V_{GS} = - 1.0V and (c) V_{GS} = - 4V

Solution: The expression for drain current I_D, in the saturation region is,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

(a) When VGS = 0, from Eq(1), $I_D = I_{DSS} = \boldsymbol{10mA}$

(b) (b) When V_{GS} = -1.0V, the drain current from Eq (1) is,

$$I_D = 10x10^{-3}\left(1 - \frac{(-1)}{(-4)}\right)^2 = \boldsymbol{5.6\ mA}$$

(c) When V_{GS} = -4V = V_p, then from Eq(1),

$$I_D = \boldsymbol{0}$$

2.2 A JFET produces gate current of 2nA when gate is reverse biased with 8V. Determine the resistance between gate and source.

Solution: Since reverse gate-source voltage, V_{GS}, of 8v produces gate current, I_G of 2nA, Therefore, gate-to-source resistance, R_{GS}, is

$$R_{GS} = \frac{V_{GS}}{I_D} = \frac{8}{2x10^{-9}} = \mathbf{4000M\Omega}$$

2.3 The reverse gate voltage of JFET when changes from 4.4V to 4.2V, the drain current changes from 2.2 mA to 2.6 mA. Find out the value of transconductance of the transistor.

Solution: The transconductance, g_m is defined as

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Where ΔID is change in drain current when change in gate-source voltage is ΔVGS.

In the given problem,

Δ_{ID} = (2.6 – 2.2) mA = 0.4 mA and,

ΔV_{GS} = (4.4 – 4.2) V = 0.2 V

$$\therefore g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.4x10^{-3}}{0.2} = \mathbf{2}\boldsymbol{m}\ \mathbf{mho}$$

2.4 Find out the operating point current and voltage values (I_{DQ} and V_{DSQ}) for a self biased JFET having the supply voltage V_{DD} = 20V and maximum value of drain current as 12 mA.

Solution: We know that the value of drain current at Q-point may be taken as half of the maximum current, that is

$$I_{DQ} = \frac{I_{DSS}}{2} = \frac{12x10^{-3}}{2} = \mathbf{6}\ \boldsymbol{mA}$$

In the same way, the value of drain-source voltage at Q-point may be taken as half of supply voltage VDD. That is,

$$V_{DSQ} = \frac{V_{DD}}{2} = \frac{20}{2} = \mathbf{10}\boldsymbol{V}$$

Therefore, I_{DQ} = **6 mA** and V_{DSQ} = **10V.**

2.5 Calculate the value of source resistance RS required to self bias a n-JFET such that V_{GSQ} = - 3V. The n-JFET has maximum drain-source current I_{DSS} = 12 mA, and pinch-off voltage, Vp = - 6V.

Solution: **Given**, IDSS = 12 mA, VGS = -3V and Vp = -6V,
The drain current, ID, in a JFET, in the saturation region is,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 \qquad I_D = 12mA\left[1 - \left(\frac{-3}{-6}\right)\right]^2 \qquad I_D = 9.0\ mA$$

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{3V}{9mA} \simeq 333\Omega \qquad \boldsymbol{R_S = 333\ \Omega}$$

Multiple Choice Questions

1. Junction Field Effect Transistors (JFET) contain how many diodes?

   A. 4 C. 2

   B. 3 D. 1

2. A MOSFET has how many terminals?

   A. 2 or 3 C. 4

   B. 3 D. 3 or 4

3. I_{DSS} can be defined as:

   A. the min. possible drain current C. the max. possible current with V_{GS} held at 0 V

   B. the max. possible current with V_{GS} held at –4 V D. the max.drain current with the source shorted

4. When $V_{GS} = 0$ V, a JFET is:

   A. Saturated C. an open switch

   B. an analog device D. cut off

5. When the JFET is no longer able to control the current, this point is called the:

   A. breakdown region C. saturation point

   B. depletion region D. pinch-off region

6. With a JFET, a ratio of output current change against an input voltage change is called:

   A. Transconductance C. Resistivity

   B. Siemens D. Gain

7. The trans-conductance curve of a JFET is a graph of:

   A. I_S versus V_{DS} C. I_D versus V_{GS}

   B. I_C versus V_{CE} D. $I_D \times R_{DS}$

8. A JFET has three terminals, namely ……

   A. cathode, anode, grid C. emitter, base, collector

   B. source, gate, drain D. none of the above

9. A JFET is also called …… transistor

   A. unipolar C. unijunction

   B. bipolar D. none of the above

10. A JFET is a …… driven device

    A. current C. both current and voltage

    B. voltage D. none of the above

11. The gate of a JFET is …… biased

    A. reverse C. reverse as well as forward

    B. forward D. none of the above

12. The input impedance of a JFET is ……. that of an ordinary transistor
    A. equal to
    B. less than
    C. more than
    D. none of the above
13. When drain voltage equals the pinch-off-voltage, then drain current ……. with the increase in drain voltage
    A. decreases
    B. remains constant
    C. increases
    D. none of the above
14. If the reverse bias on the gate of a JFET is increased, then width of the conducting channel
    A. is decreased
    B. remains the same
    C. is increased
    D. none of the above
15. A MOSFET has …… terminals
    A. two
    B. five
    C. four
    D. three
16. A MOSFET can be operated with ……..
    A. negative gate voltage only
    B. positive gate voltage only
    C. positive as well as negative gate voltage
    D. none of the above
17. A JFET has …….. power gain
    A. small
    B. very high
    C. very small
    D. none of the above
18. The input control parameter of a JFET is ……
    A. gate voltage
    B. source voltage
    C. drain voltage
    D. gate current
19. A common base configuration of a pnp transistor is analogous to …… of a JFET
    A. common source configuration
    B. common drain configuration
    C. common gate configuration
    D. none of the above
20. A JFET has high input impedance because ……
    A. it is made of semiconductor material
    B. input is reverse biased
    C. of impurity atoms
    D. none of the above
21. In a JFET, when drain voltage is equal to pinch-off voltage, the depletion layers ……
    A. almost touch each other
    B. have large gap
    C. have moderate gap
    D. none of the above
22. In a JFET, I_{DSS} is known as ……..
    A. drain to source current
    B. drain to source current with gate shorted
    C. drain to source current with gate open
    D. none of the above
23. The two important advantages of a JFET are ……..
    A. high input impedance and square-law property
    B. inexpensive and high output impedance
    C. low input impedance and high output impedance
    D. none of the above
24. Which of the following devices has the highest input impedance?
    A. JFET
    B. ordinary transistor
    C. Crystal diode
    D. MOSFET
25. A MOSFET uses the electric field of a ……. to control the channel current
    A. capacitor
    C. generator

B. battery
D. none of the above

26. If the gate of a JFET is made less negative, the width of the conducting channel…….
A. remains the same
C. is increased
B. is decreased
D. none of the above

27. The input impedance of a MOSFET is of the order of ……..
A. Ω
C. kΩ
B. a few hundred Ω
D. several MΩ

28. An SCR has …….. semi-conductor layers
A. Two
C. Four
B. Three
D. None of the above

29. An SCR has three terminals viz ……
A. Cathode, anode, gate
C. Anode, cathode, drain
B. Anode, cathode, grid
D. None of the above

30. An SCR is sometimes called ……
A. Triac
C. Unijunction transistor
B. Diac
D. Thyristor

31. An SCR is made of …….
A. Germanium
C. Carbon
B. Silicon
D. None of the above

32. In the normal operation of an SCR, anode is …… w.r.t. cathode
A. At zero potential
C. Positive
B. Negative
D. None of the above

33. An SCR combines the features of ……..
A. A rectifier and resistance
C. A rectifier and capacitor
B. A rectifier and transistor
D. None of the above

34. The control element of an SCR is …….
A. Cathode
C. Anode supply
B. Anode
D. Gate

35. The normal way to turn on a SCR is by ……..
A. Breakover voltage
C. Appropriate gate current
B. Appropriate anode current
D. None of the above

36. An SCR is made of silicon and not germanium because silicon ……
A. Is inexpensive
C. Has small leakage current
B. Is mechanically strong
D. Is tetravalent

37. An SCR is turned off when ……..
A. Anode current is reduced to zero
C. Gate is reverse biased
B. Gate voltage is reduced to zero
D. None of the above

38. We can control a.c. power in a load by connecting ……
A. Two SCRs in series
C. Two SCRs in parallel opposition
B. Two SCRs in parallel
D. None of the above

39. When SCR starts conducting, then ……. loses all control
A. Gate
C. Anode
B. Cathode
D. None of the above

40. CMOS inverter circuit has pair of transistors which are

A. two PMOS
B. two BJTs
C. two NMOS
D. two complementary CMOS

Key Answers:

1.C, 2. D, 3. C, 4. A, 5. A, 6. A, 7. C, 8. B, 9. A, 10. B, 11. A, 12. C, 13. B, 14. A, 15. D, 16. C, 17.B, 18.A, 19.C, 20.B, 21.A, 22.B, 23.A, 24.D, 25.A, 26.C, 27.D, 28.C, 29. A, 30. D, 31. B, 32. C, 33.B, 34.D, 35.C, 36.C, 37.A, 38. C, 39.A, 40.D