NITC/EE/JG/MT

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DEPARTMENT OF ELECTRCAL ENGINEERING

II[nd] SEMESTER, M-TECH, INTERIM TEST - WINTER SEMESTER 2022

EE6304D MODERN DIGITAL SIGNAL PROCESSORS.

Time: Two Hours

Maximum: 30 Marks

27 1/2 / 29

Answer all questions

Note : Write the answers in the space provided against each of the questions. *Check all the 29 Questions are printed correctly.*

Questions 1. to 12. carry 1/2 Mark each.

1. What is the use of PGIE bit in CSR register ? – (Previous Global Interrupt enable – PGIE)
   It stores the previous value of GIE once an interrupt comes. (before executing interrupt)

2. What is the difference between Mnemonics and Opcode? Explain with an example.
   Mnemonics are the english like words which are defined by manufacturer. Opcode is the corresponding hex or binary value assigned.
   Ex: MOV A, B → mnemonic
   ⇒ 1F → corresponds opcode.

3. What is the disadvantage of Machine language? Why then Machine language exists?
   - Machine language is hard to remember write, modify by human. They exist because computer understands only machine language (0's & 1's).

4. Demonstrate the steps involved in converting 3AFH to decimal number.
   3AF H
   $16^2\ 16^1\ 16^0$
   ⇒ The weights of numbers are indicated. Value multiplied by weight gives corresponding decimal.
   ⇒ $3\times16^2 + 10\times16^1 + 15\times16^0 = 943_d$
   (A) (F)

5. What type of error will be identified before compiling? Syntax error. (Like grammer mistakes in programs)

6. What is the difference between compiler and cross-compiler? Explain with the help of proper examples.
   Compiler converts highlevel language to corresponding m/c code. Code is also running in same processor (ex: turbo c). Cross compiler generates m/c code which runs in another processor. Ex: Mplab IDE.

7. Which is the first microprocessor ? Who (Engineer) made it?
   INTEL 4004 is the first 4 bit µP. engineer – Ted..

8. Explain the law governing the development of RISC processors from then existing CISC processors.
   – Moors Law.
   Specialities of RICS →
   1. equal size instructions
   2. large no. of registers
   3. Single cycle execution
   4. Reduced no. of instructions.
   5. Harvard architecture.
   6. Micro instructions are hardwired.
   7. Load/store architecture.

9. Why most of the memory is 'Byte Addressable'?

(Also 2 hex no. together can represent)

We can easily access byte addressable manner. Even if word size is 32 bit, 4 byte can be accessed easily. lower order compatibility also available. Two bytes combined, 4 byte combined can also access } easy word alignment

10. What are the advantages of Digital systems over Analog systems? Explain.

1. Noise immunity - Analog are easily prone to errors
2. Low power consumption - (works in cutoff or saturation region)
3. Reproducibility
4. Easily stored in memory (memory are digital)
5. low size systems
6. Biasing issues are absent ...

11. List any eight important classes of processors used in digital systems.

1. Microprocessor / micro Controllers
2. DSP - Digital Signal Processors
3. FPGA - Field programmable gate array
4. PPU - Physics processing Unit
5. GPU - Graphics " "
6. TPU - Tensor " "
7. NPU - Neural " "
8. ASIC, 9. ASIP

12. What is the technical difference between EPROM and EEPROM?

Both are erasable EPROM can be erased by keeping chip under ultraviolet radiations for some time. But EEPROM is erased by electrically (easy).

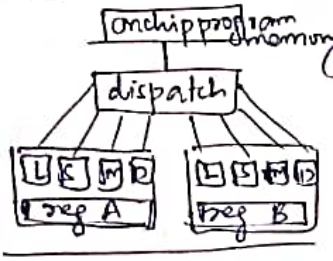
Questions 13. to 22. carry 1 Mark each.

13. When TMS6713 DSP is turned ON (starting), what is the order in which various memory are populated with opcodes? Explain how an opcode is reaching the decoder in this case.

- Same as 26.

14. Explaining the VLIW concept with reference to any processor.

VLIW - Very Long Instruction Word. As TMS320C67xx dsp concerned, 256 bits comprising 8 instructions are constituting one instruction word. In once cycle, this data is accessed. It is decoded and dispatched to different functional units for parallely operate instructions if independence of code is available. (Increases speed)



15. "Think Digital Act Analog" - What is the context of this slogan? Explain.

Processing can be done in digital way. But output world mostly give/need analog signals. So take/act in smooth/analog way but do processing in fast/efficient/low power digital way.

16. List the control registers associated with the Cache memory in TMS6713 DSP.

LIP - CSR, CCFG, LIPFBAR, LIPFWC
LID - CSR, CCFG, LIDFBAR, LIDFWC
L2 - CCFG, L2FBAR, L2FWC, L2FLUSH, L2CLEAN, L2CBAR, L2CWC.

Flush Base Address Reg
Flush Word Count

17. What is the precaution to be taken in storing the data in the memory of TMS6713 DSP, with reference to the size of data to be stored? (w. r. t. starting address) → This is word alignment.

32 bit data can be stored in 4 bytes (4 locations needed). So the Least significant byte should be stored at address ending at 00. (then 01, 10, 11)
16 bit data can be stored at address locations ending at 0 (least sign. byte)
8 bit data can be stored - The least significant byte (only one byte is present) can at any address locations.

. is the difference between available ILP and achievable ILP?

Available ILP – It is the degree of independence present in code (Code should be - (instructions) sufficiently independent for parallelism).

Achievable ILP - It is the level of parallelism that can be provided by - hardware : Like no. of functional units (independent) so that parallel execution improves

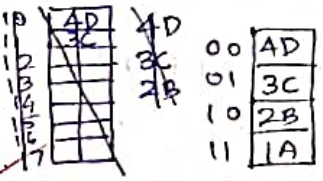
9. Shakti (From IIT Madras) is India's first '64-bit processor'. What will you understand from this statement, about its hardware, from the user perspective?

- The meaning is word size is 64 bits. Means 64 bits of data can be processed at a time. hardware units, ALU - 64 bits
data bus - 64 bits, registers - 64 bits.
- As word size increases speed of processing increases.

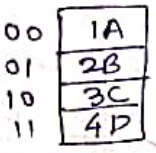
10. TMS 6713 is a "32 bit Little Endian" DSP - Explain the 'Endian' concept (with the help of an example).

Little endian means, lower data bytes are stored in lower address memory.

Ex: for 32 bit data - 1A 2B 3C 4D (1A: higher byte, 4D: lower byte) → little endian ⇒



Big endian

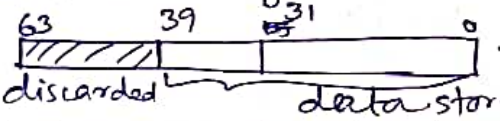


11. How many cycles will the CPU take to get a data in TMS6713 DSP?

- for a data to get from data memory, CPU asks for a data to L1D first. If it is available in L1D, L1D hit happens. It takes just one cycle. If it is not available there, L1D controller asks to L2. (L1D miss) If it is available in L2. It is given to CPU. It takes 4 cycles. If it is not available there also, asks to external memory through EDMA. That speed depends on external memory speed.

12. When you have to deal with 40-bit data in TMS6713 DSP, have you noticed any restriction that is existing with reference to the usage of GP registers? Explain.

GP registers are of 32 bit size. But as we need 40 bit data here, we need to combine registers in pairs and the lower 40 bits are used, remaining discarded. So we have 16 such register pairs.



⇒ register pair → lower byte (even register)

A1:A0, A3:A2, ..., A15:A14

B1:B0, B3:B2, ..., B15:B14

16 pairs

13. Give the Size and Type of L1 and L2 Cache memory along with the data path size in each case, in TMS6713 DSP. [1.5 Marks] (Continued at end →)

L1P Cache - static RAM. - 256 bits data + 32 bit address - 4 kB Size.

L1D Cache - static RAM - 32 bit data (2 data paths) - 4 kB Size (L, S, D data path) Load - 64 bit, Store - 32, DA - 32 bit

L2 Cache - 64 kB - divided into 4 banks ((3/4 Cache, 1/4 RAM)(1/4 Cache, 3/4 RAM) → All combinations possible) (RAM - lesser transistors)

14. Explain with the help of an example, step by step method of 'turning ON' of a microprocessor, when you first power it. [1.5 Marks]

1. PC will be loaded with initial address.
2. It is placed on the address bus. (~~data~~ memory address bus)
3. Address reaches program memory location.
4. CPU generates necessary $\overline{CS}$, $\overline{RD}$ Signals to read data
5. Data is placed on data bus. Reaches Control unit.
6. opcode goes to Instruction register. and then to instruction decoder
7. There it decodes and understand instruction
8. Necessary operands are fetched.
9. Operands reaches ALU.
10. Operations executed.
11. Results are stored back.

15. Can a location in L1P go 'dirty'? Why? Explain. [1.5 Marks]

→ Ans is in the back page.

Ans - No.

26. When TMS6713 DSP is turned ON (starting), what is the order in which various memory are popula... Explain how an opcode is reaching the decoder in this case.

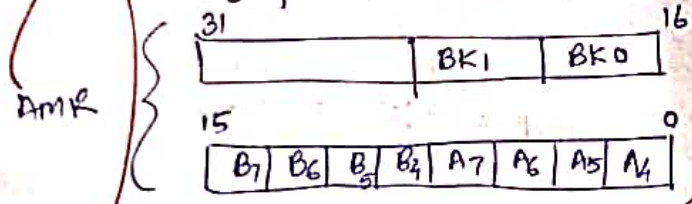
- As the memory turns ON Core asks the LIP Cache with initial add... Usually for initial calls, instruction opcode will not be present so LIP miss happens. The LIP controller asks to L2 to check for opcode. If th... also miss happens (L2 miss - 5 cycles) then L2 will asks EDMA to ask to external ROM. So, through EMIF stall opcode from external ROM reaches to L2, the... LIP, then Core and decoder. Successive opcode fetch can be done from LIP. 8 instructions can be loaded at a time.

27. What are the two invalidation methods in L1D? Explain. [2 Marks]

- By putting a 1 to ID field of CCFG register, we can invalidate entire tags in L1D memory block.
- Another way is setting the start address of the block needed to invalidate in L1DFBAR (L1D Flush Base Address Register), and put the no. of elements to clear in L1DFWC (L1DFWC) - (L1D Flush Word Count) then that block of data starting from L1DFBAR to "L1DFBAR + L1DFWC - 1" address will be cleared.
- We should be careful here. Set the count only after the address is set. clearing happens soon after count is set.

28. What is the use of AMR register? Explain various fields of AMR register? [2 Marks]

Addressing Mode Register. - This is to set the addressing mode to be followed by processor (AMR). → Either linear or circular.



A4-A7 and B4-B7 (8 registers) are used here to store the addresses. Two bits are available in these fields to set the mode.

0	0	linear addressing
0	1	circular, taking block size from BK0
1	0	circular, from BK1
1	1	not used

BK0 and BK1 are present to set the block size in circular addressing (for modes 01, 10)

for BKx values (5 bits) block sizes are as shown

BK (5 bits)	Block Size
00000	2
00001	4
00010	8
⋮	⋮
11111	⋮

29. With the help of a neat sketch, explain the architecture of TMS6713 DSP. [4 Marks]

- Ans is given in the last pages.

Core is connected to 2 level cache memory. In which level 1 is divided into program and data But level 2 is having both program and data together and which is configurable to contain both ~~dat~~ RAM & cache. Then L2 is connected to peripherals by EDMA (Enhanced Direct memory Access). External memory is connected to the processor through EMIF (Ext. memory Interface). Then many peripherals are available (timer, serial ports, GPIO)

Power down logic is to work in low power low freq. operation. PLL - phase locked loop to stabilise clock signals. For the core to work ~~prop~~ control registers, control logic are present to generate necessary control signals. Interrupt control, in circuit emulator (for simulation purpose). are also present.

This is a harward architecture as we can see separate data and programs memories with separate sets of buses.

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23. Contd.

→ L2 Cache - 64kB size with 64 bit ~~bus~~ wide storage.

It can be configured in RAM / cache mode

Full RAM, 3/4 RAM + 1/4 Cache, ~~3/~~ 1/2 RAM, 1/2 Cache, 1/4 RAM, 3/4 Cache,

Full Cache.

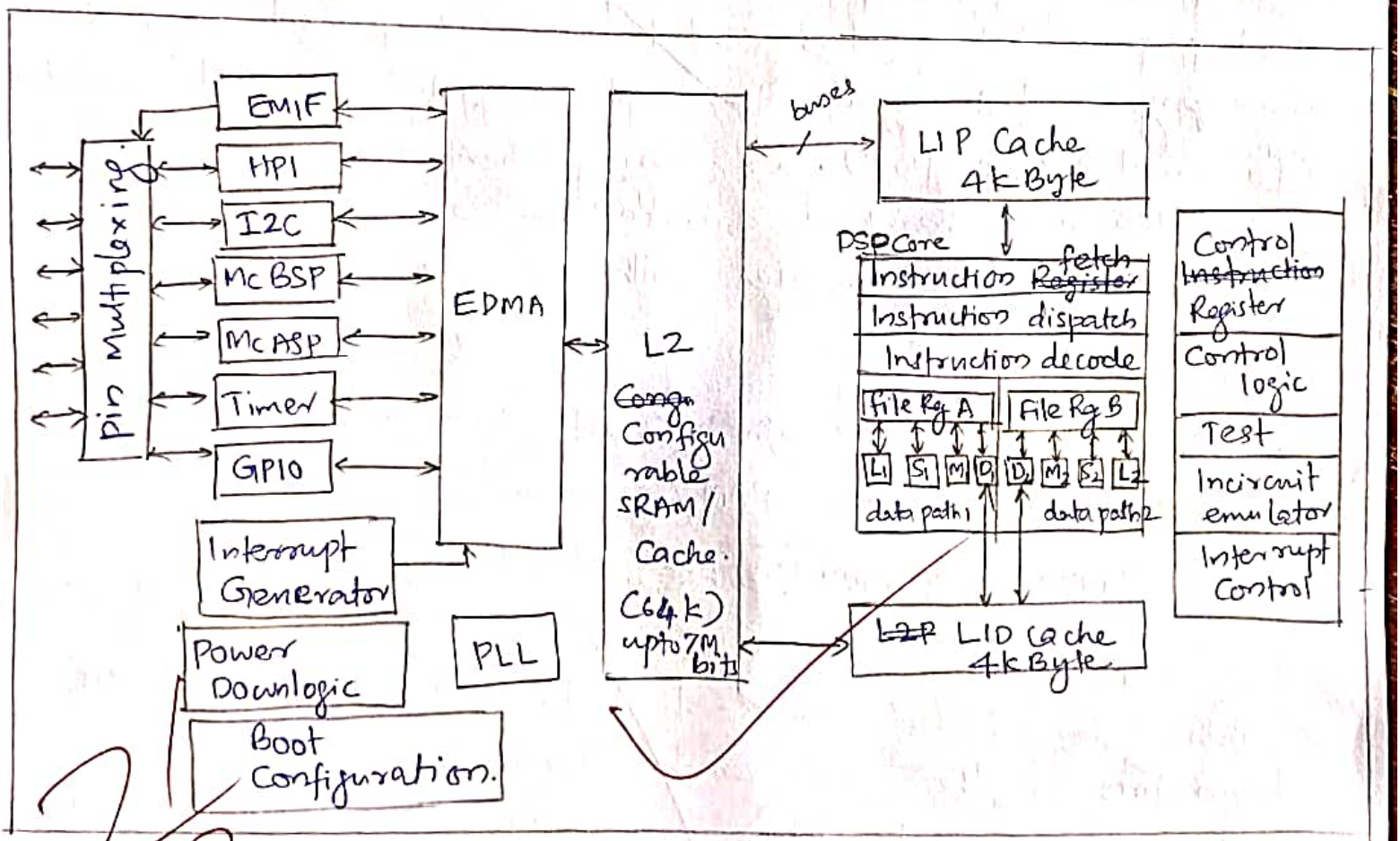
Both code and data can be stored here It is made is less transistors, so the size can be large.

→ But L1 cache - 5 transistors - So in less nos we made - less size But faster.

No.

(25). LIP location ~~can~~ cannot go dirty. The meaning of dirty is that, if an updation of data done in one location in LIP and if it is not evicted back to corresponding location in L2, or external memory, then there is mismatch of datas. ~~They~~ Then we call the location in LIP is dirty. But as LIP is program memory and CPU is not allowed to write/modify a location in LIP, the mismatch wont happen. So, LIP location cannot go ~~dit~~ dirty

(29) Architecture of TMS6713 DSP.



This is the overall architecture of TMS320C6713 DSP. DSP Core is shown which is having instruction fetch/decode/dispatch region and two data paths in which 2 file register sets A+B are available (which are composed of 16 registers of 32 bits each. Then 4 ~~of~~ functional units L,S,M,D are present in which 3 are arithmetic logic units and one sets of multiplication units. Such 2 units in each data paths.