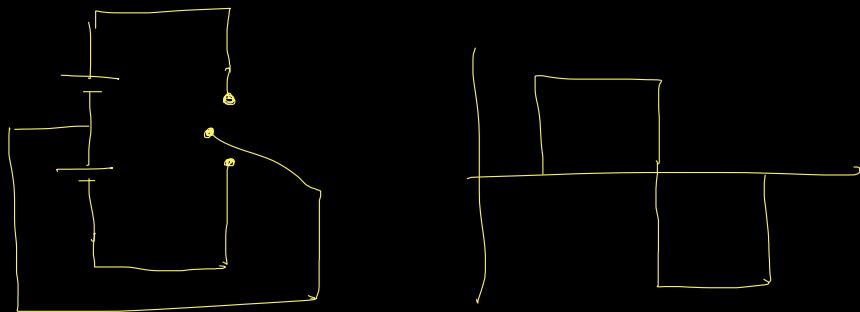




Multilevel inverters tech has emerged in the area of high power & voltage applications

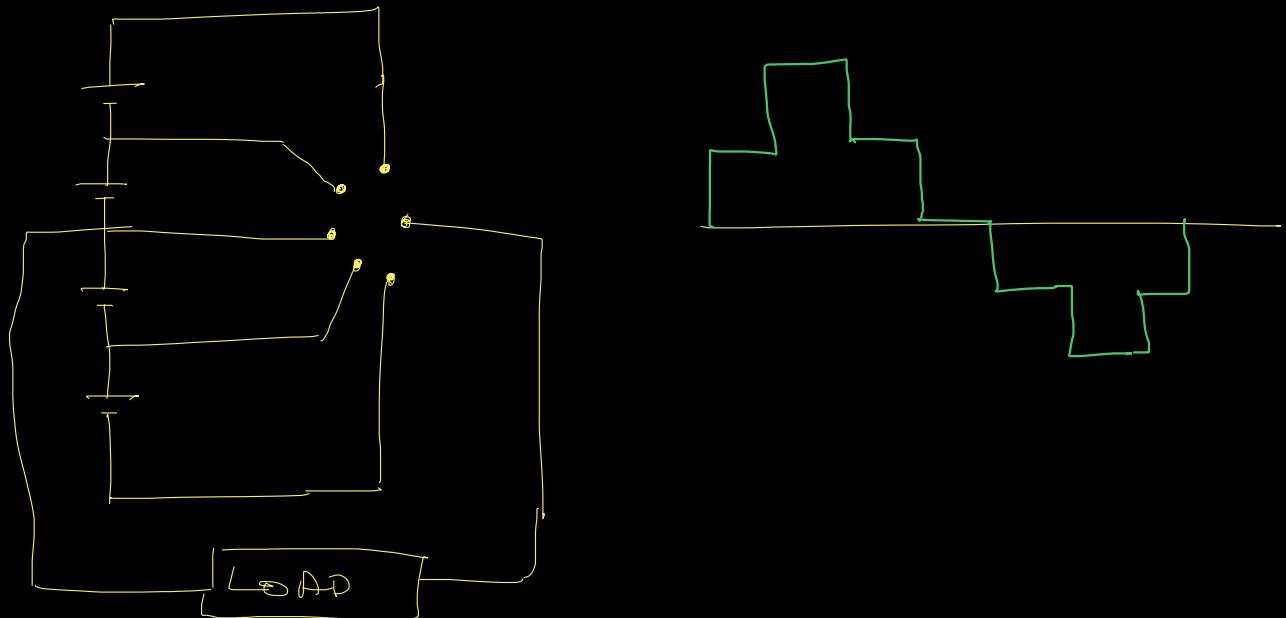
### Two Level inverter



### Three level inverter



### 5 - level inverter









$V_{AN}$	$S_{11}$	$S_{21}$	$S_{31}$	$S_{41}$	$S_{12}$	$S_{22}$	$S_{32}$	$S_{42}$	$V_{H1}$	$V_{H2}$
$2E$	1	1	0	0	1	1	0	0	$E$	$E$
$E$	1	1	0	0	1	0	1	0	$E$	0
	1	1	0	0	0	1	0	1	$E$	0
	1	0	1	0	1	1	0	0	0	$E$
	0	1	0	1	1	1	0	0	0	$E$
0	1	0	1	0	1	0	1	0	0	0
	1	0	1	0	0	1	0	1	0	0
	0	1	0	1	1	0	1	0	0	0
	0	1	0	1	1	0	1	0	0	0
	1	1	0	0	0	0	1	1	$E$	$-E$
	0	0	1	1	1	1	0	0	$-E$	$E$
$-E$	0	0	1	1	1	0	1	0	$-E$	0
	0	0	1	1	0	1	0	1	$-E$	0
	0	1	0	1	0	0	1	1	0	$-E$
	1	0	1	0	0	0	1	1	0	$-E$
$-2E$	0	0	1	1	0	0	1	1		

Certain voltage levels are produced by more than one switching states called redundant states.

Voltage level  $E$  can be produced by 4 sets of switching states. This provides great flexibility for switching pattern design especially for sum.

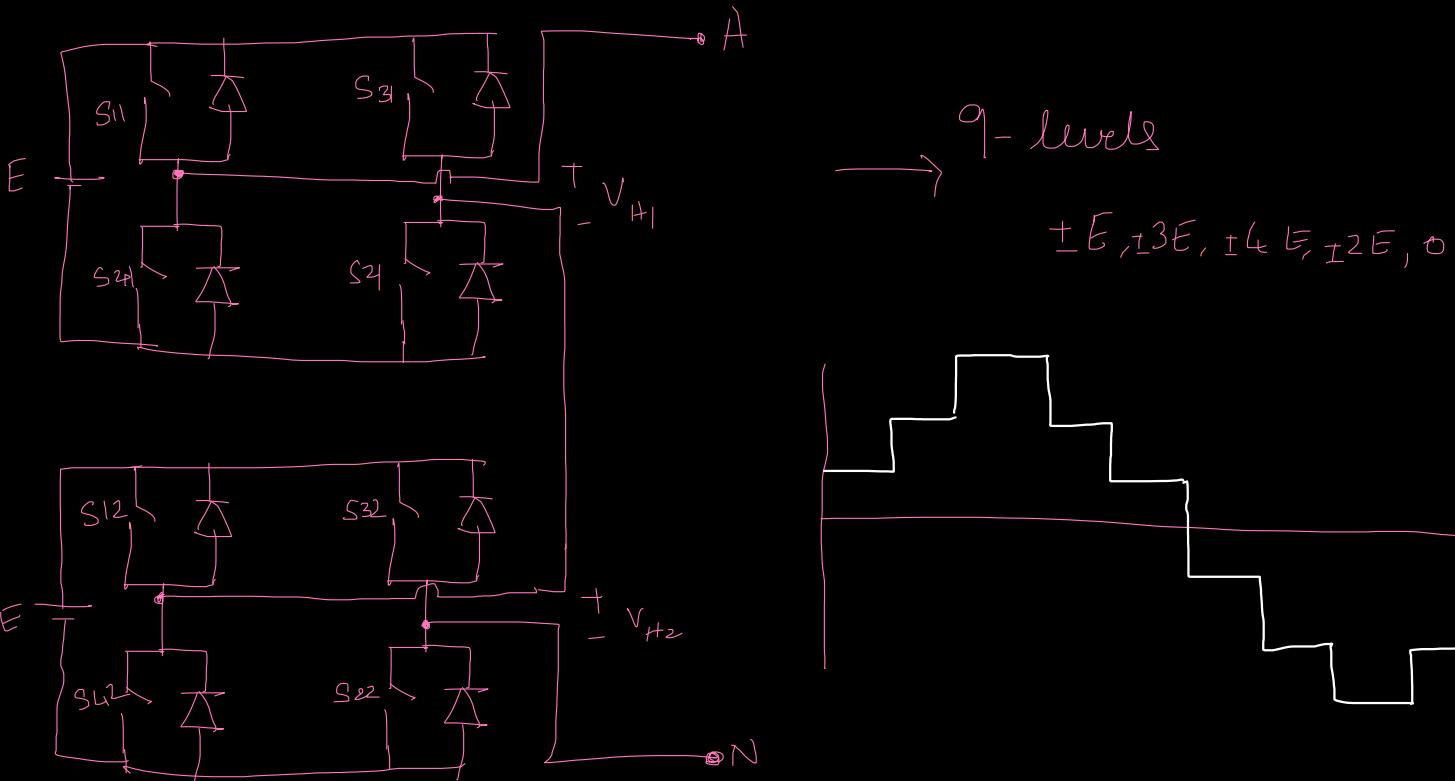
Number of voltage levels in CHTB is

$$m = 2H + 1$$

$H \rightarrow$  no of H bridge cells per phase.







## PWM Voltage Control for CHB MLI

### Coupler wave based Schemes

#### SPWM Schemes

- Phase Shifted Modulation Scheme
- Level Shifted Modulation Scheme

### ① Phase Shifted Modulation Scheme

- \* A CHB MLI having  $m$  voltage levels requires  $m-1$  phase shifted triangular coupler wave.
- \* All couplers have same freq & peak to peak amplitude
- \* Phase shift between 2 adjacent coupler waves is

$$\phi_{cr} = \frac{360}{m-1}$$



$V_{cr3} < V_{cr3^-}$  are for  $H_2$

$V_{mA} > V_{cr3} \rightarrow S_{13}$  is gated

$V_{mA} > V_{cr3^-} \rightarrow S_{23}$  is gated

$V_{mA} < V_{cr3} \rightarrow S_{43}$  gated

$V_{mA} < V_{cr3^-} \rightarrow S_{33}$  is gated

#### 7.4 Carrier-Based PWM Schemes

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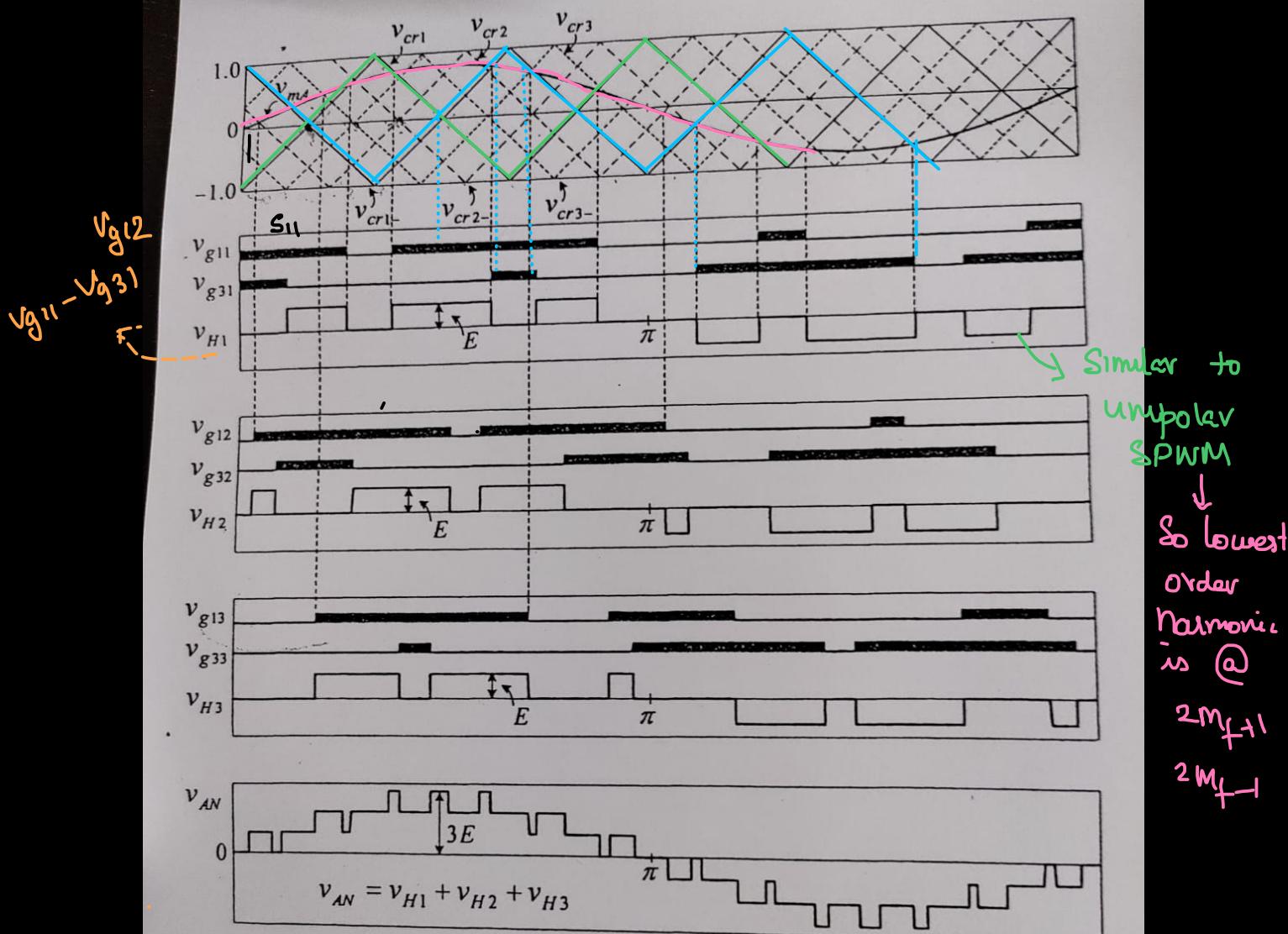


Figure 7.4-1 Phase-shifted PWM for seven-level CHB inverters ( $m_f = 3$ ,  $m_a = 0.8$ ,  $f_m = 60$  Hz, and  $f_{cr} = 180$  Hz).









Consider 7 level inverters,

$$V_{mA} > V_{cr1} \rightarrow S_{11}$$

$$V_{mA} < V_{cr1} \rightarrow S_{41}$$

$$V_{mA} > V_{cr2} \rightarrow S_{21}$$

$$V_{mA} < V_{cr2} \rightarrow S_{31}$$

134 Chapter 7 Cascaded H-Bridge Multilevel Inverters

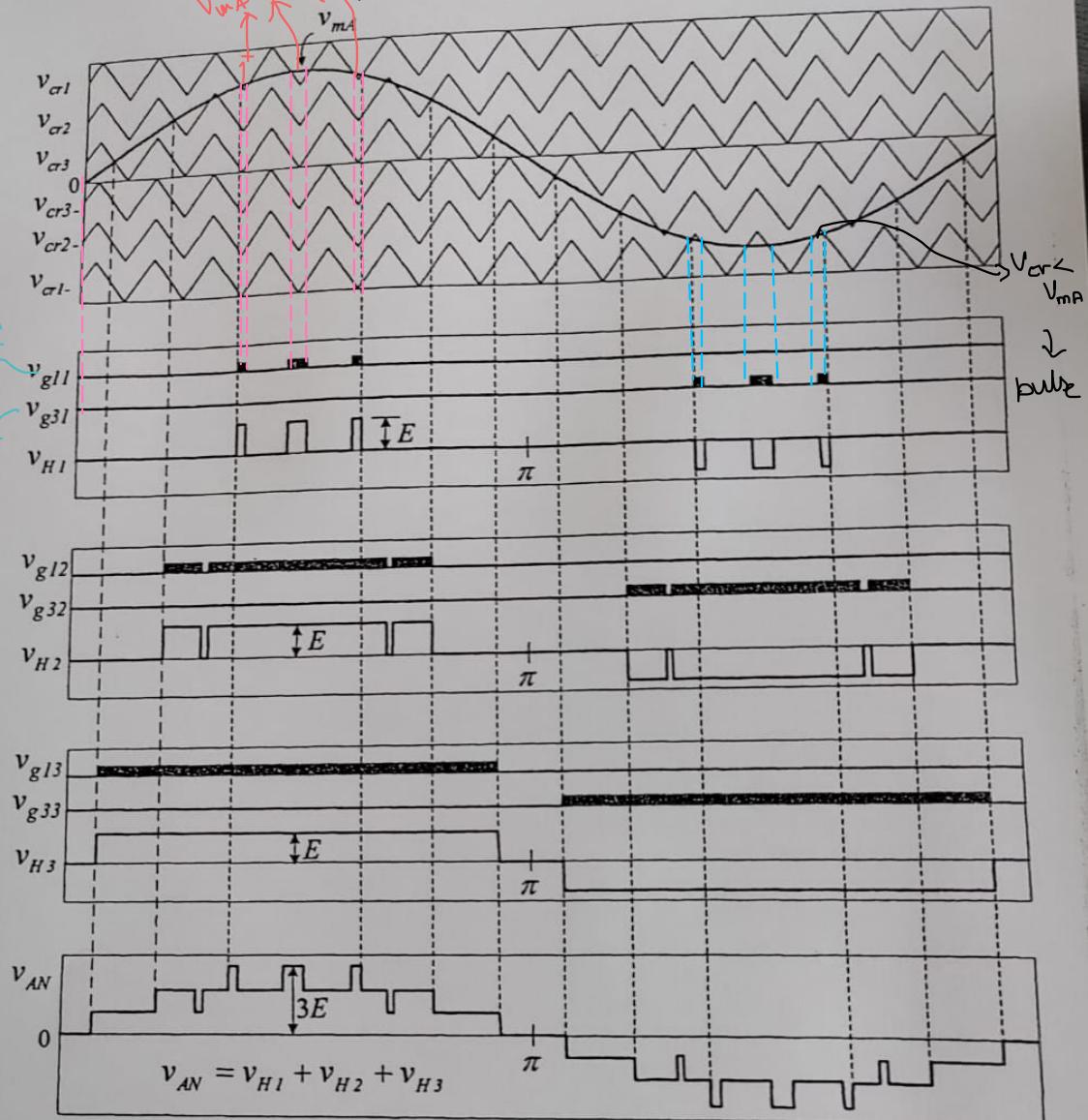


Figure 7.4-5 Level-shifted PWM for a seven-level CHB inverter ( $m_f = 15$ ,  $m_a = 0.8$ ,  $f_m = 60$  Hz, and  $f_{cr} = 900$  Hz).



DC bus is split into 3 levels by 2 series capacitors

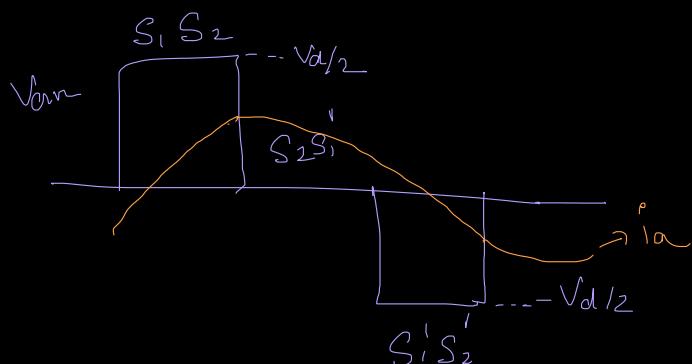
Output voltage  $V_{an}$  has 3 levels

$$+V_d/2, 0, -V_d/2$$

for  $V_{an} = +V_d/2 \rightarrow S_1 \wedge S_2$  are closed

$V_{an} = -V_d/2 \rightarrow S'_1 \wedge S'_2$  are closed

$V_{an} = 0 \rightarrow S_2 \wedge S'_1$  are closed.

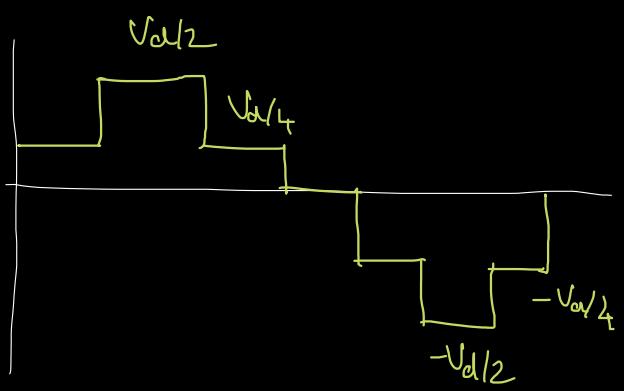


When  $S_1 \wedge S_2$  are on,

Voltage across  $S'_1$  is clamped to  $\frac{V_d}{2}$  through  $D'_1$   
 $S'_2$  is clamped to  $-\frac{V_d}{2}$  through  $D_2$

So called as diode clamped inverter

5 level diode clamped Inverter



\*  $V_{an} = +\frac{V_d}{2} \rightarrow S_1, S_2, S_3, S_4$  are closed

\*  $V_{an} = \frac{V_d}{4} \rightarrow S_2, S_3, S_4, S'_1$  are closed.

If  $i_a$  is +ve the current path is

$$C_2 \rightarrow D_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_4 \rightarrow a$$

If  $i_a$  is -ve the current path is

$$S'_1 \rightarrow D_1' \rightarrow C_2$$

\*  $V_{an} = 0 \rightarrow S_3, S_4, S'_1, S'_2$  are closed.

If  $i_a$  is +ve , path is

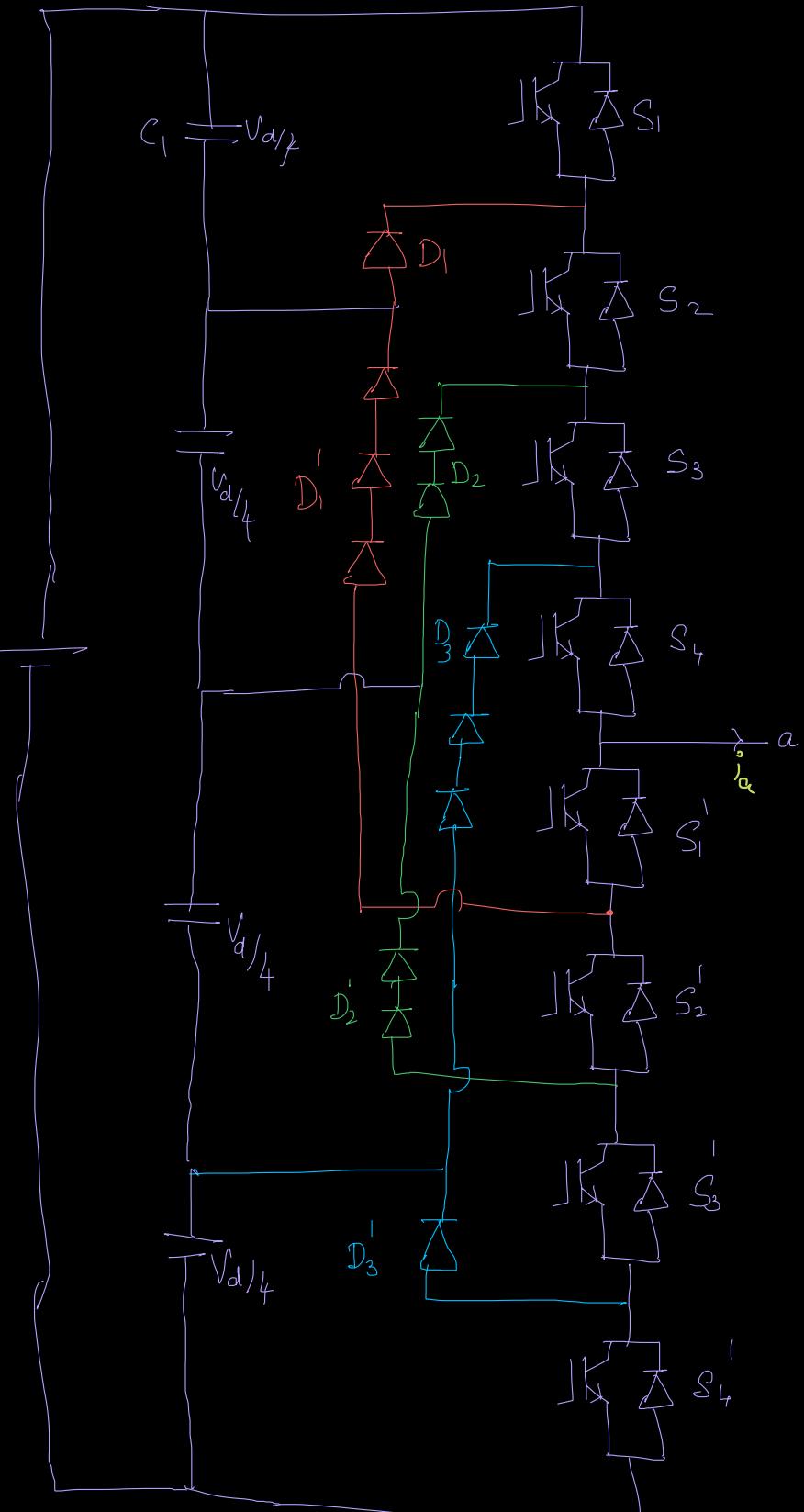
$$n \rightarrow D_2 \rightarrow S_3 \rightarrow S_4 \rightarrow a$$

If  $i_a$  is -ve , the path

$$a \rightarrow S'_1 \rightarrow S'_2 \rightarrow D_2' \rightarrow n$$

\*  $V_{an} = -\frac{V_{dc}}{4} \rightarrow S'_1, S'_2, S'_3, S'_4$  are closed

\*  $V_{an} = -\frac{V_{dc}}{2} \rightarrow S'_1, S'_2, S'_3, S'_4$  are closed.



Each switching device of an  $m$  level inverter is required to block a voltage of  $\frac{V_d}{m-1}$  volts.

Clamping diode has different reverse voltage ratings

Consider  $S_1, S_2, S_3, S_4$  are closed.

$$V_{D1} = \frac{V_d}{4} \rightarrow 1 \text{ diode of } \frac{V_d}{4} \text{ rating}$$

$$V_{D2} = \frac{V_d}{2} \rightarrow 2 \text{ diodes in series } (\frac{V_d}{4} \text{ rating each})$$

$$V_{D3} = \frac{3V_d}{4} \rightarrow 3 \text{ Diodes in Series}$$

Consider  $S'_1, S'_2, S'_3, S'_4$  are closed

$$V_{D'_1} = \frac{3V_d}{4} \rightarrow 3 \text{ diodes in Series}$$

$$V_{D'_2} = \frac{V_d}{2} \rightarrow 2 \text{ diodes in Series}$$

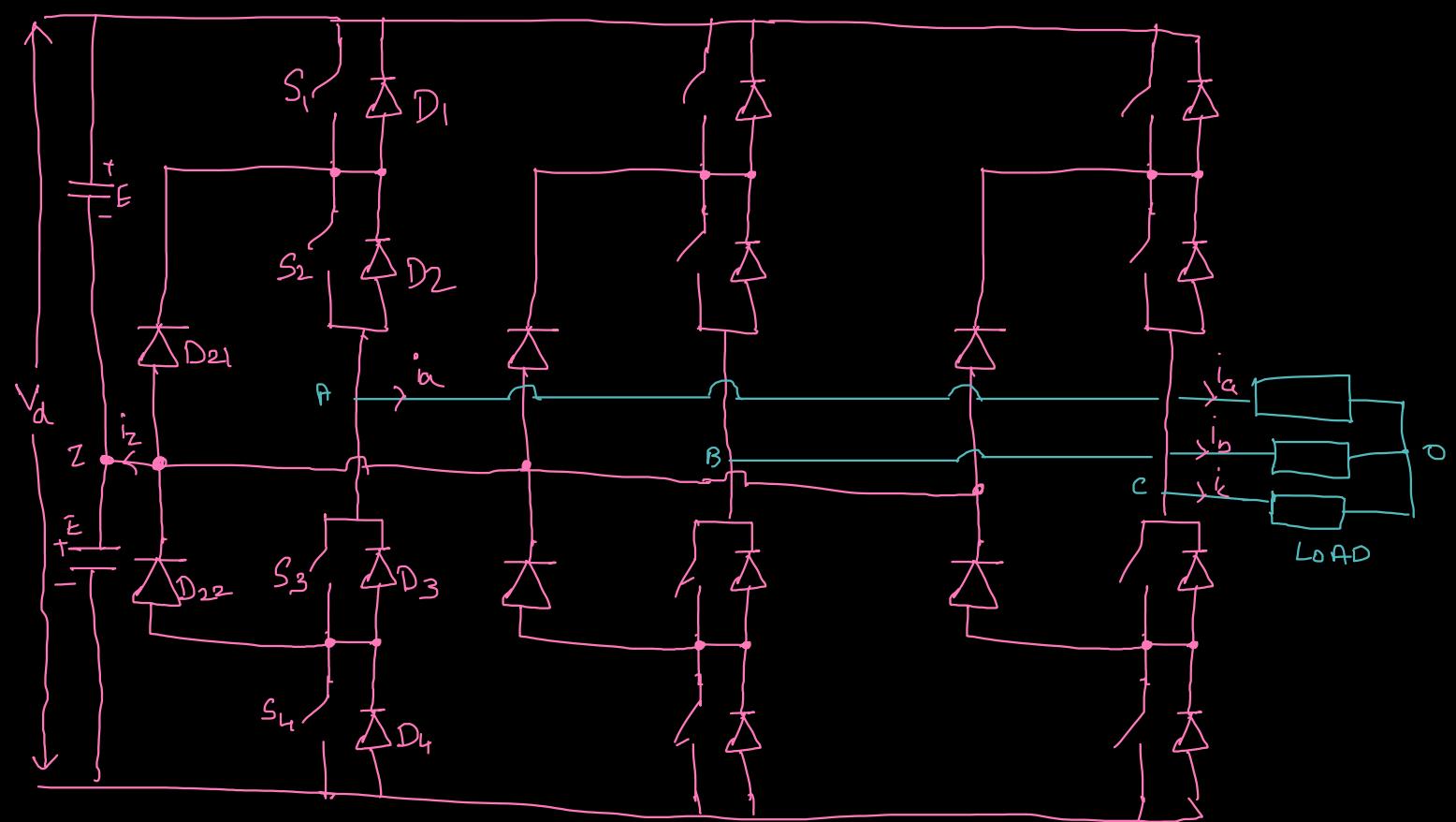
$$V_{D'_3} = \frac{V_d}{4} \rightarrow 1 \text{ diode}$$

So no of diodes for a  $m$  level inverter per phase

$$= (m-1)(m-2)$$

# 3φ 3 level diode clamped MLI

## Voltage Control



\* Each leg has 4 active switches & 4 anti-parallel diodes \$D\_1\$ to \$D\_6\$

\* The dc bus capacitor is split into 2 each of voltage \$V\_d/2\$ with

\$D\_{21}\$ & \$D\_{22}\$ are called clamping diodes

The capacitors charge or discharge by neutral current \$i\_z\$

\$i\_z\$ contains reverse leakage current  
of \$D\_{21}, D\_{22} \dots\$

## Switching States of the inverter

① leg A

\* P denotes the upper 2 switches  $S_1 S_2$  of leg A are on.

Pole Voltage  $V_{AZ} = +E$

\* N denotes the lower 2 switches  $S_3 S_4$  of leg A are on.

Pole Voltage  $V_{AZ} = -E$

\* O denotes that the inner 2 switches  $S_2 S_3$  are on

Pole Voltage  $V_{AZ} = 0$

i.e. clamped to 0 through clamping diodes

Switching State	Device Status				$V_{AZ}$
	$S_1$	$S_2$	$S_3$	$S_4$	
P	ON	ON	OFF	OFF	$E$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-E$

For +ve load Current ( $i_a > 0$ )

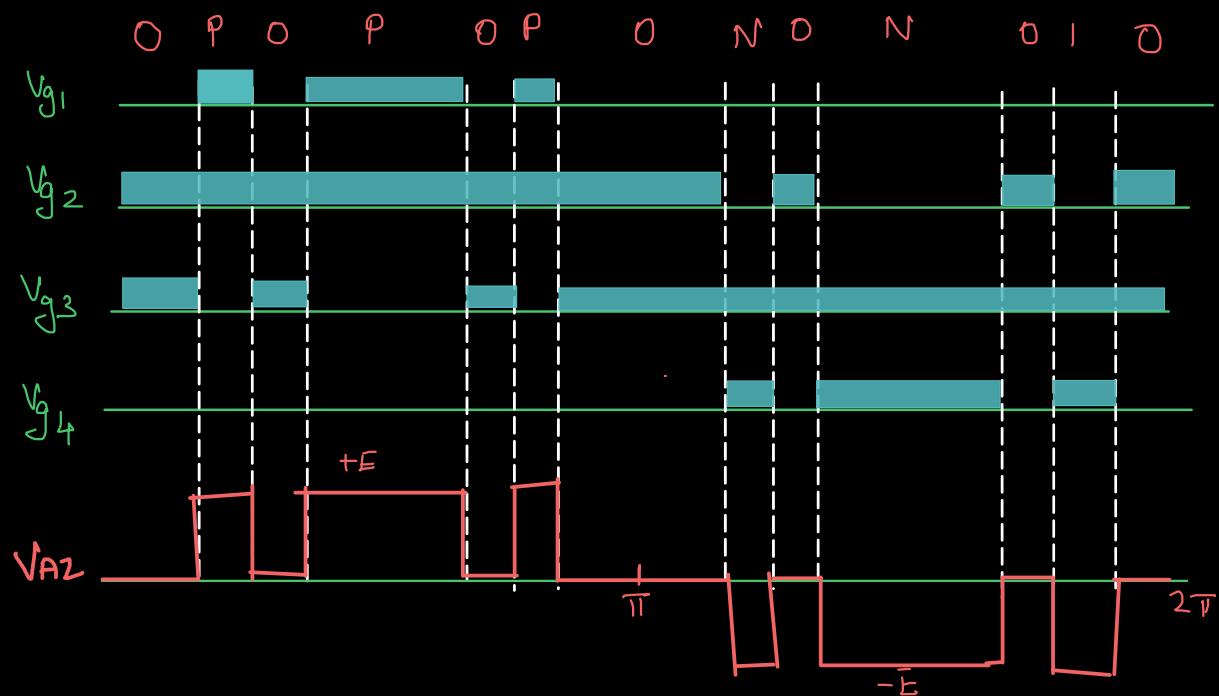
$D_{z1}$  is on, A is connected to Z through  $D_{z1} \& S_2$  ( $i_z > 0$ )

For -ve load Current ( $i_a < 0$ )

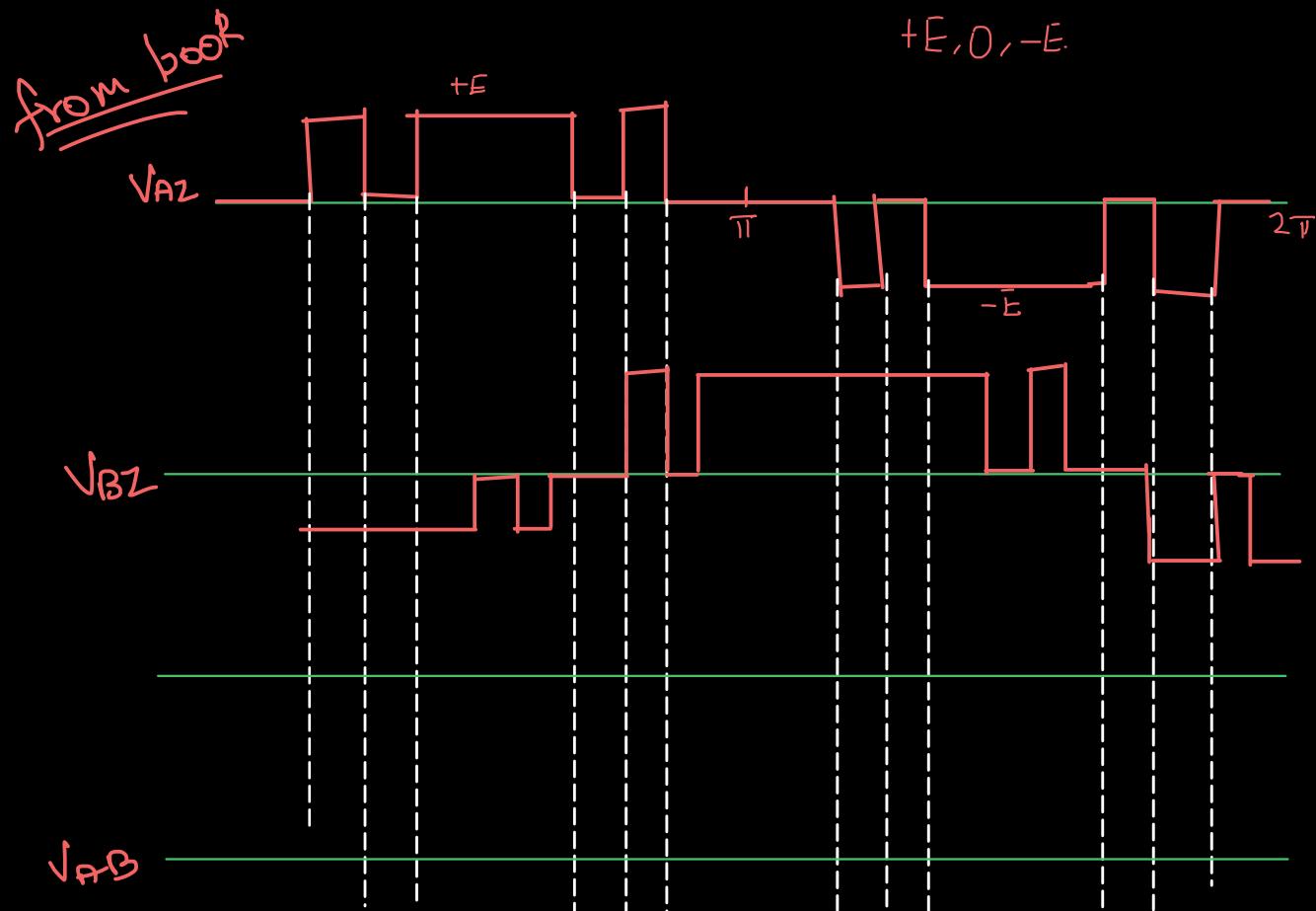
$D_{z2}$  is on, A is connected to Z through  $S_3 \& D_{z2}$  ( $i_z > 0$ )

# PWM of 3 level diode clamped MLI

- The gating signals can be generated by Carrier based modulation, SVM, , SHE etc



The waveform for  $\sqrt{A_Z}$  has 3 voltage levels.



# Commutation of Switching Device

Leg A

Assumptions:

→ Load current  $i_A$  is constant during commutation interval due to inductive nature of load.

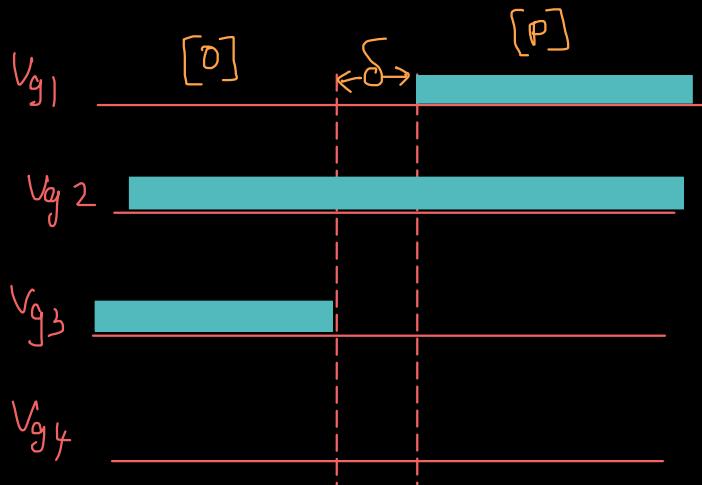
→ DC bus capacitors  $C_{d1}$  &  $C_{d2}$  are sufficiently large such that the voltage across each capacitor is kept at const value  $E$

→ All switches are ideal

Consider the transition from O ( $S_2 \perp S_3$ ) to P ( $S_1 \perp S_3$ )

$S_3$  is turned off &  $S_1$  is turned on

A blanking interval of  $\delta$  is required in between this.



Commutation with  $i_A > 0$

during Switching State [0]

$S_{1,2} S_4 \rightarrow \text{OFF State}$

$S_2 \& S_3 \rightarrow \text{ON State}$

Positive load current  $i_A > 0$

flows through the

clamping diode  $D_{21} \& S_2$

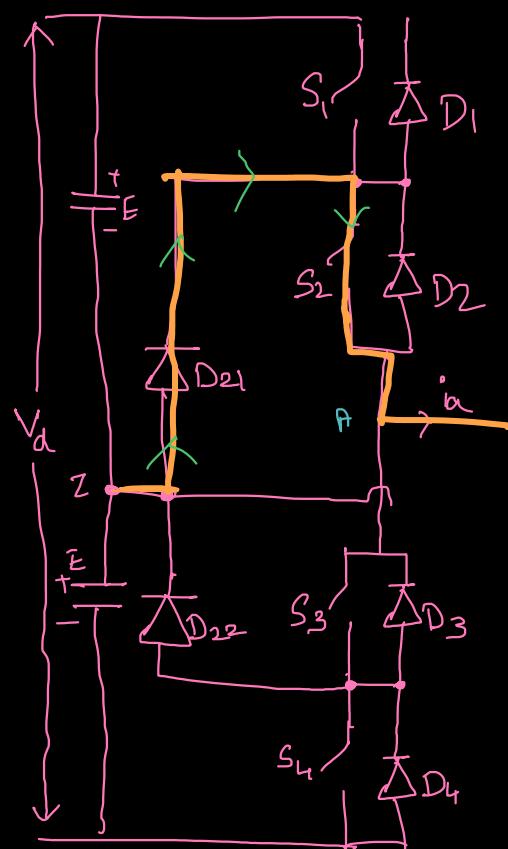
$$V_{S2} = 0 = V_{S3}$$

$$V_{S1} = E$$

$$V_{S4} = E$$

during interval  $\delta$ ,

$S_3 \rightarrow \text{turned off}$



the clamping diode  $D_{21} \& S_2$

When  $S_3$  is completely switched off.

$$\begin{aligned} V_{S3} &= E/2 & \left( \text{Across } V_{S3} \& V_{L_L} = E \right) \\ V_{S4} &= E/2 & \Rightarrow V_{S4} = V_{S3} = E/2 \end{aligned}$$

during - Switching State P,

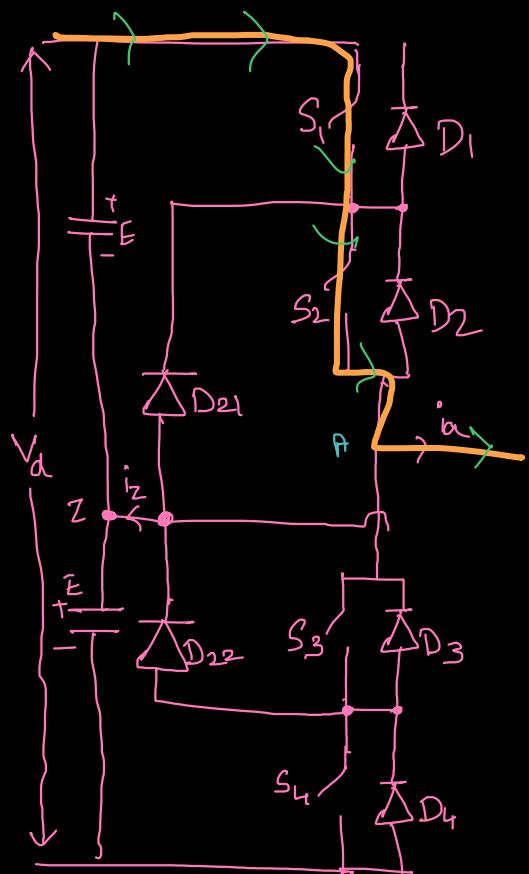
$S_1$  is gated ( $V_{S1}=0$ )

$D_{21}$  is reverse biased & turned off

The load current  $i_A$  is commutated from  $D_{21} \leftarrow S_1$

$$V_{S3} = E$$

$$V_{SE} = E$$



Commutation with  $i_A < 0$

During switching state [0]

$S_1, S_4 \rightarrow \text{off}$

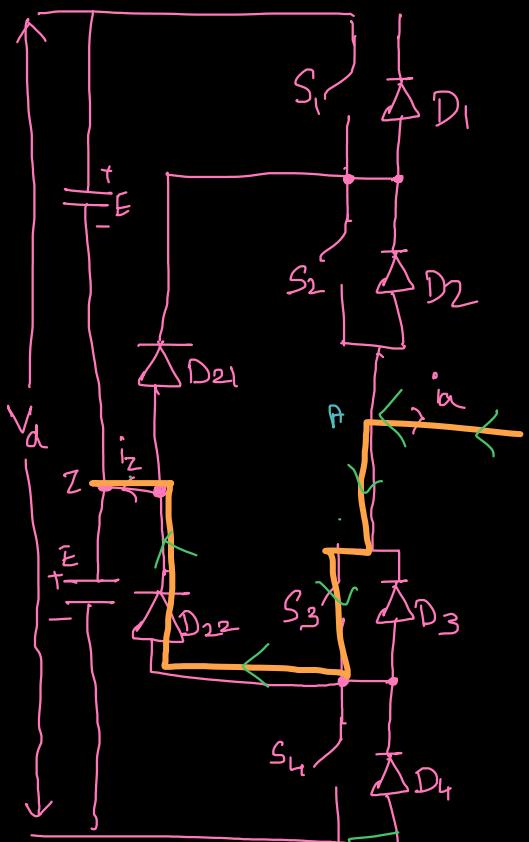
$S_2, S_3 \rightarrow \text{on}$

Negative load current ( $i_A < 0$ ) flows through  $S_3$  & diode  $D_{22}$

$$V_{S2} = 0 \Rightarrow V_{S3}$$

$$V_{S1} = E$$

$$V_{S4} = E$$



during interval  $\delta$ ,

$S_3 \rightarrow \text{turned off}$

-ve inductive load current

$i_a$  flows through diode

$D_1, D_2$

$$V_{S1} \approx 0 \approx V_{S2}$$

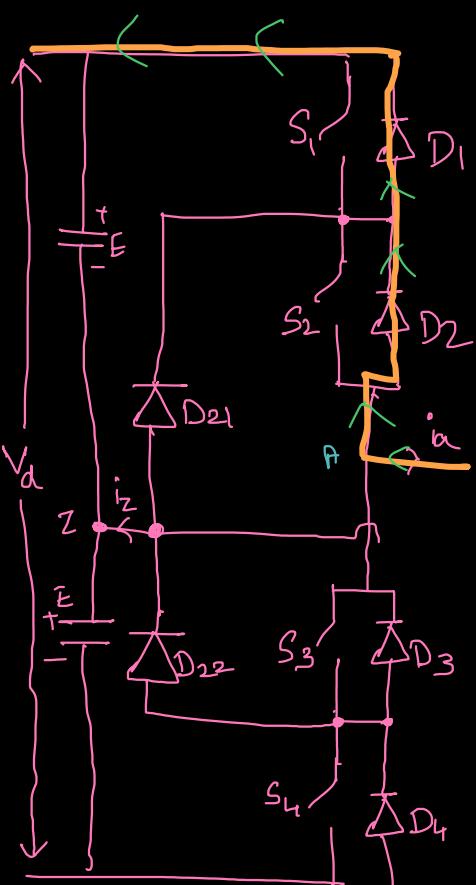
$V_{AZ} = E$  (so when current -ve  
there is no voltage gain)

during switching state [P],

The turn-on of  $S_1$

does not affect the operation

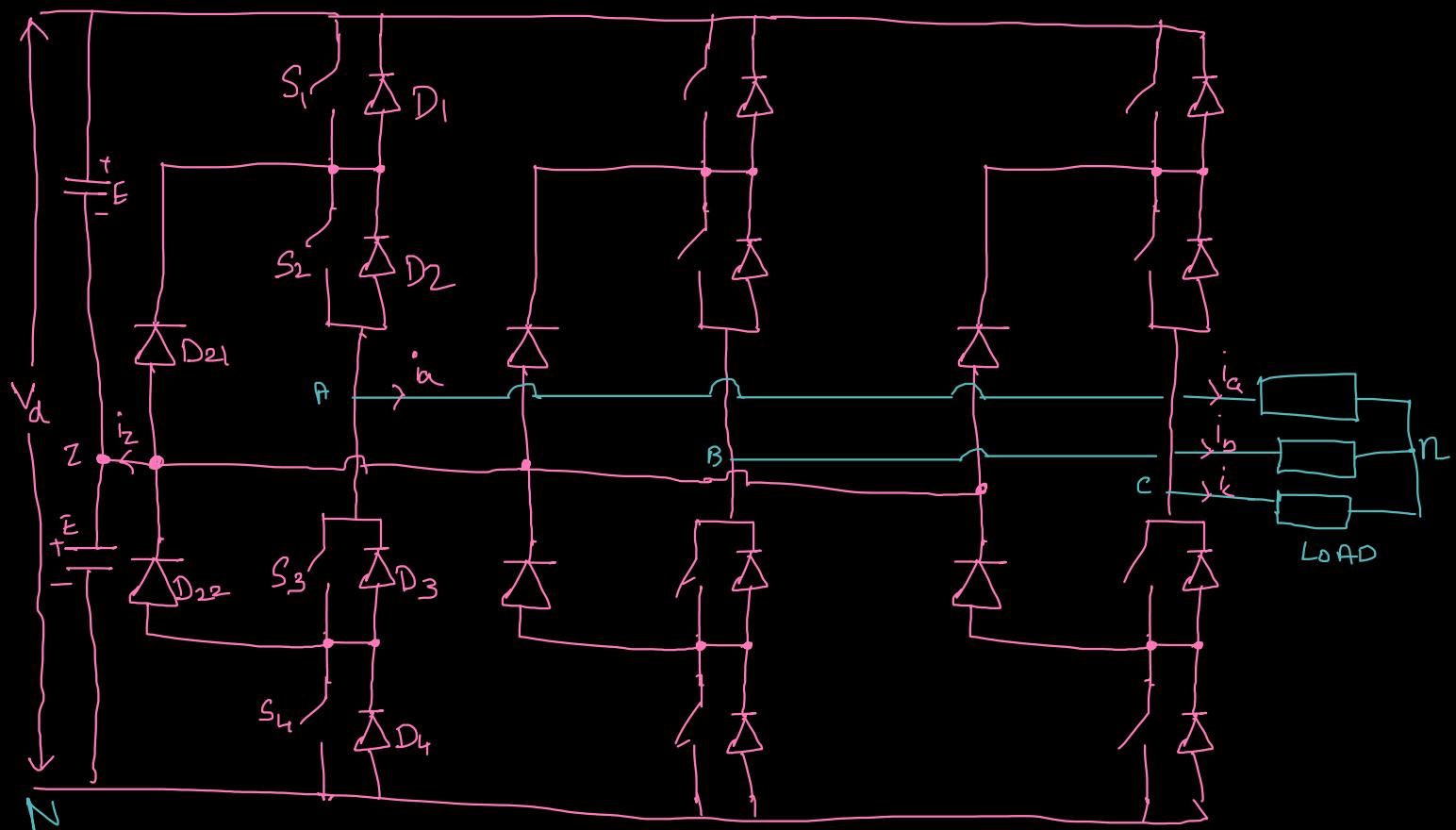
of the circuit.



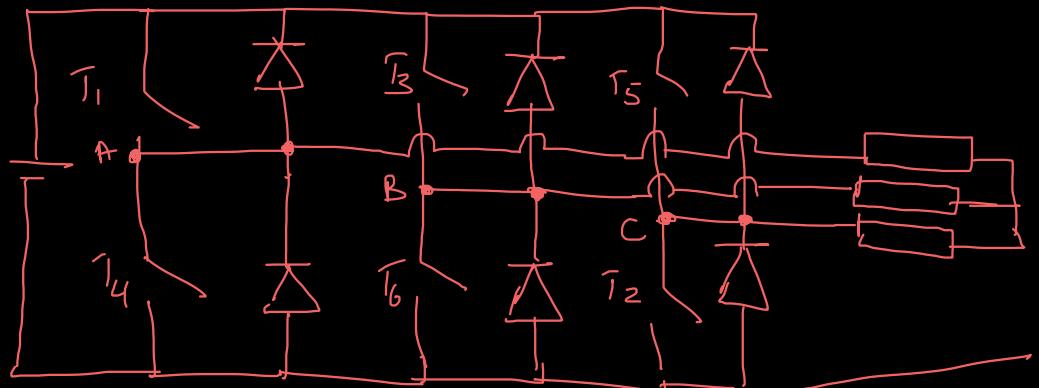
$S_1$  &  $S_2$  do not carry load current due to

Conduction of  $D_1$  &  $D_2$ .

Space Vector Modulation in 3 $\phi$  3 level inverter



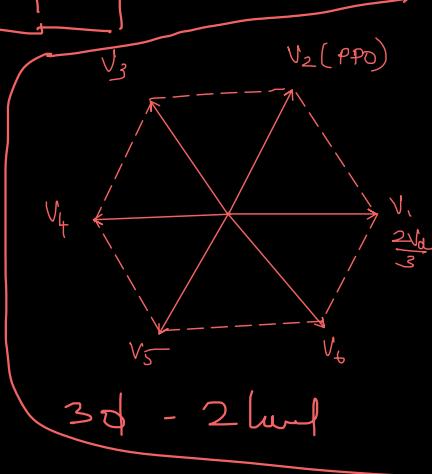
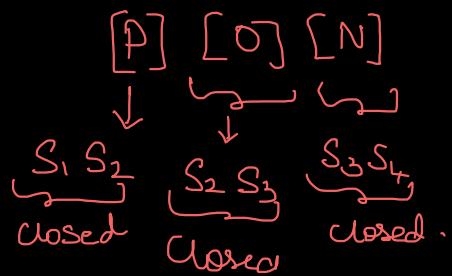
for 2 level  
 $3 \phi$   
 $\frac{2^3}{2} = 8$  States



for 3 level  $3\phi$ ,

$$3^3 = 27 \text{ States}$$

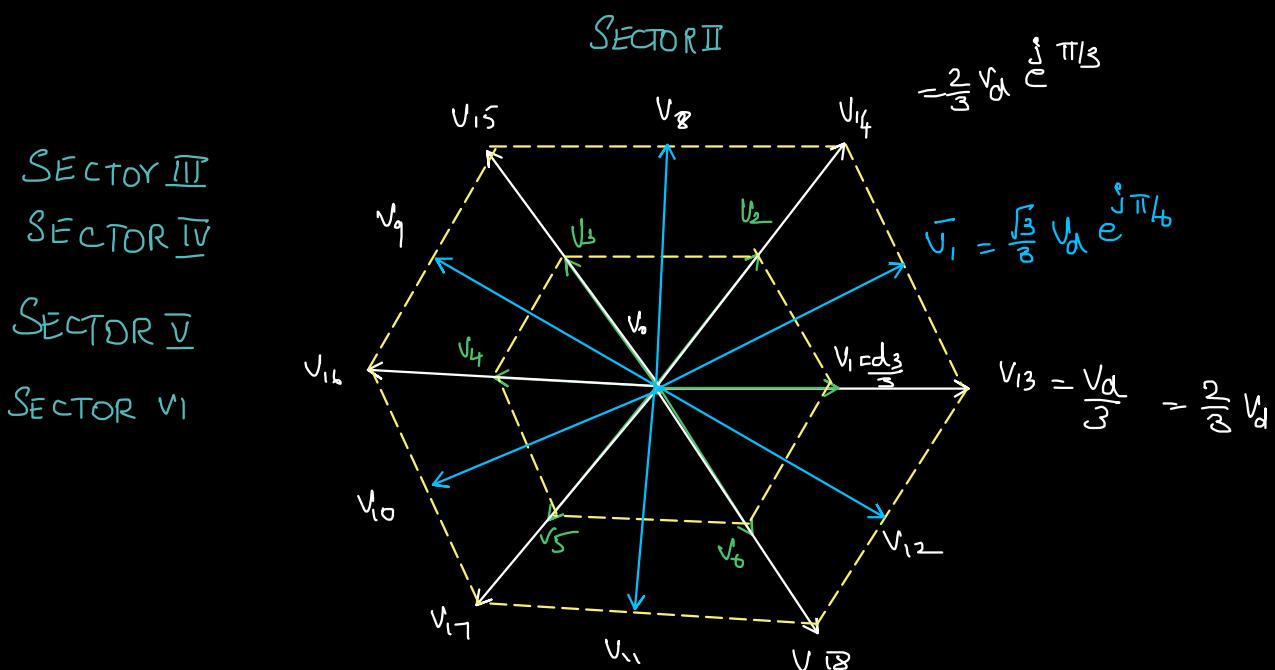
Each leg has 3 switching states



Total  $3^3 = 27$  possible switching states.

they are represented by 27 vectors.

These voltage vectors can be divided into 4 groups



## ① Zero Vectors

↳ represents 3 zero switching states

$$[PPP] \quad [OOO] \quad [NNN]$$

$$\text{magnitude of } V_0 = 0$$

## ② Small Vectors

$$V_1 \text{ to } V_6$$

Each small vector represents 2 switching states, that contain [P] state called P-type small vector

| - Contain [N] state called N-type small vector  
of magnitude  $V_{d\beta}$

## Medium Vectors

$$V_7 - V_{12}$$

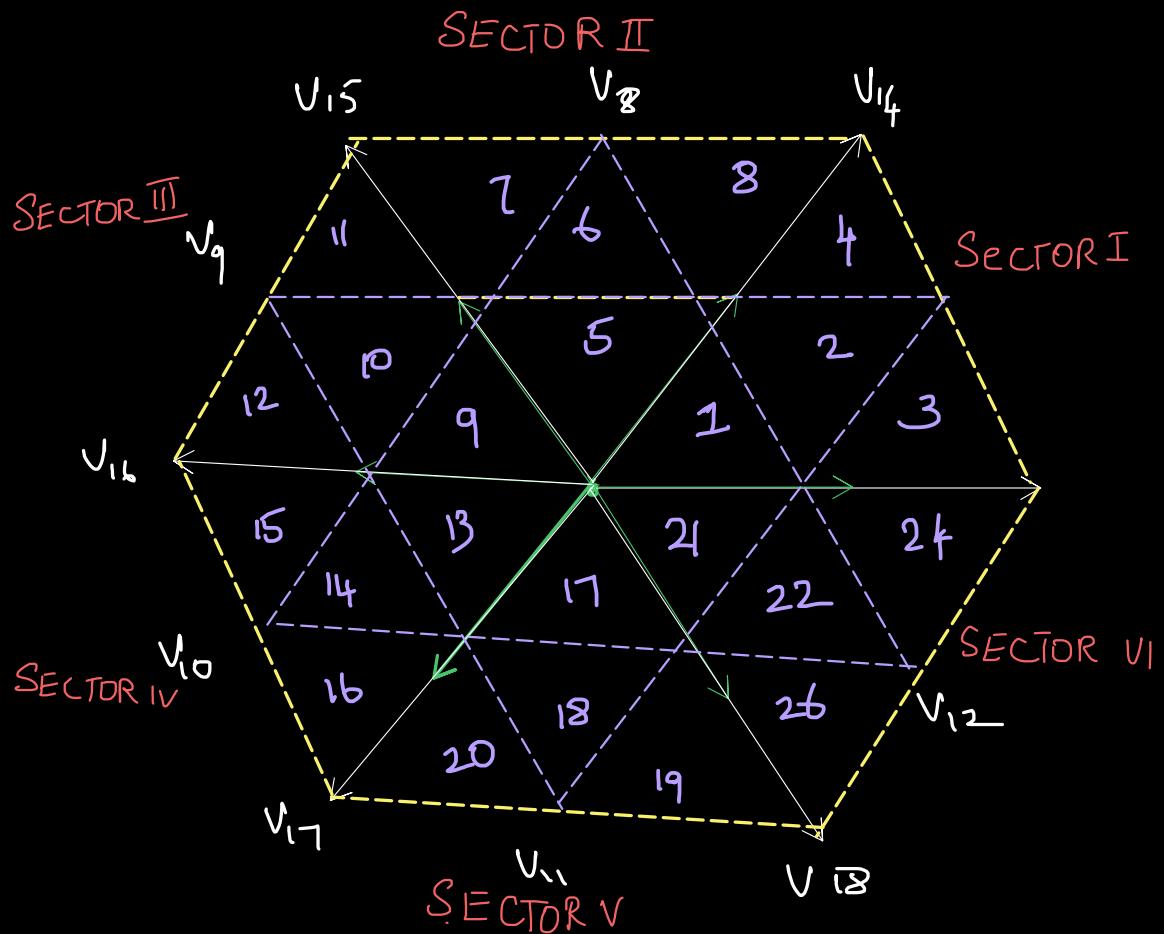
$$\text{magnitude } \frac{\sqrt{3}V_d}{3}$$

## Large Vectors

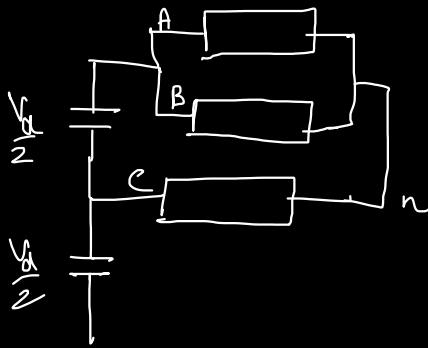
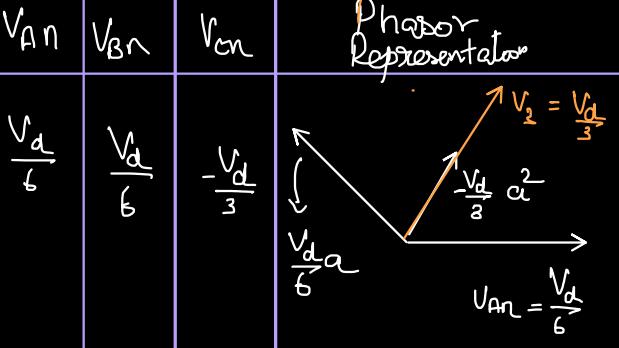
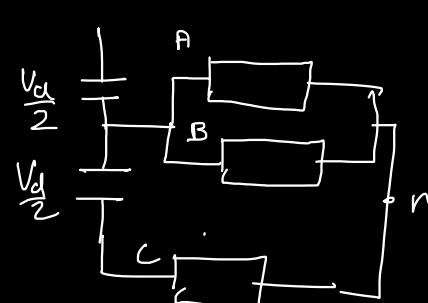
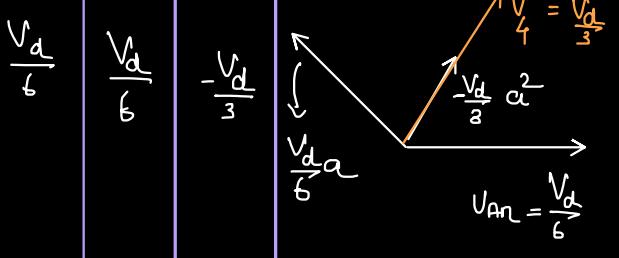
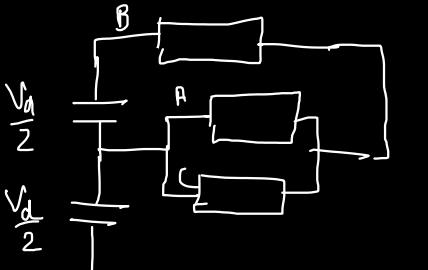
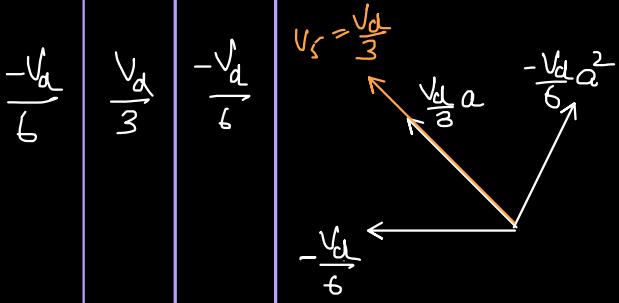
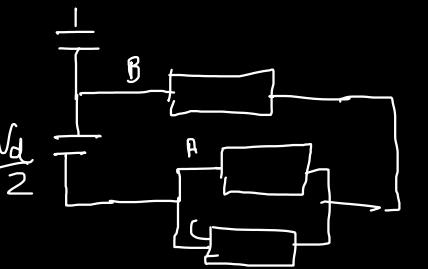
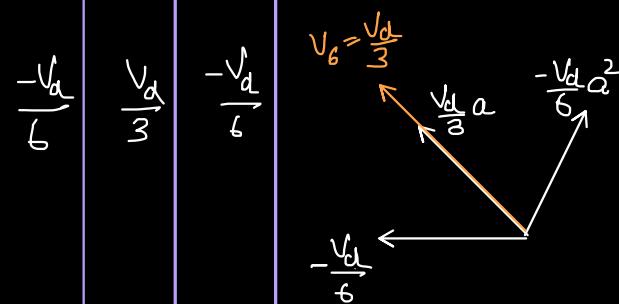
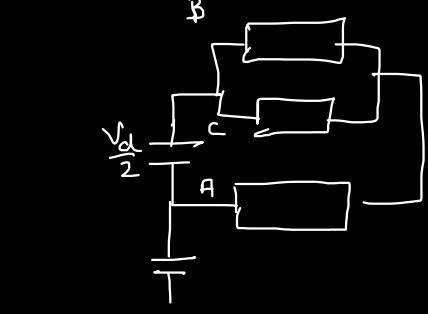
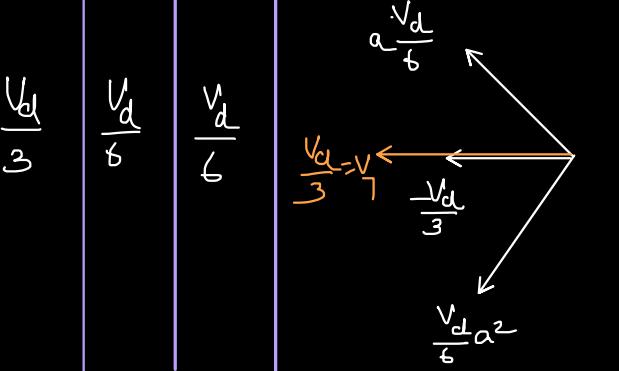
$$V_{13} - V_{18}$$

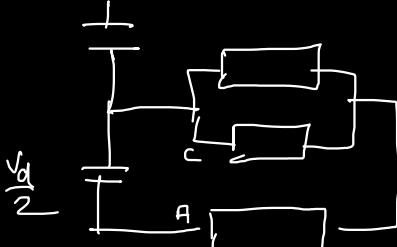
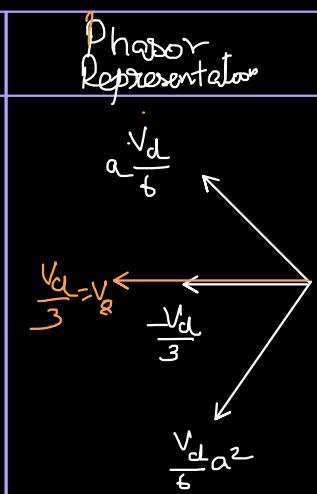
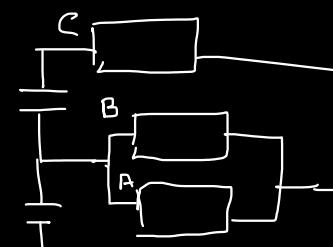
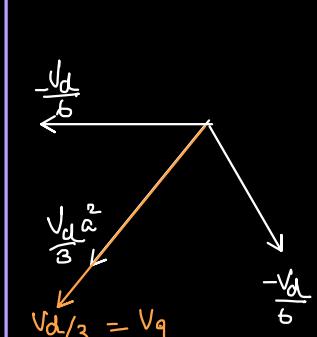
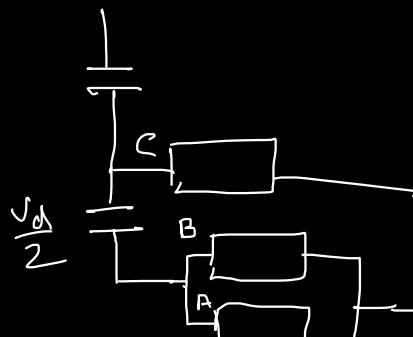
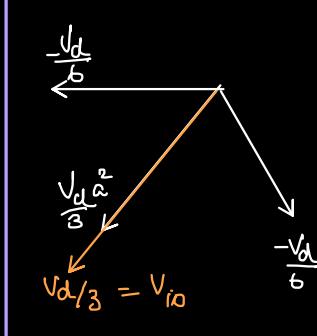
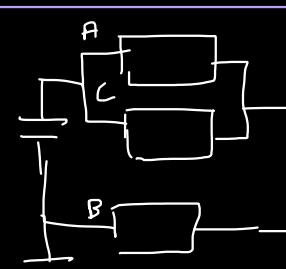
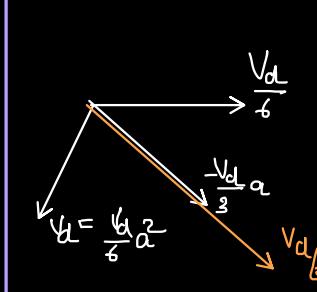
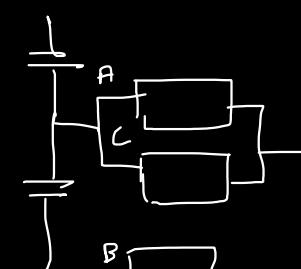
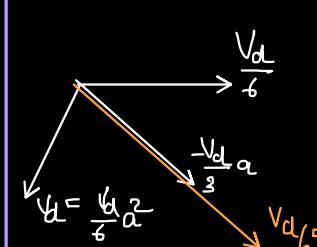
$$\text{magnitude } 2V_d \frac{\sqrt{3}}{3}$$

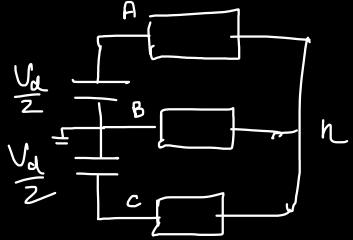
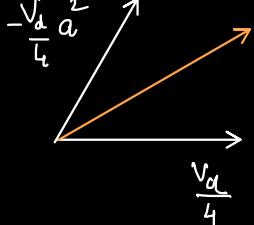
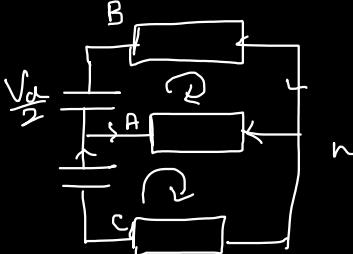
SPACE VECTOR	SWITCHING STATE	VECTOR CLASSIFICATION	VECTOR MAGNITUDE
$\vec{V}_0$	[PPP] [000] [NNN]	Zero Vector	0
$\vec{V}_1$	$\vec{V}_{1P}$	P00	$\frac{V_d}{3}$
	$\vec{V}_{1N}$	0NN	
$\vec{V}_2$	$\vec{V}_{2P}$	PP0	Small Vectors
	$\vec{V}_{2N}$	00N	
$\vec{V}_3$	$\vec{V}_{3P}$	0 P0	$\frac{V_d}{3}$
	$\vec{V}_{3N}$	N0N	
$\vec{V}_4$	$\vec{V}_{4P}$	0 PP	Medium Vectors
	$\vec{V}_{4N}$	N00	
$\vec{V}_5$	$\vec{V}_{5P}$	00P	$\frac{\sqrt{3}}{2} V_d$
	$\vec{V}_{5N}$	NN0	
$\vec{V}_6$	$\vec{V}_{6P}$	P0P	Large Vectors
	$\vec{V}_{6N}$	NON	
$V_7$	PON		
$V_8$	OPN		
$V_9$	NPO		
$V_{10}$	NOP		
$V_{11}$	DNP		
$V_{12}$	PND		
$V_B$	PNN		
$V_{14}$	PPN		
$V_{15}$	NPN		
$V_{16}$	NPP		
$V_{17}$	NNP		
$V_{18}$	PNP		



State	Equivalent Circuit	$V_{An}$	$V_{Bn}$	$V_{Cn}$	Phasor Representation
P00	<p> <math>V_{An} = \frac{V_d}{2} \times \frac{2}{3} = \frac{V_d}{3}</math>  <math>V_{Bn} = \frac{V_d}{2} \times \frac{1}{3} = \frac{V_d}{6}</math>  <math>V_{Cn} = \frac{V_d}{2} \times \frac{1}{3} = \frac{V_d}{6}</math> </p>	$\frac{V_d}{3}$	$-\frac{V_d}{6}$	$-\frac{V_d}{6}$	$V_s = \frac{2}{3} [V_{An} + aV_{Bn} + a^2V_{Cn}]$ $a^2 \left( -\frac{V_d}{6} \right) = a^2 V_{Cn}$ $V_1 = V_d / 3$ $V_{An} = V_d / 3$ $aV_{Bn} = a \left( -\frac{V_d}{6} \right)$
0NN	<p> <math>V_{An} = \frac{V_d}{2} \times \frac{2}{3} = \frac{V_d}{3}</math>  <math>V_{Bn} = \frac{V_d}{2} \times \frac{1}{3} = \frac{V_d}{6}</math>  <math>V_{Cn} = \frac{V_d}{2} \times \frac{1}{3} = \frac{V_d}{6}</math> </p>	$\frac{V_d}{3}$	$-\frac{V_d}{6}$	$-\frac{V_d}{6}$	$a^2 \left( -\frac{V_d}{6} \right) = a^2 V_{Cn}$ $V_d / 3 = V_2$ $V_{An} = V_d / 3$ $aV_{Bn} = a \left( -\frac{V_d}{6} \right)$

State	Equivalent Circuit	$V_{An}$	$V_{Bn}$	$V_{Cn}$	Phasor Representation
PPO		$\frac{V_d}{6}$	$\frac{V_d}{6}$	$-\frac{V_d}{3}$	
00N		$\frac{V_d}{6}$	$\frac{V_d}{6}$	$-\frac{V_d}{3}$	
OPO		$-\frac{V_d}{6}$	$\frac{V_d}{3}$	$-\frac{V_d}{6}$	
NON		$-\frac{V_d}{6}$	$\frac{V_d}{3}$	$-\frac{V_d}{6}$	
OPP		$-\frac{V_d}{3}$	$\frac{V_d}{6}$	$\frac{V_d}{6}$	

State	Equivalent Circuit	$V_{An}$	$V_{Bn}$	$V_{Cn}$	Phasor Representations
NOO		$-\frac{V_d}{3}$	$\frac{V_d}{6}$	$\frac{V_d}{6}$	
OOP		$-\frac{V_d}{6}$	$-\frac{V_d}{6}$	$\frac{V_d}{3}$	
NNO		$-\frac{V_d}{6}$	$-\frac{V_d}{6}$	$\frac{V_d}{3}$	
POP		$\frac{V_d}{6}$	$-\frac{V_d}{3}$	$\frac{V_d}{6}$	
ONO		$\frac{V_d}{6}$	$-\frac{V_d}{3}$	$\frac{V_d}{6}$	

State	Equivalent Circuit	$V_{An}$	$V_{Bn}$	$V_{Cn}$	Phasor Representator
PON		$\frac{V_d}{2}$	0	$-\frac{V_d}{2}$	
OPN					

State	Equivalent Circuit	$V_{An}$	$V_{Bn}$	$V_{Cn}$	Phasor Representator

# Desired output voltage of 3φ 3 level inverter

$$V_{An}^* = V_m^* \sin \omega^* t$$

$$V_{Bn}^* = V_m^* \sin(\omega^* t - 120^\circ)$$

$$V_{Cn}^* = V_m^* \sin(\omega^* t + 120^\circ)$$

$V_m^*$  → Desired output peak magnitude

$\omega^*$  → Desired output frequency.

This 3φ system results in a reference space vector  $\bar{V}_{ref}$  of magnitude  $V_m^*$  that rotates with angular velocity  $\omega^*$

The inverter switches are controlled between the nearest 3 vectors

When  $\bar{V}_{ref}$  lies in region I, the inverter state is switched between  $V_0, V_1, V_2$ .

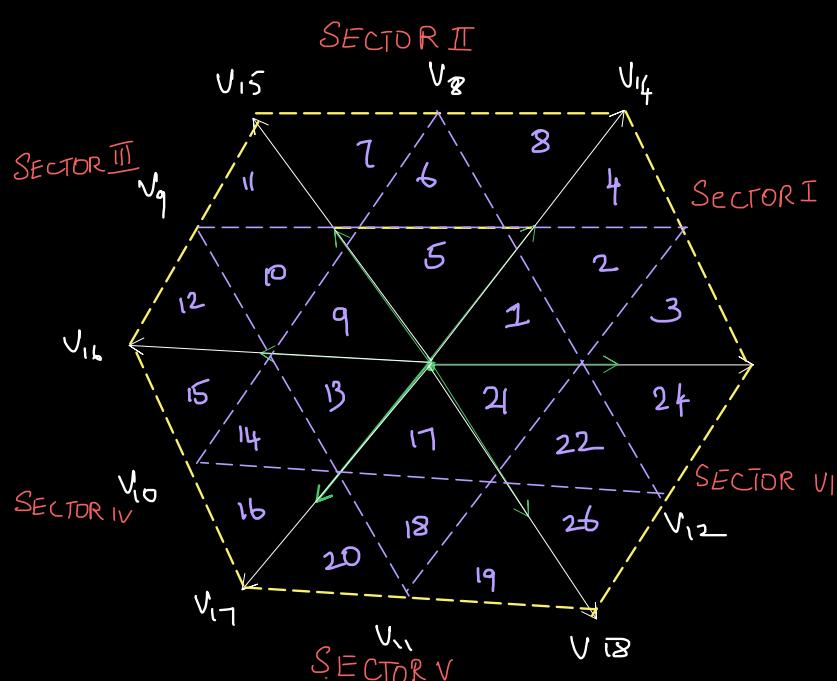
## Dwell Time Calculation

based on volt second balance principle,

Product of the reference voltage  $\times$  Sampling period.

$$= V_1 \times \text{interval allocated for } V_1 +$$

$$V_2 \times \text{interval allocated for } V_2 + V_0 \times \text{interval allocated for } V_0$$



Reference vector  $\vec{V}_{ref}$  can be synthesised by 3 nearest stationary vectors

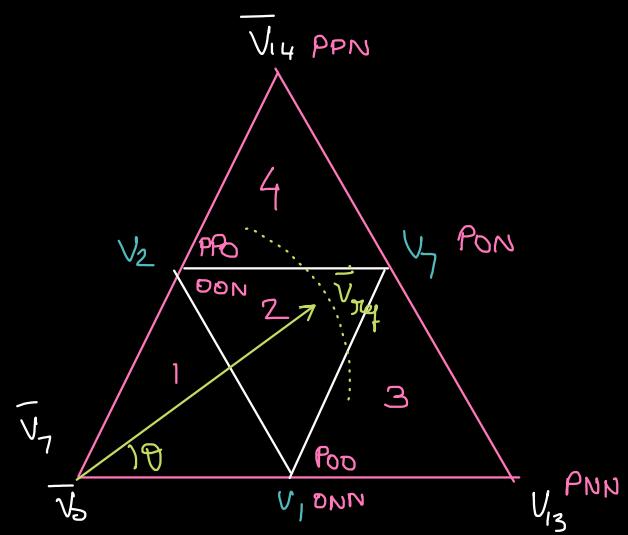
When  $\vec{V}_{ref}$  falls into region 2 of Sector I, 3 nearest vectors are.

$$V_1, V_7, V_2$$

Let,  
 $T_a, T_b, T_c$  are the dwell times for  $V_1, V_7, V_2$

$$V_1 T_a + V_2 T_b, V_7 T_c = V_{ref} T_s$$

$$T_a + T_b + T_c = T_s$$



The magnitude of voltagee  $V_1, V_2, V_7 \perp V_{ref}$  are

$$\bar{V}_1 = \frac{1}{3} V_d$$

$$\bar{V}_2 = \frac{1}{3} V_d e^{j\pi/3}$$

$$\bar{V}_7 = \frac{\sqrt{3}}{3} V_d e^{j\pi/6}$$

$$\bar{V}_{ref} = V_{ref} e^{j\theta}$$

$$\therefore \frac{1}{3} V_d T_a + \frac{1}{3} V_d e^{j\pi/3} T_b + \frac{\sqrt{3}}{3} V_d e^{j\pi/6} T_c = V_{ref} e^{j\theta} T_s$$

$$\frac{1}{3} V_d T_a + \frac{1}{3} V_d \left( \cos \frac{\pi}{3} + j \sin \frac{\pi}{3} \right) T_b + \frac{\sqrt{3}}{3} V_d \left( \cos \frac{\pi}{6} + j \sin \frac{\pi}{6} \right) T_c = V_{ref} \left( \cos \theta + j \sin \theta \right)$$

equaling Real parts

$$\frac{1}{3}V_d T_a + \frac{1}{3}V_d \cos\frac{\pi}{3} T_b + \frac{\sqrt{3}}{3}V_d \cos\frac{\pi}{6} T_c = V_{ref} \cos\theta T_s$$

$$T_a + \frac{3}{2}T_b + \frac{1}{2}T_c = 3 \frac{V_{ref}}{V_d} \cos\theta T_s \quad \text{--- (1)}$$

Imaginary Parts

$$\frac{\sqrt{3}}{2} T_b + \frac{\sqrt{3}}{2} T_c = 3 \frac{V_{ref}}{V_d} \sin\theta T_s \quad \text{--- (2)}$$

$$T_a + T_b + T_c = T_s. \quad \text{--- (3)}$$

Solving for  $T_a, T_b, T_c$ ,

$$\frac{\sqrt{3}}{2} (T_s - T_a) = 3 \frac{V_{ref}}{V_d} \sin\theta T_s$$

$$T_a = \left(1 - \frac{2\sqrt{3} V_{ref}}{V_d} \sin\theta\right) T_s$$

$$T_a = (-2m_a \sin\theta) T_s$$

$$T_b = \left[2m_a \sin\left(\frac{\pi}{3} + \theta\right) - 1\right] T_s$$

$$T_c = \left[1 - 2m_a \sin\left(\frac{\pi}{3} - \theta\right)\right] T_s$$

(for  $0 < \theta < \pi/3$ )

The maximum length of reference vector  $V_{ref\ max}$

Corresponds to the radius of largest circle that can be inscribed within the vector.

This is equal to the length of medium vector.

$$\overline{V}_{ref\ max} = \frac{\sqrt{3}}{3} V_d$$

$$m_{a\ max} = \frac{\sqrt{3} V_{ref\ max}}{V_d}$$
$$= \frac{\sqrt{3} \times \sqrt{3} V_d}{3 V_d} = 1$$

Range of  $m_a$  is 0-1

$$0 \leq m_a \leq 1$$

Region 1  $\rightarrow \vec{V}_o \vec{V}_{1P} \vec{V}_{2P}$

Region 2  $\rightarrow \vec{V}_1 \vec{V}_7 \vec{V}_2$

Region 3  $\rightarrow \vec{V}_1 \vec{V}_{L3} \vec{V}_7$

Region 4  $\rightarrow \vec{V}_2 \vec{V}_7 \vec{V}_{L4}$

Relation between  $V_{ref}$  location & dwell time

Assume that the head  
of  $V_{ref}$  point points  
to center Q of region 4

Distance Q to  $v_2, v_2, v_4$

are the same.

The dwell times of  
these vector should  
be identical

When,  $V_{ref}$  moves moves forward, longer will be  
the dwell time for  $v_2$  &  $v_4$

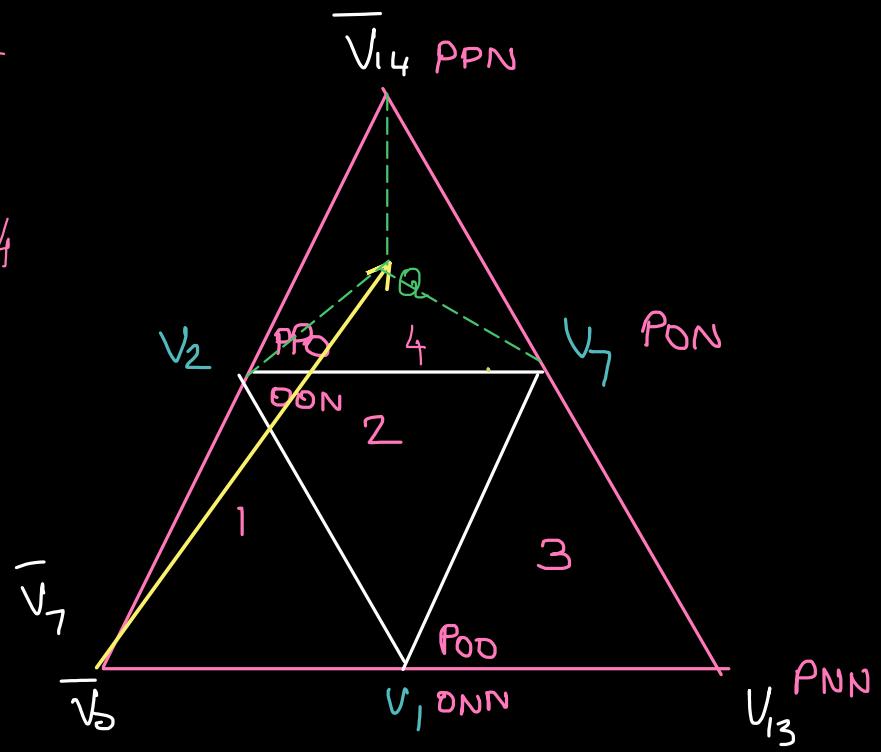
When  $V_{ref}$  coincides with  $v_2$ , the dwell time  
for  $T_c$  for  $v_2$  is  $T_s$

$T_a + T_b$  for  $v_{14} \& v_7$  diminishes to 0.

Neutral point Voltage  $v_z$

Voltage between the neutral point z and negative  
dc bus is defined as neutral point voltage

ideally across  $C_{d1} \& C_{d2}$  voltage should be  
equal and exactly  $\frac{V_d}{2}$



It depends on the switching state of NPC inverter

Assume that the inverter is in motoring mode

i.e) power flows from DC source  
↓  
AC load.

## Effect of Switching States on Neutral point voltage derivation

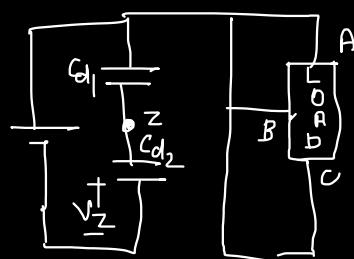
### Assumptions

- \* Inverter is in motoring mode
- \* Power flow: DC  $\rightarrow$  AC

## ★ Zero Vector State $V_0$ [PPP]

- \* Inverter terminals A B & C are connected to +ve bus

- \* The neutral point Z is left unconnected



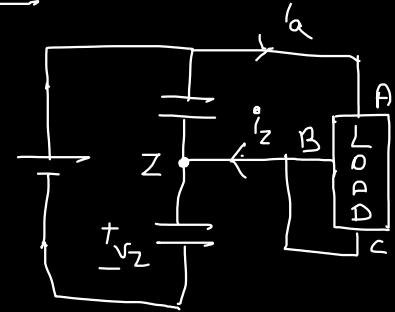
- \* This switching states doesn't affect  $V_Z$

- \* i.e. [000] [NNN] doesn't cause  $V_Z$  shift.

## Effect of Positive Small Vector State on $V_Z$

$V_1 [P00]$

\* Terminal A is connected to +ve dc bus



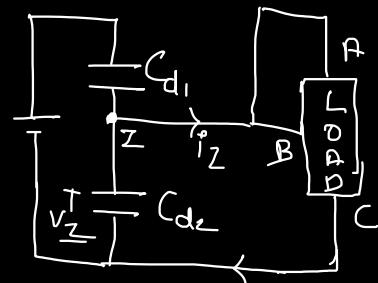
\* B & C are connected to Z

\* Neutral current  $i_z$  flows to Z causing  $V_Z$  to increase

## Effect of Negative Small Vector State on $V_Z$

$V_1 [DNN]$

\* Inverter terminal A is connected to Z



\* B & C  $\rightarrow$  -ve dc bus

\* Neutral current  $i_z$  flows out of Z, causing  $V_Z$  to decrease (discharging)

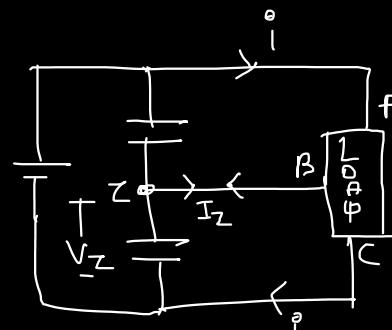
## Effect of Medium Small Vector State on $V_Z$

$V_7 [P0N]$

A  $\rightarrow$  +ve dc bus

B  $\rightarrow$  Z

C  $\rightarrow$  -ve dc bus.



$i_z \rightarrow$  depends on load & currents in other arms

Depending on the inverter operating condition, the

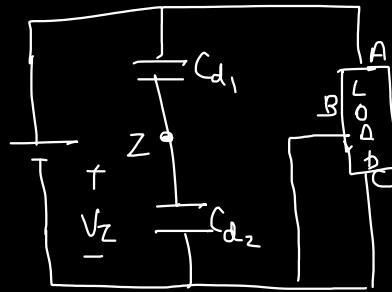
neutral point Voltage  $V_Z$  may rise or drop depending on the instantaneous value of  $I_Z$ .

## Effect of Large Vector State on $V_Z$

$V_{13}$  [PNN]

A  $\rightarrow$  +ve dc bus

B, C  $\rightarrow$  -ve dc bus



Z is left unconnected. So there is no deviation in  $V_Z$

In conclusion :

Zero vectors }  
Large vectors } dont affect  $V_Z$

Small Vectors

$\rightarrow$  P-type  $\rightarrow V_Z$  increases

$\rightarrow$  N-type  $\rightarrow V_Z$  decreases

Medium Vectors

$\hookrightarrow$  affects  $V_Z$  but direction of deviation is uncertain.

## Design of Switching Sequence

Switching sequence is selected after considering the following factors

① Transition from one state to next

Should involve only 2 switches in the same leg

② Transitions from one sector or region

to next Should involve zero or minimum switching

③ Neutral point voltage deviation  
Should be minimum.

## Switching Sequence with minimal neutral point voltage deviation

\* P type small vector causes  $V_Z$  to rise while N type cause  $V_Z$  to fall.

\* Dwell period is calculated for a small vector during one sampling period  $T_S$

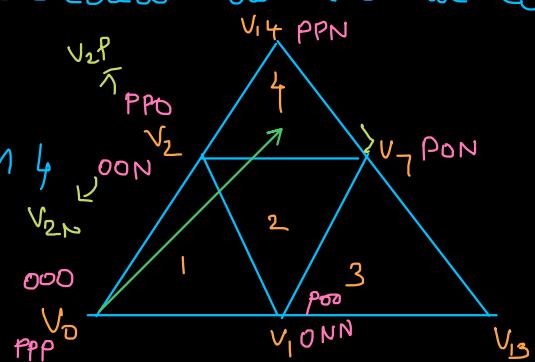
It is equally divided into 2 halves

And allotted to each of the small vectors (P+N type) available @ the point.

## Case(i)

One Vector among the 3 Selected is a Small Vector.

\* Consider that  $V_{ref}$  is in region 4 of Sector I



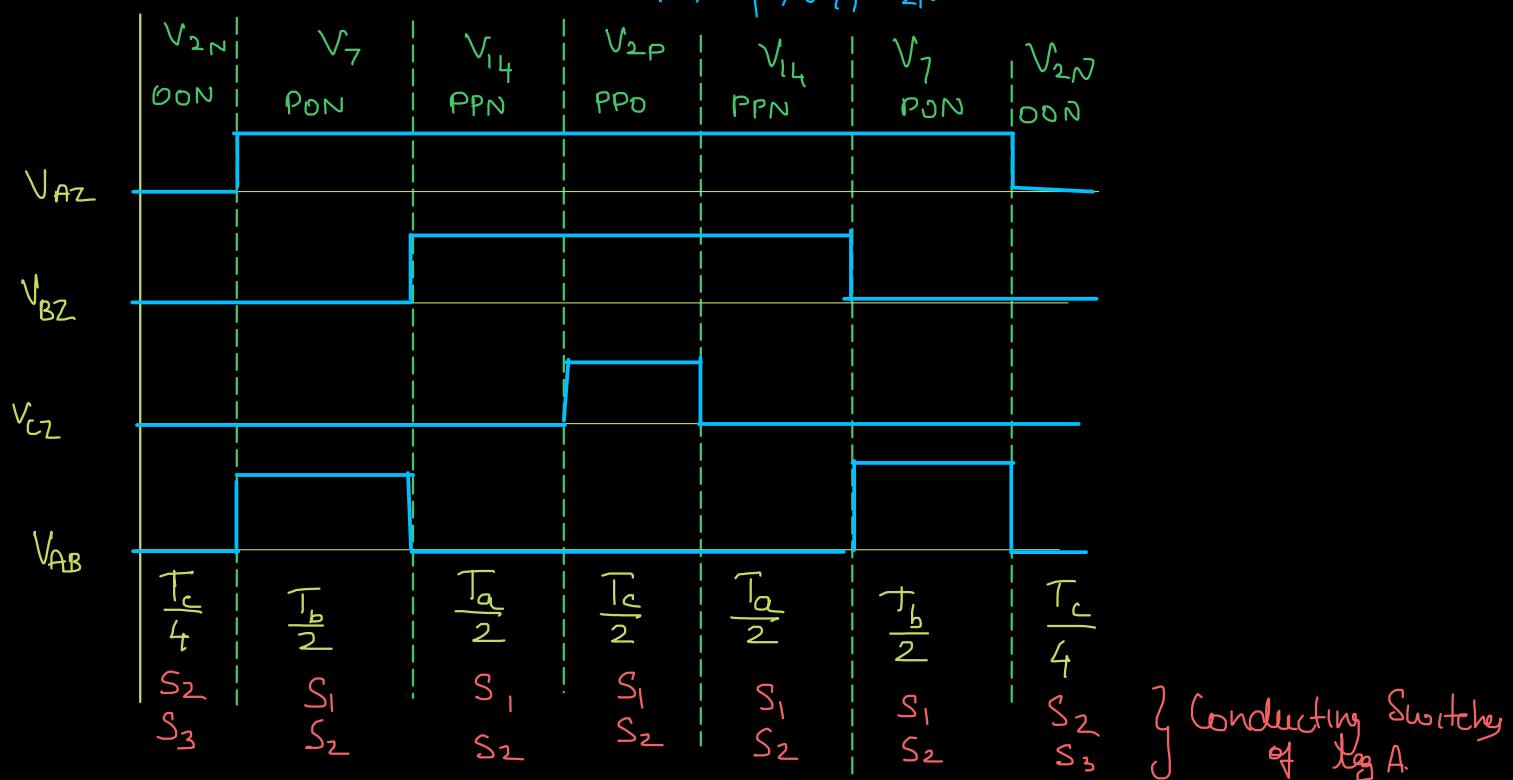
\* It can be synthesised by one small vector  $V_2$  + medium vector  $V_7$  + one large vector  $V_{14}$ .

\* The small vector  $\overrightarrow{V_2}$  has 2 switching states  
[PP0] + [OON] recent to  $V_{ref}$ .

\* The dwell time for  $V_2$  should be equal between the states [PP0] [OON]

\* Switching Sequence is  $V_2, V_7, V_{14}$

$$V_{2N}, V_7, V_{14}, V_{2P}, V_{14}, V_7, V_{2N}$$



Sampling period of PWM pattern ( $T_s = T_a + T_b + T_c$ )

During the transition from [OON] to [PON]  $S_1$  is turned on &  $S_3$  is turned off.

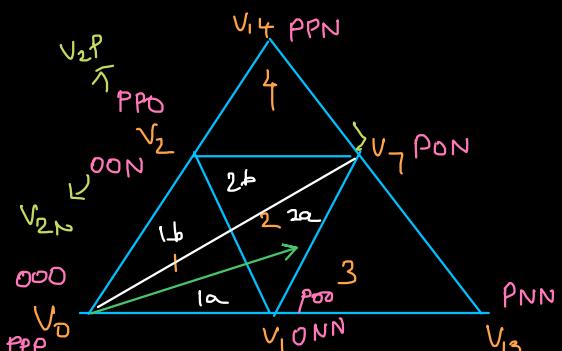
Dwell time for  $T_c$  for small vector  $V_2$  is equally divided between P+N switching states to minimize  $V_2$  deviation.

Only 2 switches in a leg are turned on --.

Case (ii) 2 Small Vectors among 3 Selected Vectors

When  $V_{ref}$  is in region 1 or 2 of Sector I, 2 of 3 Selected Vectors are Small Vectors

To reduce neutral voltage deviation each of the 2 regions is further divided into 2 sub regions  $(1a, 1b), (2a, 2b)$



Assume  $V_{ref}$  lies in region 2a.

It can be approximated by  $V_1, V_2, V_4$

$v_{ref}$  is closer to  $v_1$  than  $v_2$ ,

Dwell time  $T_a$  for  $v_1$  is longer than  $T_c$  for  $v_2$

The Vector  $v_1$  is referred to as dominant vector

whose dwell time is equally divided between  $v_{1P} \leftarrow v_{1N}$

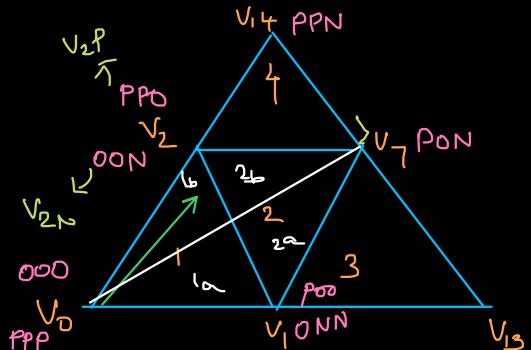
Switching seq

$v_{IN}$	$v_2$	$v_1$	$v_{1P}$	$v_1$	$v_2$	$v_{1N}$
0NN	00N	P0N	P00	P0N	00N	0NN
$\frac{T_a}{4}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_a}{4}$

In region 2b or 4b,  $v_{ref}$  is closer to  $v_2$

So  $v_2$  is dominant

time is equally divided  
between  $v_{2P} \leftarrow v_{2N}$



00N	P0N	P00	PPO	P00	P0N	0NN
$\frac{T_c}{4}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$	$\frac{T_c}{2}$	$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{4}$

### Causes of Neutral Point Deviations

In addition to influence of Small + Medium Voltage Vectors,  $v_2$  may also be affected by,

\* Unbalanced dc capacitors due to manufacturing tolerances

\* In Constant in switching device char

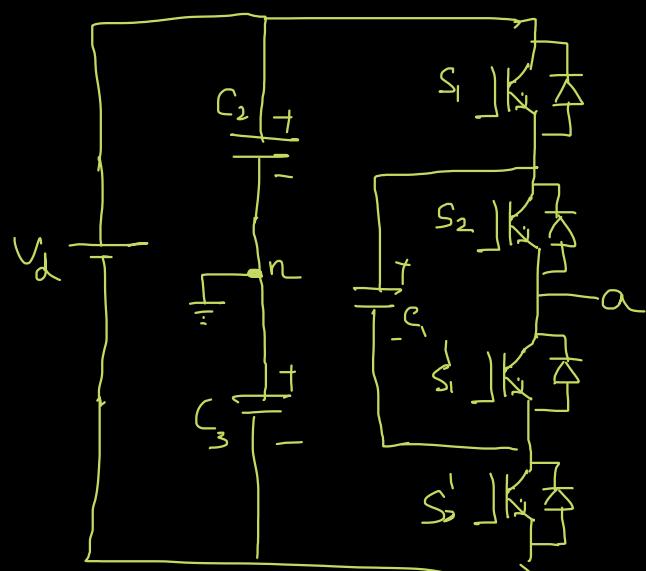
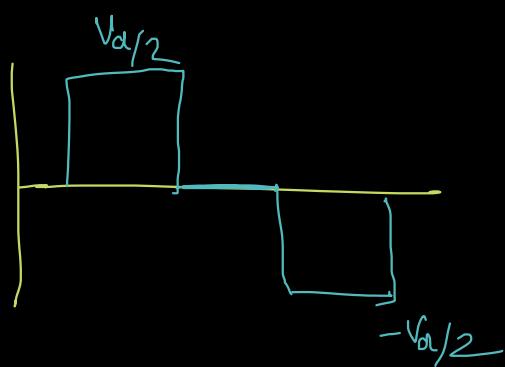
\* Unbalanced 3φ operations.

To minimize the neutral point voltage

Shift, a feedback control scheme can be implemented where a neutral point voltage is detected & controlled.

Three level capacitor clamped MLI  
(6v)

Flying Capacitor ML



$$\text{for } V_{an} = +\frac{V_d}{2}$$

$S_1, S_2 \rightarrow \text{closed}$

$$V_{an} = V_{C2} = V_d/2$$

$$V_{an} = -\frac{V_d}{2}$$

$S'_1, S'_2 \rightarrow \text{closed}$

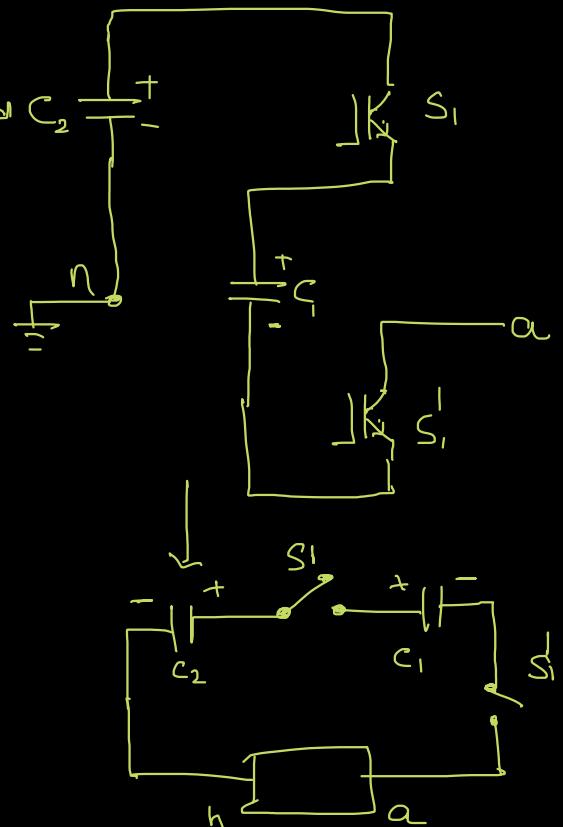
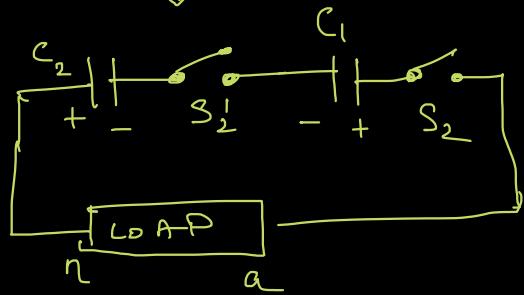
$$V_{an} = \frac{V_d}{2} = -\frac{V_d}{2}$$

For  $V_{an} = 0$

$S_1, S_1'$  are closed

or

$S_2, S_2'$  are closed



5-level capacitor clamped MLI

for  $V_{an} = +V_d/2$

$S_1, S_2, S_3, S_4 \rightarrow \text{closed}$

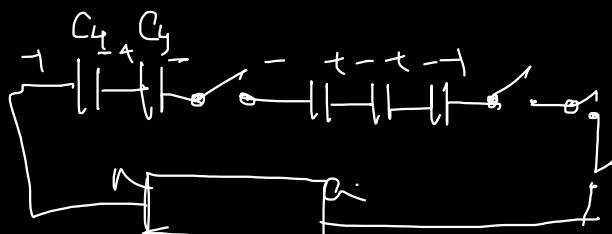
$$V_{an} = -\frac{V_d}{2}$$

$S'_1, S'_2, S'_3, S'_4 \rightarrow \text{closed}$

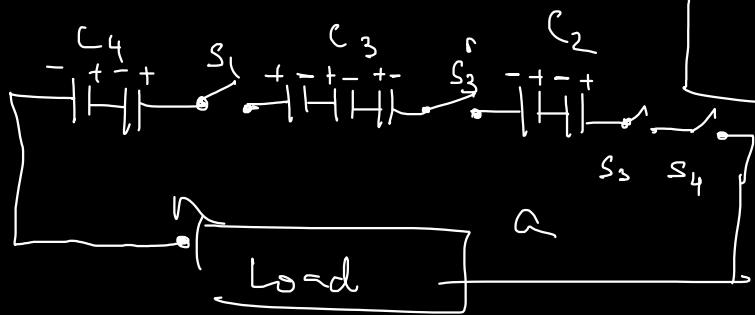
$$V_{an} = \frac{V_d}{4}$$

①  $S_1, S_2, S_3, S'_1 \rightarrow \text{closed}$

②  $S_4, S_3, S_2, S'_4 \rightarrow \text{closed}$

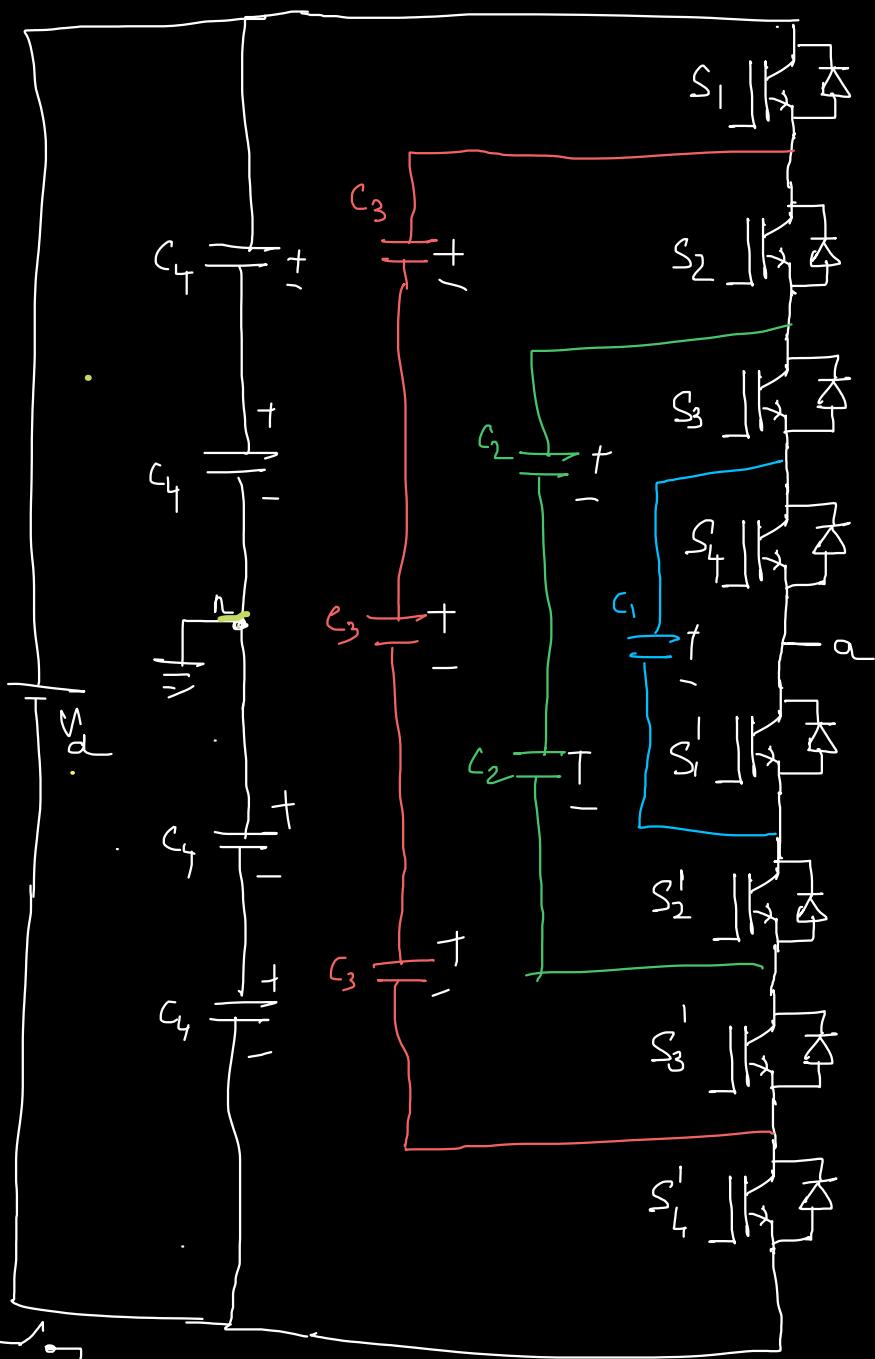
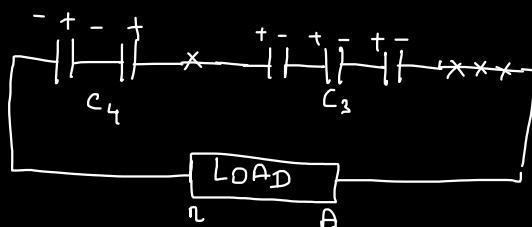


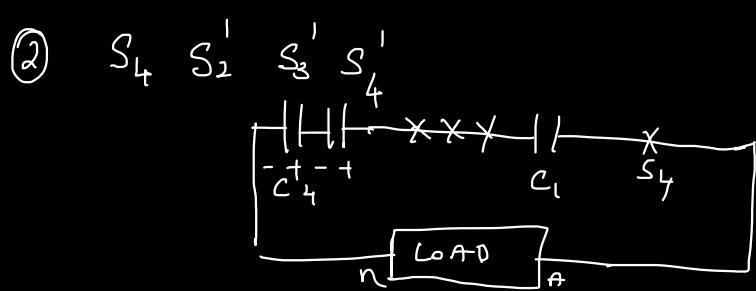
③  $S_4, S_3, S'_3, S_1$



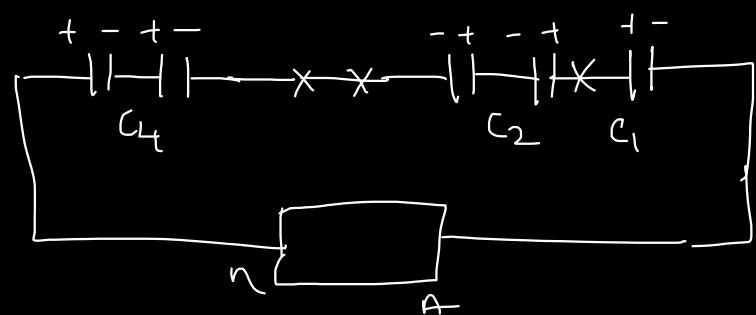
For  $V_{an} = -V_d/4$

①  $S'_1, S'_2, S'_3, S_1 \rightarrow \text{closed}$



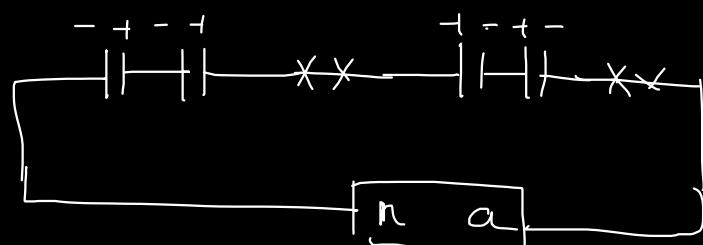


③  $S_1' \ S_3 \ S_3' \ S_4' \rightarrow \text{closed}$

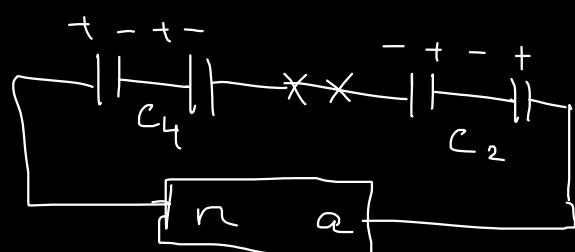


For  $V_{an} = 0$

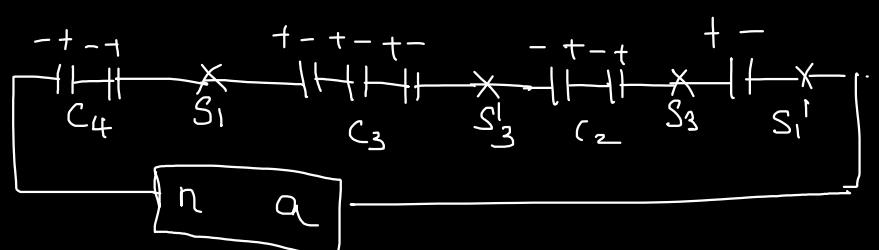
①  $S_1 \ S_2 \ S_1' \ S_2' \rightarrow \text{ON}$



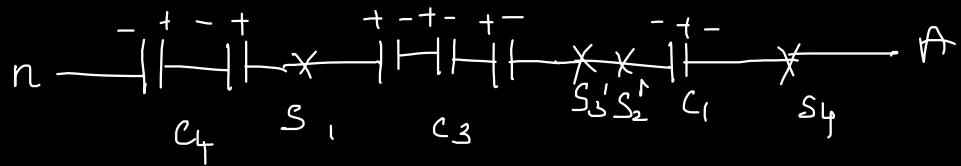
②  $S_3 \ S_4 \ S_3' \ S_4'$



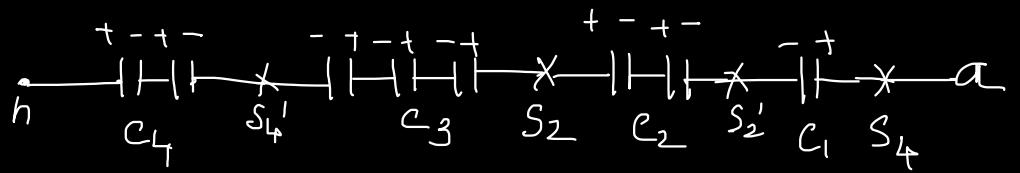
③  $S_1 \ S_3 \ S_1' \ S_3'$



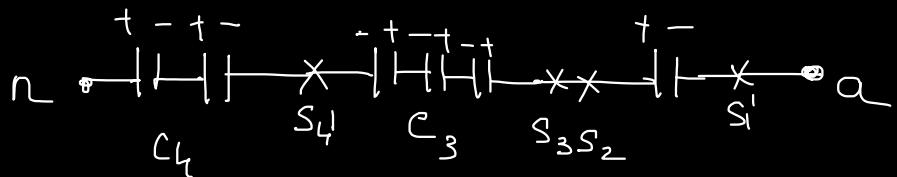
(4)  $S_1 \quad S_4 \quad S_2' \quad S_3'$



$$\textcircled{5} \quad S_2 \ S_4 \ S_2' \ S_4'.$$



(6)  $S_1 S_3 S'_1 S'_4$



Investors are generally classified

→ VSI

↳ produces defined voltage waveform  
for the load

↳ CSI

↳ produces defined current waveform  
for the load.

## Current Source Inverter

\* Power Transfer takes place between an adjustable direct current source & an ac load.

\* Op has defined current waveform

\* Current Source (Front end of CSI)

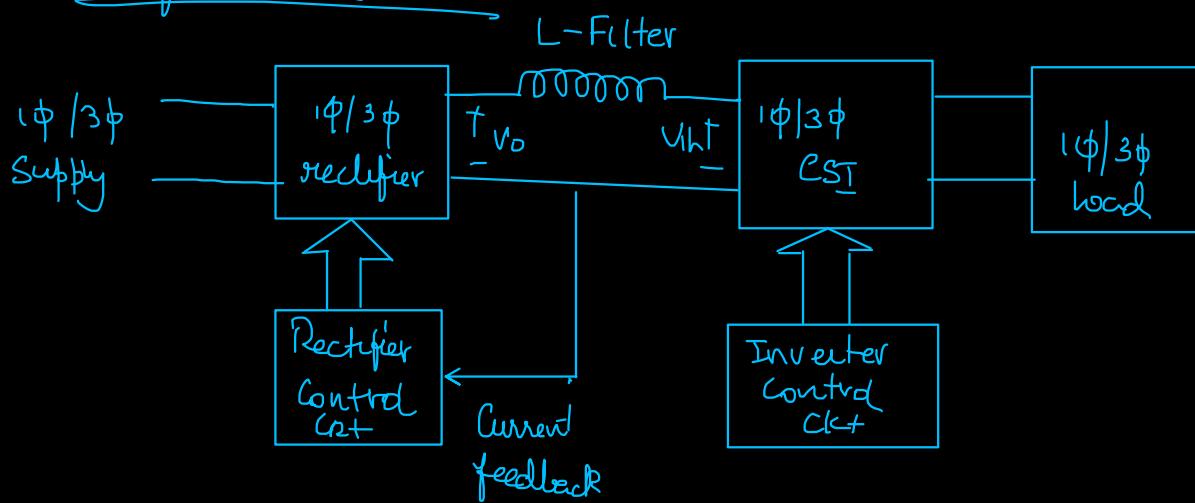
- ↳ Controlled rectifier bridge or dc chopper
- ↳ Filter is connected to get ripple free op current which is ip to the inverter

\* Inverter

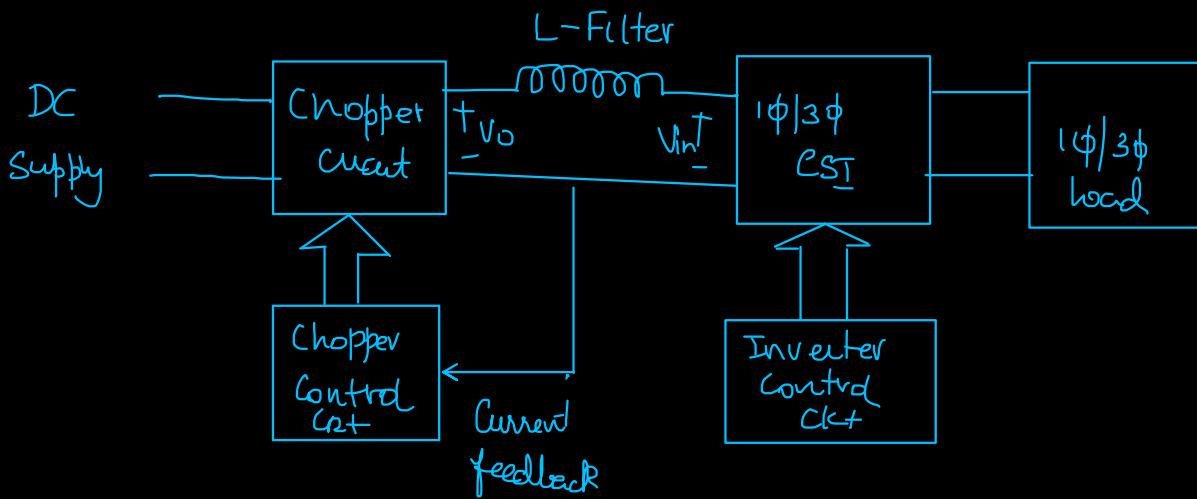
Converts dc @ input to Ac @ op.

Freq & Mag of op controlled by the control circuitry of inverter

CSI from AC Source



CSI From DC Source



Types of CSI used in MR drive

- ↳ Load Commutated inverters (LCI)
- ↳ PWM inverters

LCI employs Thyristors whose commutation is achieved by additional commutating circuits

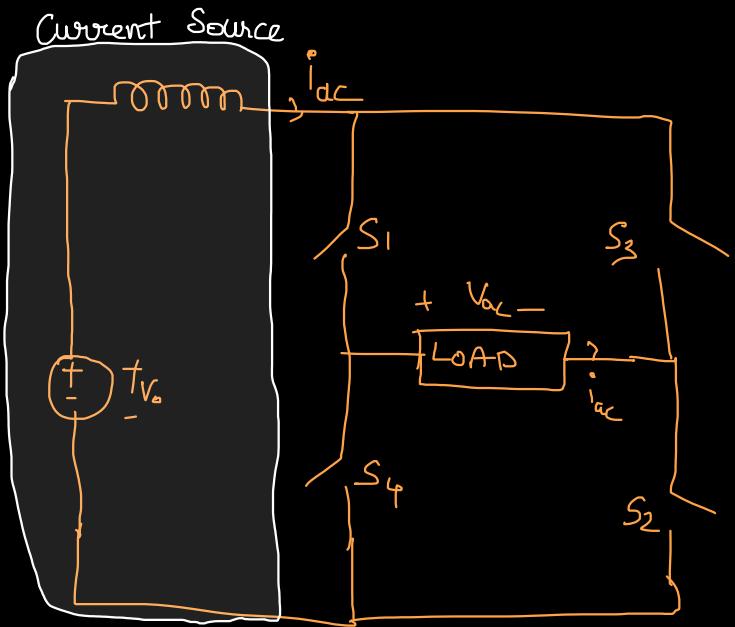
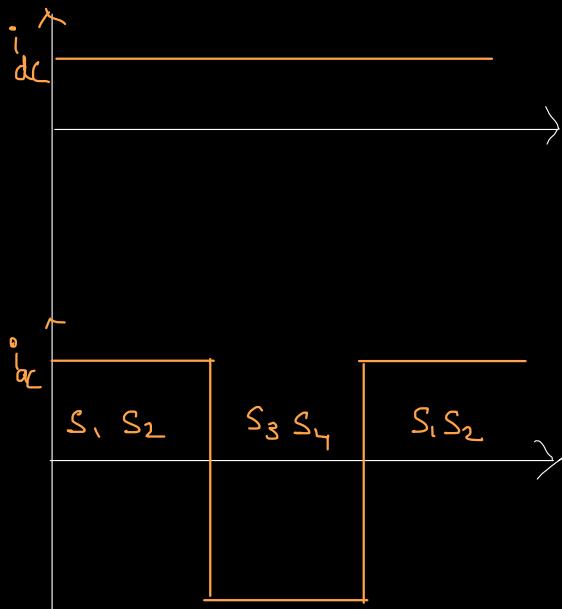
Suitable for large Synch Motor drives with a power rating up to 100 MW

PWM inverters uses switching devices with self extinguishable capability

no gate signal  $\downarrow$  OFF.

# Load Commutated Inverter ('DUBE')

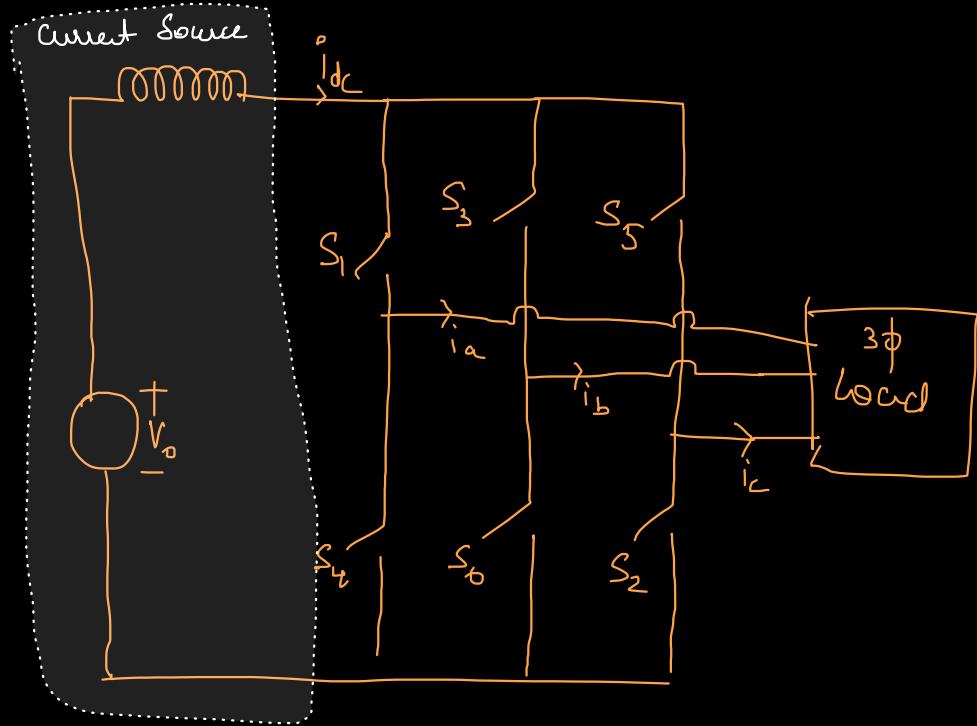
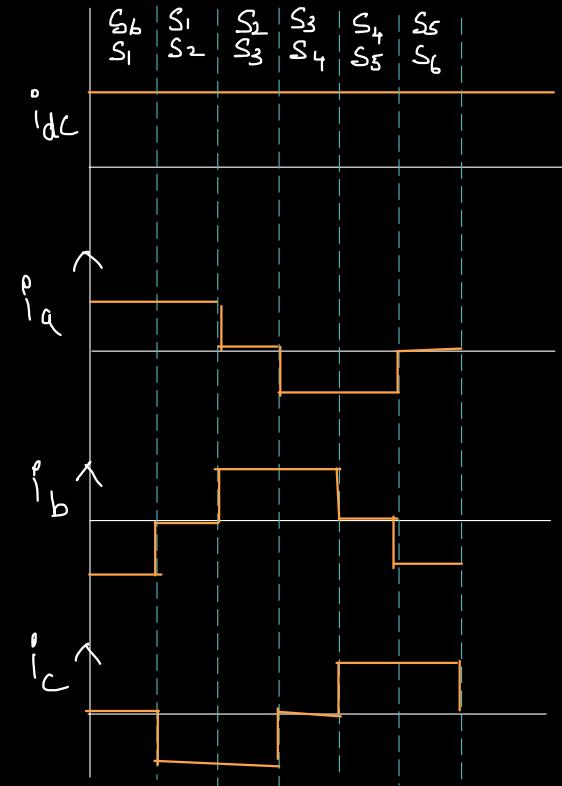
## 1φ CSI with ideal Switches



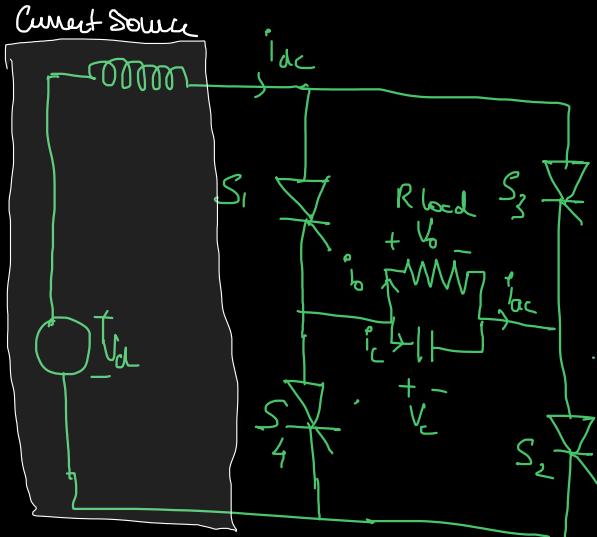
\* Load current has defined shape.

\* Load voltage depends on nature of load.

## 3φ CSI with ideal switches :



# 1φ Capacitor Commutated Current Source Inverter :



$$T \rightarrow \text{output period} = \frac{1}{f}$$

For  $t < 0$

$S_3, S_4$  were conducting  
So load current  
 $i_o \rightarrow -V_e$   
 $\Rightarrow V_c = -V_e$   
 $i_{dc} \rightarrow \text{const}; i_{S1} = i_{S2} = 0$   
 $i_{AC} = -i_{dc}$

@  $t = 0$

$S_1, S_2 \rightarrow \text{ON}$

$\Rightarrow$  Capacitor voltage

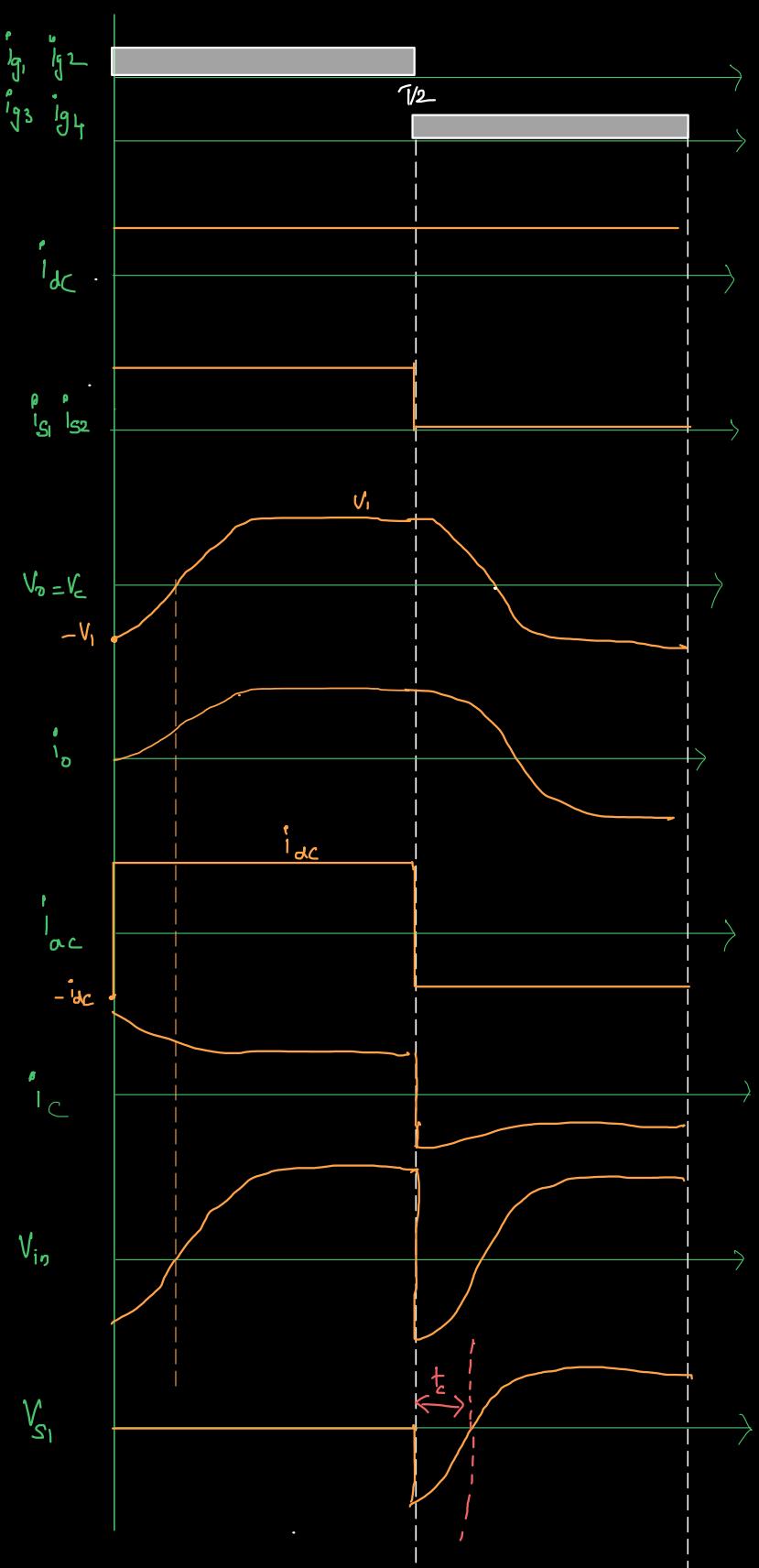
comes across  $S_3 + S_4$ ,  
so they are turned off  
this is called Complementary  
voltage Commutation.

During  $0 - T/2$

$S_1, S_2 \rightarrow \text{ON}$   
 $S_3, S_4 \rightarrow \text{OFF}$

Capacitor gets charged  
to  $-V_1$  to  $V_1$

$$i_o = \frac{V_e}{R} ; i_c = i_{AC} - i_o = i_{dc} - i_o ; I_{S1} = I_{AC}$$



@  $t = \frac{T}{2}$

$S_3 \wedge S_4 \rightarrow$  turned on

$S_1 \wedge S_2$  are commutated

between,  $\frac{T}{2} - T$

$S_3 \wedge S_4 \rightarrow ON$

$S_1 \wedge S_2 \rightarrow OFF$

$$\overset{\circ}{i}_{ac} = -\overset{\circ}{i}_{dc}$$

$$V_D = -V_I$$

$$V_{in} = -V_C$$

$$V_{S1} = -V_C \rightarrow (\text{commutation})$$

$$i_D = \frac{V_C}{R}$$

$$i_C = i_{ac} - i_D = -i_{dc} - i_D$$

$$i_{S3} = i_{dU} = i_{S4}$$

Turn off time ( $T_2$ ) of switch should be selected

Such that it should be less than  $T_c$

\*  $\overset{\circ}{i}_{ac}$  has a definite shape and resolved into its Fourier components.

\* The fundamental component of  $\overset{\circ}{i}_{ac}$  is at the frequency of  $1/T$

\* Period  $T$  is determined by the gating circuit as per operating frequency requirement

$$i_{ac} = \sum_{n=1,3,5}^{\infty} \frac{4I_{dc}}{n\pi} \sin(n\omega t)$$

$$i_D = i_{ac} \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \rightarrow RIC$$

$$= \frac{i_{ac}}{\sqrt{1 + (n\omega RC)^2}}$$

$$\dot{i}_o = \sum_{n=1,3,5,\dots}^{\infty} \frac{4I}{n\pi} \sin(n\omega t + \phi_n) \frac{1}{\sqrt{1 + (n\omega RC)^2}}$$

$$\phi_n = \tan^{-1}(n\omega RC)$$

$$\omega = 2\pi f = \frac{2\pi}{T}$$

- \* Higher order harmonics are bypassed through Capacitor
- \* Load Current & Voltage waveforms depend on relative values of R & C

## Time Domain Analysis

$$0 < t < \frac{T}{2} \quad V_o(t) = i_o(t)R = V_c(t)$$

$$= -V_i + \frac{1}{C} \int_0^t [I_{dc} - i_o(t)] dt$$

$$i_o(0) = -I_i$$

$$-V_i = -I_i R$$

$$i_o(t)R = -I_i R + \frac{1}{C} \int_0^t [I_{dc} - i_o(t)] dt$$

$$D i_o(t)R = 0 + \frac{1}{C} [I_{dc} - i_o(t)]$$

$$D i_o(t)R + i_o(t) = \frac{I_{dc}}{C}$$

$$i_o(t) = I_{dc} \left( 1 - e^{-t/RC} \right) - I_1 e^{-t/RC}$$

②  $t = T/2$ ,  $i_o(t) = +I_1$

$$I_1 = I_{dc} \left( 1 - e^{-T/2RC} \right) - I_1 e^{-T/2RC}$$

$$= I_{dc} \frac{\left( 1 - e^{-T/2RC} \right)}{\left( 1 + e^{-T/2RC} \right)}$$

$| \quad T \gg 2RC$

$I_1 \approx I_{dc}$

$i_o(t) = I_{dc} \left[ 1 - \frac{2e^{-t/RC}}{1 + e^{-T/2RC}} \right]$

- \*  $t_c$  is the interval in which the device remains reverse biased
- \* It depends on  $R, C$  &  $I_{dc}$

→ turn off time provided by the circuit for a device

\*  $V_c$  @  $t = t_c = 0$

$$\therefore i_c = i_o(t)R \quad @ t = t_c = 0$$

$$\therefore O = I_{dc} \left[ \frac{2e^{t_c/RC}}{1 + e^{-T/2RC}} \right]$$

$$1 - 2 e^{-\frac{t_c}{RC}} = 0$$

$$1 = 2 e^{-\frac{t_c}{RC}}$$

$$t_c = RC \ln \frac{2}{1 + e^{-T/2RC}}$$

if  $T \gg 2RC$

$$\text{then } t_c \approx 0.69 RC$$

## Design

### Sq wave mode

- \* @ low values of inverter freq  $I_i = I_{dc}$
- + load current approximates to Sq wave (previously seen)
- \* To get Sq wave,  $T > 10RC$

Also,

$$\because T \gg 2RC, \quad t_c \approx 0.69 RC$$

- \* If  $t_q$  is the turn off time of device used then  $t_c$  should be greater than  $t_q$
- \* minimum value of  $t_c$  should be  $t_q$  if minimum value of  $0.69RC = t_q$
- \* Minimum value of  $C$  must be  $\frac{t_q}{0.69R}$ .

\* C is Selected Such that

$$C = \frac{t_q}{0.69R}$$

$R \rightarrow$  Load  
Resistance.

\* To get Sq wave, T must be  $> 10RC$

$\frac{1}{T}$  must be less than  $\frac{1}{10RC}$

i.e. frequency must be less than  $\frac{1}{10RC}$

$$f_{max} = \frac{1}{10RC}$$

$$RC = \frac{t_q}{0.69}$$

$$\Rightarrow f_{max} = \frac{0.69}{t_q}$$

To get Sq wave load current

for a given load R, the device turn off time  $t_q$

C is selected as  $C = \frac{t_q}{0.69R}$

maximum frequency of operation is kept below  $\frac{0.69}{t_q}$

## Sinewave mode

For higher range of frequency, capacitance offers low impedance for harmonics and load current approximates sine wave.

Third harmonic is the most dominant. C is selected such that its impedance for 3rd harmonics  $X_{C3}$  is less than 50% of R @ minimum value of the range of required output frequency.

All higher harmonics will be bypassed from load resistance to capacitance.

$$X_{C3} = \frac{1}{2\pi 3f_{min} C} < \frac{R}{2}$$

$$3\pi f_{min} C > \frac{1}{R}$$

$$\boxed{C > \frac{1}{10 R f_{min}}}$$

To get sinewave load current

For a given load  $R_L$  device turnoff time  $t_q$ , C is selected such that  $C > \frac{1}{10 R f_{min}}$

$f_{min}$  is the minimum required output frequency.

The maximum frequency should be limited such that turn off time be provided by  $\alpha$  is greater than device turn off time  $t_{off}$

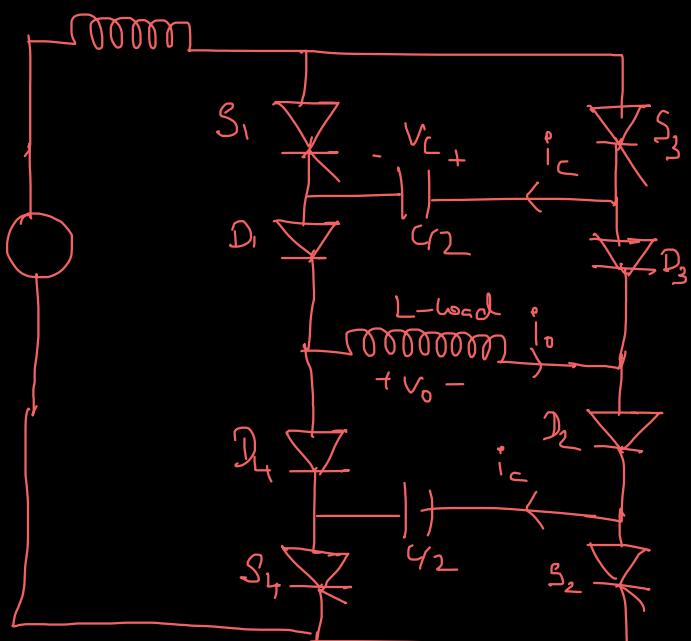
$$RC \ln \frac{2}{1 + e^{-1/(f_{max}^2 RC)}}$$

1Φ Load Commutated CSI with purely Inductive load :

\* At low frequency of inverter operation - Output current approximates square waveform. This low frequency range is called "No overlap region"

\* At higher frequency of inverter operation output current waveform approximates sine waveform. This frequency range is called "Fully overlap region"

\* Frequency range greater than fully overlap region is called partial overlap region.



\* One cycle is divided into 6 modes

\* Prior to mode 1,

$S_3 \& S_4 \rightarrow$  Conducting

Load current path:  $S_3 \rightarrow D_3, D_4, S_4$

$\therefore$  For  $t \leq 0$

$$i_o(0) = -I_{dc}$$

$$V_o(0) = V_{co}$$

Mode 1

$S_1 \downarrow S_2 \rightarrow$  turned on

$S_3 \& S_4 \rightarrow$  RB  $\Rightarrow$  turned off  
(due to  $V_{co}$ )

Load current remains  
@  $-I_{dc}$

Current path: Source,  $S_1, C, D_3$ ,  
load,  $D_4, C, S_2$

$V_c$  varies linearly due to  
constant current  $I_{dc}$

$$V_c(t) = V_{co} + \frac{1}{C/2} \int_0^t I_{dc} dt$$

$$V_c(t) = V_{co} + \frac{2 I_{dc} t}{C}$$

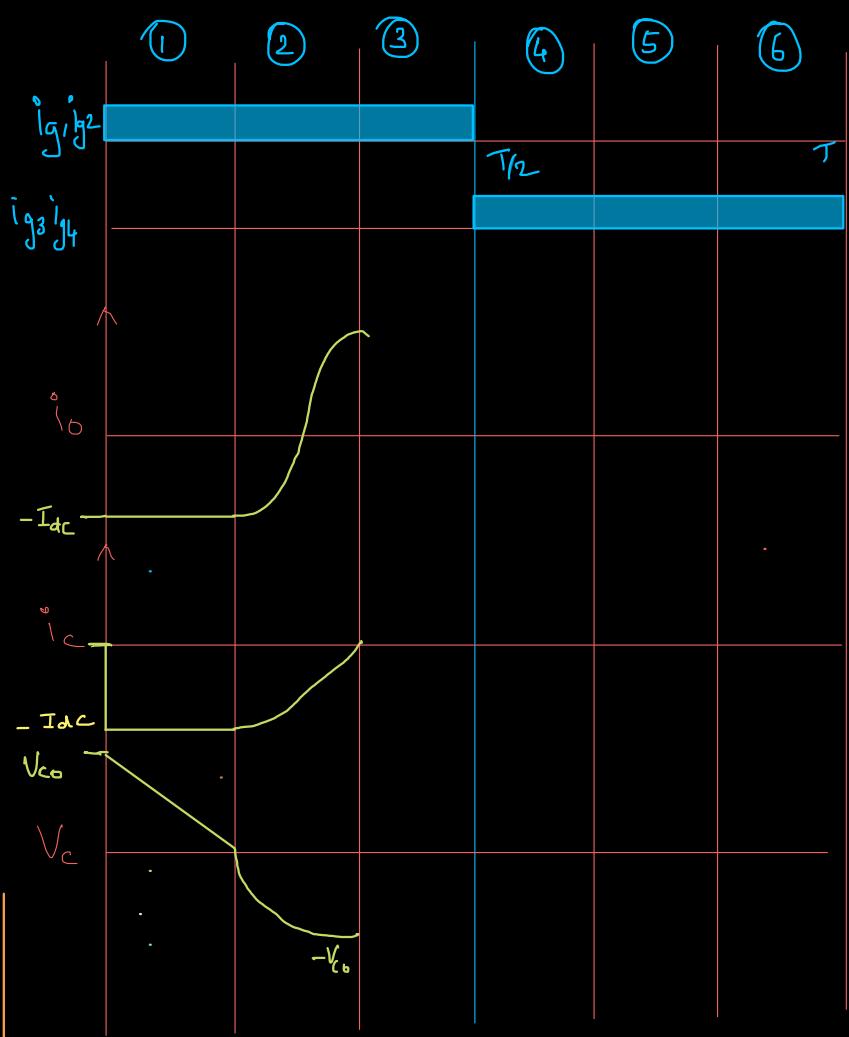
Mode 1 ends when  $V_c = 0$

Period of mode 1

$$V_c = 0$$

$$0 = V_{co} + \frac{2 I_{dc} t}{C}$$

$$t = \frac{C V_{co}}{2 I_{dc}}$$



Mode - ②

\* When  $V_c = 0$ ,  $D_1 \& D_2$  becomes on

$L + C$  are shorted through  $D_1, D_2, D_3, D_4$

\* Current enters to  $L, C$  parallel circuit through  $S_1$  & leaves through  $S_2$  by  $K_{CL}$ ,

$$I_{dc} + 2i_c = i_o$$

$$V_o = -V_c$$

$$\text{i.e. } L \frac{di_o}{dt} = -\frac{1}{C} \int_0^t i_c dt.$$

$$= -\frac{1}{C} \int_0^t - \left( \frac{I_{dc} - i_o(t)}{2} \right) dt$$

\* Initial condition for second mode

$$i_o(0) = -I_{dc}$$

$$\therefore \left. L \frac{di_o}{dt} \right|_{t=0} = V_C \Big|_{t=0} = 0$$

$$L \frac{di_o^2}{dt^2} = \frac{2}{C} \left[ I_{dc} - i_o(t) \right]$$

$$\zeta^2 I(s) - s I(\omega) - I(0) = \frac{2}{C} \left[ \frac{I_{dc}}{s} - \overline{I}(s) \right]$$

$$C \zeta^2 I_o(s) + I_o(s) = \frac{2 \overline{I}_{dc}}{s}$$

$$I_o(s) \left( C \zeta^2 + 1 \right) = \frac{2 \overline{I}_{dc}}{s}$$

$$I_o(s) = \frac{2 \overline{I}_{dc}}{s(C \zeta^2 + 1)}$$

$$I_o(s) = \frac{2 \overline{I}_{dc} / C}{s(C \zeta^2 + 1/C)}$$

$$\frac{2 \overline{I}_{dc} / C}{s(C \zeta^2 + 1/C)} = \frac{A}{s} + \frac{B s + D}{s^2 + 1/C}$$

$$\frac{2 \overline{I}_{dc}}{s(C \zeta^2 + 1)} = \frac{A}{s} + \frac{C(Bs + D)}{(s^2 + 1/C)}$$

$$2 \overline{I}_{dc} = A(C \zeta^2 + 1) + C(sBs + D)$$

$$A = 2 \overline{I}_{dc} \quad B = -2 \overline{I}_{dc}$$

$$I_o(s) = \frac{2 \overline{I}_{dc}}{s} - \frac{2 \overline{I}_{dc}}{s^2 + 1/C} \quad \left\{ \begin{array}{l} I_o(t) = -\overline{I}_{dc} (2 \cos \omega_0 t - 1) \\ \Rightarrow i_o(t) = -\overline{I}_{dc} \cos \omega_0 t \end{array} \right.$$

$$\therefore V_C(t) = \frac{1}{C/2} \int i_C(t) dt$$

$$= \frac{2}{C} \int_0^t -\bar{I}_{dc} \cos \omega_0 t dt$$

$$= -\frac{2\bar{I}_{dc}}{\omega_0 C} \sin \omega_0 t$$

$$= \frac{-2\bar{I}_{dc}}{\frac{1}{\sqrt{LC}}} \sin \omega_0 t$$

$$= -V_{co} \sin \omega_0 t ; \quad V_{co} = 2 \sqrt{\frac{L}{C}} \bar{I}_{dc}$$

Mode 2 ends when  $i_C = 0$

$$\text{ie) } \omega_0 t = \pi/2$$

$$\text{then } i_o = +\bar{I}_{dc}$$

$$\text{Duration of mode 2, } t_2 = \frac{\pi}{2\omega_0}$$

$$= \frac{\pi}{2 \frac{1}{\sqrt{LC}}}$$

$$t_2 = \frac{\pi \sqrt{LC}}{2}$$

The current commutation interval is  $t_c = t_1 + t_2$

$$t_c = \frac{CV_{co}}{2\bar{I}_{dc}} + \frac{\pi \sqrt{LC}}{2}$$

As  $i_C = 0$ ,  $D_3, D_4 \rightarrow \text{OFF}$  @ end of mode-2

(Load current is constant so no drop across it & cap potential  $V_C = -V_{CO}$ )

### Mode ③

\* Current path is Source,  $S_1$ ,  $D_1$ , load,  $D_2$ ,  $S_2$

\* No current through capacitor, so voltage remains @  $V_{CO}$

\* Load connected in series with source

$$i_C = 0 ; i_D = I_{DC}$$

$$V_C = -V_{CO}$$

\* This Mode continues till

$S_3$  +  $S_4$  are turned on

$$@ \frac{T}{2}$$

$$t_3 = \frac{T}{2} - (t_1 + t_2)$$

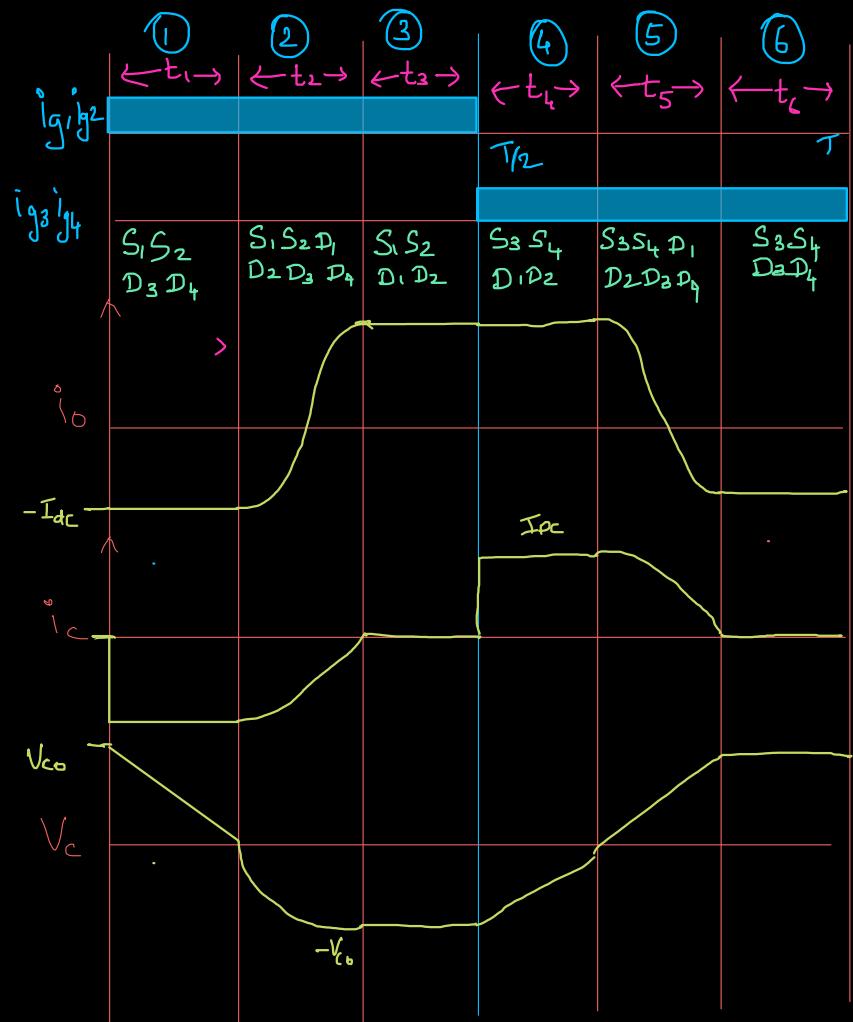
$$= \frac{T}{2} - \left( \frac{C V_{CO}}{2 I_{DC}} + \frac{\pi}{2 \omega_0} \right)$$

$$= \frac{T}{2} - \left[ \frac{C 2 \sqrt{L C} I_{DC}}{2 I_{DC}} + \frac{\pi}{2 \omega_0} \right]$$

$$= \frac{T}{2} - \left( \sqrt{LC} + \frac{\pi}{2 \omega_0} \right)$$

$$= \frac{T}{2} - \left( \frac{1}{\omega_0} + \frac{\pi}{2 \omega_0} \right)$$

$$\boxed{t_3 = \frac{T}{2} - \left( \frac{1 + \frac{\pi}{2}}{\omega_0} \right)}$$



$$\frac{\pi}{2 \omega_0}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

for a given inverter circuit, the duration of mode 3 is decided by inverter frequency  $f_0 = \frac{1}{\tau}$

### Mode ④

\* At the end of mode 3,  $S_3 \wedge S_4$  are gated.  $S_1 \wedge S_2$  are commutated

\* Load path  $S_3, C, D_1, \text{Load}, D_2, L, S_4$

\* Constant current  $I_{DC}$  flows through capacitor

$\therefore V_C$  varies  $-V_{CO} \rightarrow 0$  linearly

\*  $I_o$  remains @  $I_{DC}$  &  $I_c = I_{DC}$

\* Mode 4 ends when  $V_C = 0$

### Mode ⑤

Drop across  $D_3 \wedge D_4$  are 0 ( $V_C = 0 \wedge I_o \rightarrow \text{const}$ )

At the end of mode 5

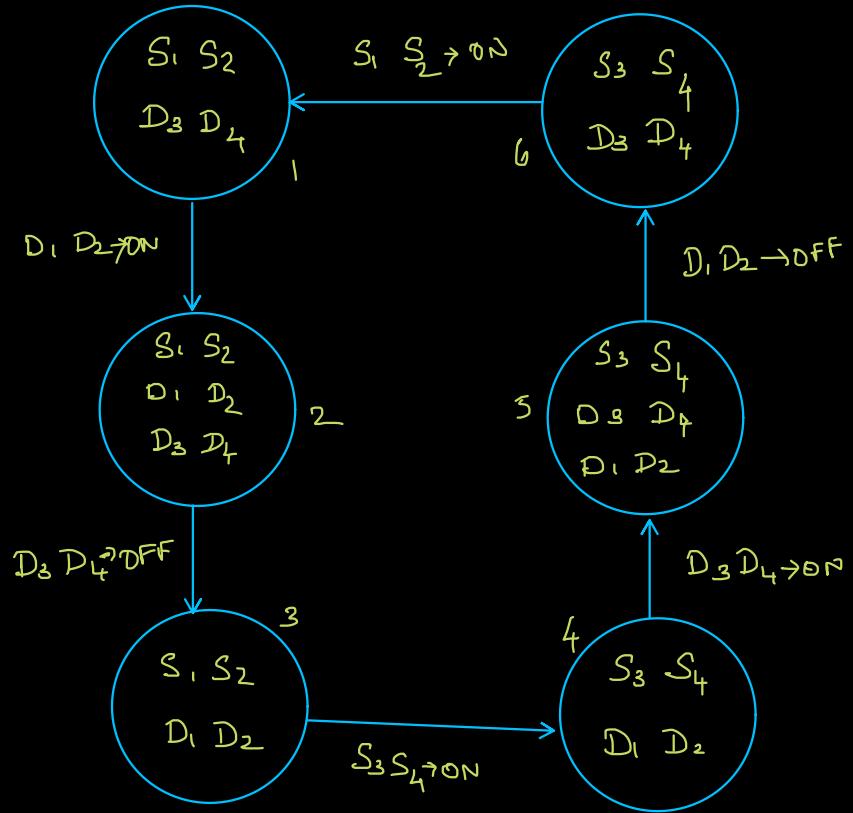
$$I_c = 0$$

$\therefore I_{D1} \wedge I_{D2}$  are reduced to 0.

Current path  $S_3 \ D_3 \ \text{Load} \ D_4 \ S_4$

$$I_c = 0$$

### Transition Diagram of 1φ CS in no overlap region



Commutation interval

$$t_c = \frac{1}{\omega_0} \left( 1 + \frac{\pi}{2} \right)$$

$$t_c = \frac{2.57}{\omega_0}$$

Duration of mode 3

$$\left\{ t_3 = \frac{T}{2} - \frac{2.57}{\omega_0} \right\}$$

- \* When inverter frequency is increased,  $T$  is decreased,  $t_3$  is also decreased.
- \* At a particular frequency,  $t_3$  becomes 0
- \* This is the maximum limit of frequency for no overlap condition. or Sq wave mode.
- \* This maximum limit of frequency for no overlap is given by  $\frac{T_{NL}}{2} - \frac{2.57}{\omega_0} = 0$

$T_{NL} \rightarrow$  is the minimum period for no overlap condition

$$\frac{T_{NL}}{2} = \frac{2.52}{\omega_0}$$

$$\Rightarrow f_{LN} = \frac{\omega_0}{5.14} = \frac{0.19}{\sqrt{LC}}$$

## PARTIAL OVERLAP FREQUENCY RANGE

\* Inverter frequency is greater than  $f_{NL} = \frac{0.19}{\sqrt{LC}}$

\* Modes 3 & 6 are absent

\* For  $t < 0$ ,  
the inverter was in mode 5.

\*  $S_3, S_4, D_1, D_2, D_3, D_4$  were conducting.

\* Load current was oscillatory

$$i_C 4V_C \rightarrow +V_C$$

$$i_D \rightarrow -V_C$$

@  $t=0$   $S_1$  &  $S_2$  are turned on.

$\Rightarrow S_3$  &  $S_4$  are turned off due to  $V_C$

This results in mode 2 operation

\*  $S_1, S_2, D_1, D_2, D_3, D_4$  are conducting

\*  $i_C$  becomes  $-V_C$  & rises in  $-ve$  direction

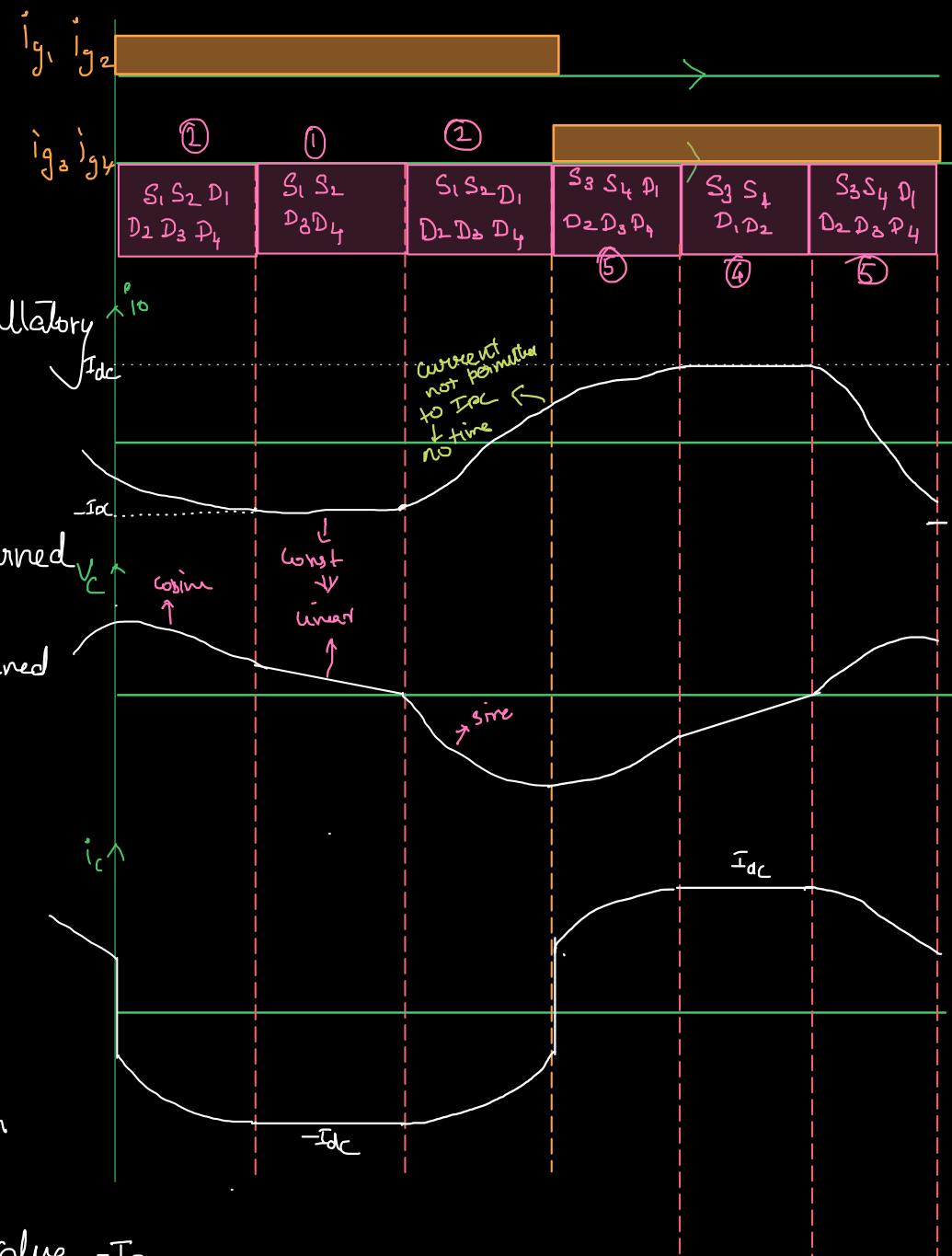
\*  $i_D$  which is  $-V_C$  rises to constant value  $-I_{DC}$

\* Drop across load = 0 due to const current  $I_{DC}$ .

\* So  $D_1, D_2$  becomes off due to capacitor potential.

\* Current path is

$S_1, C, D_3, \text{load}, D_4, C, S_2$



This results in mode 1 operation

$V_C$  decreases with  $-ve$  slope.

$$I_C = -I_{dc}$$

$$I_O = -I_{dc}$$

\* Mode 1 ends when  $V_C = 0$

\*  $D_3$  &  $D_4$  are brought into conduction.

\*  $S_1, S_2, D_1, D_2, D_3, D_4$  are conducting.

\*  $V_C$  rises in -ve direction.

\*  $I_o$  reverses to a value that is less than  $I_{dc}$ .

\*  $I_c$  decreases in -ve direction.

⋮

∴ In partial overlap condition, Sequence of modes in one cycle is 2, 1, 2, 5, 4, 5

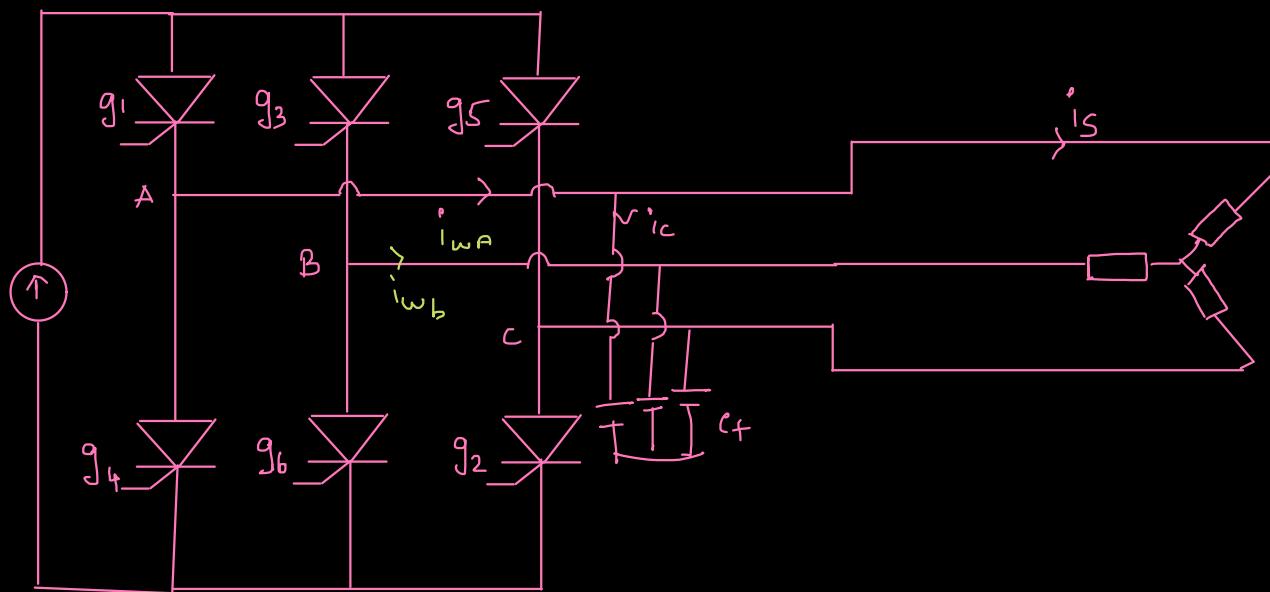
\* Maximum frequency limit for partial overlap condition is  $f_{PL} = \frac{0.24}{\sqrt{LC}}$

### FULLY OVERLAP CONDITION

\* If the inverter frequency is further increased mode 1 & mode 4 are absent & the diodes conduct continuously resulting in sine wave load current

\* Fully overlap condition, Sequence of modes are 2, 5, 2, 5

# PWM in 3φ CURRENT SOURCE INVERTER



- \* The inverter produces a defined PWM output current  $i_w$ .
- \* DC Side of the inverter is an ideal DC Source.
- \* The CSI requires a 3φ Capacitor  $C_f$  @ its output for the commutation of switching devices
- \* The capacitor provides a current path for the energy trapped in the load inductor
- \* This avoids the damage of the switching devices due to high voltage drops.
- \* The capacitor also acts as a harmonic filter improving the load current & voltage waveforms.
- \* The capacitor value can be reduced with the increase of switching frequency

Switching pattern for CSI Should satisfy the following condition:

①  $I_d$  should be continuous

→ one device from top group & one device from bottom group should conduct  
→ If only 1 device conducts, then there is no path for continuous current & high voltage will be induced by DC side inductance  
This causes damage to the switches

② Inverter current  $i_w$  should be defined for PWM control. It should be either  $I_d$  or zero

→ If  $S_1, S_2, S_3$  are conducting, the currents in  $S_1$  &  $S_3$ , equal to the PWM currents in the inverter phases A & B which is load-dependent

Sum of 2 currents =  $I_d$

## Space Vector Modulation of CST

\* Only one switch from upper group & one switch from lower group conduct at a time

### 3 Zero States

\* 1, 4  $\rightarrow$  ON

\* 3, 6  $\rightarrow$  ON

\* 5, 4  $\rightarrow$  ON

DC Side current is bypassed

$$i_{wA} = i_{wB} = i_{wC} = 0$$

This is called bypass operation

Load is 3 $\phi$  balanced

$$i_{wA}(t) + i_{wB}(t) + i_{wC}(t) = 0$$

3 $\phi$  currents can be transformed into 2 $\phi$  currents in  $\alpha\beta$  plane

$$\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{wA}(t) \\ i_{wB}(t) \\ i_{wC}(t) \end{bmatrix}$$

Current Space vector can be expressed in terms of 2 $\phi$  Currents

$$\vec{I}(t) = i_\alpha(t) + j i_\beta(t)$$

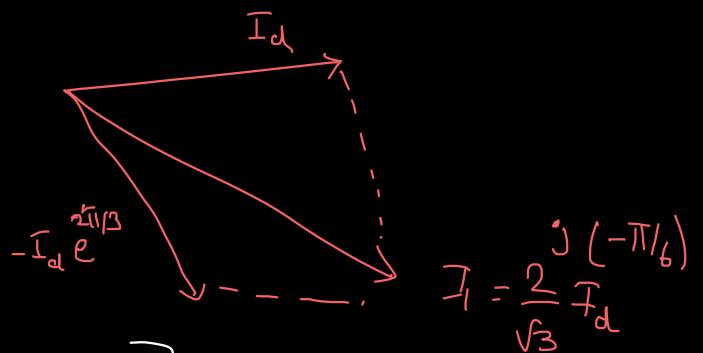
Sub  $\mathcal{I}_\alpha \perp \mathcal{I}_\beta$

$$\overline{\mathcal{I}}(t) = \frac{2}{3} \left[ i_{\omega_A}(t) e^{j0} + i_{\omega_B}(t) e^{j2\pi/3} + i_{\omega_C}(t) e^{j4\pi/3} \right]$$

## 6 active States

(1)  $i_{\omega_A}(t) = \mathcal{I}_d ; \quad i_{\omega_B}(t) = \mathcal{I}_d \angle \omega_C(t) = 0$

$$\mathcal{I}_l = \frac{2}{\sqrt{3}} \mathcal{I}_d e^{j(-\pi/6)}$$



(2)

$$\mathcal{I}_2 = \frac{2}{3} \left[ \overline{\mathcal{I}}_d e^{j0} + 0 - \mathcal{I}_d e^{j\frac{4\pi}{3}} \right]$$

$$= \frac{2}{3} \mathcal{I}_d$$

$$= \frac{2}{3} (\cos 0 - \underbrace{\cos \frac{4\pi}{3}}_{-\frac{1}{2}} - j \sin \frac{4\pi}{3})$$

$$= \frac{2}{3} \left( 1 + \frac{1}{2} + j \frac{\sqrt{3}}{2} \right)$$

$$= \frac{2}{3} \left( \frac{3}{2} + j \frac{\sqrt{3}}{2} \right)$$

$$= \frac{1}{3} (3 + j\sqrt{3})$$

$$\mathcal{I}_2 = \frac{\sqrt{3}}{3} \mathcal{I}_d (\sqrt{3} + j) = \frac{2}{\sqrt{3}} \tan^{-1} \left( \frac{1}{\sqrt{3}} \right) = \frac{2 \mathcal{I}_d}{\sqrt{3}} e^{j(\pi/6)}$$

$$\begin{aligned} I_3 &= \frac{2}{3} \left[ 0 + I_d e^{j\frac{2\pi}{3}} - I_d e^{-j\frac{4\pi}{3}} \right] \\ &= \frac{2}{3} I_d \left[ e^{j\frac{2\pi}{3}} - e^{-j\frac{4\pi}{3}} \right] \end{aligned}$$

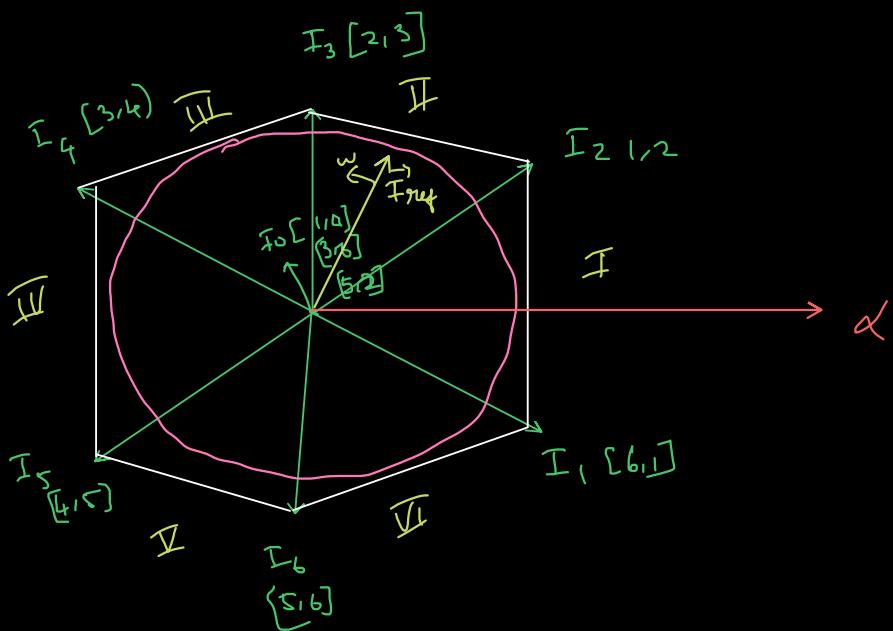
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$$\begin{aligned} I_4 &= \frac{2}{3} \left[ -I_d e^{j0} + I_d e^{j\frac{2\pi}{3}} \right] \\ &= \frac{2}{3} I_d \left[ e^{j0} - e^{j\frac{2\pi}{3}} \right] \\ &= \frac{2}{3} I_d \left[ -\frac{1}{2} + j\frac{\sqrt{3}}{2} - 1 \right] \\ &= \frac{2}{3} I_d \left[ \dots \right] \end{aligned}$$

$\therefore$  All active vectors can be expressed as

$$\overrightarrow{I_k} = \frac{2}{\sqrt{3}} I_d e^{j \left( (k-1) \frac{\pi}{3} - \frac{\pi}{6} \right)}$$

Type of State	Switching State	on State Switches	Inverter PWM Current	Space Vector	
			$i_{WA}$	$i_{WB}$	$i_{WC}$
1, 4	$S_1, S_4$	0	0	0	$\vec{I}_0$
3, 6	$S_3, S_6$	0	0	0	$\vec{I}_d$
5, 2	$S_5, S_2$	0	0	0	$\vec{I}_o$
6 1	$S_6, S_1$	$I_d$	$-I_d$	0	$I_1 = \frac{2}{\sqrt{3}} I_d e^{j(-\pi/6)}$
1 2	$S_1, S_2$	$I_d$	0	$-I_d$	$I_2 = \frac{2}{\sqrt{3}} I_d e^{j\pi/6}$
2 3	$S_2, S_3$	0	$-I_d$	$-I_d$	$I_3 = \frac{2}{\sqrt{3}} I_d e^{j(\pi/2)}$
4 3	$S_4, S_3$	$-I_d$	$I_d$	0	$I_4 = \frac{2}{\sqrt{3}} I_d e^{j\pi/3}$
4 5					$I_5 = \frac{2}{\sqrt{3}} I_d$
5 6					$I_6 = \frac{2}{\sqrt{3}} I_d$

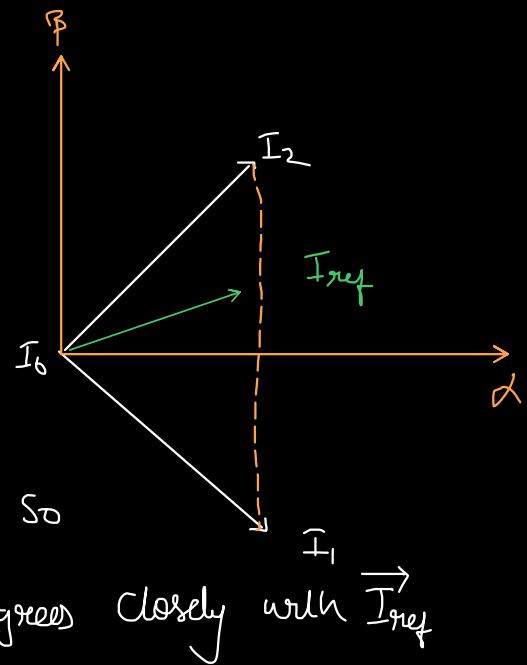


- \* Current reference vector  $\vec{I}_{ref}$  rotates @ an angular velocity  $\omega = 2\pi f_1$
- \*  $f_1$  is the required fundamental frequency of inverter op current
- \* Angular displacement between  $\vec{I}_{ref}$  &  $\alpha$  axis of  $\alpha$ - $\beta$  plane is  $\theta(t) = \int_{0}^t \omega(t) dt + \theta(0)$
- \* For any position of  $\vec{I}_{ref}$  it can be synthesized by 3 nearly stationary vectors
- \* Magnitude of op current is adjusted by adjusting the length of reference phasor & frequency by adjusting Speed of rotation

### Dwell time calculation

---

\* Let  $\vec{I}_{ref}$  lie in Sector I



\* Inverter is controlled such that States of the inverter shifts between States 1+2+0 on port time basis so that the resultant current vector agrees closely with  $\vec{I}_{ref}$

$\vec{I}_{ref}$  can be synthesized by  $\vec{I}_0, \vec{I}_1, \vec{I}_2$ .

$$\text{Sampling period} = T_S = \bar{T}_1 + \bar{T}_2 + \bar{T}_3$$

Ampere - Second balance

$$\vec{I}_{ref} \vec{I}_s = \vec{I}_1 \vec{I}_1 + \vec{I}_2 \vec{I}_2 + \vec{I}_0 \vec{I}_0$$

$\vec{I}_1, \vec{I}_2, \vec{I}_0$  are dwell times along  $\vec{I}_1, \vec{I}_2, \vec{I}_0$

$$\vec{I}_{ref} = I_{ref} e^{j\theta}$$

$$\vec{I}_1 = \frac{2}{\sqrt{3}} I_d e^{j(-\pi/6)}$$

$$\vec{I}_2 = \frac{2}{\sqrt{3}} I_d e^{j(\pi/6)}$$

$$\vec{I}_0 = 0$$

$$\therefore I_{ref} e^{j\theta} \vec{I}_s = \frac{2}{\sqrt{3}} I_d e^{j(-\pi/6) \vec{T}_1} + \frac{2}{\sqrt{3}} I_d e^{j(\pi/6) \vec{T}_2} + \vec{I}_0 \vec{T}_0$$

equating real & imaginary,

$$I_{ref} \cos\theta \vec{T}_s = \frac{2}{\sqrt{3}} I_d \cos \frac{\pi}{6} \vec{T}_1 + \frac{2}{\sqrt{3}} I_d \cos \frac{\pi}{6} \vec{T}_2$$

$$= \frac{2}{\sqrt{3}} I_d \frac{\sqrt{3}}{2} \vec{T}_1 + \frac{2}{\sqrt{3}} \frac{\sqrt{3}}{2} \vec{T}_2 I_d$$

$$I_{ref} \cos\theta \vec{T}_s = I_d (\vec{T}_1 + \vec{T}_2)$$

$$\frac{I_{ref} \cos\theta \vec{T}_s}{2} = \frac{I_d}{2} (\vec{T}_1 + \vec{T}_2)$$

$$\vec{T}_s I_{ref} \cos\theta \sin 30 = \frac{I_d}{2} (\vec{T}_1 + \vec{T}_2) - \textcircled{1}$$

11)

$$\bar{I}_{ref} \sin \theta \bar{T}_s = \frac{1}{\sqrt{3}} \bar{I}_d (-\bar{T}_1 + \bar{T}_2)$$

$$\bar{I}_{ref} \sin \theta \frac{\sqrt{3}}{2} = \frac{1}{2} \bar{I}_d (\bar{T}_2 - \bar{T}_1)$$

$$\bar{T}_s \bar{I}_{ref} \sin \theta \cos 30^\circ = \frac{\bar{I}_d (\bar{T}_2 - \bar{T}_1)}{2} \quad (2)$$

Solving (1) & (2)

$$\bar{T}_s \bar{I}_{ref} \cos \theta \sin 30^\circ + \bar{T}_s \bar{I}_{ref} \sin \theta \cos 30^\circ = \frac{\bar{I}_d}{2} (\bar{T}_1 + \bar{T}_2) + \frac{\bar{I}_d}{2} (\bar{T}_1 - \bar{T}_2)$$

$$\bar{T}_s \bar{I}_{ref} [\cos \theta \sin 30^\circ + \sin \theta \cos 30^\circ] = \frac{\bar{I}_d}{2} [\bar{T}_1 + \bar{T}_2 + \bar{T}_1 - \bar{T}_2]$$

$$\bar{T}_s \bar{I}_{ref} \sin(\theta + 30^\circ) = \frac{\bar{I}_d}{2} (2\bar{T}_1)$$

$$\bar{T}_1 = \bar{T}_s \frac{\bar{I}_{ref}}{\bar{I}_d} \sin(\theta + 30^\circ)$$

$$\boxed{\bar{T}_1 = \bar{T}_s m \sin(\theta + 30^\circ)}$$

$$\left\{ \begin{array}{l} \bar{T}_1 = \bar{T}_s \frac{\bar{I}_{ref}}{\bar{I}_d} \sin(30^\circ + \theta) \\ \bar{T}_2 = \bar{T}_s \frac{\bar{I}_{ref}}{\bar{I}_d} \sin(30^\circ - \theta) \end{array} \right. \quad \text{check.}$$

$$\text{Modulation Index } m_a = \frac{\hat{I}_{ref}}{\bar{I}_d} = \frac{\hat{I}_{w_1}}{\bar{I}_d} -$$

$$T_1 = \bar{T}_s m_a \sin(30 + \theta)$$

$$T_2 = \bar{T}_s m_a \sin(30 - \theta) ; \quad T_o = \bar{T}_s - T_1 - T_2$$

\* Maximum value of reference vector  $\bar{I}_{ref\ max}$  corresponds to the radius of the largest circle that can be inscribed in the hexagon.

\* Length of active vector is  $\frac{2}{\sqrt{3}} I_d$

$$* \bar{I}_{ref\ max} = \frac{2}{\sqrt{3}} I_d \cos 30$$

$$= \frac{2}{\sqrt{3}} I_d \frac{\sqrt{3}}{2}$$

$$= \bar{I}_d$$

$$\therefore m_{a\ max} = \frac{\bar{I}_{ref\ max}}{\bar{I}_d}$$

$$m_{a\ max} = 1$$

## Trapezoidal PWM (TPWM)

\*  $V_m$  is the trapezoidal modulating wave &  $V_c$  is a  $\Delta^c$  carrier

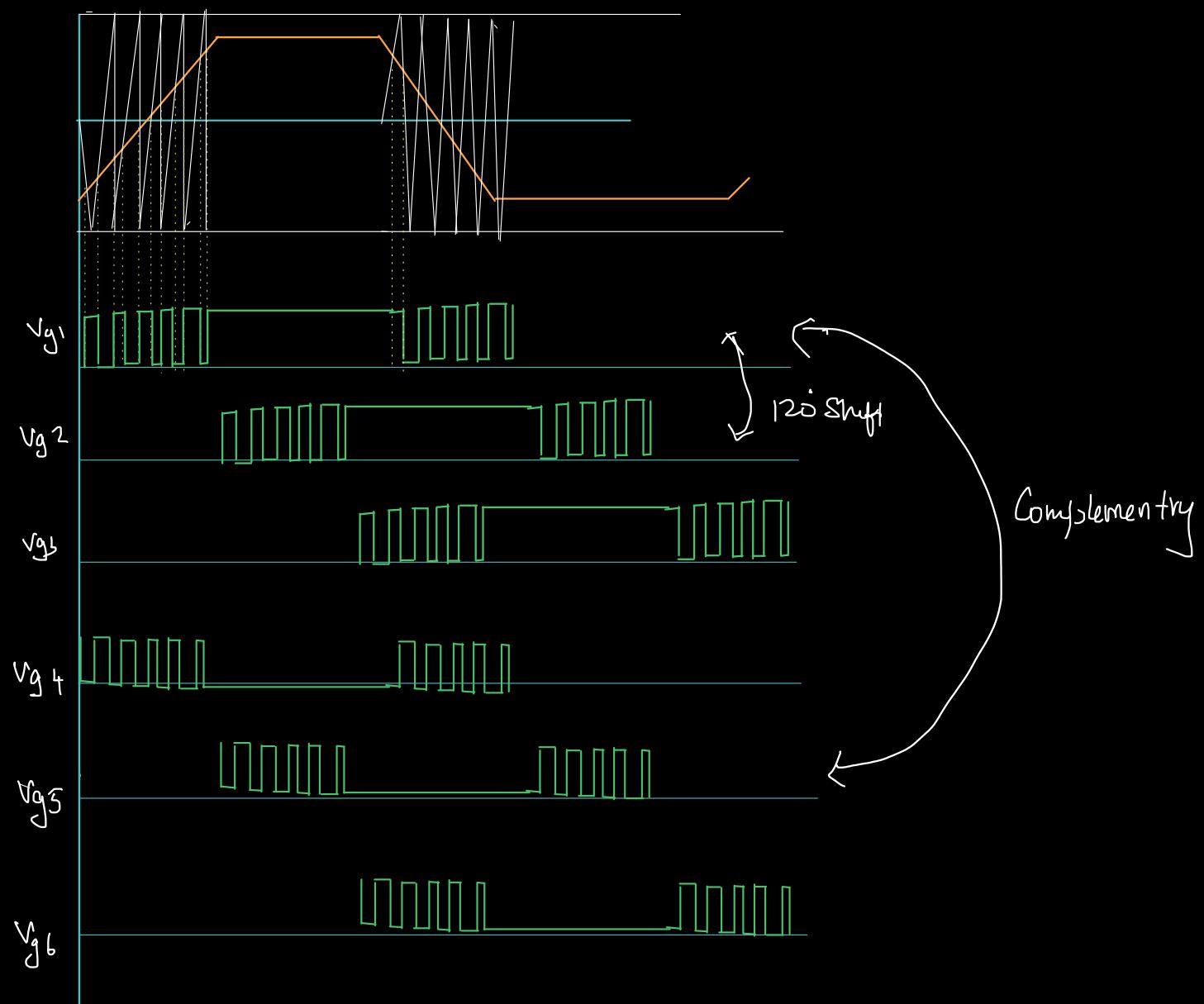
\* The amplitude modulation index =  $m_a = \frac{\hat{V}_m}{\hat{V}_c}$

\*  $\hat{V}_m \rightarrow$  peak of modulating (Trapezoidal) wave  
 $\hat{V}_c \rightarrow$  peak of carrier wave

\* Only 2 devices conduct @ a time

\* The magnitude of

# TRAPEZOIDAL PNM



- \* Fundamental frequency Component  $I_{w1}$  does not vary significantly with the modulation index  $m_a$ .
- \* When  $m_a$  varies from 0 to maximum value of 1,  $I_{w1}$  changes from minimum of  $0.89 I_{w1\text{max}}$  to  $I_{w1\text{max}}$ . presenting only 11% increase.
- \* This is due to the fact that  $i_w$  is not modulated in centre  $\frac{\pi}{3}$  region of each half cycle.

\* In practice the adjustment of fundamental component  $I_{w1}$  is accomplished by varying the dc current  $I_d$  through the ip Side rectifier instead of varying  $m_a$ .

### SELECTIVE HARMONIC ELIMINATION PWM

Same as in VSI

### Series Inverter

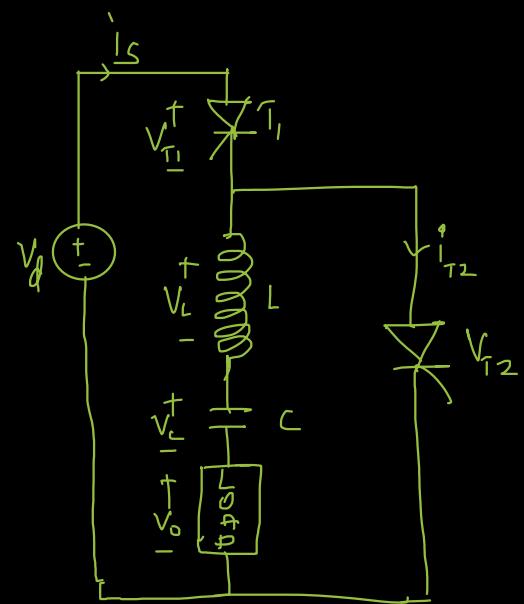
↳ high frequency, high current

\* Commutating elements L & C are connected in series with load

\* Load current flows continuously through L & C

\* Hence thus CRL is used in high frequency application  
(low freq  $\rightarrow$  large L & C)

\* L & C are selected such that combined RLC is underdamped



②  $t=0$   $T_1 \rightarrow ON$   
 $T_2 \rightarrow OFF$

Let C charged to

$$-V_C$$

$$V_d = R_i(t) + L \frac{di(t)}{dt} + \frac{1}{C} \int i(t) dt - ①$$

$$+ V_{CO}(0) ; 0 < t < \frac{T}{2}$$

③  $t=0$

$$i(0) = 0 ; V_C(0) = -V_{CO}$$

$$L \frac{di(t)}{dt} \Big|_{t=0} = V_d + V_{CO}$$

diff ①

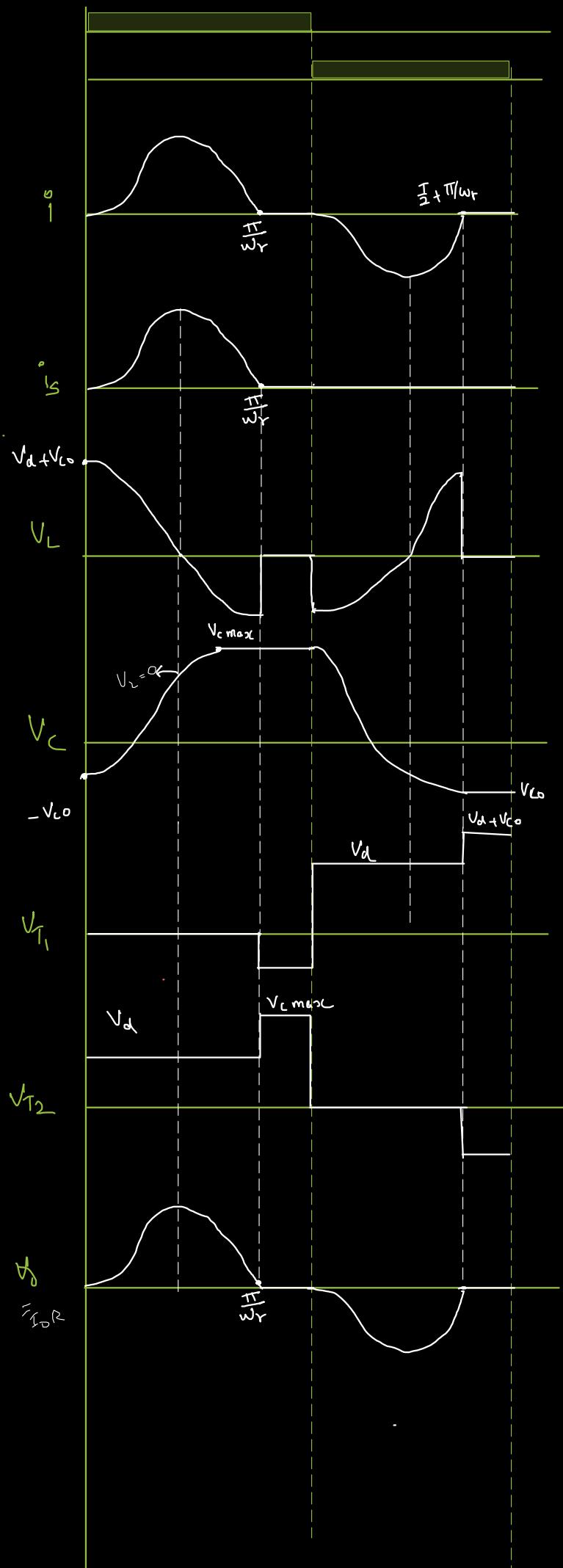
$$0 = R \frac{di(t)}{dt} + L \frac{d^2i(t)}{dt^2} + \frac{i(t)}{C}$$

$$0 = R S I(S) + L S^2 I(S) - L S(0) - L(V_d + V_{CO}) + \frac{I(S)}{C}$$

$$0 = I(S) \left[ RS + L S^2 + \frac{1}{C} \right] - L(V_d + V_{CO})$$

$$I(S) = \frac{L(V_d + V_{CO})}{RS + L S^2 + \frac{1}{C}}$$

$$I(S) = \frac{V_d + V_{CO}}{S^2 + \frac{RS}{L} + \frac{1}{LC}}$$



$$i(t) = \frac{V_d + V_{C0}}{\omega_r L} e^{-\delta t} \sin \omega_r t$$

$$\delta = \frac{R}{2L} \quad ; \quad \omega_t = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2} \quad ; \quad \omega_0 = \frac{1}{\sqrt{LC}}$$

$$V_L = L \frac{di(t)}{dt}$$

$$= L \frac{V_d + V_{C0}}{\omega_r L} \left[ \omega_r e^{-\delta t} (\cos \omega_r t + \sin \omega_r t (-\delta)) e^{-\delta t} \right]$$

$$= L \frac{V_d + V_{C0}}{\omega_r L} \left[ \right.$$

$$= \frac{\omega_0}{\omega_t} \left[ V_d + V_{C0} \right] e^{-\delta t} \cos(\omega_r t + \phi)$$

$$\phi = \tan^{-1} \left( \delta / \omega_r \right)$$

$$V_C(t) = V_d - V_L - iR$$

$$\pi/\omega_r \leq t \leq \frac{\pi}{2}$$

\* Both switches are off

$$i(t) = i_s(t) = 0$$

$$V_L(t) = 0 \quad ; \quad V_C = V_{Cmax}$$

$$V_{T1} = V_d - V_{Cmax}$$

$$V_{T2} = V_{Cmax}$$

$$V_0 = i(t)R = 0$$

$$\frac{\pi}{2} < t < \frac{\pi}{2} + \frac{\pi}{\omega_r}$$

$$t' = t - \frac{\pi}{2}$$

@  $t' = 0$ ,  $T_2$  is turned on

$$0 = R i(t) + L \frac{di(t)}{dt} + \frac{1}{C} \int i(t) dt + V_0$$

@  $t' = 0$

$$i(0) = 0 \quad V_L(0) = V_{cmax}$$

$$\frac{di(t')}{dt} \Big|_{t'=0} = -\frac{V_0}{L}$$

$$i(t') = \frac{-V_{cmax}}{\omega_r L} e^{-\delta t'} \sin \omega_r t'$$

$$V_L(t') = L \frac{di(t')}{dt} = -\frac{\omega_0}{\omega_r} V_0 e^{-\delta t'} \cos(\omega_r t' + \phi)$$

$$V_C(t') = -V_L - iR$$

$$V_{T1} = V_0 ; \quad V_{T2} = 0 \quad V_o = i(t') R$$

@  $\omega_r t' = \pi$ ,  $i(t') = 0$

$\Rightarrow T_2$  turned off

## Drawbacks of Series Inverter

\* Maximum inverter frequency is limited to a value less than the circuit's natural frequency

\* For a very low value of inverter frequencies load voltage is highly distorted.

## Design of L

\* L is chosen on the basis of attenuation factor

$$* i(t) = \frac{V_d + V_{co}}{\omega_r L} e^{-R/2L t} \sin \omega_r t$$

$$\text{Peak of } i(t) = \frac{V_d + V_{co}}{\omega_r L} e^{\frac{-R}{2L} \frac{\pi}{2\omega_r}}$$

\* If there is no attenuation, then  $i(t)$  would be  $\frac{V_d + V_{co}}{\omega_r L} \sin \omega_r t$  & peak is  $\frac{V_d + V_{co}}{\omega_r L}$

\* Attenuation factor

$$AF = \frac{\frac{V_d + V_{co}}{\omega_r L} e^{\frac{-R}{2L} \frac{\pi}{2\omega_r}}}{\frac{V_d + V_{co}}{\omega_r L}} = e^{\frac{-R}{2L} \frac{\pi}{2\omega_r}}$$

$$\ln(AF) = \frac{-R}{8f_L L}$$

$$L = \frac{-R}{8f_r \ln(AF)}$$

Usually  $AF = 0.5$

## Design of C

\* C is selected from value of  $\omega_r$

$$* \omega_r = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$$

$$C = \frac{1}{L} \left\{ \frac{1}{\omega_r^2 + \left(\frac{R}{2L}\right)^2} \right\}$$

If load is variable, then C is selected such that for the maximum possible value of R so that the circuit is underdamped

Voltage rating of C is  $V_d + V_{co}$

## Selection of Thyristor

\* Forward blocking voltage must be greater than  $V_{cmax}$ .

\* Peak current rating must be greater than peak load current for minimum load resistance

$$\frac{V_d + V_{co}}{\omega_r L} \geq \frac{R_{min}}{2L} \frac{\pi}{2\omega_r}$$

\* Turn off time  $t_{q_2}$  must be less than,

$$t_c = \frac{T}{2} - \frac{\pi}{\omega_r}$$

## Modified Series Inverter

$$L_1 = L_2$$

$$C_1 = C_2$$

$L_1$  &  $L_2$  are tightly coupled

(Singh & Kang - dev)

