1. NITC/EE/SG/ 2022-23/Winter

Name:

Roll No: Pawali P.P M220098EE

DEPARTMENT OF ELECTRICAL ENGINEERING

II SEMESTER, M TECH, MID-TERM EXAM-WINTER SEMESTER 2022-23

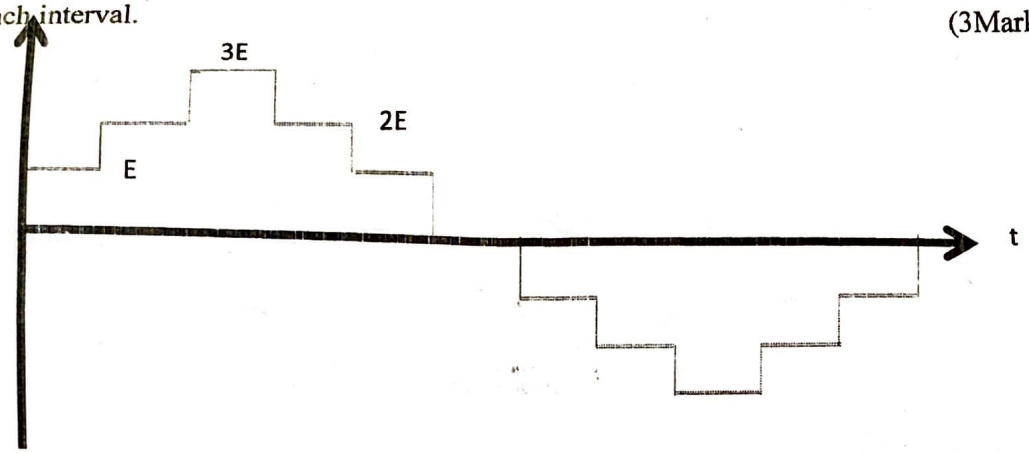
EE6302D - ADVANCED POWER ELECTRONIC CIRCUITS

Time: 2.0 Hours

Maximum Marks: 30

*Answer **all** questions*

1. Draw a 2 unit cascaded H-bridge configuration feeding an R-L load for achieving a single phase output voltage as shown below. Sketch the current waveform and indicate the devices conducting in each interval. (3Marks)



2. A 3 level H bridge inverter is connected between a 220V dc source and load. Phase shifted SPWM technique with frequency modulation ratio 3 and amplitude modulation ratio 0.8 is used for voltage control. With relevant circuit diagram and waveforms, obtain the gating signals for each device and the output voltage. (6 Marks)

3. A single phase capacitor commutated CSI is operated at 50Hz with a pure resistance load of 5 Ω. SCR turn off time is 62μs. Find the value of capacitance for successful commutation. Find the maximum value of frequency to have square wave mode.
For the same capacitor, find the maximum value of frequency to have sine wave output.
Plot the waveforms for load voltage, capacitor current and device voltage.
Draw the circuit and derive the expressions used. (10Marks)

4. A three phase star connected load which requires phase voltages as $v_{an} = 100\sin 100\pi t$, $v_{bn} = 100\sin(100\pi t - 2\pi/3)$, $v_{cn} = 100\sin(100\pi t - 4\pi/3)$ is connected to a dc source of 240V through a three phase, three level diode clamped bridge inverter circuit.
With required diagrams, explain how space vector PWM scheme with a switching frequency of 2.5kHz is implemented to achieve this condition.
At t = 2ms, find the magnitude and position of the reference vector.
Derive and obtain the dwell periods at this position.
Indicate the seven segment switching scheme and corresponding pole voltages for this position.
What are the factors to be considered while selecting switching sequence? (11marks)