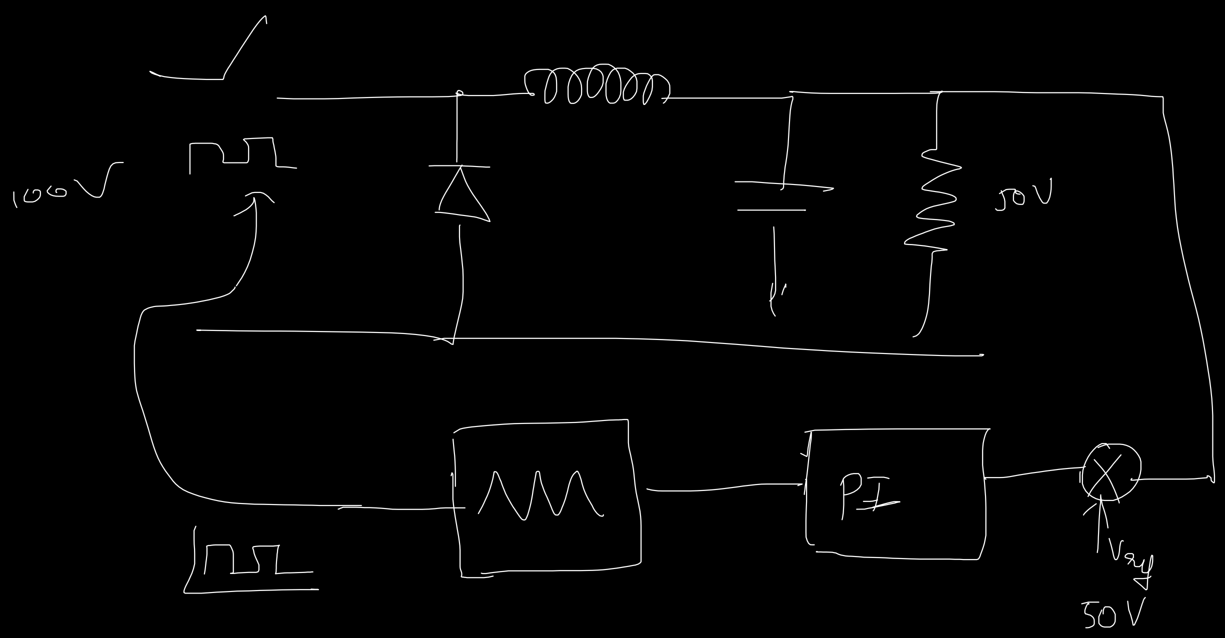
DIGITAL CONTROL OF POWER ELECTRONIC CIRCUITS

C1 - Slot

F28379D
TI Launch Pad

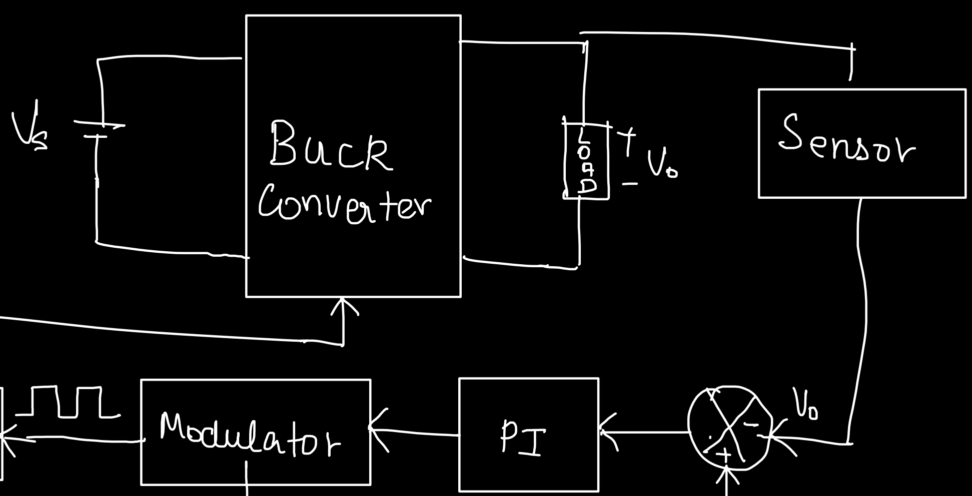
Tentative

End Sem Theory	– 30
End Sem Lab	– 20
Midsem Theory	– 20
Lab session	– 20
Theory Assignment	– 10



One class missed

Analog

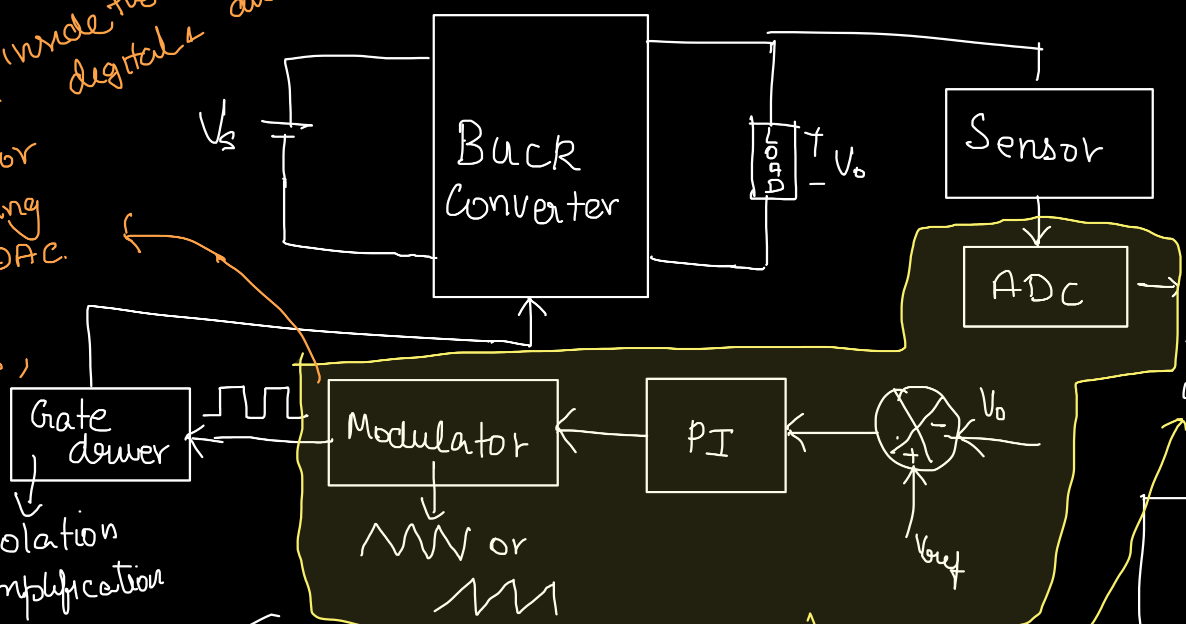


* isolation
* Amplification

Digital

inside the processor digital & discrete

Modulator is behaving as an DAC.
It gives continuous, digital signal



* isolation
* Amplification

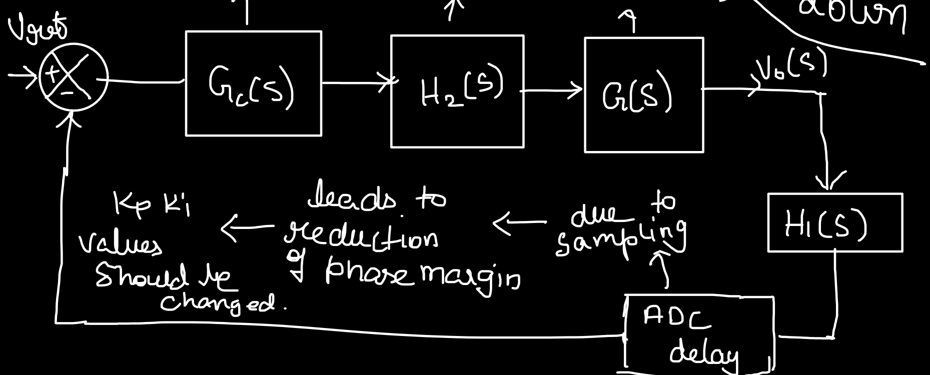
for DSP It will be integrated within the chip

FPGA
↓
we need to add all those peripherals
↓
the code is hardwired

DSP → Can take i/p of 0–3.3V & give o/p of 0–3.33V
So we ensure that the sensor o/p is scaled down to 3.3V.
↓
Will this affect the values of control loop. because we decide to design based on

eq Control loop (Approx)

$K_p + \frac{K_i}{s}$
PI



Kp Ki values Should be changed. ← leads to reduction of phase margin ← due to sampling

ADC → Sampling
↳ values @ diff time
→ Quantisation
→ Amplitude Quant } rounded to the nearest level ↓ depends on resolution
→ Time Quant

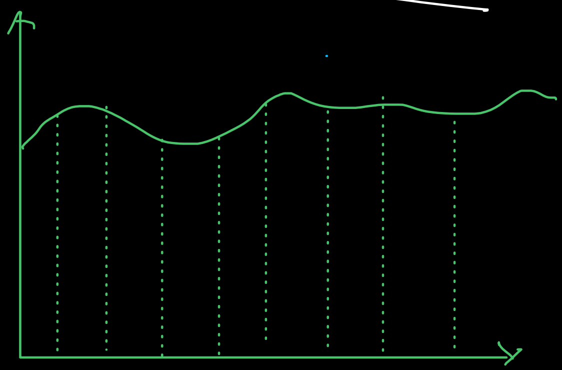
introduces non linear effects

∴

We can just scale it up in the code to the designed values.

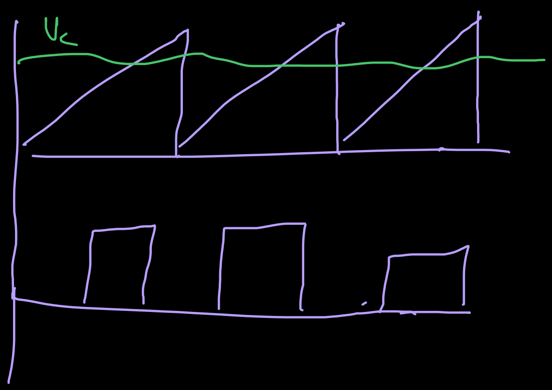
buck op voltage before step down to 3.3 V.

(back to buck voltage from 3.3V)



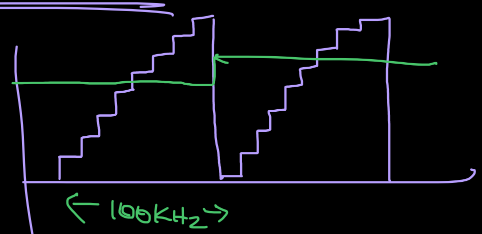
We have to consider all the effects of Digital Control (ADC, Sensors ...etc) while designing Control loop.

Analog PWM

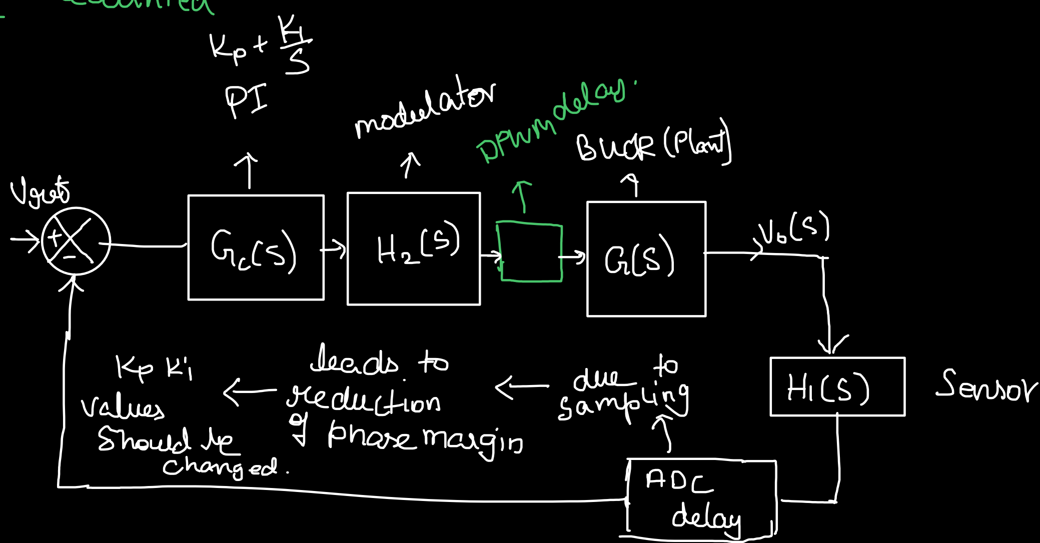


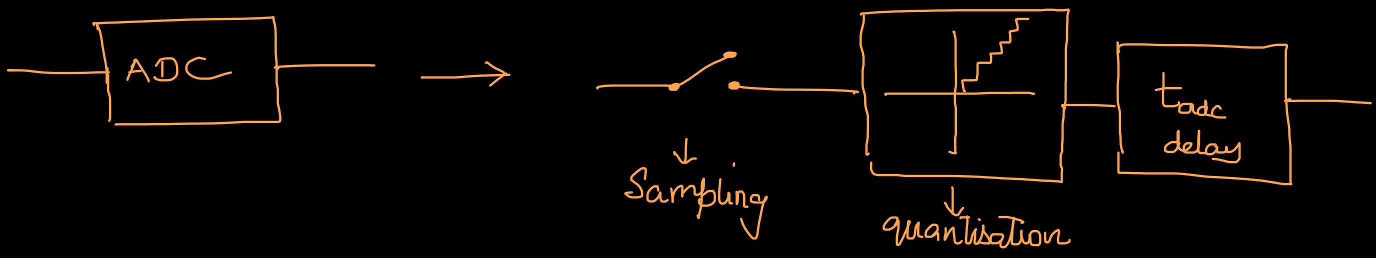
here the variation in V_c is reflected instantenously, So they are accounted

Digital PWM (essentially a counter)



Since 100kHz, the disturbance is only updated once in $\frac{1}{100k}$ s, so there is another delay in the Control loop.

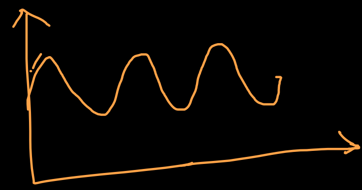




Switching Frequency choice

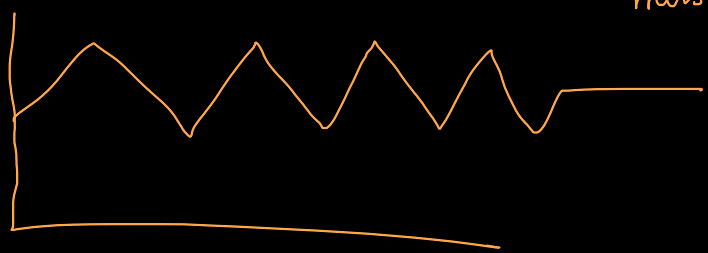
- the instance of sampling
- no of samples per cycle

} matters



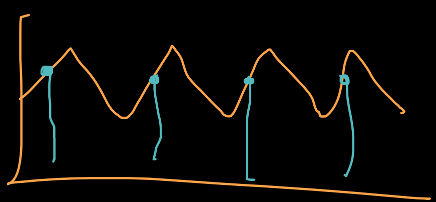
only if we sample @ peak we miss peak.

The buck converter has output ripple.



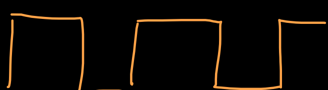
we need to eliminate the ripple because it will affect the control loop design

we can eliminate by sample @ f_s so that we get a DC value



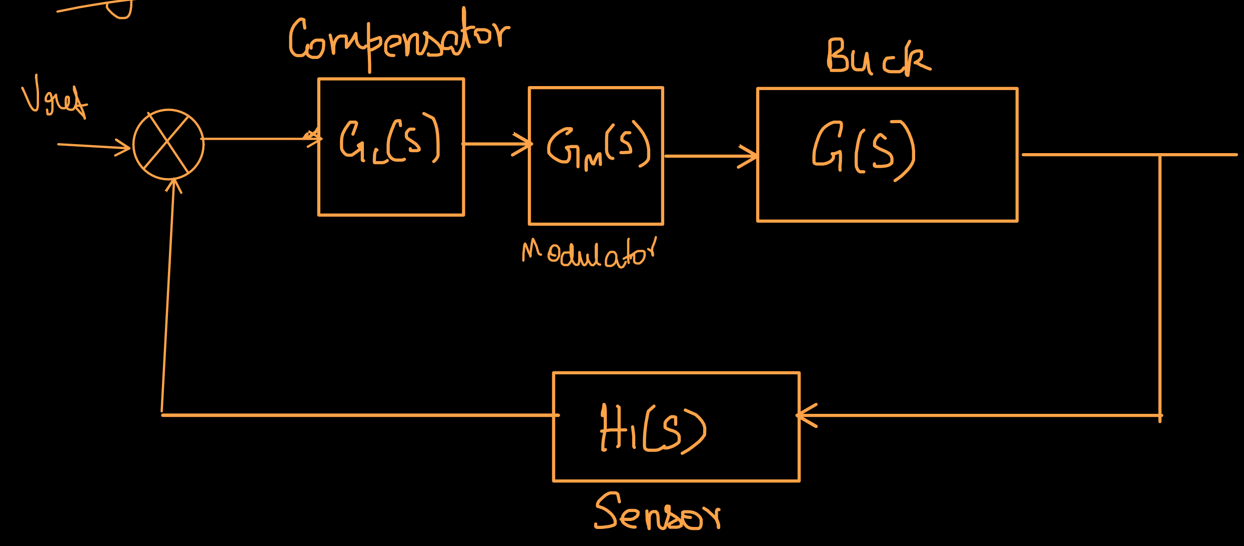
But to get the DC value we need to sample at the midpoint of the signals. ie we need to sample @ midpoint of rising or falling slope. But finding midpoint is difficult.

But we know duty ratio



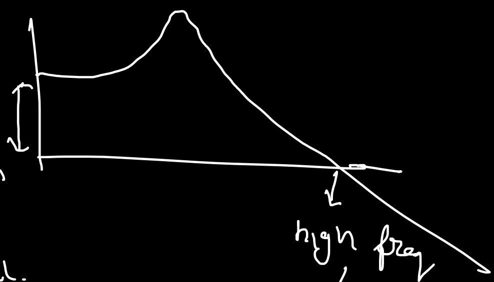
So we can sample @ midpoint of on time or off time which will correspond to the mid of risetime.

Analog Control loop



Uncompensated loop gain = $G(S)\, G_M(S)\, H_1(S)$

Draw bode plot →



low DC gain → allows DC signal. So we need to increase

high freq → need to reduce because to reduce switching ripple.

Compensated loop gain = $G_c(S)\, G(S)\, G_M(s)\, H_1(S)$

high DC gain

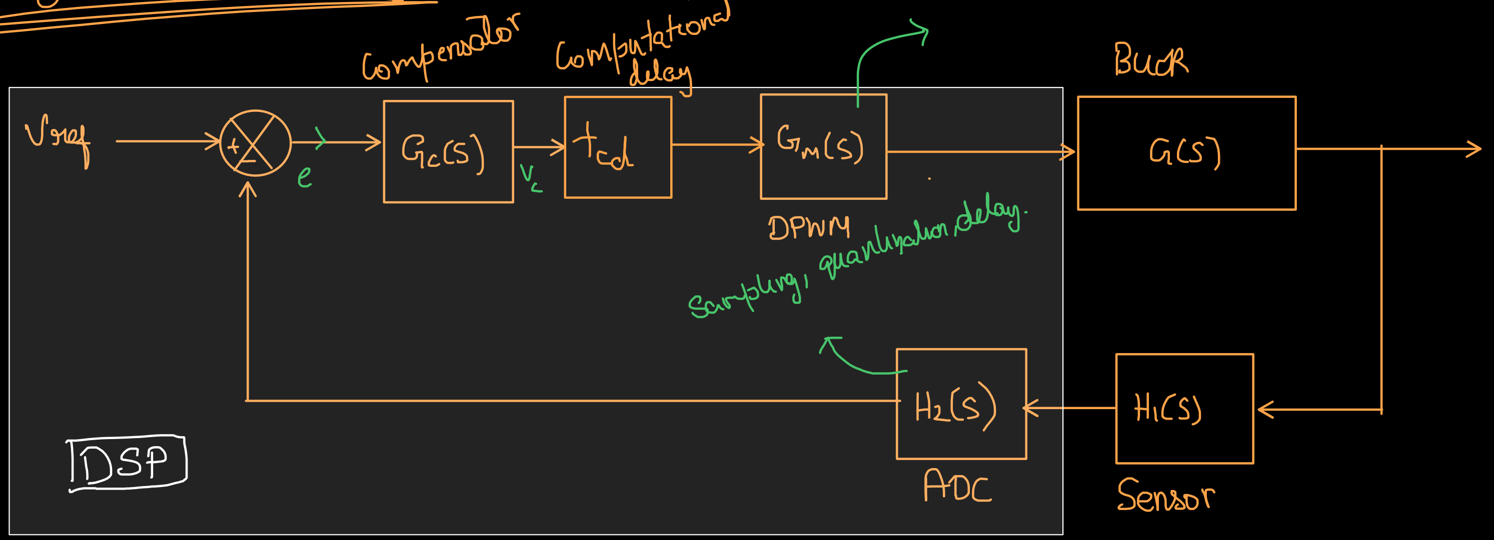
generally $\frac{1}{10}^{th}$ of f_s

low freq ⇒ less switching ripple.

We need to to get ↑ this desired shape

So our $G_c(S)$ should be such that we need to get the desired shape.

Digital Control loop

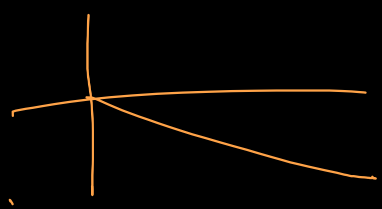


Value of $G_c(s)$ found in analog has to be redesigned because new components

$t_{cd} \rightarrow$ delay $\Rightarrow$ can be represented as e^{-st}

$\downarrow$

phase plot has a decreasing slope



$\leftarrow$ So @ higher frequencies phase margin reduces $\leftarrow$ might be in verge of instability

$\rightarrow$ So when we directly apply analog design the op will have sustained oscillations or even shootup.

PEC $\rightarrow$ Non Linear time Variant System

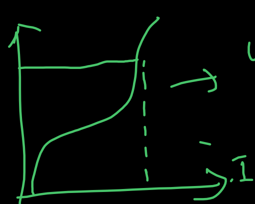
due to switching $\hookrightarrow$ 2 Configs exist

So changes with time

How come we use TF ?

$\rightarrow$ we can linearise the system

we can make it time invariant by writing 2 sets of equations (for on & off) and average it $\rightarrow$ gives non linear time invariant } then linearise



we can take i/p o/p in around a small band then, we can assume within that band, it is linear

to implement the $G_c(s)$ in code
we need TF to be in time domain

generally it will look like

$$V_c[n] = V_c[n-1] + a\, e[n] + b\, e[n-1]$$

So we use z transform, and we convert
to Z-domain and get difference equation.

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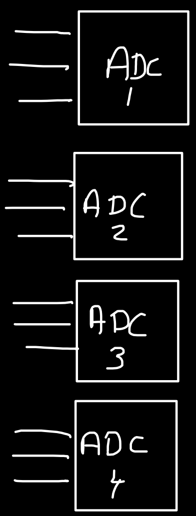
difference between fixed point vs floating point representation

Fixed no of digits after decimal

↳ Variable no of digits after decimal



4 ADC
↳ 4 channels each

So we can sample 16 signals.

but only 4 signals at once can be sampled

MODULE – II

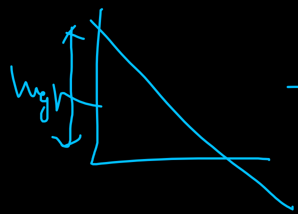
* System Variable → Controlled Variable (duty cycle, Switching Sequence)
* Control Variable $\xrightarrow{\text{Controls}}$ ↑
  ↳ usually one variable

Consider DC-DC Converter
↳ freq Components of V_o → DC
→ f_s
→ multiples of f_s

When there is a small disturbance there will also be a low freq Component for a while
↳ The time it takes to Settle to SS is called Settling time

Our Consideration

* Stability → poles → LH side
  or +ve GM & PM
* Steady State error →



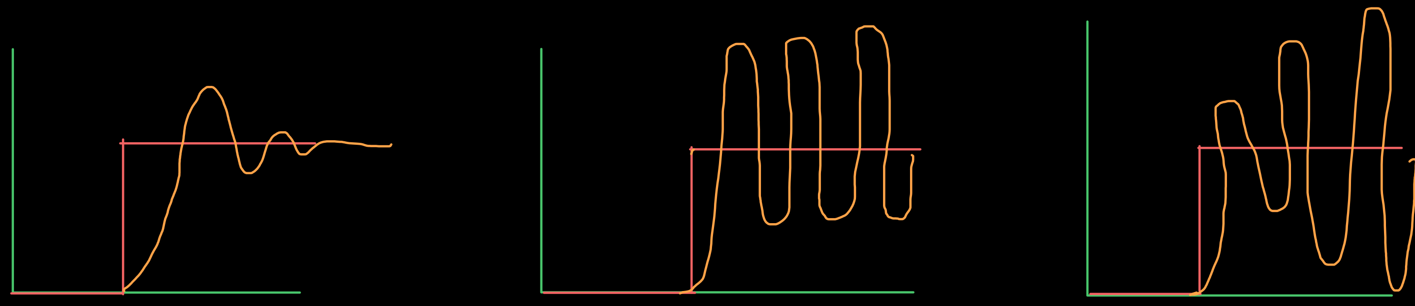
→ allows only DC to pass through
↳ we use Compensator

* Transient Response →

Standard test inputs → They are extreme condition to test our converters so that it works properly.

Usually only Step is used to test

There may be 3 possible outcomes



(a) Stable (b) Sustained oscillation (c) Unstable

* In root locus, poles on RHS will result in e^{t} (exponentially increasing) so it will cause unstability. So when poles are in LHS e^{-t} (exponentially decaying) so it will die down so it is stable.

* In bode, we saw gain & phase margin is positive for stability.

  * we have a -ve feedback system
  * We calculate gm & pm @ phase & gain crossover freq.
  * If it goes below, i.e magnitude becomes -ve, so the -ve feedback becomes +ve so it will amplify the error.

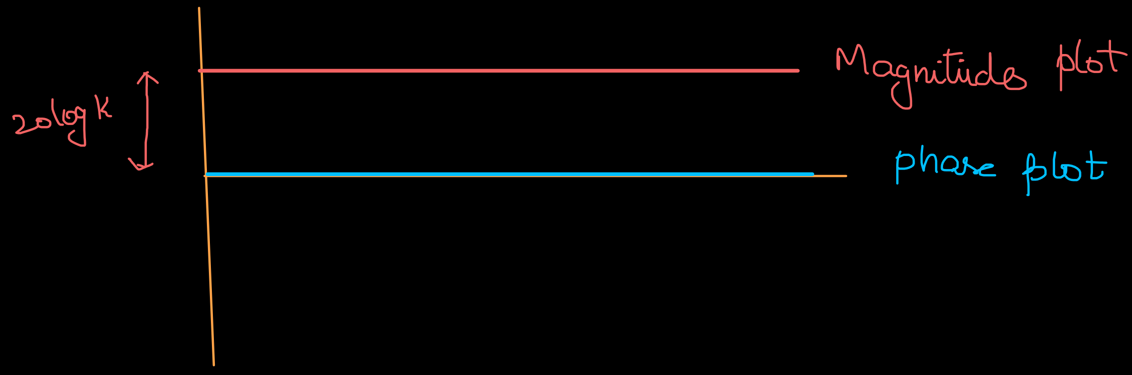
Systems that have right half zeros are called non-minimum phase system.

eg boost converter, buck boost converter

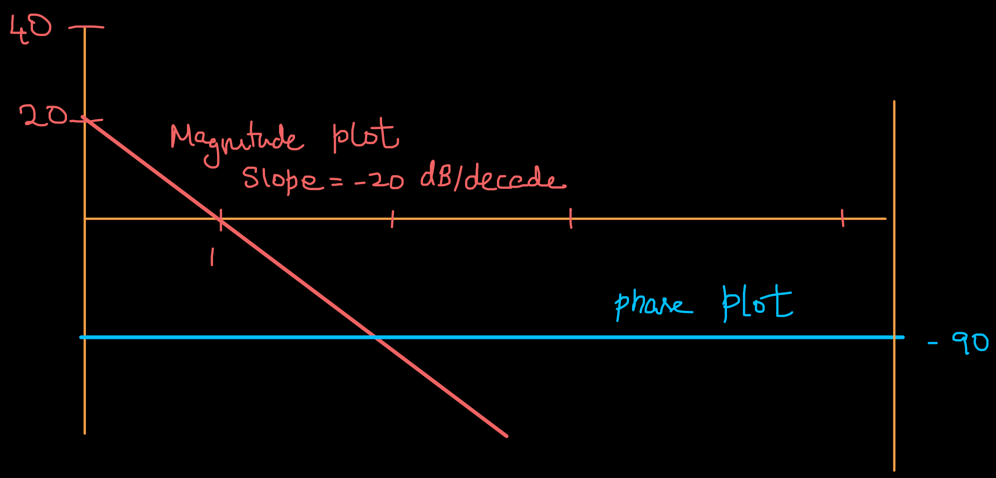
In boost converter first energy is stored in inductor, Then after that transferred to load

Bode plot

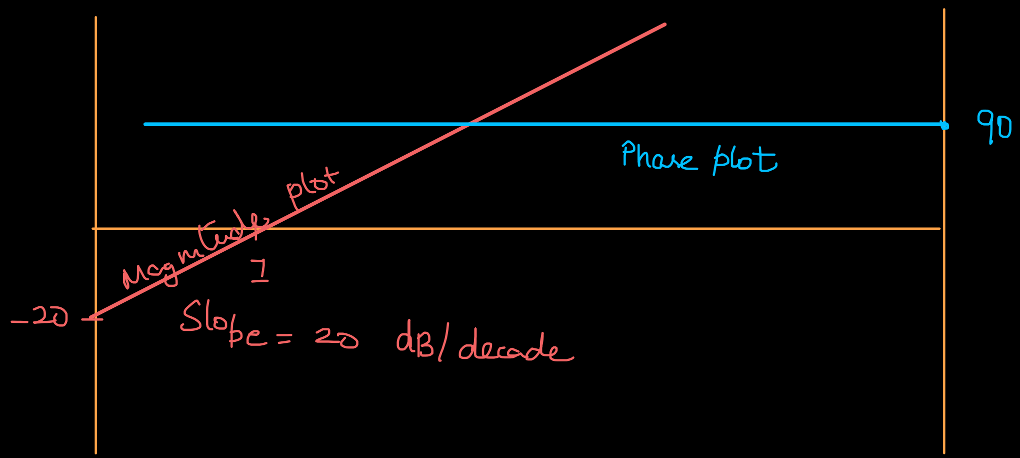
① K



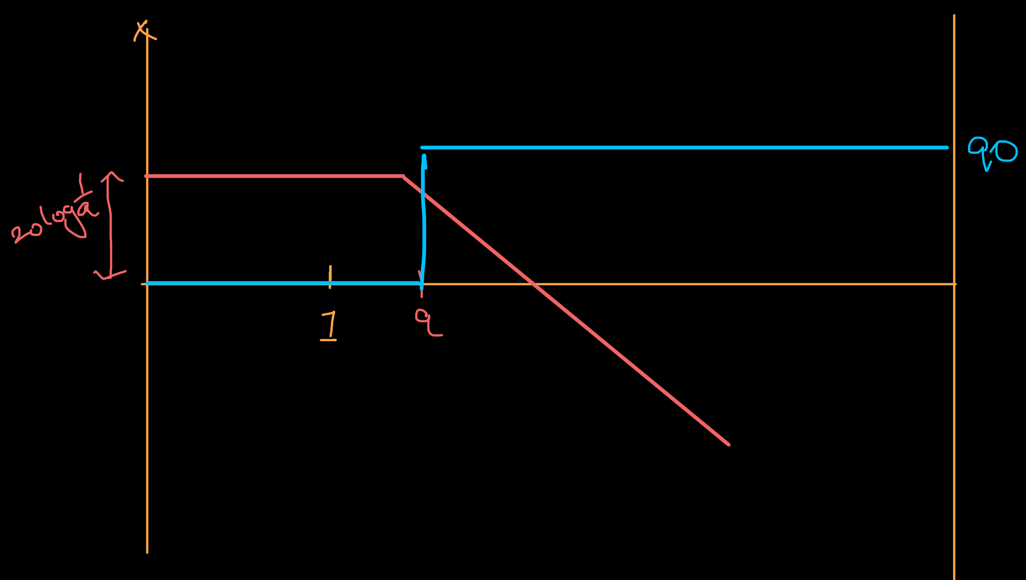
② $\frac{1}{s}$



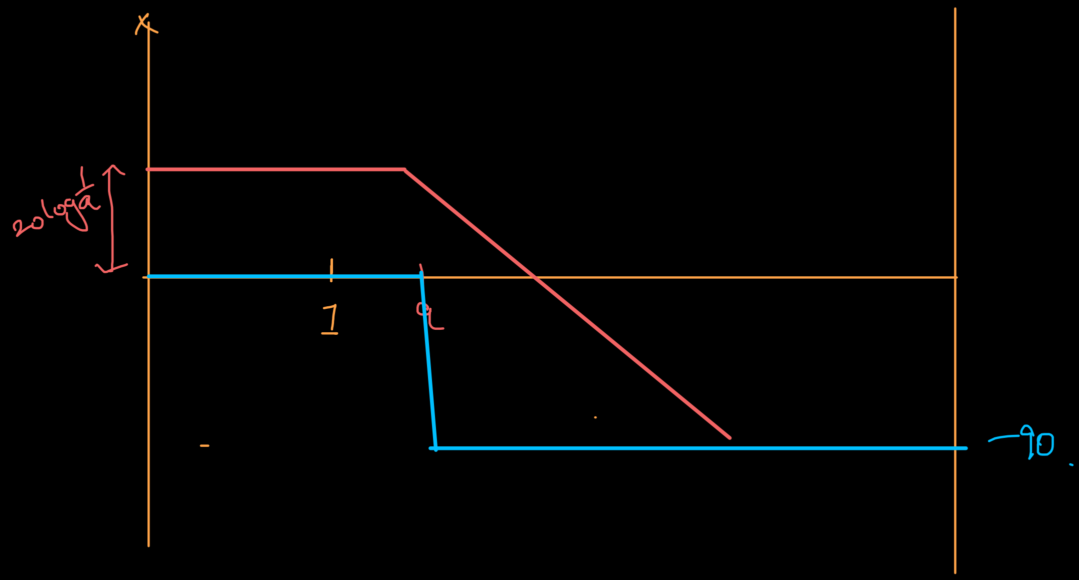
③ s



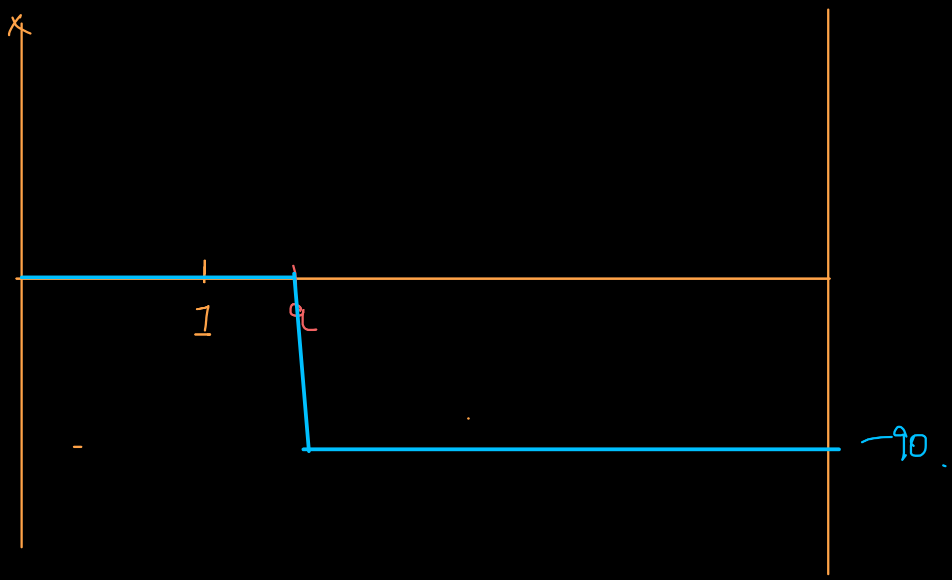
$$\frac{1}{s+a} = \frac{1}{a\left(1+\frac{s}{a}\right)}$$

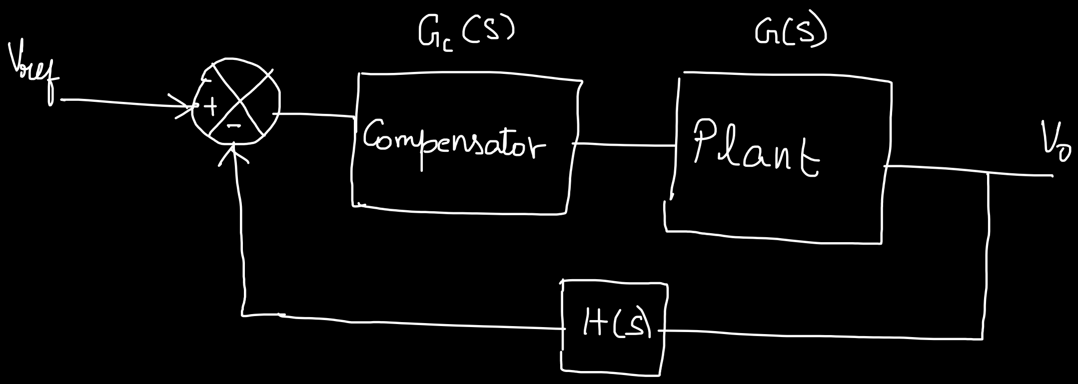


(5) $\frac{1}{S-a}$



(6) $S+a$



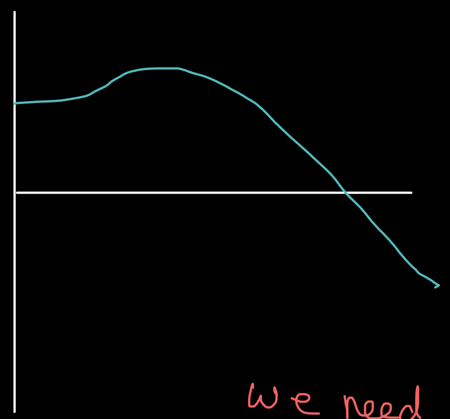


uncompensated loop Gain $= G(S)H(S) = G_1(S)$

Compensated loop Gain $= G_c(S)\,G(S)H(S) = G_2(S)$

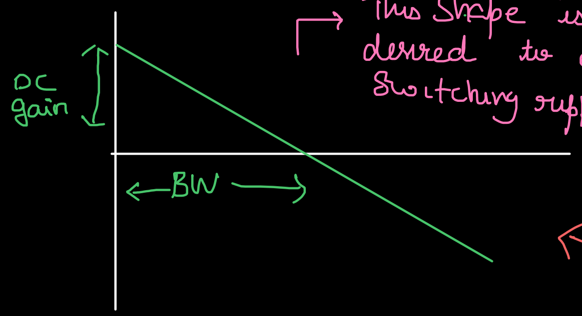
Say,

$G_1(S)$



desired bode plot

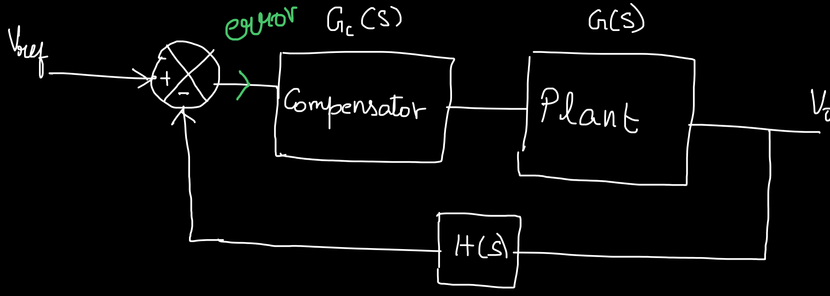
$G_2(S)$



This shape is desired to eleminate switching ripple & noise

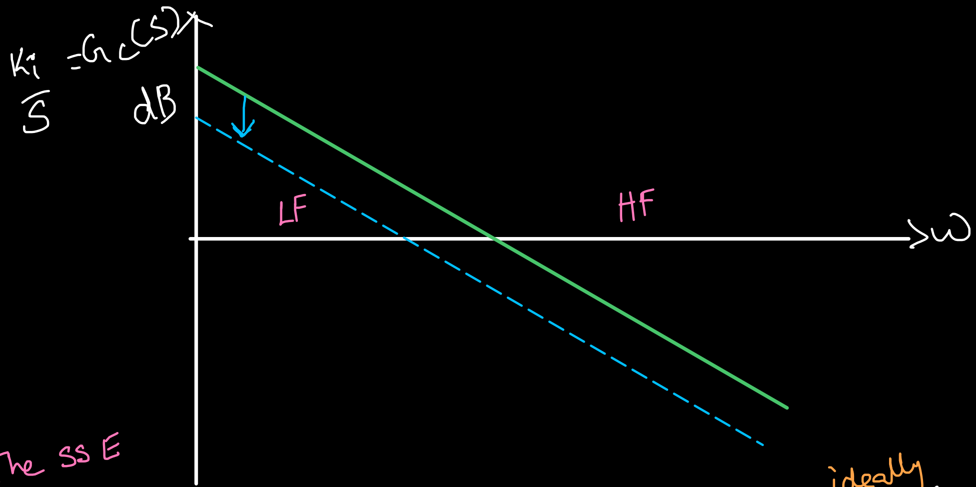
We need to design $G_c(S)$ such that the bode plot becomes like that

We can place poles and zeros to get the desired shape.

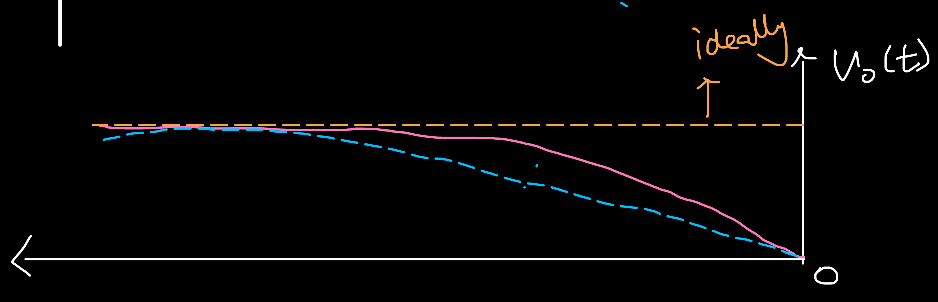


Ideally we need infinite gain to make the error 0.

So that more effort is put in the corrective action



time response to unit step input



The SS E is 0 because we have high dc gain

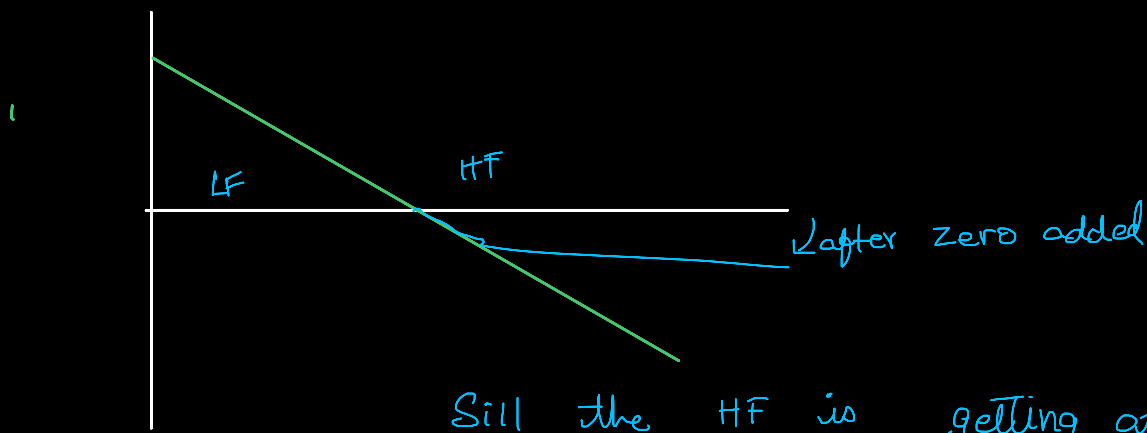
When we shift it down the responce becomes slower

The blue curve is filtering more frequency.

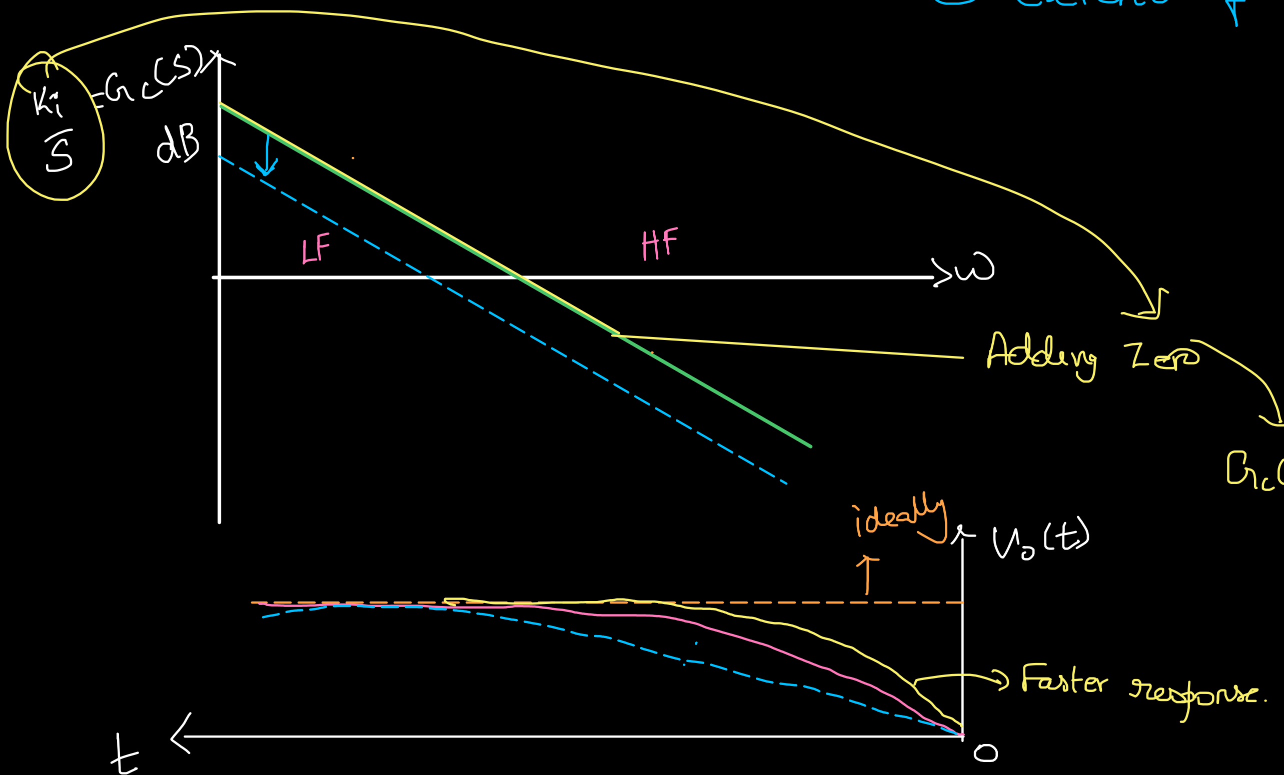
The DC gain is anyway ∞ @ 0. So it affects the BW.

The BW is low so response has become slower.

So to improve the transient response, we can add a Zero in the High frequency region.



Still the HF is getting attenuated but not to the extent of before

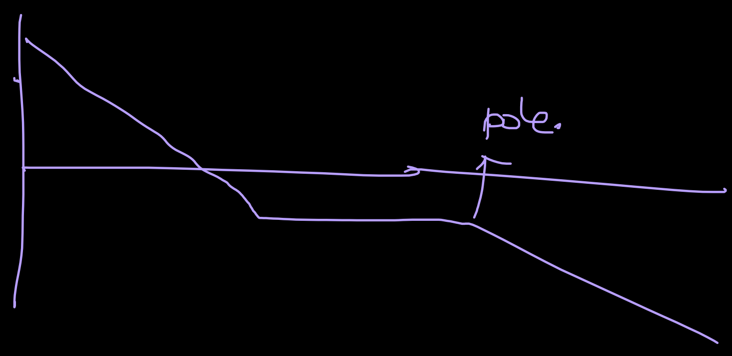


$$G_c(S) = K_p + \frac{K_i}{S}$$

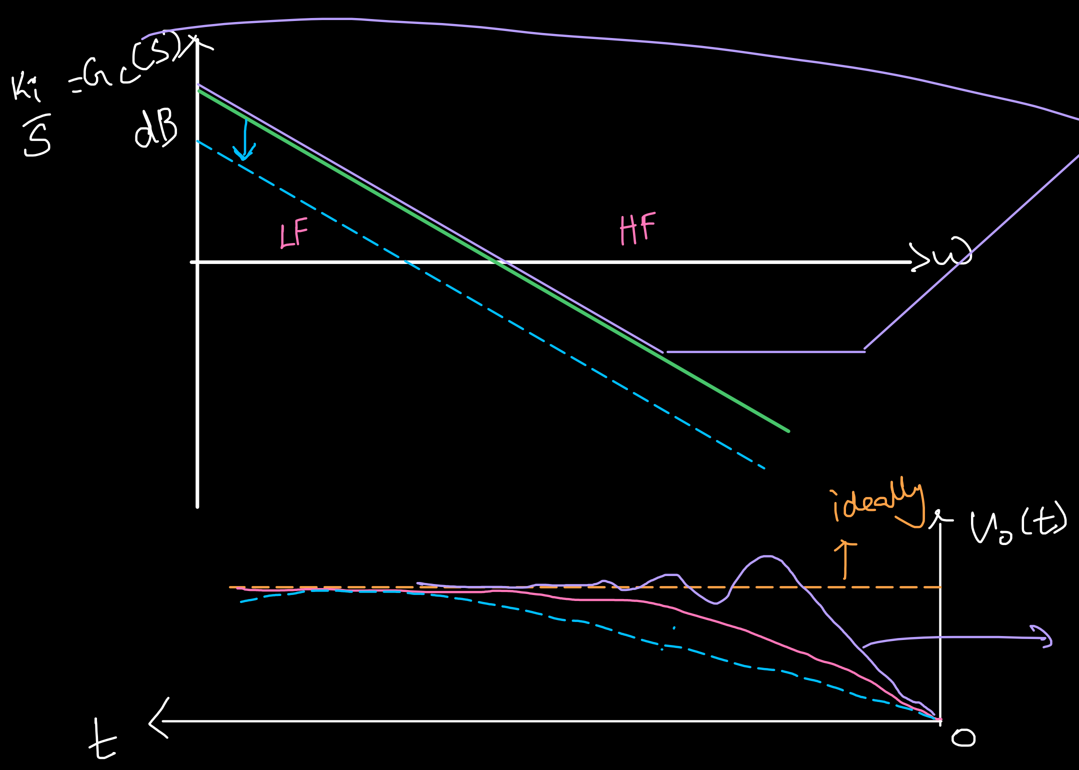
$$= \frac{SK_p + K_i}{S}$$

new Zero

To remove high frequency noise, we can put a pole somewhere further



To get even faster response, we can add another zero.



after adding one more zero,

↓

$G_c(S) = K_d + K_p + \frac{K_i}{S}$

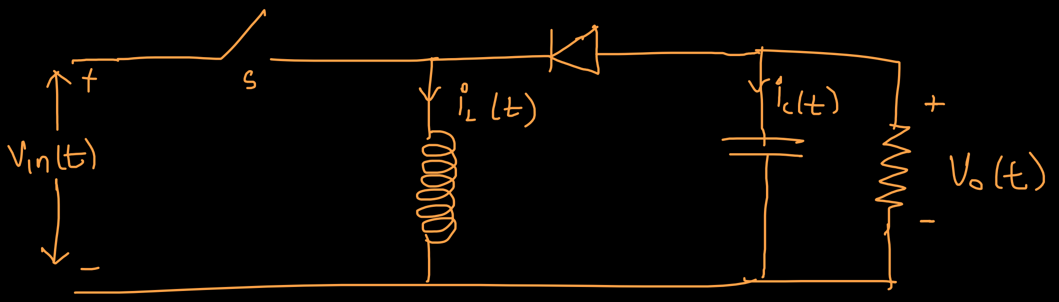
even faster response.

So in Conclusion,

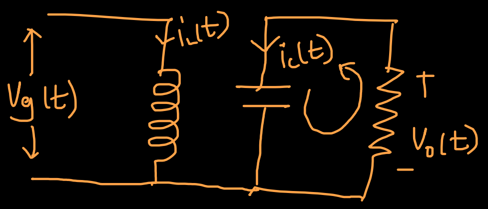
* SS response is affected by DC gain
* TS response is affected by B.W.

* P, PI, ... lag, lead .- are all linear controllers.
To track fast changing waves like high frequency Sine we need non linear controllers.

Modelling of Converter



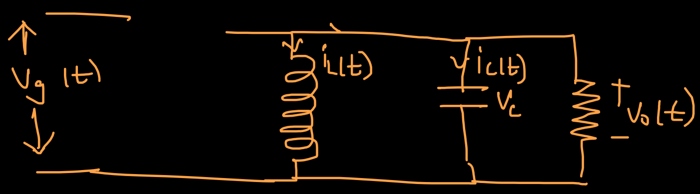
DT_s	$(1-D)T_s$



$$V_g(t) = L\frac{di_L(t)}{dt} \quad \text{—} \; (1)$$

$$i_c(t) = -\frac{V_o(t)}{R}$$

$$C\frac{dV_o}{dt} = -\frac{V_o(t)}{R} \quad \text{—} \; (2)$$



$$V_o(t) = \frac{L\,di_L(t)}{dt} \quad \text{—} \; (3)$$

$$\frac{C\,dV_o}{dt} = \frac{-V_o}{R} - i_L(t) \quad \text{—} \; (4)$$

Now we average them to reduce to 1 set of eqn.

$$\left[(1) \times DT_s + (2) \times (1-D)T_s \right] \div T_s$$

$$\frac{V_g(t)\,DT_s + V_o(t)(1-D)T_s}{T_s} = DT_s\,\frac{L\,di_L(t)}{dt} + (1-D)T_s\,\frac{L\,di_L(t)}{dt}$$

$D \to$ also function of time

$D \to D(t)$

$$d(t)\, V_g(t) + (1-d(t))V_o(t) = d(t) L \frac{di_L(t)}{dt} + (1-d(t)) \frac{L\, di_L(t)}{dt}$$

$$d(t)\, V_g(t) + (1-d(t))V_o(t) = L \frac{di_L(t)}{dt} \quad \text{—— (5)}$$

$$\text{III}^{y} \left[(2)\, d(t) T_s + (4)\, (1-d(t)) T_s \right] \div T_s$$

$$d(t)\, \frac{C\, dv_o(t)}{dt} + [1-d(t)]\, \frac{C\, dv_o(t)}{dt} = -\frac{V_o(t)}{R} d(t) - (1-d(t)) \frac{V_o(t)}{R} - (1-d(t))\, i_L(t)$$

$$\frac{C\, dV_o(t)}{dt} = \frac{-V_o(t)}{R} - (1-d(t))\, i_L(t) \quad \text{—— (6)}$$

$\underbrace{(5) \text{ \& } (6)}_{}$ $\Rightarrow$ has averaged the dynamics of 2 modes of ckt

Called as "Time averaged model"

So we have made it time invariant in one switching cycle

But still is non-linear

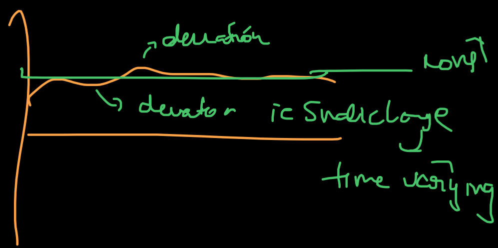
↓ done by linearization.

* Consider a small operating region.
* We can assume it is linear in a small region around the operating point.

So the controller will be able to handle only small variations within the eqn we will derive will become invalid.

This is called 'small signal model'

$$d(t) = \overset{\text{const}}{D} + \overset{\text{small chang } \Delta d}{\hat{d}}$$



$$v_g(t) = V_g + \hat{v}_g$$

$$v_o(t) = V_o + \hat{v}_o$$

$$i_L(t) = I_L + \hat{i}_L$$

$$\therefore (5) \Rightarrow L\frac{d}{dt}(I_L + \hat{i}_L) = (D+\hat{d})(V_g+\hat{v}_g) + (1 - D - \hat{d})(V_o + \hat{v}_o)$$

$$L\frac{dI_L}{dt} + L\frac{d\hat{i}_L}{dt} = DV_g + D\hat{v}_g + \hat{d}V_g + \hat{d}\hat{v}_g + V_o - DV_o - \hat{d}V_o + \hat{v}_o - D\hat{v}_o - \hat{d}\hat{v}_o$$

$$= DV_g + V_o - DV_o + D\hat{v}_g + \hat{d}V_g - \hat{d}V_o - \hat{v}_o D + \hat{v}_o + \hat{d}\hat{v}_g - \hat{d}\hat{v}_o$$

$$\overset{\approx 0}{\boxed{L\left(\frac{dI_L}{dt} + \frac{d\hat{i}_L}{dt}\right) = \underbrace{\left[DV_g + (1-D)V_o\right]}_{\text{DC terms}}} + \underbrace{\left[D\hat{v}_g + (1-D)\hat{v}_o + (V_g - V_o)\hat{d}\right]}_{\text{1st order ac terms}} + \boxed{\underbrace{\left[\hat{d}(\hat{v}_g - \hat{v}_o)\right]}_{\text{2nd order ac terms}}}$$

2nd order ac terms $\downarrow$ Can be neglected because very small.

$$\therefore \quad L\frac{d\hat{i}_L}{dt} = D\hat{v}_g + (1-D)\hat{v}_o + (V_g - V_o)\hat{d} \quad \text{——} (7)$$

$$(6) \Rightarrow \quad C\frac{d}{dt}\left(V_o + \hat{v}_o\right) = -\frac{V_o}{R} - \frac{\hat{v}_o}{R} - (1-D-\hat{d})(I_L + \hat{i}_L)$$

$$C\frac{dV_o}{dt} + C\frac{d\hat{v}_o}{dt} = -\frac{V_o}{R} - \frac{\hat{v}_o}{R} - I_L - \hat{i}_L + DI_L + D\hat{i}_L + \hat{d}I_L + \hat{d}\hat{i}_L$$

$$= -\frac{V_o}{R} - I_L + DI_L - \frac{\hat{v}_o}{R} - \hat{i}_L + D\hat{i}_L + \hat{d}I_L + \hat{d}\hat{i}_L$$

$$\underbrace{C\left(\frac{dV_o}{dt}\right.}_{\text{Amp-Sec balance.}} + \left.\frac{d\hat{v}_o}{dt}\right) = \underbrace{\left[-(1-D)I_L - \frac{V_o}{R}\right]}_{\text{DC term} = 0} + \left[-(1-D)\hat{i}_L - \frac{\hat{v}_o}{R} + I_L\hat{d}\right] + \underbrace{\boxed{\hat{d}\,\hat{i}_L}}_{\text{2nd order term neglected because small}}$$

$$\therefore \quad C\frac{d\hat{v}_o}{dt} = -(1-D)\hat{i}_L - \frac{\hat{v}_o}{R} + I\hat{d} \quad \text{——} (8)$$

(7) & (8) $\rightarrow$ Small Signal forms.

We are using d to control V_o. So we need the transfer function $\left.\dfrac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{V_g(s)=0}$

Laplace 7 & 8

7 $\Rightarrow \quad L\,s\,\hat{I}_L(s) = 0 + (1-D)\,\hat{V}_o(s) + (V_g - V_o)\,\hat{D}(s)$

$$(1-D)\,\hat{V}_o(s) = L\,s\,\hat{I}_L(s) - (V_g - V_o)\,\hat{D}(s)$$

8 $\Rightarrow \quad C s\,\hat{V}_o(s) = (1-D)\,\hat{I}_L(s) - \frac{\hat{V}_o(s)}{R} - I_L\,\hat{D}(s)$

$$\left(Cs + \frac{1}{R}\right)\hat{V}_o(s) = (1-D)\,\hat{I}_L(s) - I_L\,\hat{D}(s)$$

$$\hat{I}_L(s) = \frac{\left(Cs + \frac{1}{R}\right)\hat{V}_o(s) + I_L\,\hat{D}(s)}{Cs + 1/R}$$

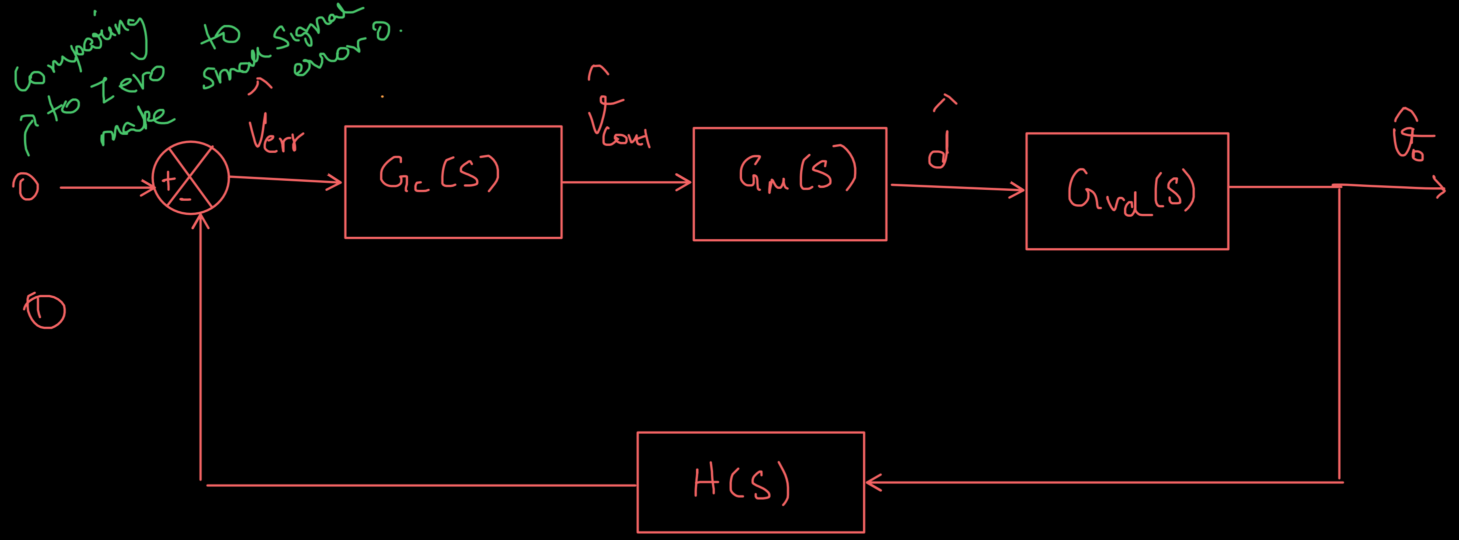
$I_L \rightarrow$ in terms of I_o

$I_o = \frac{V_o}{R}$

$=$

$$G_{v_d}(s) = \frac{\hat{V}_o(s)}{\hat{d}(s)} = \frac{G_{do}\left(1 - \frac{s}{\omega_2}\right)}{1 + \frac{s}{Q\,\omega_o} + \frac{s^2}{\omega_o^2}}$$

	G_{do}	ω_o	Q	ω_2
Buck	V_o/D	$1/\sqrt{LC}$	$R\sqrt{\frac{C}{L}}$	∞
Boost	$V_o/_{1-D}$	$\frac{1-D}{\sqrt{LC}}$	$(1-D)\,R\sqrt{\frac{C}{L}}$	$(1-D)^2\frac{R}{L}$
Buck-Boost	$\frac{V_o}{D(1-D)}$	$\frac{(1-D)}{\sqrt{LC}}$	$(1-D)\,R\sqrt{\frac{C}{L}}$	$\frac{(1-D)^2 R}{DL}$



①

There are 2 approaches to closed loop control

① We can take the small signal value. ie deviation from average value. and find $\hat{d}$ which is chand in duty - So we need to add $D+\hat{d}$ and give to converter - And while sensing V_o we need to extract $\hat{v}_o$ from the signal by subtracting with average value.

② We can directly sense the $V_o(t)$ and comput $d(t)$.

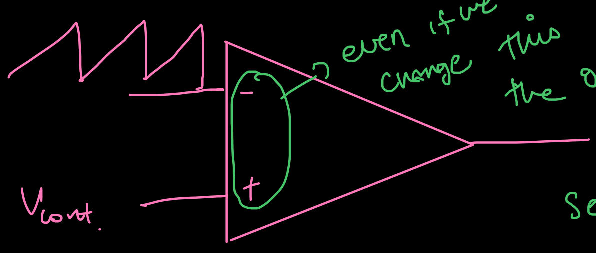
ie) * in ① we are trying to make $\hat{v}_o$ zero

* in ② we are trying to make $v(t)$ equal to average value

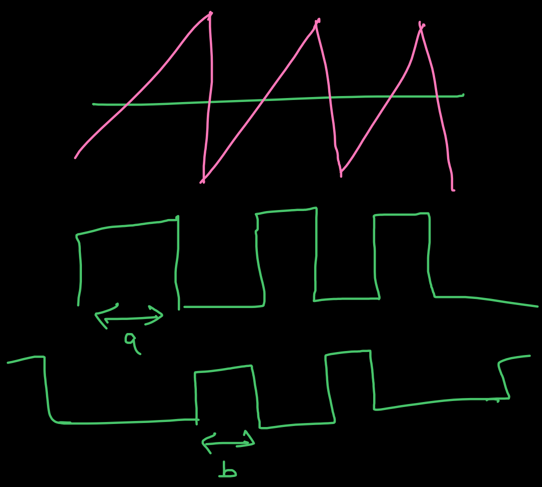
$\hat{V}_o$ is very small.

The time taken by integrator to settle bigger number is more.

So ② will have sluggish response

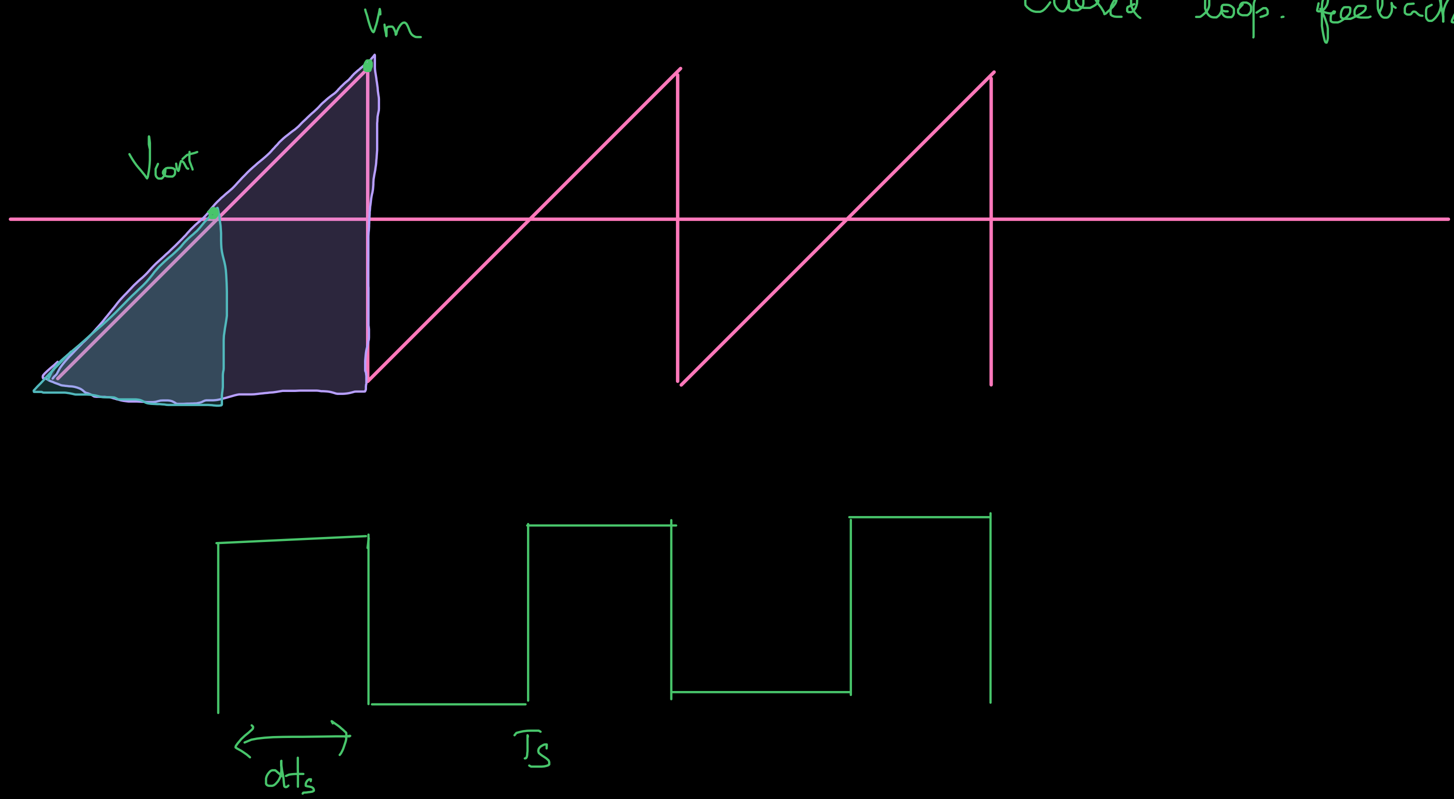


even if we change this the output will eventually settle @ desired o/p due to the closed loop.



$a \neq b$

but due to closed loop eventually $a \to b$ due to closed loop. feedback.



$$V_m \propto T_s$$

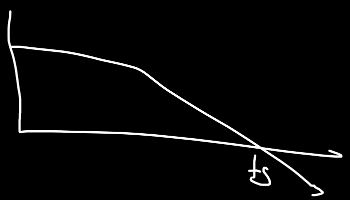
$$V_{cont} \propto d(t) T_s$$

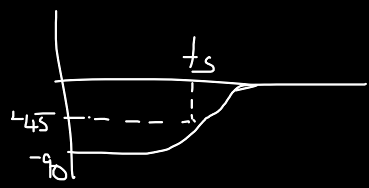
$$\frac{V_m}{V_{cont}} = \frac{T_s}{d(t) T_s}$$

$$d(t) = \frac{V_{con}(t)}{V_m}$$

$$\Rightarrow \boxed{\frac{d(t)}{V_{cont}(t)} = \frac{1}{V_m}}$$

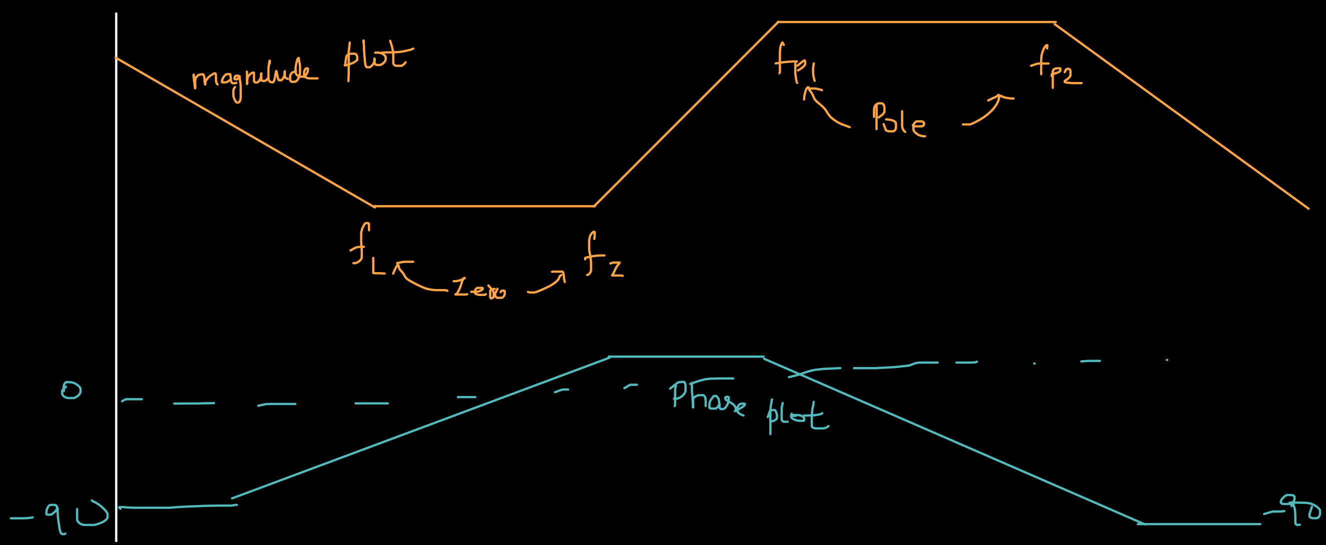
Lab - Session 1





① Lag Compensator $\longrightarrow$ PI

② Lag lead Compensator $\longrightarrow$ PID



$$G(s) = \frac{G_0\left(1+\frac{\omega_L}{s}\right)\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{P_1}}\right)\left(1+\frac{s}{\omega_{P_2}}\right)}$$

Buck Converter

$V_g = 28\,V$

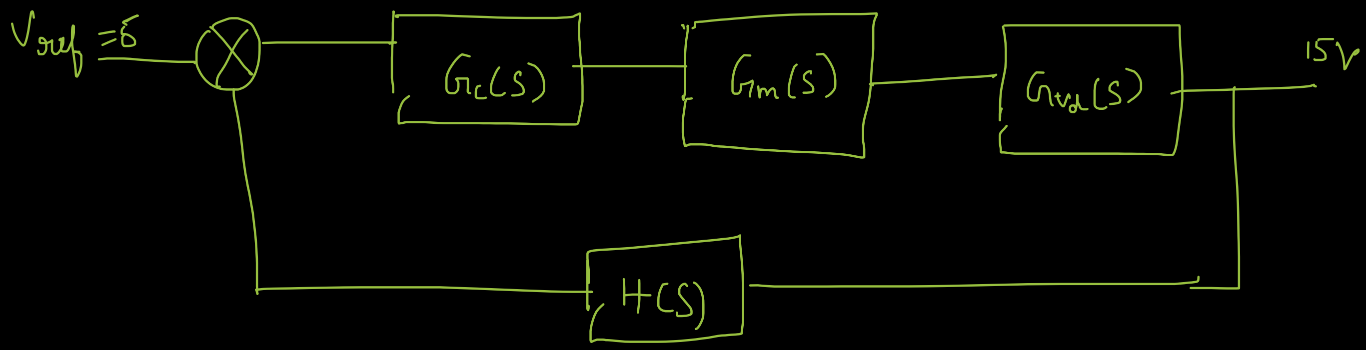
$V_o = 15\,V$

$I_o = 5\,A$

$R = 3\,\Omega$

$V_{ref} = 5\,V$

$V_{in} = 4\,V$



$$H(s) = \frac{5}{15} = \frac{1}{3}$$

$$G_m(s) = \frac{1}{V_m} = \frac{1}{4}$$

$$G_{v_d}(s) = \frac{\hat{V}_o(s)}{\hat{d}(s)} = \frac{G_{do}\left(1 - \frac{s}{\omega_2}\right)}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}$$

$$G_{do} = \frac{V_o}{D} = \frac{15}{0.5357} = 28$$

$$Q = R\sqrt{\frac{C}{L}} = 3\sqrt{\frac{500 \times 10^{-6}}{50 \times 10^{-6}}} = 9.4868$$

$$GV_d(s) = \frac{28\left(1 - \frac{s}{\infty}\right)}{1 + \frac{s}{9.4868(6324.555)} + \frac{s^2}{(6324.555)^2}}$$

$$\omega_o = \frac{1}{\sqrt{LC}} = 6324.555$$

$$= \frac{28}{2.5\times10^{-8}s^2 + 1.6\times10^{-5}s + 1}$$

Uncompensated loop gain $= G_{vd}(s)\ G_m(s)\ H(s)$

$$= \frac{2.33}{2.5\times10^{-8}s^2 + 1.6\times10^{-5}s + 1}$$

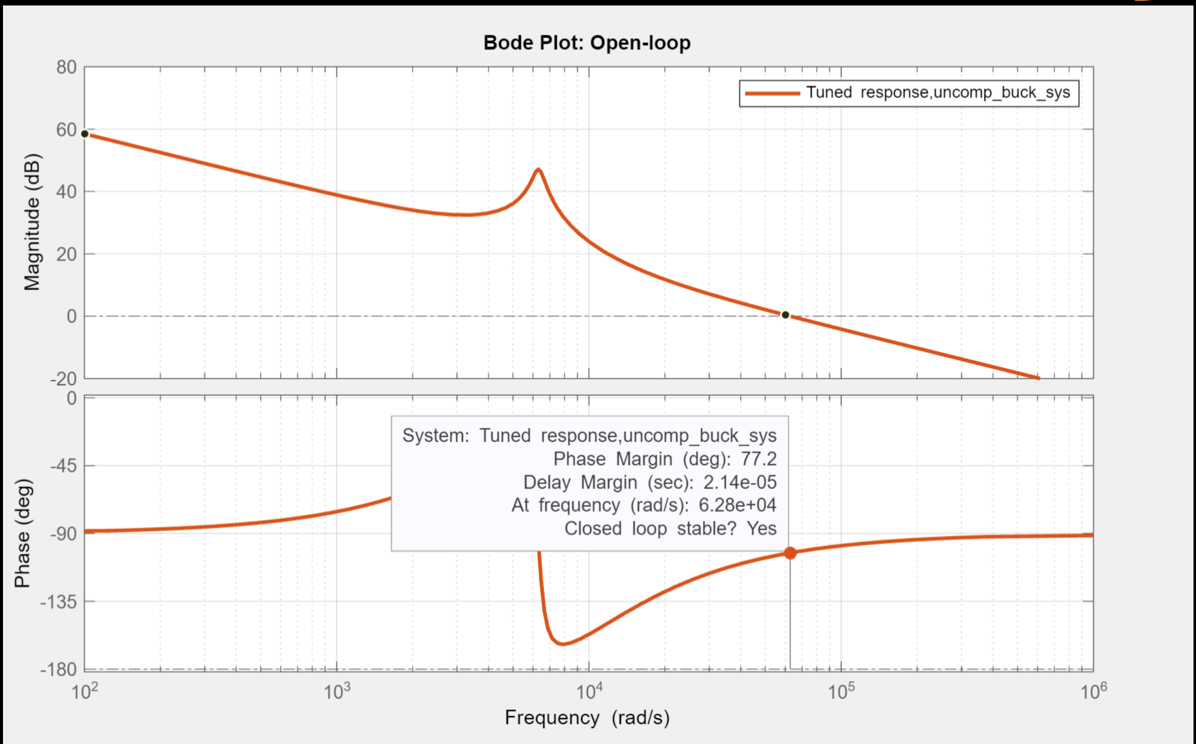
Desired B.W $= 10$ kHz

PM $= 60^\circ$

DC gain $= \infty$

Compensated TF $= T_c(s) = T_u(s)\ \underbrace{G_c(s)}_{}$

$\uparrow$ P.D



	Tuned
Kp	9.7454
Ki	36071.3877
Kd	0.00065823
Tf	n/a

```
PID =

             1
  Kp + Ki * --- + Kd * s
             s

  with Kp = 9.75, Ki = 3.61e+04, Kd = 0.000658
```

Now convert the $G_c(s)$ to $G_c(z)$

→ Forward Euler Method

→ Backward Euler Method

→ Tustin Method

(bilinear Transformation)

$$s = \frac{2}{T_s}\left(\frac{z-1}{z+1}\right)$$

c2d

matlab function

$$\therefore G_c(s) = 9.75 + \frac{36071.3877}{s} + 0.00065823\, s$$

$$= 9.75 + \frac{36071.3877}{2(100\times 10^{3})\left(\frac{z-1}{z+1}\right)} + 0.00065823\; 2(100\times10^{3})\left(\frac{z-1}{z+1}\right)$$

$$= 9.75 + 0.18035\left(\frac{z+1}{z-1}\right) + 131.646\,\frac{z-1}{z+1}$$

$$= \frac{(z-1)(z+1) + 0.18035\,(z+1)^2 + 131.646\,(z-1)^2}{(z+1)\,(z-1)}$$

$$= 9.75z^2 - 9.75 + 0.18035\,z^2 + 0.18035 + 0.36070z + 131.646\,z^2$$

$$+ 131.646 - 263.292z$$

~~263.6527~~

$$= 142.57635\,z^2 + -262.9313 + \frac{120}{}$$

Backward Euler	Forward Euler	Tustin (Bilinear Transformation)
$S = \frac{z-1}{z\,T_{samp}}$	$S = \frac{z-1}{T_{samp}}$	$S = \frac{2}{T_{samp}}\left(\frac{z-1}{z+1}\right)$

Backward Euler

$$G_c(s) = 9.75 + \frac{36071.3877}{s} + 0.00065823\, s$$

$$= 9.75 + \frac{36071.3871\, z}{(z-1)\, 100\times10^{3}} + \frac{0.00065823\,(z-1)\, 100\times10^{3}}{z}$$

$$= 9.75 + \frac{0.36071\, z}{(z-1)} + \frac{65.823\,(z-1)}{z}$$

$$= 9.75\,(z-1)z + 0.36071\, z^2 + 65.823\,(z-1)^2 \,/\, (z-1)\, z$$

$$= \frac{9.75\, z^2 - 9.75 z + 0.36071 z^2 + 65.823 z^2 + 65.823 - 131.646 z}{z(z-1)}$$

$$= \frac{75.93371 z^2 - 141.396\, z + 65.823}{z^2 - z}$$

Forward Euler

$$G_c(s) = 9.75 + \frac{36071.3877}{s} + 0.00065823\, s$$

$$= 9.75 + \frac{36071.3877}{(z-1)\, 100\times10^{3}} + 0.00065823\,(z-1)\, 100\times10^{3}$$

$$= 9.75 + \frac{0.36071}{z-1} + 65.823\,(z-1)$$

$$= \frac{9.75z - 9.75 + 0.36071 + 65.823z^2 + 65.823 - 131.646z}{z-1}$$

$$= \frac{65.823z^2 - 121.896z + 53.43371}{z-1}$$

Try for diff frequencies,

---

from tustin we got,

$$\frac{15z^2 - 26z + 12}{z^2 - 1} = \frac{Y(z)}{X(z)}$$

$T_{samp} = 10\,\mu s$

Taken inverse,

$$\frac{15 - 26z^{-1} + 12z^{-2}}{1 - z^{-2}} = \frac{Y(z)}{X(z)}$$

$$15X(z) - 26z^{-1}X(z) + 12z^{-2}X(z) = Y(z) - z^{-2}Y(z)$$

$$15x(n) - 26x(n-1) + 12x(n-2) = y(n) - y(n-2)$$

$x \rightarrow$ error

$x(n) \rightarrow$ present error

$x(n-1), (n-2) \rightarrow$ past errors

y = Duty ratio (Compensator o/p duty)

$$y(n) = 15\,x(n) - 26\,x(n-1) + 12\,x(n-2) + y(n-2)$$

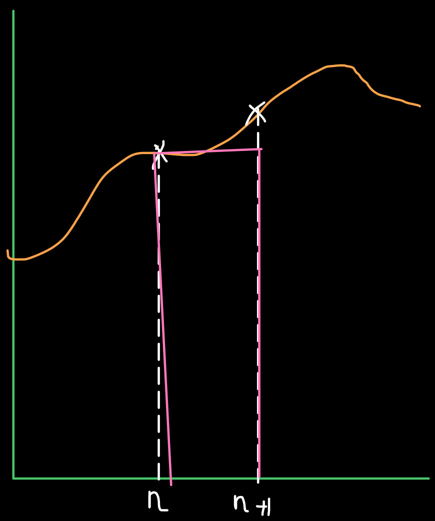
ie) $$d(n) = 15\,e(n) - 26\,e(n-1) + 12\,e(n-2) + d(n-2)$$

this expression to be implemented in dsp.

Forward Euler

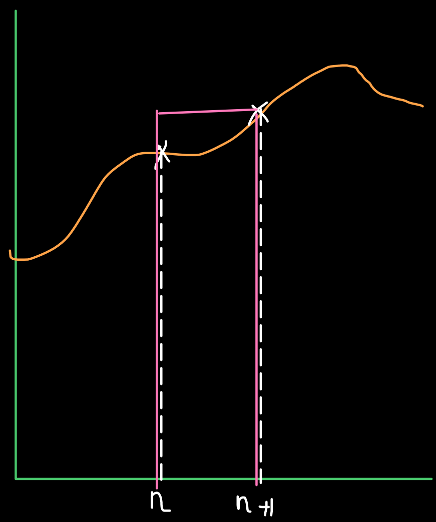
Backward Euler

Tustin



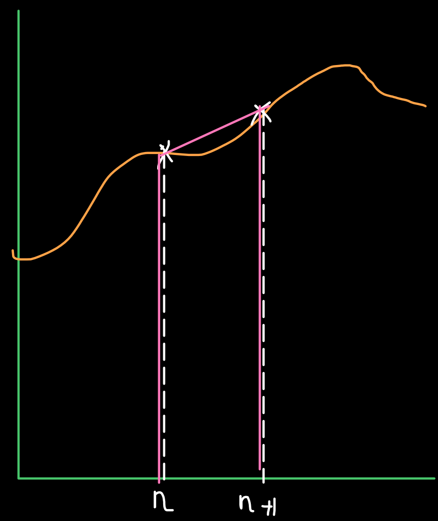
$n \to n+1$

Rectangle



$n+1 \to n$

Rectangle

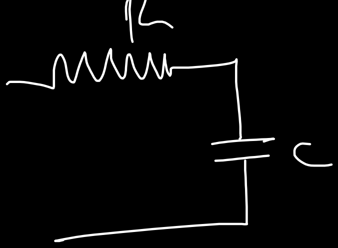


$n \leftrightarrow n+1$

Straight line joining

$\Rightarrow$ Trapezoid

—XX —XX — MIDSEM EXAM — XX — XX —



$\frac{1}{2\pi RC} \rightarrow$ cutoff frequency

Sampling freq should be higher than this

If phase margin is not correct

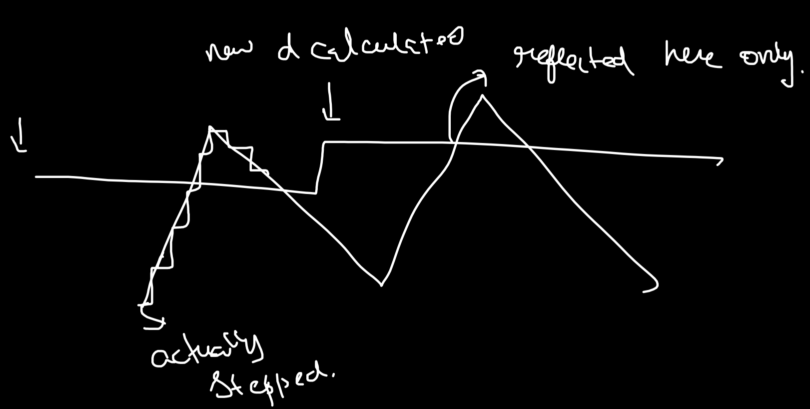
↳ cause ossilatory behaviours.

Because we have not considered parasitic elements, delays in ADC, Sensor

So to get the actual bode plot we can use a network analyser.

delays : ADC delay
Sensor delay
Computational delay
DPWM delay

↓



Delay is represented as transportation delay

Can be modelled as e^{-st_d}

e^{-st_d}

Magnitude: 1

phase: $= -\omega t_d$

$\left(e^{-j\theta} = \cos\theta - j\sin\theta \right.$

$|e^{-j\theta}| = 1$

$\angle e^{-j\theta} = \tan^{-1}(\tan\theta)$

$= -\theta$

So magnitude is not affected by the delay but phase is decreasing linearly, when decreases the phase margin.

also $f \propto$ phase
(ω)

So higher switching frequency will also decrease the phase

There are the causes for oscillations.

SiC

GaN

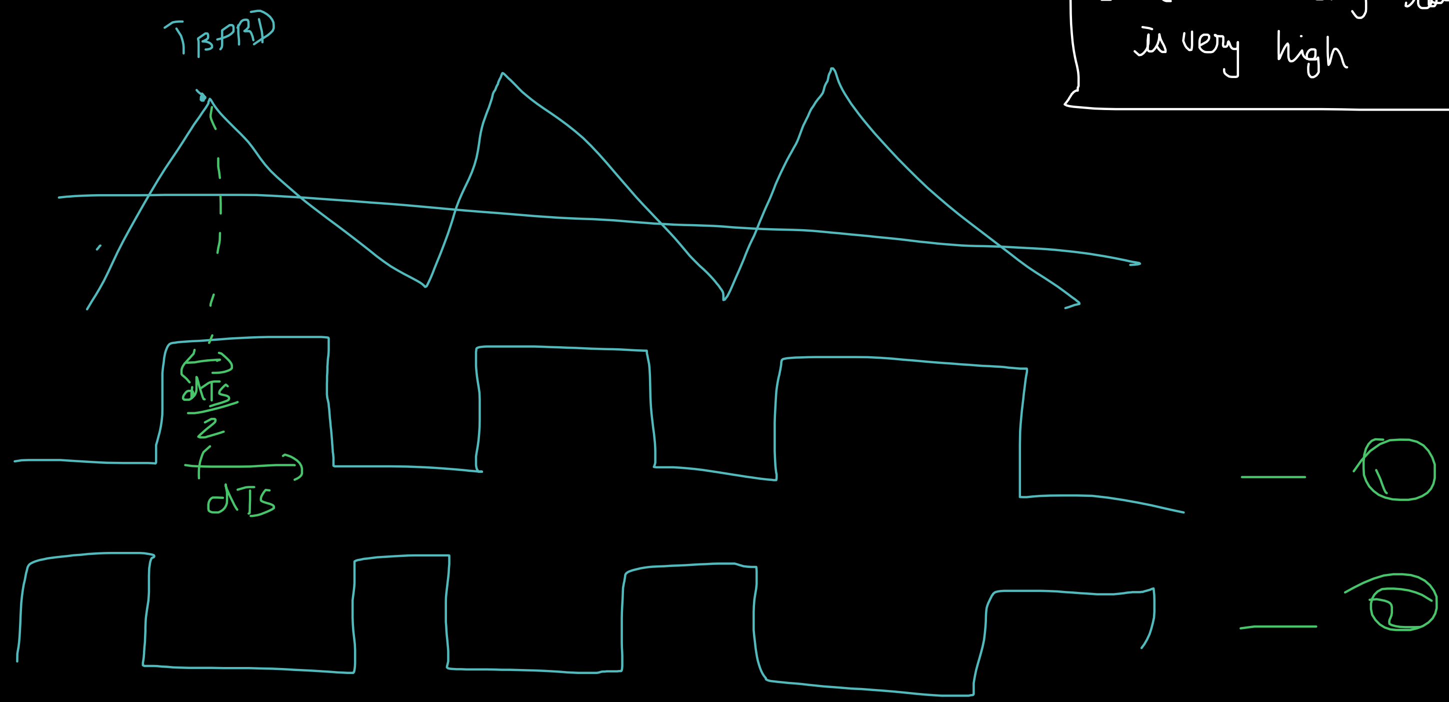
Mosfets

$\downarrow$

Capable of

MHz $\leftarrow$ high frequency switching with lower switching loss

& mosfets also can switch fast but switching loss is very high

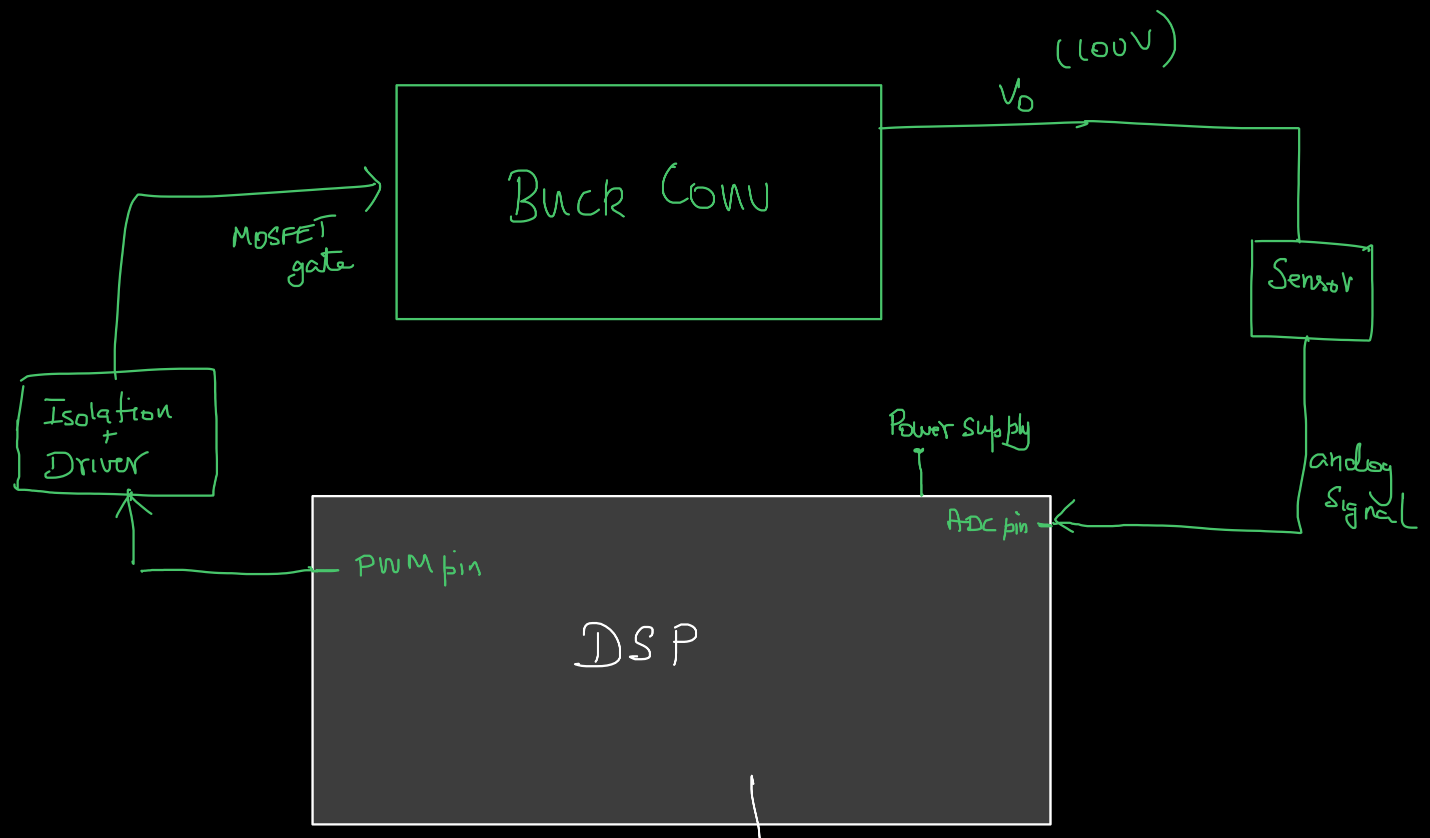


@ What time we need to sample?

If we want the average value of inductor current, it will occur @ the middle of duty $\left(\frac{dT_s}{2}\right)$.

So if we use up down counter we can sample @ TBPRD to get midpoint (in ①)

(in ② @ 0 to get midpoint)



→ inside DSP

(i) PWM module
- → T_{sw} → TBPRD
- → UP / Down / Up-Down
- → Action qualifier

(ii) ADC Module
- → Signal to be sampled
- → T_{samp}
- → Configure instant of sampling.

① V_{ref} value

② Compensated difference equation

③ Sampling rate

④ (i) PWM module
(ii) ADC module.

Code Structure

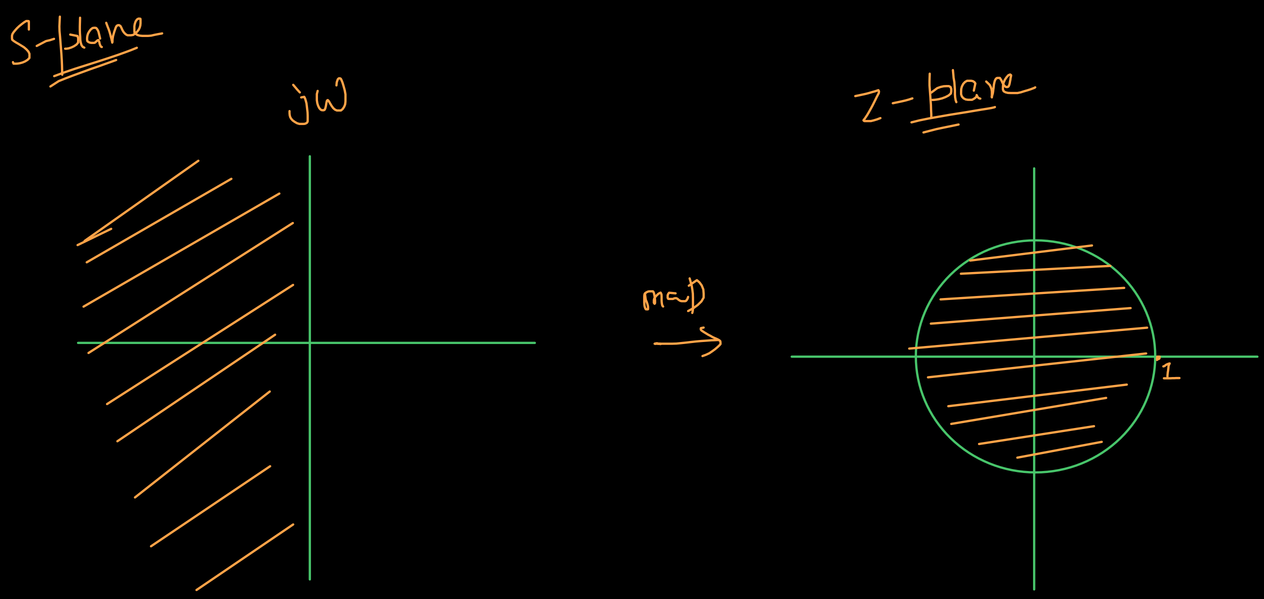
→ Initialize System Control

→ Configure PWM, ADC module

→ Implement Compensator

↳ Inside while{1}

→ Computed 'd' is given to pwm module's CMP register.

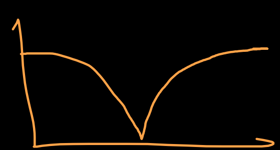


* The infinite jw is mapped to unit circle of length 2π $(2\pi r = 2\pi(1) = 2\pi)$

* So mapping is not linear

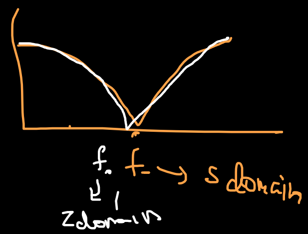
* Thats the reason for deviation in the bode plot before and after transformation.

Notch filter → rejects a single frequency.



↳ Used to attenuate specific frequency.

* When mapping due to deviation, the filter frequency may deviate. So the desired frequency wont be filtered out.



* This is called frequency warping.

* To avoid this we can use frequency prewarping

↳ It may not be required for PI, or LPF (basically simple filters).

Frequency Prewarping

↳ while doing transformations, we will make sure @ certain frequencies the digital & analog match exactly.

These frequencies are called "critical frequency"

$$S = \frac{2}{T}\,\frac{Z-1}{Z+1} \rightarrow \text{Tustin} \quad (1)$$

W.K.T

$$S = j\omega_a \qquad \omega_a \rightarrow \text{analog freq}$$

$$Z = e^{j\omega_d T} \qquad \omega_d \rightarrow \text{digital freq}$$

Sub in ①

$$S = \frac{2}{T}\left(\frac{1 - z^{-1}}{1 + z^{-1}}\right)$$

$$j\omega_a = \frac{2}{T}\left(\frac{1 - e^{-j\omega_d T}}{1 + e^{-j\omega_d T}}\right)$$

$$= \frac{2}{T}\,\frac{e^{\frac{-j\omega_d T}{2}}\left(e^{j\omega_d T/2} - e^{-j\omega_d T/2}\right)}{e^{-j\omega_d T/2}\left(e^{j\omega_d T/2} + e^{-j\omega_d T/2}\right)}$$

$$= \frac{2}{T}\,\frac{e^{j\omega_d T/2} - e^{-j\omega_d T/2}}{e^{j\omega_d T/2} + e^{-j\omega_d T/2}}$$

$$\cos\theta = \frac{e^{j\theta} + e^{-j\theta}}{2}$$

$$\sin\theta = \frac{e^{j\theta} - e^{-j\theta}}{2j}$$

$$j\omega_a = \frac{2}{T}\,\frac{2j\sin\frac{\omega_d T}{2}}{2\cos\frac{\omega_d T}{2}}$$

$T \to$ Sampling Frequency

$$\boxed{\omega_a = \frac{2}{T}\tan\left(\frac{\omega_d T}{2}\right)}$$

↳ plot W_a Vs W_d

$W_{ao} \to$ critical frequency of interest.

(which we need to preserve in Z domain)

$$W_{ao} = K\,\frac{2}{T}\tan\left(\frac{W_{do}\,T}{2}\right)$$

Scaling factor ← $K = \dfrac{\omega_{c0} \frac{T}{2}}{\tan\left(\frac{\omega_{d0} T}{2}\right)}$

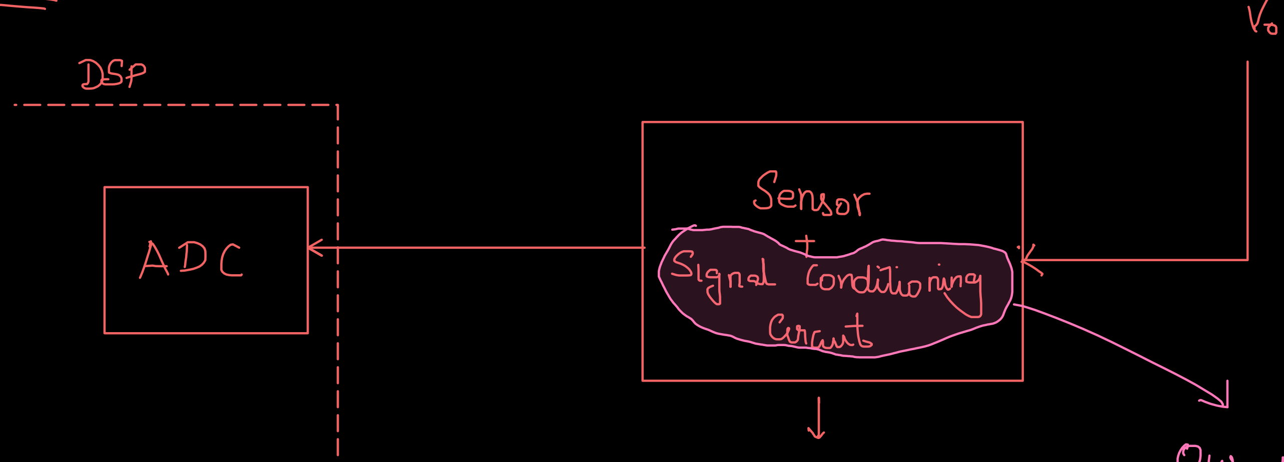
Such that atleast @ Critical frequency, it is Same in both domains

$$S = K \frac{2}{T}\left(\frac{z-1}{z+1}\right)$$

$$\boxed{S = \frac{\omega_{c0}}{\tan\left(\frac{\omega_{d0} T}{2}\right)}\left(\frac{z-1}{z+1}\right)}$$

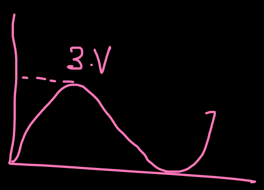
Frequency warped bilinear transformation

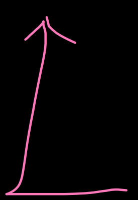
ADC



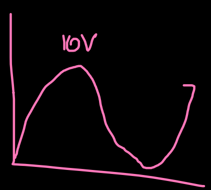
gain + delay

Our ADC can only take 0 - 3V.
If we want to Sensor Sine wave (like for inductor current)



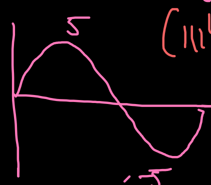


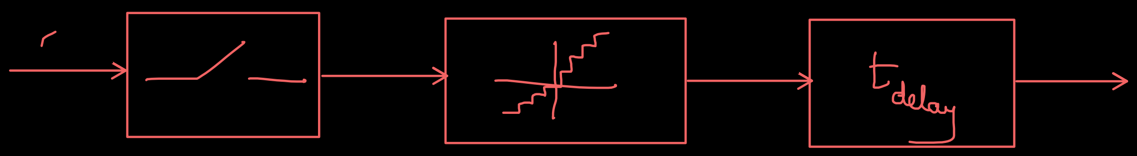
now we Scale



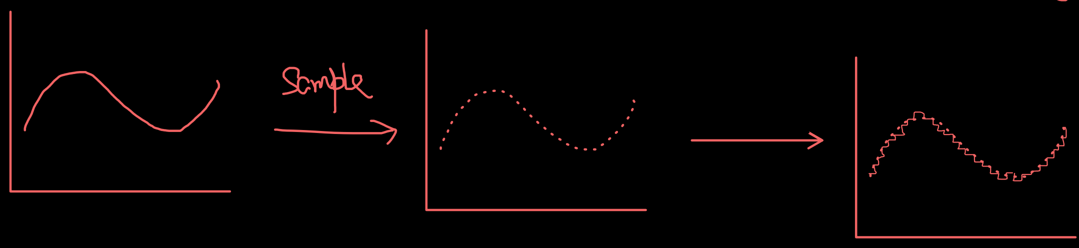
So we give offset

it cant -5 V





Sampler   Quantizer   Conversion delay (also additional delay due to using multiple channels to sample multiple signals)



$$\underbrace{\text{ADC Resolution}} = q = \frac{V_{FS}}{2^n}$$

Smallest change the ADC can sense & convert ??

$n \rightarrow$ no of bits of ADC

$\downarrow$

$V_{FS} = 3V$

10 bit ADC

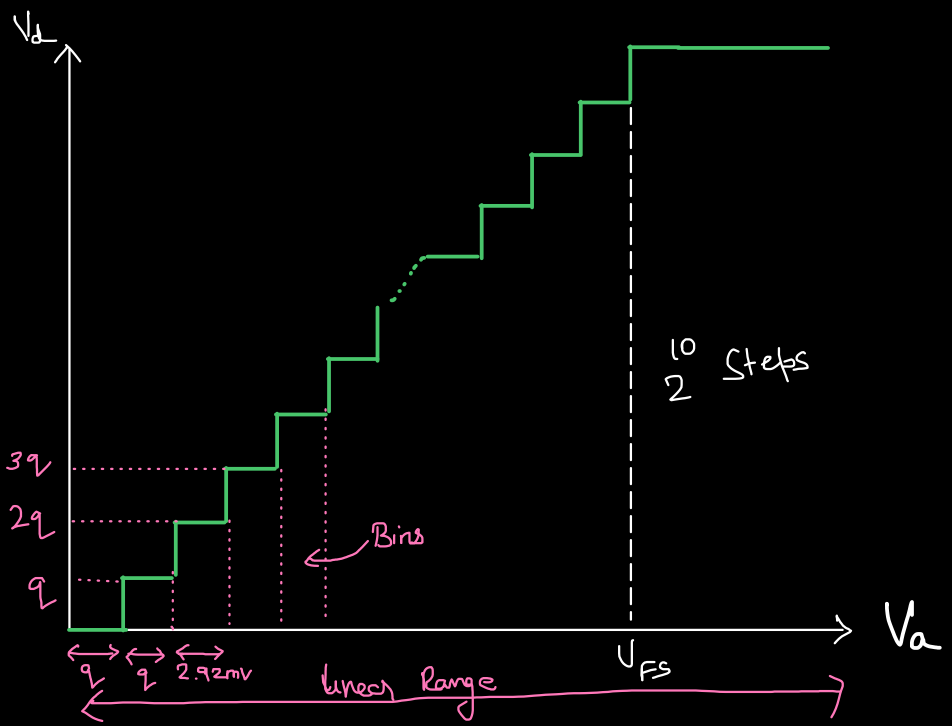
$$q = \frac{3}{2^{10}}$$

$$q = \underbrace{2.92\,mV}$$

Smallest change the ADC can sense

Quantization
- $\rightarrow$ Amplitude Quantization $\rightarrow$ leads to non linear effects
- $\rightarrow$ Time Quantization $\rightarrow$ leads to delay

The sampled value may be anything but during quantization it is rounded off to the nearest multiple of q.



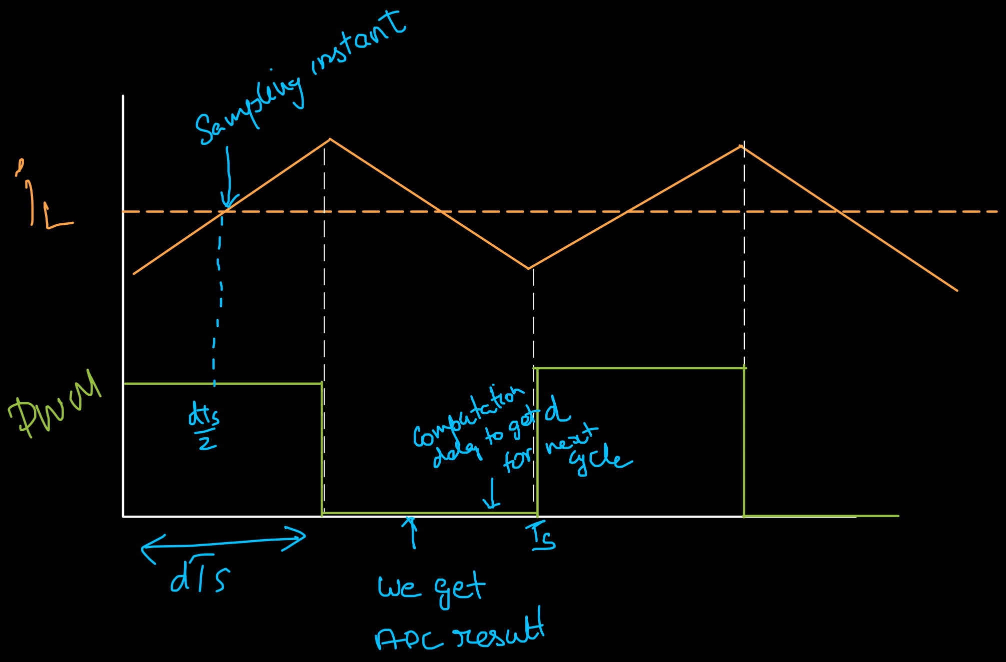
Sampling

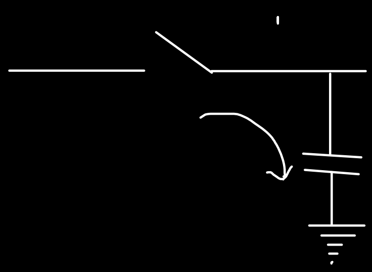
In digital control, always try to avoid Sampling @ the Switching instance.

$2.92 \times 5 = 14.6$

If the Sampled Value is 14.4

It is rounded to 14.5





The Switch should be closed for Sufficient time to the Capacitor to charge upto the Sample Value

↳ This can be set with Aquisition register in ADC module

DPWM Module

* n_bit DPWM
  - → up Counter
  - → down Counter
  - → up-down Counter

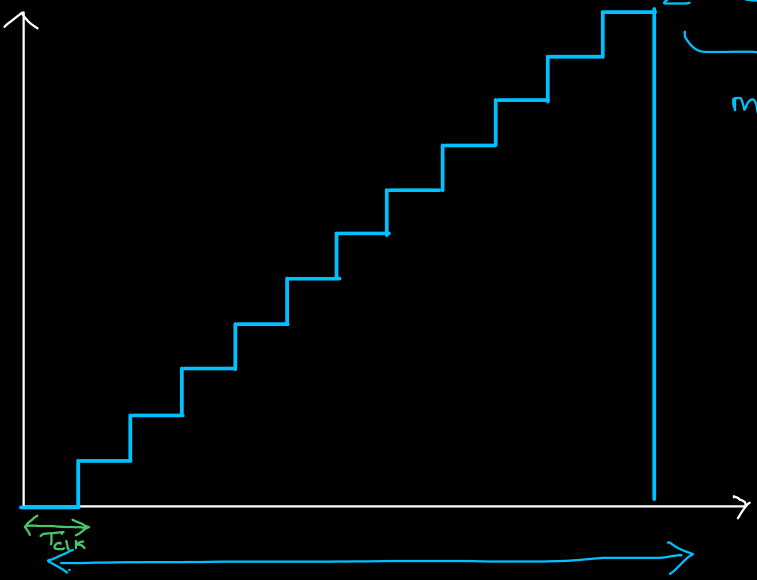
} Carrier waves

16-bit

in TMS

$2^n = 2^{16} = 65536$

$\underbrace{\hspace{6em}}_{\text{maximum possible count}}$



$T_{PWM} = T_s$

TBPRD register $\rightarrow$ no of steps in carrier

$T_{clk} \rightarrow$ not same as system clk

↳ in Type 4 epwm (current generation)

↳ the freq is divided by 2

ie $T_{clk} = 100$ MHz

$$\text{duty Resolution} = \frac{T_{clk}}{T_{PWM}} \rightarrow \text{minimum Time frame.}$$

$$= \frac{T_{clk}}{N \times T_{clk}}$$

$N \rightarrow$ no of count/step

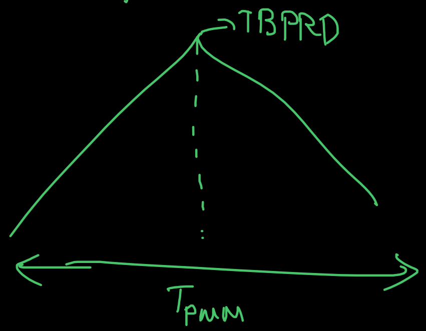
$$= \frac{1}{N}$$

$$= \frac{1}{2^n}$$

Say, $f_{PWM} = 1\,kHz$; $T_{PWM} = \frac{1}{f_{PWM}}$

$$T_{PWM} = \frac{T_{clk} \times TBPRD}{\underbrace{(\text{Clk DIV} \times \text{HS PCLK})}_{\text{prescalers.}}} \rightarrow \text{check.}$$

↳ in up-down counter



$$\frac{T_{PWM}}{2} = T_{clk} \times TBPRD$$

Delays → Significant effect on higher switching frequency. Converters (50 kHz & above)

↳ Cause reduction in gain margin.

in digital control,

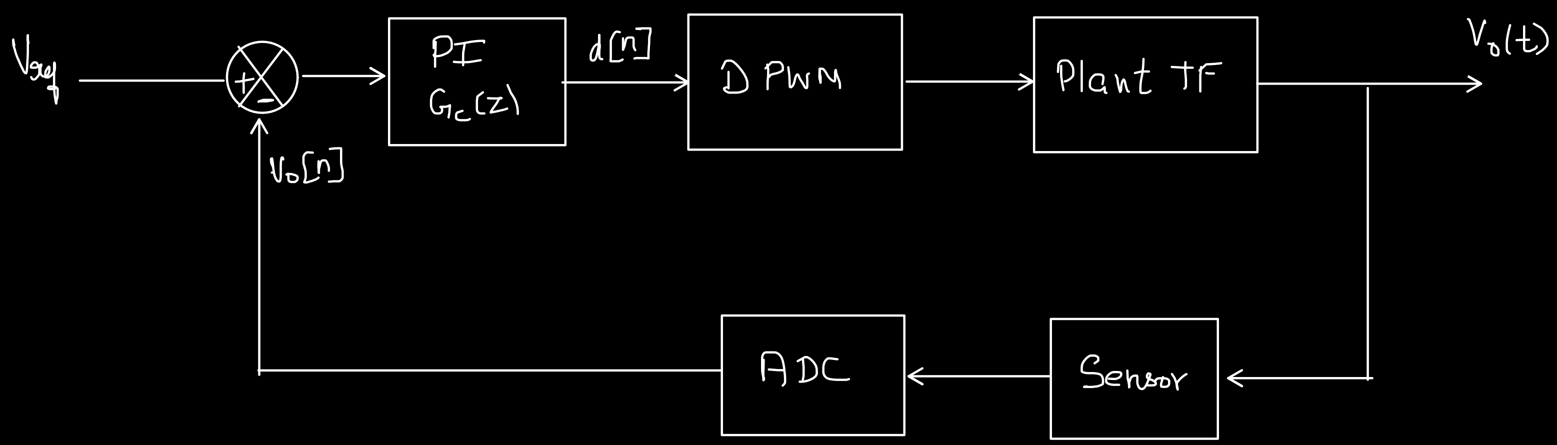
1. Sense the System Variables
2. Signal Conditioning of Sensed Variables
3. ADC
   - (i) Sampling
   - (ii) Conversion (quantization)
   - (iii) Store in register

DSP ←

4. Compensator evaluation (difference eqn computation)

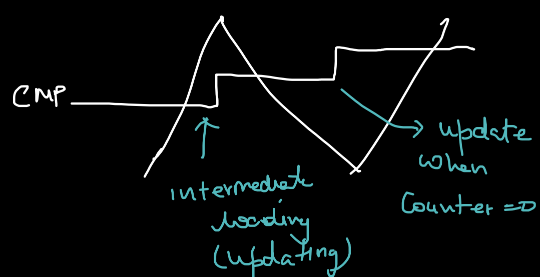
5. Compare d[n] with carrier in DPWM.

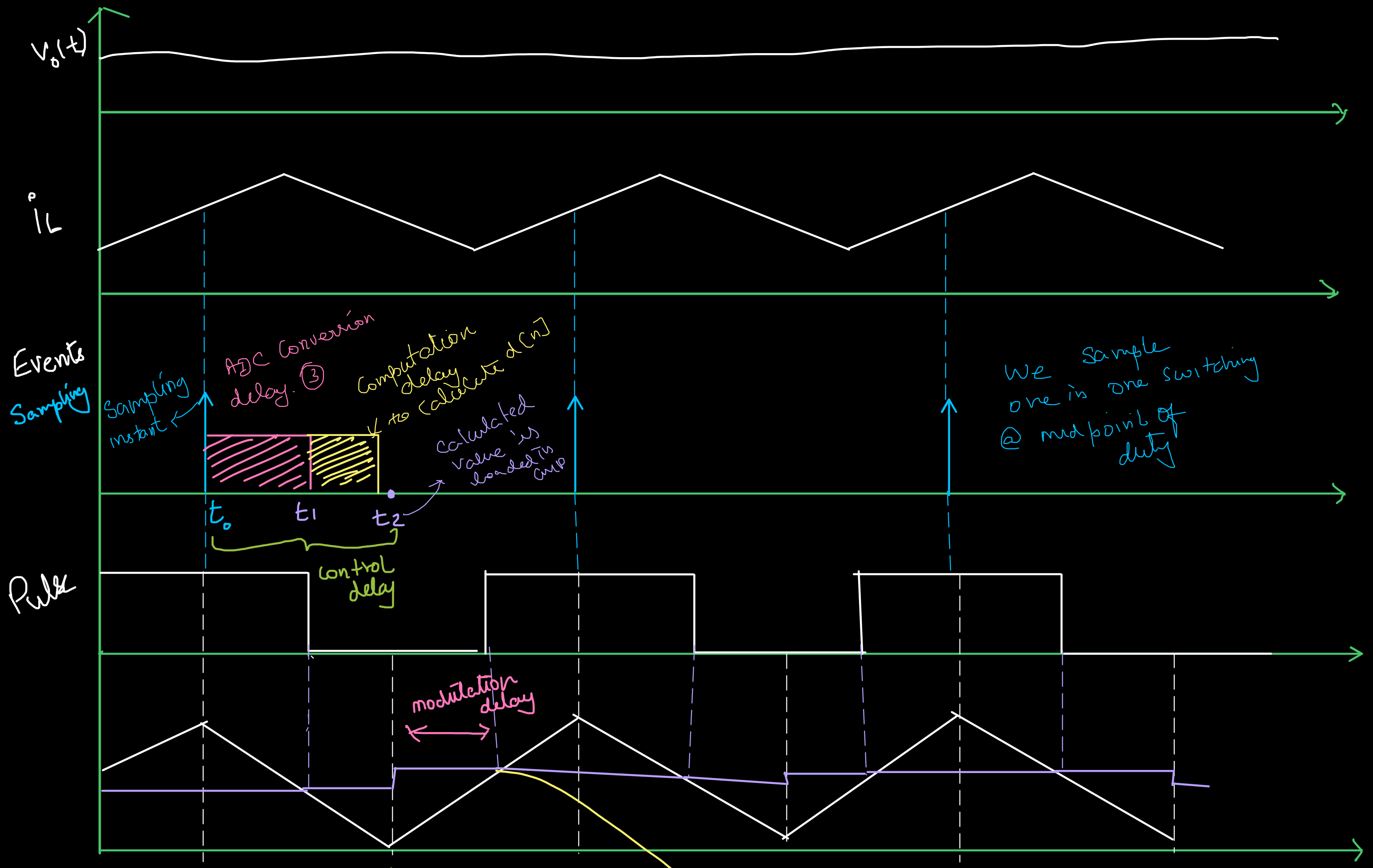
6. Pulse to Gate driver



Assumption

1. DC-DC Converter in CCM
2. Voltage Mode Control
3. Consider all possible non idealities in DSP implementation
4. $T_{samp} = T_s$
5. Up-down counter for DPWM
6. Load the CMP register only when counter becomes 0
   ie no intermediate loading
   The value is loaded only after the switching cycle.
7.





error is detected here

Corrective action takes place here.

duty is applied to the converter

Total delay = Control delay + Modulation delay

$$\text{Uncompensated TF} = G_{vd}(s)\,\underbrace{G_M(s)}\,\underbrace{H(s)}_{\text{Sensor}}$$

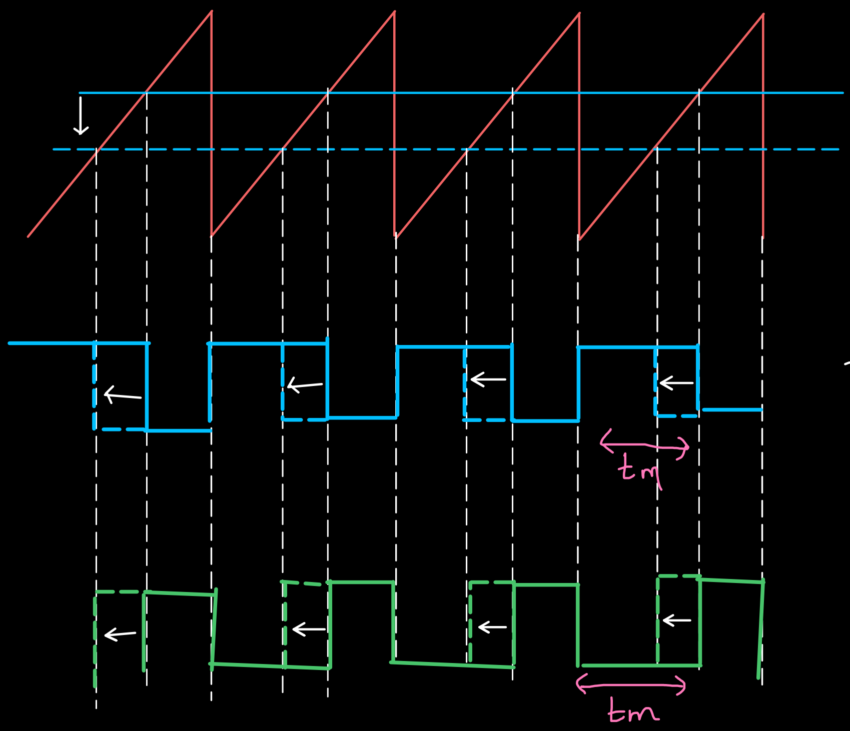
$$G_m = \frac{1}{V_m} e^{-st_m}$$

$$\hookrightarrow \underbrace{H_g}_{\text{Sensor gain}}\ \underbrace{e^{-t_s e}}_{\text{Sensor delay.}}$$

we need to add Control delay

$$e^{-st_c}$$

Modulation Delay (DPWM)



Trailing edge modulation

$t_m = DT_s$

Leading edge modulation

$t_m = (1-D)T_s$

Model:

Trailing edge : $e^{-j\omega D T_s}$

Leading edge: $e^{-j\omega (1-D) T_s}$

$\therefore$ The DPWP model

Trailing edge : $\dfrac{e^{-j\omega D T_s}}{\text{Peak of carrier}}$

Leading edge: $\dfrac{e^{-j\omega (1-D) T_s}}{\text{Peak of carrier}}$

Updown Counter: $\simeq \dfrac{e^{-j\omega T_s/2}}{\text{Peak}}$ (approx)

gives less problems.

No duty dependence.

$\therefore$ The uncompensated loop gain

$$= G_{vd}(s)\, H(s)\, \frac{1}{V_m}\, e^{-st_s}\, e^{-st_m}\, e^{-st_c}$$

Taylor Series: $e^{-x} = 1 - x + \frac{x^2}{2} - \frac{x^3}{3!} + \cdots$

Pade's approx: $e^{-x} = \frac{2-x}{2+x}$

↳ used in control applications

Sometimes, rarely, the uncompensated loop gain itself we may get the required characteristics. In that case we just close the loop and put a unity gain ($K_p = 1$) compensator.

Say,

$V_{in} = 100\,V$

$V_o = 10 - 500\,V$

(for which V_o will we design the compensator)

→ We need to design for the worst case condition

↳ design for both,

$10V \rightarrow GC_1$ $\quad$ $500V \rightarrow GC_2$

then,

$$\left.\begin{matrix} G_{c1} & G_{vd1} \\ G_{c2} & G_{vd2} \end{matrix}\right\}$$ See if both are Stable

(or)

$$\left.\begin{matrix} G_{c2} & G_{vd1} \\ G_{c2} & G_{vd2} \end{matrix}\right\}$$ See if both are Stable.

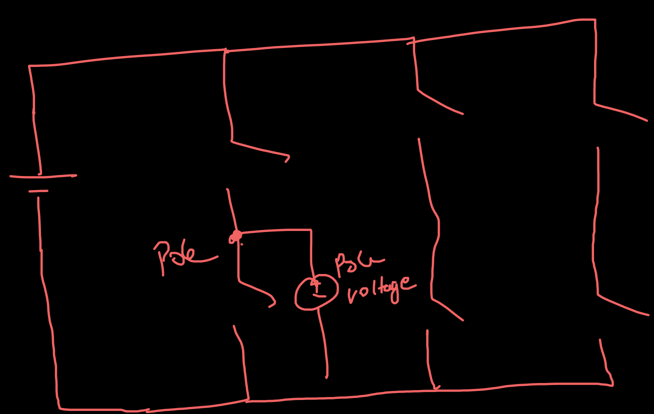
→ Which ever one gives Stable for both we will choose that

Also if we know that most of the time it works @ a nominal voltage. we can design for that. & See if it is Stable in extremities.

SVM

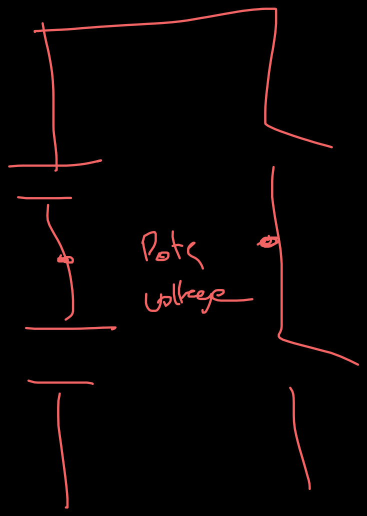
↳ 3 phases → resultant vector

→ If we attempt to track this resultant vector we automatically 3 phase waveforms (which caused the resultant) will be achieved.



w.r.t pole
↳ 2 level inv
V 2 0

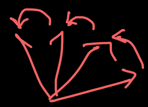
output
↳ 3 levels inv



→ Still 2 level inverter.

→

→ Determine step size of V_{ref}



→ Find which sector

→ Find dwell time

→ load in CMPA

→