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EE6308D Switched Mode and Resonant Converters

End Semester Exam.

1a). Cycle Average: It is for discrete functions

$$x_{cav}[n] = \frac{1}{T_s}\int_{(n-1)T_s}^{nT_s} x(t)\,dt.$$

Running average: $x_{rav}(t) = \frac{1}{t}\int_{0}^{t} x(t)\,dt$

→ for continous functions

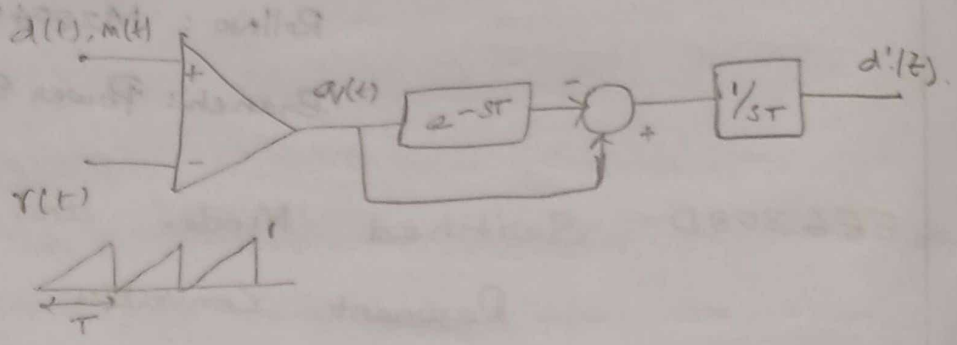
Local average:

→ also called Moving average

$$x_{ma}(t) = \frac{1}{T_s}\int_{t-T_s}^{t} x(t)\,dt$$

→ It is used for finding duty ration function

b). A non-linear problem has no satisfactory easy solution. We try the easiest strategy we use the required $d(t)$ and $m(t)$ interms of $q(t)$ by using local average




We can make d'(t) as nearly equal to d(t) as we wanted.

↳ d'(t) is a continuous function of time it is always a piecewise linear function

↳ d'(t) track the smooth d(t) very closely when f is small compared to 1/T

↳ Increase in f make tracking worst

↳ d(t) is always sinusoidal where d(t) is nearly a sinusoidal due to increase in f

↳ As f ↑, amplitude of fundamental component of d'(t) becomes different to that of d(t). & the phase lag between d'(t) & d(t) increase

So PWM Modulation strategy is acceptable provided the duty ratio function demanded by the controller doesn't have a frequency components above 1/10T.
d(t) vary slowly compared to switching frequency cycle

3). a) If we are using continuous time state-space average model for designing of control system. The BW of the control loop must be within the validity range of frequency for the modulating technique. All state variables input variables and d(t) must be slow varying if state space averaging to be used. If this condition is not met in design, then we can't be sure that designed control system, will intended to do. we may get unstable system or erratic switching. frequency range over which state space average modelling is accurate enough upto 1/10 of $f_s$.

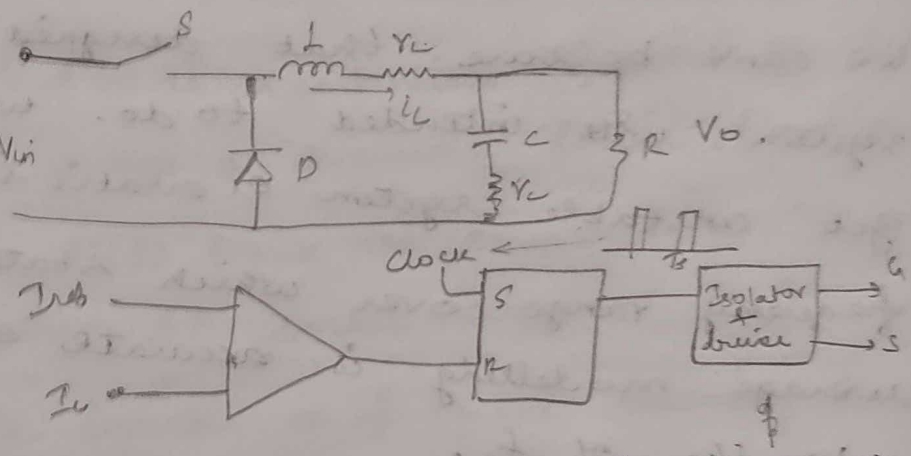
b) The designed controller is applied for correcting the output. Duty ratio is a local average of switching fn q(t). The m(t) generates q(t). The effective duty ratio function that we achieve will have lower amplitude, delay in phase, harmonics in sinusoidal context. These undesirable effects is tolerable upto $\pm f_s/10$. The phase delay contributed by modulator, additional harmonics injected into output possible subharmonics switching patterns

Can't be ignored so closed loop bandwidth possible is $f_s/10$

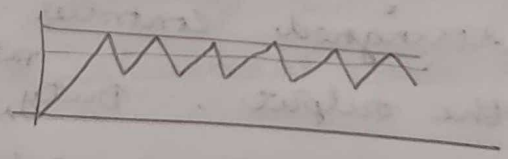
$f_s$ closed loop B.W will be after $f_{co}$

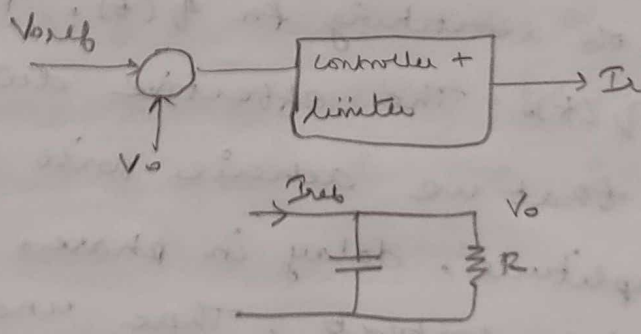
$f_s$ closed loop B.W is guaranteed to above $f_{co}$. Compensator design is done by specifying loop gain crossover frequency and required phase margin

4 a).




It will make current limit as in peak.

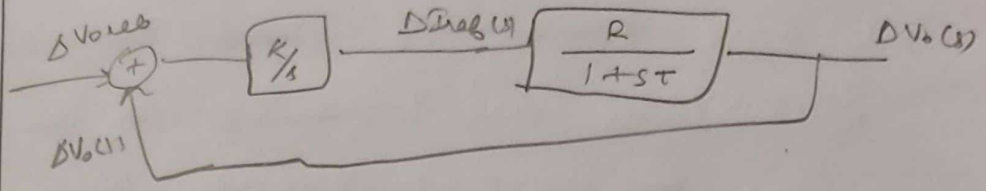





Exponential rise of $V_o$ with time constant $\tau = RC$.

$$\frac{\Delta V_o}{\Delta I_{ref}} = \frac{R}{1+s\tau}.$$

We make Type I compensator.




$$\frac{\Delta V_o(s)}{\Delta V_{ref}} = \frac{K_R/T}{s^2 + \frac{1}{T}s + \frac{K_R}{T}}$$

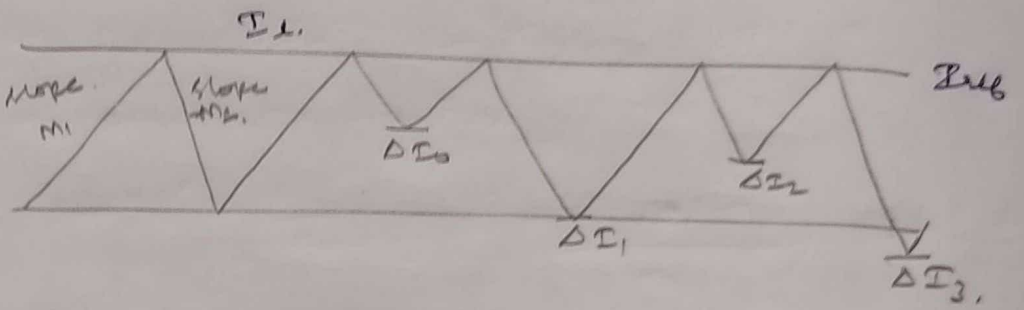
## Advantages

- Inherent over-current protection of all components during startup, large transients overload etc.
- Well controlled cold startup and large transients — no special circuitry for soft starting is needed
- In Buck & Buck derived topologies, CMC converts the filter inductor into a constant current drive and hence reduces the order of converter to 1. With a PI controller in the outer voltage control loop it is possible to design a closed loop system with first order dynamics that is fast while remaining non-oscillatory
- CMC is very easy and natural cure for flux walking problem. The duty ratio of switches will be suitably adjusted to become unequal by CMC if converter flux has a tendency to

walk.

- Easy paralleling and modular design if modules are connected in the CMC ensures the current sharing. No speed control is needed to ensure current sharing.
- Inherently excellent line regulation

4. b) Subharmonic instability in CMC.




In order to calculate $\Delta I_1$, $\Delta I_2$ ... We used a generalised formula

$$\Delta I_n = (-1)^n \left(\frac{m_2}{m_1}\right)^n \Delta I_0.$$

Here slope is varying so the gate pulse varys according to the slope of $I_L$. This will happens when sudden change appears.

$\Delta I_n \to 0$ as $n \to \infty$ iff $\frac{m_2}{m_1} < 1$, subharmonic instability will result if $\frac{m_2}{m_1} \geq 1$

for ideal Buck converter

$$m_1 = \frac{V_{in} - V_o}{L}, \quad m_2 = V_o/L$$

$$\frac{m_2}{m_1} = \frac{d}{1-d}. \quad \frac{m_2}{m_1} < 1, \Rightarrow 2d < 1$$

$$\Rightarrow d < 0.5$$

subharmonic instability will happen for $d \geq 0.5$ in Buck converter similarly for Boost converter subharmonic instability is happend for $d \geq 0.5$

This can be resolved by slope compensation. for this $m_c > \frac{m_2 - m_1}{2}$.

$m_c \rightarrow$ slope of clock

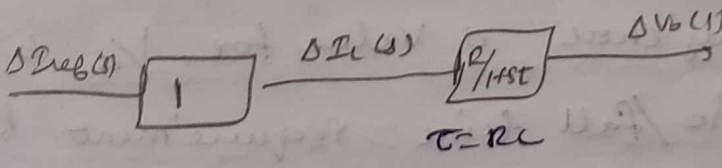
for buck, $m_c \geq \frac{V_o}{2L}$

for boost, $m_c > \frac{V_o}{2L}$.

4.c) With a properly choosen compensation slope $m_c = \frac{m_2}{2} = V_o/2L$

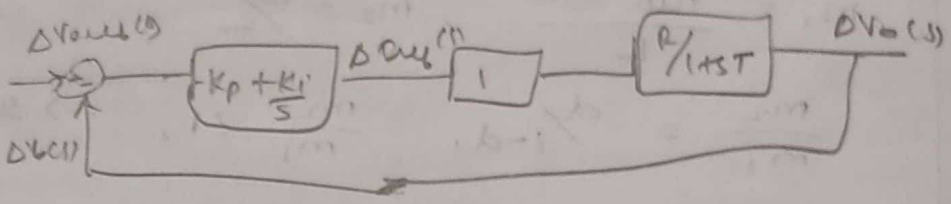
$$I_L = I_{ref} - \frac{m_2}{2} T_s = I_{ref} - V_o/2f_s L$$

so $\Delta I_L$ is simply $\Delta I_{ref}$




Assuming PI controller, the outer loop

control block diagram :




$$\frac{\Delta V_o(s)}{\Delta V_{ref}(s)} = \frac{K_p R/T \left(s + K_i/K_p\right)}{s^2 + \left(\frac{1 + K_p R}{T}\right) s + K_i R/T}$$

One possible design strategy is to make this T/F a first order one by cancelling $s + K_i/K_p$ by a denominator factor.

$$(s+a)\left(s + \frac{K_i}{K_p}\right) = s^2 + \left(\frac{K_p R + 1}{T}\right) s + \frac{K_i R}{T}$$

$$\therefore K_p = \frac{aT}{R} = ac$$

$$K_i = a/R$$

with this PI controller

$$\frac{\Delta V_o(s)}{\Delta V_{oref}(s)} = \frac{a}{s+a}$$ (DC gain = 1 as it should be)

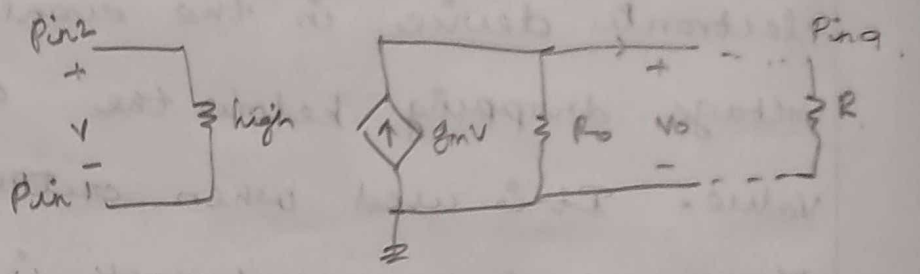
Closed loop step response is of the form $1 - e^{-at}$. $\frac{1}{a}$ time constant is $1/a$ we may chose a value for $1/a$ based on rise/fall time requirement for small disturbances.

6A). Under voltage lockout → is a electronic circuit, used to turn off the power of an electronic device in the event of the voltage dropping below the operational value. It is used when output impedance of an electrical network is higher than the input impedance of the regulator in order to prevent oscillations and possible malfunctions of the regulator.

Flip Flop → basic digital memory circuit which stores one bit of information FF are fundamental blocks of most sequential circuits. It is also known as bistable multivibrator or a binary or one bit memory. Used as a memory elements

Latch → electronic device which changes its output immediately based on the applied input. It is used to store either 1 or 0. It has two input set & Reset.

5b. Error Amplifier is of transconductance type:



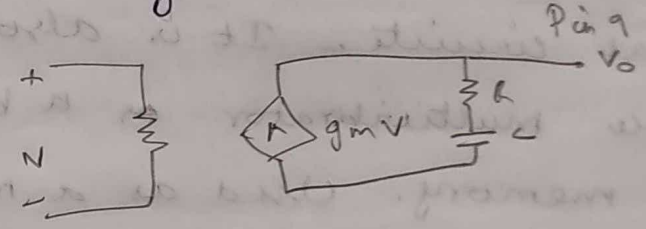

Dc voltage gain with $R_L \rightarrow \infty$ = 75dB
= 5625

Dc value of $g_m$ = $1.5 \times 10^{-3}$ ℧

$$\therefore R_o = \frac{5.625 \times 10^3}{1.5} \text{ K}$$

$$= 3.75 \text{ M}$$

Making a PI controller i.e., Type II




$$\frac{V_o(s)}{V(s)} = g_m R + \frac{g_m}{sC} = K_p + K_i/s$$

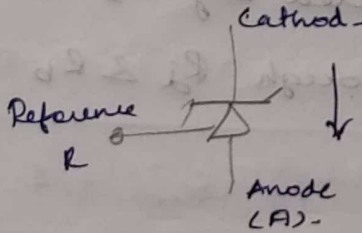
$K_p = g_m R$, $K_i = g_m/C$

Refer to demystifying Type II compensator using OP-Amps and OTA for DC/DC converters.

Texas Instrument Application Report SLVA 662 – July 2014 for designing Type II compensators.

3 b) Type III compensator with its double zero - double pole structure is capable of contributing higher phase boost than type II. It will be needed when the phase delay angle of plant at the choosen cross-over frequency is $> 125°$. This can can happen buck converter with low value of $r_c$ for ideal buck $r_c = 0$.. so the phase delay will be $> 125°$. so that the teacher stated is correct.

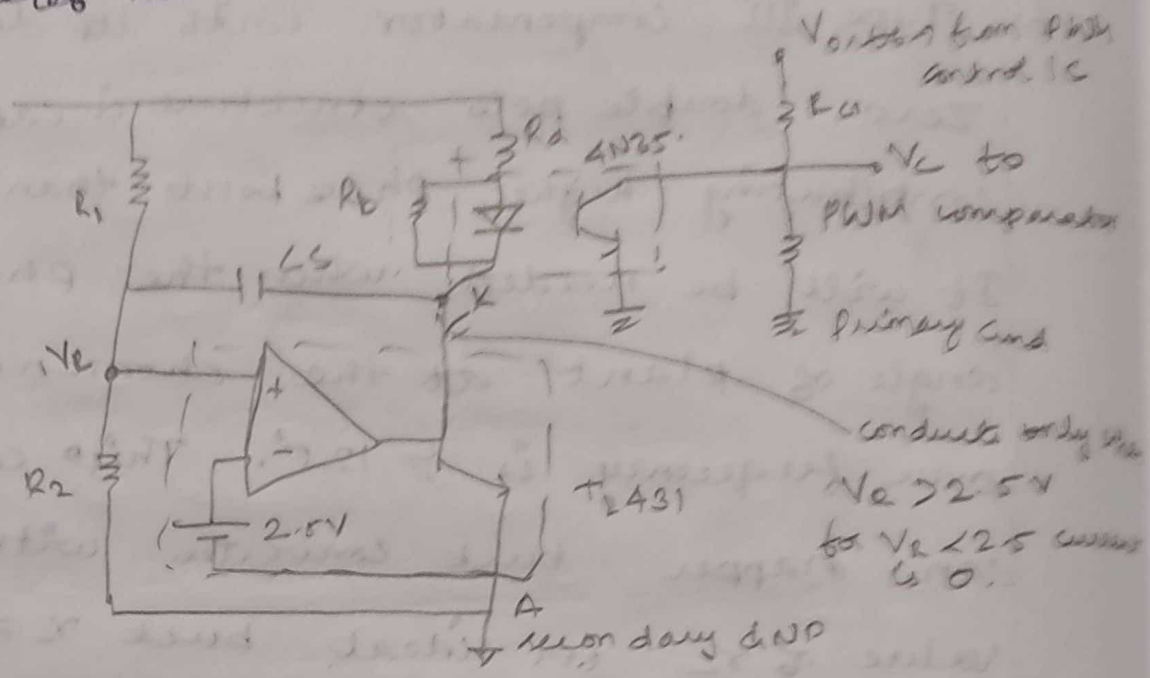
7. The problem of bringing $V_o$ value or $(V_{ref} - V_o)$ value from secondary side to primary side in transformer isolated converter without destroying galvanic isolation. The TL431 regulator diode + opto coupler system is a commonly employed solution.




This must be minimum of 1A for good accuracy of $V_{ref}$.

A high gain op-AMP donot allow $V_{KA}$ to become less than 2.5V, else diode will conduct and will draw current from R line & 2.5V

Rob value.




$C_s$ → capacitor for making $K/s$ in PI function

$V_R$ → exactly 2.5V when $V_o$ is the correct value say 12V.

$R_b$ → to ensure that $i_{KA} > 1mA$

4N35 opto coupler CTR = 2

forward voltage = 1.2V

$R_1$ & $R_2$ must be small compared to $R_d$ & $R_b$ so that potential division ratio is not affected by $C_s$ charging current coming through $R_d$ & $R_b$

6 a). $$\frac{\Delta V_o(s)}{\Delta d(s)} = \left(\frac{(1-d_o)V_o}{LC}\right) \cdot \frac{\left(1 - s\frac{LI_o}{(1-d_o)^2 V_o}\right)}{s^2 + \frac{r_{eqb}}{L}s + \frac{(1-d_o)^2}{LC}}$$

$$r_{eqb} = r_L + d_o r_s + (1-d_o)(r_d + r_c).$$

$$= 0.05 + (0.64)\,0.05 + (1-0.64)(0.06).$$

$$= 0.1036.$$

$V_o = 12\,V,\ 2\,A,\ \therefore V_{in} = 5\,V.$

$$\frac{\Delta V_o(s)}{\Delta d(s)} = \frac{144 \times 10^6 \left(1 - s\,38.58 \times 10^{-6}\right)}{s^2 + 3453.33s + 4.32 \times 10^6.}$$

b). $f_{co} = 5\,KHz.$

Phase delay of $G(j\omega_{co}) = 224.$

Maximum phase delay of $G(j\omega) = (250 - PM)$

Phase margin $PM = 250 - 224 = 26°$

(Practically

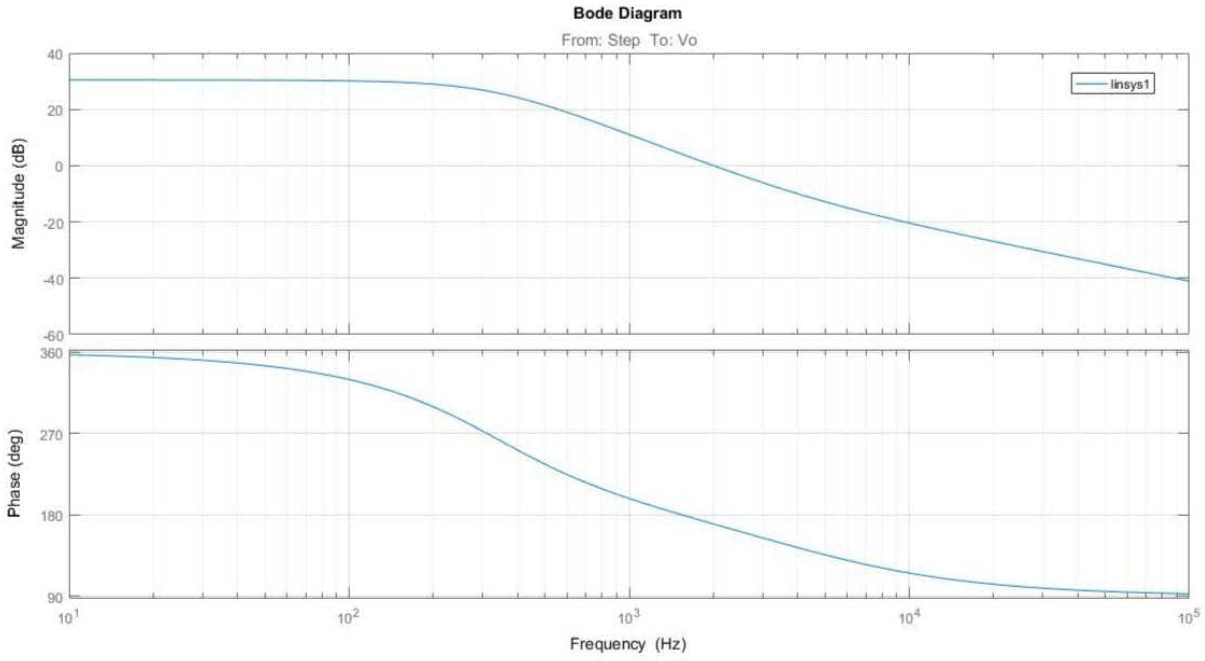
Theoritically $PM = 270 - 224$

$= 46°$

c) Maximum phase delay of $G(j\omega) \angle (250 - PM)$

$\angle (250 - 66°)$

$\angle (190°)$


Bode Diagram
From: Step To: Vo
linsys1
Magnitude (dB)
40
20
0
-20
-40
-60
Phase (deg)
360
270
180
90
$10^1$
$10^2$
$10^3$
$10^4$
$10^5$
Frequency (Hz)

$f_{co} = 1.98KHz.$

$$K = \tan\left(\frac{90 + 190^\circ + 60}{4}\right)$$

$$= 11.43$$

$$K'(j\omega_{co}) = K^2 = 130.646 \qquad 0.62dB.$$

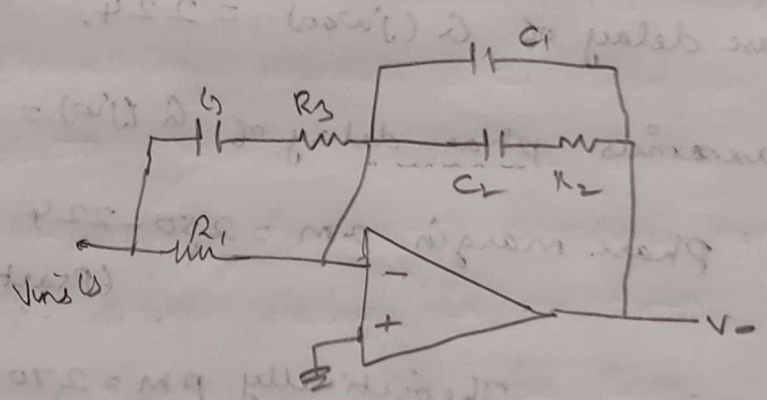
$$K = \frac{2\pi \times 1980}{130.646 \times 1.0188} = 93.464$$

$$\tau_2 = 918 \times 10^{-6} s$$

$$\tau_p = 7.0324 \times 10^{-6}.$$

$$K(s) = \frac{93.464}{s} \frac{(1+s\,918\times10^{-6})^2}{(1+7.0324\times10^{-6})^2}$$

d).




$$\frac{V_o(s)}{V_{in}} = \frac{1/R_1(C_1+C_2)}{s} \frac{(1+sR_2C_2)(1+s(R_1+R_3)C_3)}{(1+(sR_3C_3)(1+sR_2C_1\oplus C_3)}$$

$$K = \frac{1}{R_1(C_1+C_2)} \qquad \tau_2 = R_2C_2$$

$$= (R_1+R_3)C_3$$

$$\tau_p = R_2 C_1 \oplus C_2 = R_3 C_3$$

$C_2 = 0.1\mu F$

$$R_2 = \frac{918 \times 10^{-6}}{0.1 \times 10^{-6}} = 9.18\,k\Omega$$

$$C_1 \oplus C_2 = \frac{7.0324 \times 10^{-6}}{9.18\,k\Omega} = 7.6605 \times 10^{-10}$$

$$\frac{C_1 C_2}{C_1 + C_2} = 7.66505 \times 10^{-6}$$

$$0.1\mu C_1 = 7.665 \times 10^{-10} C_1 + 7.665 \times 10^{-16} \times 0.1$$

$C_1 = 0.77\,nF$

$$R_1 = \frac{1}{k(C_1 + C_2)} = 106.172\,k\Omega$$

$$t_2 = R_1 C_3 + R_3 C_3 = t_p + R_1 C_3$$

$$918 \times 10^{-6} = 7.032 \times 10^{-6} + 106.17 \times 10^{3} \times C_3$$

$C_3 = 8.561\,nF$

$$t_p = R_3 C_3 \Rightarrow R_3 = 821.419\,\Omega$$

2 a). In every compensator, we use use $K/s$

i.e., $K(s) = K/s \; K'(s)$.

Type - I $\rightarrow K/s$

Type - II $\Rightarrow K/s \; \dfrac{(1+sT_p)}{(1+sT_z)}$

Type - III $\Rightarrow K/s \; \dfrac{(1+sT_p)^2}{(1+sT_z)^2}$

This $K/s$ is necessary because integral control action is a must for every compensator

b) Starting with control to output transfer function means we can control the duty ratio function $d(t)$ in ~~CCM~~ VMC We need type -3 compensator means the phase delay is $> 125°$ and the $\gamma_c$ value will be less.