High Efficiency Hybrid Single-Phase Voltage-Source Inverter for PV Applications

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***Abstract*—Grid-connected low-power PV systems are becoming more and more popular inside the energy market. Such a systems, are commonly installed in residential and small commercial buildings, having as a main objective the reduction of the energy bill. Efficiency is a key word in the design of PV systems since this parameter contributes with economic benefits for the investors. Among low power systems, microinverters are designed to inject the generated energy from a single PV panel to the electrical grid. A single photovoltaic panel produces a voltage around 35 V, therefore microinverters are generally designed using two stages. First stage boost and regulate the output DC voltage while the second stage produces the injected AC current. Single-phase H-bridge inverter is the basic topology used in the second stage of the isolated microinverters. In this paper, a modified hybrid high-frequency H-bridge inverter is proposed using a combination between MOSFET's and IGBT's according with the low and high frequency pulse width modulated signals. The proposal is evaluated by means of numerical simulations and compared with transformerless topologies considering the total harmonic distortion and efficiency as the comparative parameters.**

I. Introduction

Nowadays PV systems are a competitive alternative in the electrical energy generation market in both stand-alone and grid-tied systems due to the technological developments and the cost reduction of PV technology [1]. In last years grid-tied systems have increased their popularity in an exponential way, because the generated electrical energy can be injected to the electrical grid without using an energy storage system. In general grid-tied systems are classified in three main groups named, string inverters, central inverters and microinverters. In particular, microinverters belong to low power systems used in single-phase installations which are constantly growing in utility scale and distributed power generation systems, due to some well recognized characteristics as: great versatility to install the system, better harnessing of the generated energy under partial shading, modularity, plug and play characteristic, no high voltage DC wiring, among others [2]. The power to be processed by a microinverter is in the range of 200 to 350 W, which corresponds in general with the electrical power generated for a single PV panel [3].

The literature reports many contributions related to power topologies and control systems for microinverters. Regarding topologies, there are two main groups to be considered: high frequency isolated (HFI) and transformerless (TL) inverters [3]. The HFI inverters are in general designed using two stages, the first stage is in charge of boost the PV panel voltage and the Maximum Power Point Tracking (MPPT) task and the second stage generates the AC signal to be injected to the electrical grid. In [4] a Flyback-type inverter is proposed for AC module based PV system where the power decoupling circuit is based on the discontinuous current mode control applied to the primary winding of the Flyback transformer, given in this way an optimum capacitance value for the decoupling operation. Another Flyback based inverter is presented in [5], in this paper a continuous conduction mode is explored in order to improve the efficiency, spite of the right half plane zero that can make difficult the controllability of the injected current. Another type of high frequency isolated inverters are those based on the isolated boost DC-DC converter, i.e., in [6] it is proposed a microinverter with multiple stages including an inverse buck, an isolated dual-boost, the high frequency isolation, a voltage doubler and a conventional H bridge circuit. The main idea is to avoid the used of the high-voltage electrolytic capacitors given in this way a long lifetime but however the efficiency reported is low, around 91%. A new concept called Optiverter for microinverters is introduced in [7], where an hybrid approach to the photovoltaic module is adopted. The main idea is to combine a wide-range buck-boost DC-DC converter with a highly efficient pass-through and variable DC-link voltage control, a conventional H-bridge inverter and a multimode control. The main advantage of the proposed concept are the good performance under partial shading and the low input voltage operation, however the efficiency can still be improved.

In the case of the transformerless inverters, in [8] a Boost-Buck converter is presented, the topology consist of a DC-DC boost interleaved converter, a DC-DC buck converter and a conventional H-bridge inverter. The first stage of this converter allows the operation in either boost or buck mode, then high efficiency is achieved as is expected since there is not galvanic isolation in the circuit. Additionally, in [9] authors proposed a converter using a three-phase extended-

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duty-ratio boost converter connected to a doubly grounded dynamic DC-link inverter. The second stage achieves zero capacitive-coupled common mode ground currents and high efficiency by using a GaN-based prototype.

As the H-bridge circuit is used in both isolated and transformerless microinverters, therefore in this paper an improve conventional H-Bridge circuit is presented. The circuit consists of two SiC MOSFETs, two IGBTs and two SiC high frequency diodes. The main idea is to increase the switching frequency using the SiC MOSFETs for high frequency signals while the IGBTs are intended to operate at the grid frequency. The SiC diodes are implemented to block the parasitic diode of the MOSFETs avoiding in this way their poor characteristics. Section II presents the analysis of the proposed topology while Section III includes the Pulse Width Modulation (PWM) strategy adopted for the proposed power circuit. Section IV presents the simulation results and a comparative study of efficiency and harmonic distortion regarding conventional circuits used in PV systems in order to validate the performance of the proposal. Finally, Section V considers the concluding remarks.

II. Analysis of the Proposed Topology

The proposed power circuit for the hybrid inverter is depicted in Fig. 1. As it can be observed there are two MOSFETs (S_3 and S_4), two IGBTs (S_1 and S_2) and four diodes (D_1 to D_4). The key idea is to use D_1 and D_2 to disable the operation of the body diode of S_3 while diodes D_3 and D_4 are used to block the parasitic diode of S_4. Thereby, the pour typical characteristics of this element can be avoided. The load current (considering a predominantly inductive load) trajectory during the positive semi-cycle and imposing a positive voltage difference between the terminals of the load is allowed through S_1, S_4 and D_3. On the other hand, when there is not voltage difference at the load, the freewheeling path is enable through S_1 and D_2. Besides, during the negative semi-cycle the load current trajectory when there is a negative voltage difference across the load is allowed through D_1, S_3 and S_2. Moreover, when the voltage difference across the load is zero, the load current trajectory is enable through S_2 and D_4. The above described operation modes are depicted in Fig. 2 and Fig. 3, being Fig. 2 the switching states during the positive semi-cycle and Fig. 3 the states used during the negative semi-cycle.

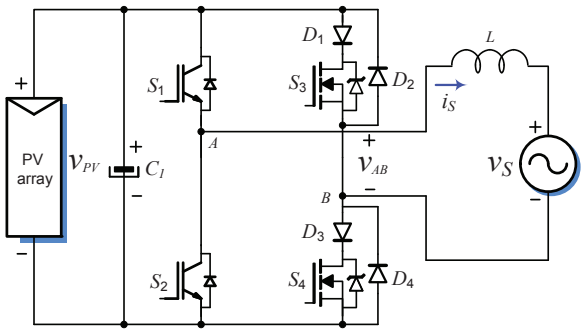

Fig. 1. H-bridge high-efficiency high-frequency single-phase proposed inverter.

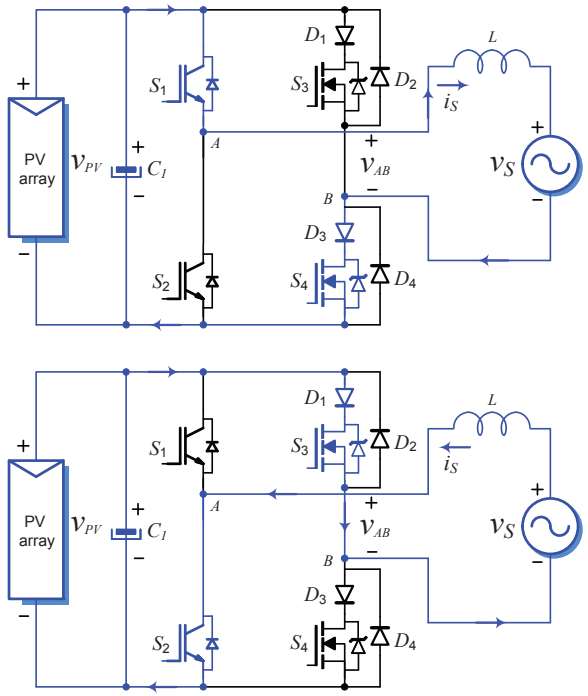

Fig. 2. Operation modes of the proposed single-phase hybrid inverter.

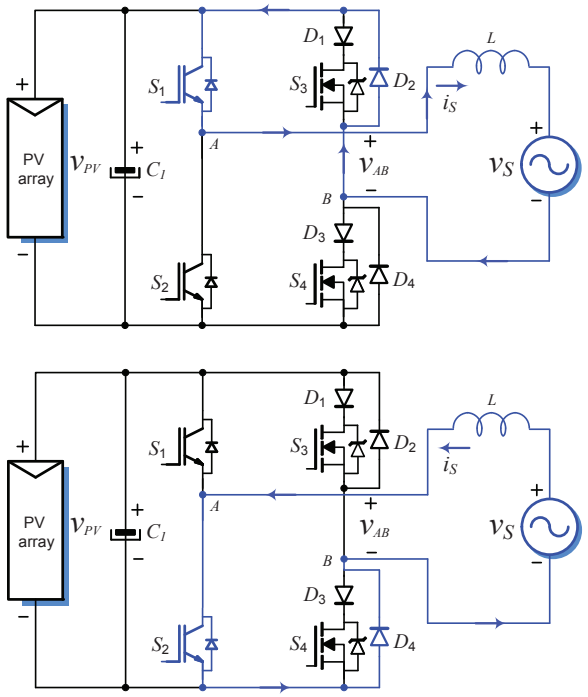

Fig. 3. Operation modes of the proposed single-phase hybrid inverter.

It should be note that during the active state in the positive semi-cycle D_1 is operating with a blocking voltage equal to zero while S_3 and D_2 are blocking V_{PV}. On the contrary, during the negative semi-cycle D_3 operates with a blocking voltage equal to zero while S_4 and D_4 are blocking V_{PV}.

Then, it should be expected that D_1 and D_3 do not increase significantly the switching losses.

III. Proposed PWM strategy

The proposed PWM is implemented using the conventional sinusoidal based PWM (SPWM) where a sinusoidal reference signal is compared with a triangular carrier signal with a relation in magnitude that corresponds with the modulation index parameter $m_a = V_{pkR}/V_{pkC}$, where V_{pkR} is the peak value of the reference voltage while V_{pkC} is the peak value of the carrier signal. The proposed SPWM is designed in order to be able to deliver three voltage levels at the output of the converter i.e. $V_{AB} = V_{PV}$, $V_{AB} = 0$ and $V_{AB} = -V_{PV}$. The obtained control signals by means of the comparison of the voltage reference and carrier signal are manipulated in order to make S_3 and S_4 to operate at high frequency, while S_1 and S_2 operate at the grid frequency. The resulted modulation signals are depicted in Fig. 4.

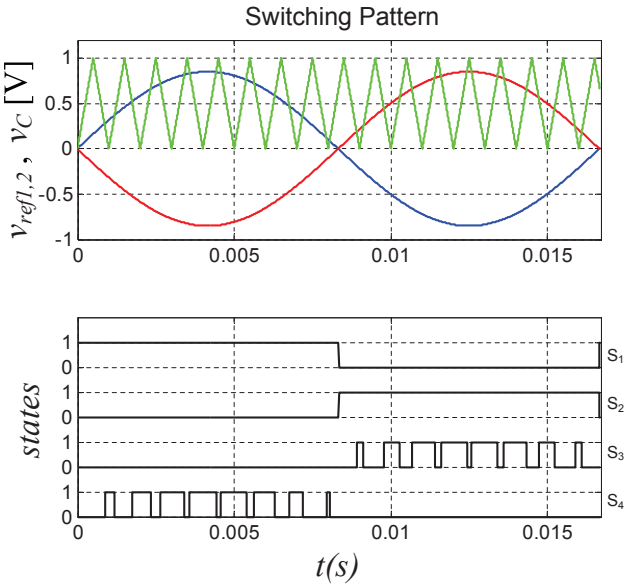

Fig. 4. Modulation signal of the proposed PWM strategy.

As it can be observed, during the positive semi-cycle the states depicted in Fig. 1 (a) are combined alternatively in order to generate the desire output voltages. On the other hand, during the negative semi-cycle the states depicted in Fig. 1 (b) are also combined alternatively to generate the $0V$ and $-V_{PV}$ voltages. It should be noted also that, switches S_1 and S_2, operates at the grid frequency while switches S_3 and S_4 operates at high frequency only during a half cycle being the rest of the time in the OFF state.

IV. Numerical implementation and comparative analysis

The proposed converter topology depicted in Fig. 1 has been implemented in a numerical simulation performed in the PSIM software. The parameters used are listed in Table I. The simulation results for V_{AB} and i_S are depicted in Fig. 5. As it can be observed the output voltage has the three voltage levels as it is expected while the output current has a sinusoidal waveform plus the switching ripple. It should be noted that the switching frequency is higher regarding conventional topologies, then the current ripple is lower and as a consequence the Total Harmonic Distortion (THD) is also lower as it will be demonstrated later.

TABLE I
Parameters for the numerical implementation.

Parameter	Value
V_{PV}	250 V
R	25 Ω
L	1.5 mH
f_{SW}	30 kHz
f_{grid}	60 Hz

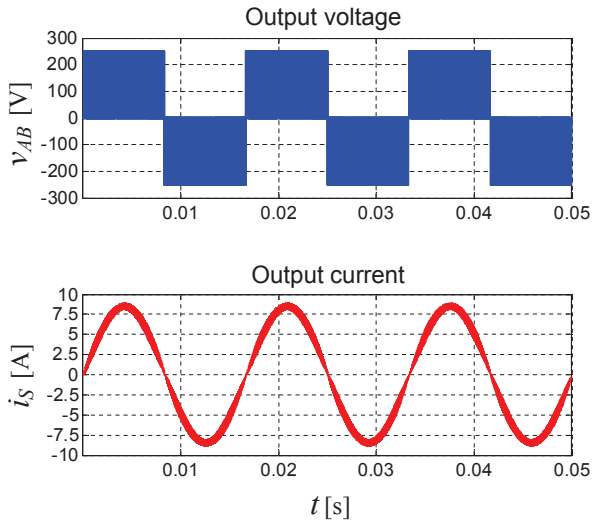

Fig. 5. Output voltage (V_{AB}) and Output current (i_S) of the proposed circuit

Regarding the current flowing during the free wheeling interval through the diodes implemented to block the body diodes of the switches S_3 and S_4, the simulation results are depicted in Fig. 6. As it can be noted, during the positive semi-cycle D_2 provides the free wheeling path for the load current. Besides, during the negative semi-cycle D_4 provides the free wheeling path for the output current. This demonstrate that the body diodes of the MOSFETs are disable and they do not influence the operation of the converter. Moreover, D_2 and D_4 have a blocking voltage equal to that voltage supplied by the input source, while across the terminals of D_2 and D_4 is all the time close to zero, because they are never inversely polarized. Finally, all the switches (MOSFETs and IGBTs) have a maximum blocking voltage equal to the voltage provided by the DC source.

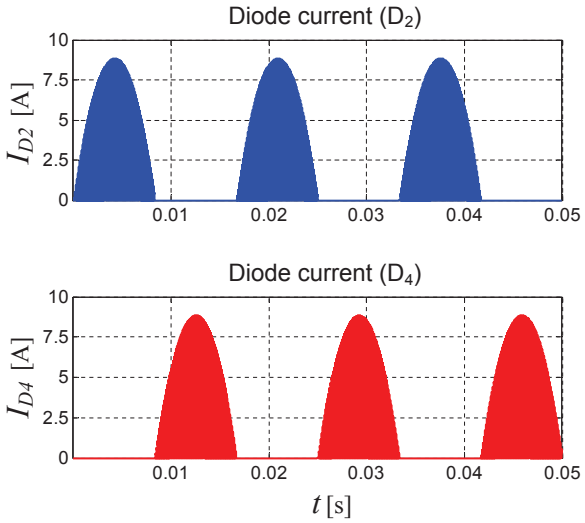

Fig. 6. Diode currents for D_2 and D_4

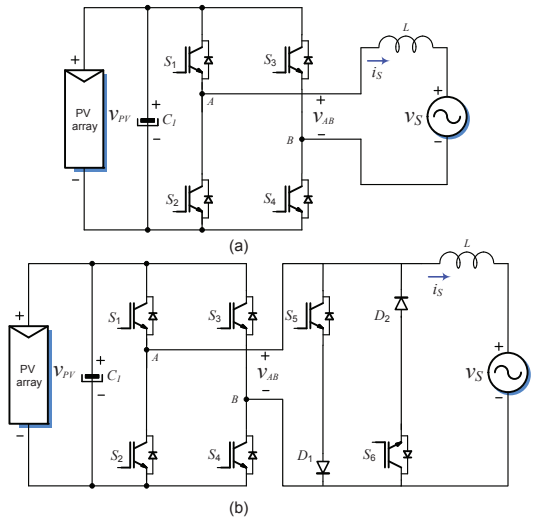

Fig. 7. H-bridge and HERIC inverters

In order to make a comparative analysis regarding efficiency and (THD), two conventional topologies are included. The first one is the conventional H-bridge inverter with unipolar SPWM. This topology is commonly used in the two types of microinverters according with the literature studied in the Section I [10], [11], [12]. The second topology considered is the Highly Efficient and Reliable Inverter Concept (HERIC) which is used in transformerless applications [13], [14], [15]. Both circuits are depicted in Fig. 7. As it can be observed, HERIC inverter is build using six switching semiconductors being two of them a bidirectional switch implemented at the AC side of the inverter. The main difference between HERIC and the conventional topology is that HERIC inverter can produce the same three-level output voltage than the conventional topology with minimum leakage ground current. It should be highlighted that for the latter mentioned topologies the are not plots in the paper, this is due that their signals are very similar to those obtained for the proposed topology. Then, the numerical simulations were performed under the same conditions, except for the switching frequency which is defined as $10kHz$ for the H-bridge and HERIC inverters in order to consider the advantages of the proposed circuit regarding THD. The Fast Fourier Transform (FFT) and the THD of the three inverters output current are depicted in Fig. 8. Notice that the proposed inverter achieves a better performance regarding current THD than the conventional converters, having a value around 5.02% while H-bridge and HERIC inverters have 7.5% and 14.66% respectively. It should be note also that the current THD can be improved by using a third order filter, but it is still advantageous since the filtering requirements will be lower for the proposed inverter.

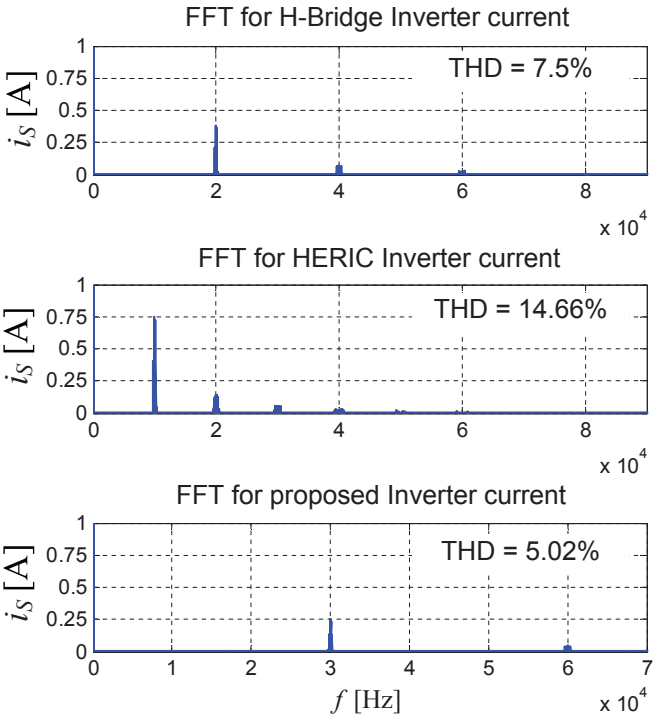

Fig. 8. FFT of the output currents for the three compared inverters

Regarding efficiency the three topologies were also simulated using the Thermal Module of PSIM software. In this case, the model of the selected semiconductors has been included in order to calculate the dynamic and static losses. The IGBT model used in the simulations was FGH20N60UFD from On Semiconductor company and the model used for the MOSFETs was C2M0080120D from the CREE company. Finally, in the case of the four extra-diodes, the model considered in this case was C3D16065D also from the CREE company. The simulation results are summarize in Fig. 9. As it can be observed the proposed inverter has a better efficiency than the conventional H-bridge inverter under the proposed switching frequency. Moreover, the HERIC inverter has a better efficiency than the hybrid proposed topology. Nevertheless, HERIC inverter requires the implementation of

two additional control signals, two extra switches and their corresponding driving circuits, increasing in this way the total cost of the system. As a conclusion of this analysis Table II summarized the results regarding THD and efficiency of the three analyzed inverters.

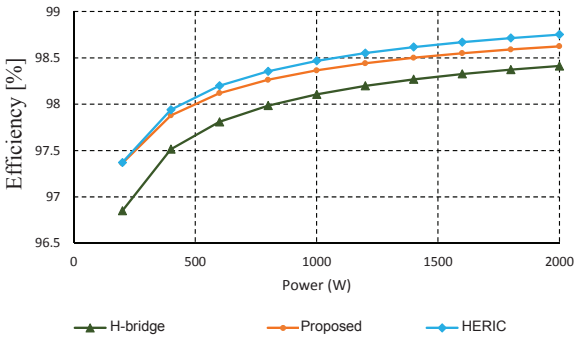

Fig. 9. Simulation results for the efficiency of the three evaluated inverters.

TABLE II
SUMMARY OF THE THD AND EFFICIENCY OF THE ANALYZED TOPOLOGIES.

Topology	THD (%)	Efficiency (%)
H-Bridge	7.5 %	97 %
HERIC	14.66 %	98.5 %
Hybrid Inverter	5.02 %	98.3 %

V. CONCLUSIONS

In this paper a single-phase hybrid inverter and its PWM control strategy have been presented. The proposed converter is based on the classical H-bridge inverter which is used in several applications where the efficiency is a key parameter. The circuit consist of two IGBTs, two MOSFETs and four diodes especially design for high-frequency high-efficiency applications. The main idea is to operate the MOSFETs with higher frequency than in the conventional converters. The numerical results have been demonstrated that the THD is lower in the proposed circuit. On the other hand, the efficiency is improved due to the implemented circuit around the MOSFET which has the objective to provide the path for the load current during the free wheeling stages. On the other hand, the PWM strategy has been designed in order to operate selectively at high frequency the specific switches i.e. MOSFETs and at low frequency the IGBTs. Then, from the analysis and simulations results it can be conclude that the proposed topology and the PWM strategy are able to improve the efficiency of the conventional H-bridge inverter.

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