







**AMC1301** SBAS667G - APRIL 2016 - REVISED APRIL 2023

# AMC1301 Precision, ±250-mV Input, Reinforced Isolated Amplifier

#### 1 Features

- ±250-mV input voltage range optimized for current measurements using shunt resistors
- Fixed gain: 8.2 V/V
- Low DC errors:
  - Offset error: ±0.2 mV (max)
  - Offset drift: ±3 μV/°C (max)
  - Gain error: ±0.3% (max)
  - Gain drift: ±50 ppm/°C (max)
  - Nonlinearity: 0.03% (max)
- 3.3-V operation on high-side and low-side
- System-level diagnostic features
- Safety-related certifications:
  - 7070-V<sub>PK</sub> reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5000-V<sub>RMS</sub> isolation for 1 minute per UL1577
- Fully specified over the extended industrial temperature range: -40°C to +125°C

## 2 Applications

- Shunt-resistor-based current sensing in:
  - Motor drives
  - Frequency inverters
  - Uninterruptible power supplies

### 3 Description

The AMC1301 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7070 V<sub>PEAK</sub> according to the DIN EN IEC 60747-17 (VDE 0884-17) and UL1577 standards, and supports a working voltage up to 1 kV<sub>RMS</sub>.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-side from voltage levels that can cause electrical damage and are potentially harmful to an operator.

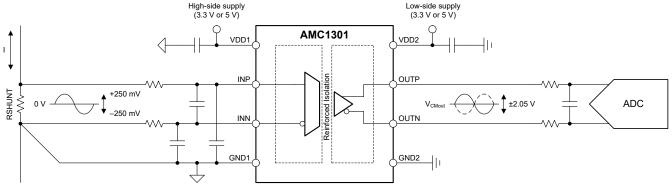
The input of the AMC1301 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The excellent DC accuracy and low temperature drift supports accurate current control in onboard chargers (OBC), DC/DC converters, frequency inverters, or other highvoltage applications. The integrated common-mode overvoltage and missing high-side supply voltage detection features of the AMC1301 simplify systemlevel design and diagnostics.

The AMC1301 is fully specified over the extended industrial temperature range of -40°C to +125°C and is available in a wide-body 8-pin SOIC (DWV) package. The AMC1301S is specified over the temperature range of -55°C to +125°C.

**Package Information** 

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
AMC1301	DWV (SOIC, 8)	5.85 mm × 7.50 mm

For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



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# **4 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

	hanges from March 14, 2023 to April 24, 2023 (from Revision F (April 2020) to Revision G April 2023))	ge
•	Changed document title	1
•	Changed Features section: Changed, deleted, and reorganized bullets	1
•	Changed isolation standard from DIN VDE V 0884-11 (VDE V 0884-10) to DIN EN IEC 60747-17 (VDE	
	0884-17) and updated the Insulation Specifications and Safety-Related Certifications tables accordingly	1
•	Deleted last bullet from Applications section	1
•	Changed Description section to include common-mode decoupling capacitors as a known best practice	1
•	Changed pin names VINP to INP, VINN to INN, VOUTP to OUTP, and VOUTN to OUTN throughout	
	document	
•	Changed Description column and added footnotes to Pin Functions table	
•	Changed CDM ESD standard from JESD22-C101 to JDEC JS-002	5
•	Changed PD from 81.4 mW to 99 mW	
•	Changed PD1 (VDD1 = 3.3 V) from 24.85 mW to 31 mW	
•	Changed PD1 (VDD1 = 5.5 V) from 45.65 mW to 54 mW	
•	Changed PD2 (VDD2 = 3.3 V) from 20.16 mW to 26 mW	
•	Changed PD2 (VDD2 = 5.5 V) from 35.75 mW to 45 mW	
•	Changed DTI from ≥0.027 mm to ≥0.021 mm in <i>Insulation Specifications</i> table	
•	Changed IDD1 (3.0 V ≤ VDD1 ≤ 3.6 V) from 5.0 mA (typ) / 6.9 mA (max) to 6.3 mA (typ) / 8.5 mA (max)	
•	Changed IDD1 (4.5 V $\leq$ VDD1 $\leq$ 5.5 V) from 5.9 mA (typ) / 8.3 mA (max) to 7.2 mA (typ) / 9.8 mA (max)	
•	Changed IDD2 (3.0 V $\leq$ VDD2 $\leq$ 3.6 V) from 4.4 mA (typ) / 5.6 mA (max) to 5.3 mA (typ) / 7.2 mA (max)	
•	Changed IDD2 (4.5 V $\leq$ VDD2 $\leq$ 5.5 V) from 4.8 mA (typ) / 6.5 mA (max) to 5.9 mA (typ) / 8.1 mA (max)	
•	Changed Timing Diagram section	
•	Changed Overview section	
•	Changed Functional Block Diagram image	
•	Changed the Analog Input section	
•	Added the Isolation Channel Signal Transmission section	
•	Added Analog Output section, deleted Fail-Safe Output section	
•	Changed Device Functional Modes section	21



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Changed Application Information section	22
Changed Typical Application section	<mark>22</mark>
Changed Best Design Practices section	25
Changed Power Supply Recommendations section	
Changed the Recommended Layout of the AMC1301 figure	
<ul> <li>Added a link to the Isolated Voltage-Measurement Circuit in the Related Documentation section</li> </ul>	
Changes from Revision E (March 2018) to Revision F (April 2020)	Page
Changed safety-related certifications details as per ISO standard	1
Changed IEC 60950-1 and IEC60065 to IEC 62368-1	
Changed VDE V 0884-10 to VDE V 0884-11 in Description section	
Changed T <sub>A</sub> parameter from specified to operating in Device Comparison Table	
Changed CLR and CPG values from 9 mm to 8.5 mm	
Changed Insulation Specifications table per ISO standard	
Changed Safety-Related Certifications table per ISO standard	
Changed Safety Limiting Values description as per ISO standard	
Changed Rise and Fall Time Test Waveforms figure	
Changed Delay Time Test Waveforms figure	
Changed Functional Block Diagram figure	



## **Device Comparison Table**

PARAMETER	AMC1301S	AMC1301
Operating ambient temperature, T <sub>A</sub>	–55°C to +125°C	-40°C to +125°C
Input offset drift, TCV <sub>OS</sub>	±4 μV/°C (max)	±3 μV/°C (max)
Gain error drift, TCE <sub>G</sub>	±60 ppm/°C (max)	±50 ppm/°C (max)

# 5 Pin Configuration and Functions

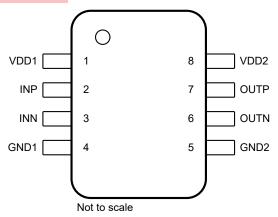


Figure 5-1. DWV Package, 8-Pin SOIC (Top View)

#### Table 5-1. Pin Functions

	PIN			
NO.	NO. NAME		DESCRIPTION	
1	VDD1	High-side power	High-side power supply. <sup>(1)</sup>	
2	INP	Analog input	oninverting analog input. Either INP or INN must have a DC current path to GND1 define the common-mode input voltage. <sup>(2)</sup>	
3	INN	Analog input	verting analog input. Either INP or INN must have a DC current path to GND1 to fine the common-mode input voltage. <sup>(2)</sup>	
4	GND1	High-side ground	High-side analog ground.	
5	GND2	Low-side ground	Low-side analog ground.	
6	OUTN	Analog output	Inverting analog output.	
7	OUTP	Analog output	Noninverting analog output.	
8	VDD2	Low-side power	Low-side power supply. <sup>(1)</sup>	

- (1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
- (2) See the *Layout* section for details.



## 6 Specifications

## 6.1 Absolute Maximum Ratings

see(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	-0.3	7	V
ower-supply voltage	Low-side VDD2 to GND2	-0.3	7	V
Analog input voltage	INP, INN	GND1 – 6	VDD1 + 0.5	V
Input current	Continuous, any pin except power-supply pins	-10	10	mA
Temperature	Junction, T <sub>J</sub>		150	°C
Temperature	Storage, T <sub>stg</sub>	-65	150	C

<sup>(1)</sup> Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

#### 6.2 ESD Ratings

			VALUE	UNIT
	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V	
V <sub>(ESD)</sub>	Electrostatic discriarge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>((2))</sup>	±1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

·		,	MIN	NOM M	AX UNIT
POWER	SUPPLY				
	High-side power supply	VDD1 to GND1	3	5	5.5 V
	Low-side power supply	VDD2 to GND2	3	3.3	5.5 V
ANALO	SINPUT				
V <sub>Clipping</sub>	Differential input voltage before clipping output	$V_{IN} = V_{INP} - V_{INN}$		±302.7	mV
$V_{FSR}$	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} - V_{INN}$	-250	2	50 mV
	Absolute common-mode input voltage <sup>(1)</sup>	(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to GND1	-2	VD	D1 V
V <sub>CM</sub>	Operating common-mode input voltage	(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to GND1	-0.16	VDD1 – :	2.1 V
TEMPER	RATURE RANGE				
т	Specified ambient temperature	AMC1301	-40	1	25 °C
T <sub>A</sub>	Specified ambient temperature	AMC1301S	-55	1	25

<sup>(1)</sup> Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V<sub>CM</sub> for normal operation. Observe analog input voltage range as specified in *Absolute Maximum Ratings* table.



### **6.4 Thermal Information**

	THERMAL METRIC(1)	DWV (SOIC)	UNIT
	I DERMAL METRIC	8 PINS	UNII
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	°C/W
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	51.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	16.0	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	64.5	°C/W
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

# 6.5 Power Ratings

	PARAMETER	TEST CONDITIONS	VALUE	UNIT
P <sub>D</sub>	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	99	mW
Б	Maximum power dissipation (high-side)	VDD1 = 3.6 V	31	mW
P <sub>D1</sub>		VDD1 = 5.5 V	54	
_	Maximum power dissipation (low-side)	VDD2 = 3.6 V	26	mW
P <sub>D2</sub>		VDD2 = 5.5 V	45	

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#### 6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	VALUE	UNIT
GENER	AL			
CLR	External clearance <sup>(1)</sup>	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage <sup>(1)</sup>	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 600 V <sub>RMS</sub>	I-IV	
	per IEC 60664-1	Rated mains voltage ≤ 1000 V <sub>RMS</sub>	1-111	
DIN EN	IEC 60747-17 (VDE 0884-17)(2)			
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	At AC voltage	1500	$V_{PK}$
,	Maximum-rated isolation	At AC voltage (sine wave)	1000	$V_{RMS}$
$V_{IOWM}$	working voltage	At DC voltage	1500	$V_{DC}$
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification test), V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production test)	7000	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(2)</sup>	Tested in air, 1.2/50-µs waveform per IEC 62368-1	7700	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V <sub>PK</sub>
	Apparent charge <sup>((5))</sup>	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$ , $t_{ini} = 60$ s, $V_{pd(m)} = 1.2 \times V_{IORM}$ , $t_m = 10$ s	≤ 5	
_		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$ , $t_{ini} = 60$ s, $V_{pd(m)} = 1.6 \times V_{IORM}$ , $t_m = 10$ s	≤ 5	pC
q <sub>pd</sub>		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$ , $t_{ini} = 1 \text{ s}$ , $V_{pd(m)} = 1.875 \times V_{IORM}$ , $t_m = 1 \text{ s}$	≤ 5	
		Method b2, at routine test (100% production) <sup>((7))</sup> , $V_{pd(ini)} = V_{pd(m)} = 1.2 \text{ x } V_{IOTM}$ , $t_{ini} = t_m = 1 \text{ s}$	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.5 V <sub>PP</sub> at 1 MHz	~1.2	pF
		V <sub>IO</sub> = 500 V at T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	
₹10	Insulation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500 V at 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	Ω
	input to output	V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic actors	AMC1301	40/125/21	
	Climatic category	AMC1301S	55/125/21	
JL1577	1	· ·		
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 s (qualification test), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1 s (100% production test)	5000	V <sub>RMS</sub>

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
- (2) Testing is carried out in air to determine the surge immunity of the package.
- (3) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier are tied together, creating a two-pin device.
- (6) Either method b1 or b2 is used in production.



#### 6.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition program
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

## 6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Is	Safety input, output, or supply current	R <sub>θJA</sub> = 110.1°C/W, VDDx = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			206	mA
Is	Safety input, output, or supply current	R <sub>θJA</sub> = 110.1°C/W, VDDx = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			315	mA
Ps	Safety input, output, or total power	R <sub>θJA</sub> = 110.1°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			1135	mW
T <sub>S</sub>	Maximum safety temperature				150	°C

The maximum safety temperature,  $T_S$ , has the same value as the maximum junction temperature,  $T_J$ , specified for the device. The  $I_S$ and P<sub>S</sub> parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I<sub>S</sub> and P<sub>S</sub>. These limits vary with the ambient temperature,  $T_A$ .

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The junction-to-air thermal resistance,  $R_{\theta JA}$ , in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where  $T_{J(max)}$  is the maximum junction temperature.  $P_S = I_S \times VDD_{max}$ , where  $VDD_{max}$  is the maximum supply voltage for high-side and low-side.



## **6.9 Electrical Characteristics**

minimum and maximum specifications apply from  $T_A$  =  $-40^{\circ}$ C to +125°C (for AMC1301S:  $T_A$  =  $-55^{\circ}$ C to +125°C), VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = -250 mV to +250 mV, and INN = GND1; typical specifications are at  $T_A$  = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG	SINPUT					
V <sub>CMov</sub>	Common-mode overvoltage detection level	(V <sub>INP</sub> + V <sub>INN</sub> ) / 2 to GND1	VDD1 – 2			V
	Hysteresis of common-mode overvoltage detection level			60		mV
Vos	Input offset voltage <sup>(1)</sup>	Initial, at T <sub>A</sub> = 25°C, INP = INN = GND1	-0.2	±0.05	0.2	mV
TCV	Input offset drift <sup>(1)</sup> (4)	AMC1301	-3	±1	3	11/1°C
TCV <sub>OS</sub>	input oliset ariit.	AMC1301S	-4	±1	4	μV/°C
CMRR	Common mode rejection ratio	f <sub>IN</sub> = 0 Hz, V <sub>CM min</sub> ≤ V <sub>CM</sub> ≤ V <sub>CM max</sub>		-93		٩D
CIVIRR	Common-mode rejection ratio	f <sub>IN</sub> = 10 kHz, V <sub>CM min</sub> ≤ V <sub>CM</sub> ≤ V <sub>CM max</sub>		-93		dB
R <sub>IN</sub>	Single-ended input resistance	INN = GND1		18		kΩ
R <sub>IND</sub>	Differential input resistance			22		kΩ
I <sub>IB</sub>	Input bias current	INP = INN = GND1; I <sub>IB</sub> = (I <sub>IBP</sub> + I <sub>IBN</sub> ) / 2	-41	-30	-24	μA
TCI <sub>IB</sub>	Input bias current drift			1		nA/°C
C <sub>IND</sub>	Differential input capacitance			1		pF
ANALOG	OUTPUT					
	Nominal gain			8.2		V/V
E <sub>G</sub>	Gain error <sup>(1)</sup>	at T <sub>A</sub> = 25°C	-0.3%	±0.05%	0.3%	
TOF	Gain drift <sup>(1) (5)</sup>	AMC1301	-50	±15	50	
TCE <sub>G</sub>	Gain drift(1) (6)	AMC1301S	-60	±15	60	ppm/°C
	Nonlinearity <sup>(1)</sup>		-0.03%	±0.01%	0.03%	
	Nonlinearity drift			±1		ppm/°C
THD	Total harmonic distortion <sup>(3)</sup>	f <sub>IN</sub> = 10 kHz		-87		dB
	Output noise	INP = INN = GND1, f <sub>IN</sub> = 0 Hz, BW = 100 kHz brickwall filter		220		μV <sub>RMS</sub>
CND	Cinnal to mains notice	f <sub>IN</sub> = 1 kHz, BW = 10 kHz	80	84		-10
SNR	Signal-to-noise ratio	f <sub>IN</sub> = 10 kHz, BW = 100 kHz		71		dB
		PSRR vs VDD1, at DC		-94		
Denn	Device symply rejection retio(2)	PSRR vs VDD1, 100-mV and 10-kHz ripple		-90		dD
PSRR	Power-supply rejection ratio <sup>(2)</sup>	PSRR vs VDD2, at DC		-100		dB
		PSRR vs VDD2, 100-mV and 10-kHz ripple		-94		
$V_{CMout}$	Common-mode output voltage		1.39	1.44	1.49	V
V <sub>CLIPout</sub>	Clipping differential output voltage	$V_{OUT} = (V_{OUTP} - V_{OUTN});$ $ V_{IN}  =  V_{INP} - V_{INN}  >  V_{Clipping} $	-2.52	±2.49	2.52	V
V <sub>Failsafe</sub>	Failsafe differential output voltage	V <sub>CM</sub> ≥ V <sub>CMov</sub> , or VDD1 missing		-2.563	-2.545	V
BW	Output bandwidth		190	210		kHz
R <sub>OUT</sub>	Output resistance	On OUTP or OUTN		< 0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, INN = INP = GND1, outputs shorted to either GND2 or VDD2		13		mA
CMTI	Common-mode transient immunity	GND1 – GND2  = 1 kV	15			kV/µs

## 6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to +125°C (for AMC1301S:  $T_A = -55^{\circ}\text{C}$  to +125°C), VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = -250 mV to +250 mV, and INN = GND1; typical specifications are at  $T_A = 25^{\circ}\text{C}$ , VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER S	UPPLY					
IDD4 Lligh side cumply current	3.0 V ≤ VDD1 ≤ 3.6 V		6.3	8.5	mΛ	
וטטו	IDD1 High-side supply current	4.5 V ≤ VDD1 ≤ 5.5 V		7.2	9.8	mA
IDD2	IDDO	3.0 V ≤ VDD2 ≤ 3.6 V		5.3	7.2	m A
IDD2 Low-side supply current	Low-side supply current	4.5 V ≤ VDD2 ≤ 5.5 V		5.9	8.1	mA

- (1) The typical value includes one standard deviation (sigma) at nominal operating conditions.
- (2) This parameter is input referred.
- (3) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
- (4) Offset error temperature drift is calculated using the box method, as described by the following equation:  $TCV_{OS} = (V_{OS,MAX} V_{OS,MIN}) / TempRange$  where  $V_{OS,MAX}$  and  $V_{OS,MIN}$  refer to the maximum and minimum  $V_{OS}$  values measured within the temperature range (–40 to 125°C).
- (5) Gain error temperature drift is calculated using the box method, as described by the following equation:  $TCE_G(ppm) = ((E_{G,MAX} E_{G,MIN}) / TempRange) \times 10^4$  where  $E_{G,MAX}$  and  $E_{G,MIN}$  refer to the maximum and minimum  $E_G$  values (in %) measured within the temperature range (–40 to 125°C).

#### 6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>r</sub>	Output signal rise time			2.0		μs
t <sub>f</sub>	Output signal fall time			2.0		μs
	V <sub>INx</sub> to V <sub>OUTx</sub> signal delay (50% - 10%)	Unfiltered output		0.7	2.0	μs
	V <sub>INx</sub> to V <sub>OUTx</sub> signal delay (50% - 50%)	Unfiltered output		1.6	2.6	μs
	V <sub>INx</sub> to V <sub>OUTx</sub> signal delay (50% - 90%)	Unfiltered output		2.5	3	μs

#### 6.11 Timing Diagram

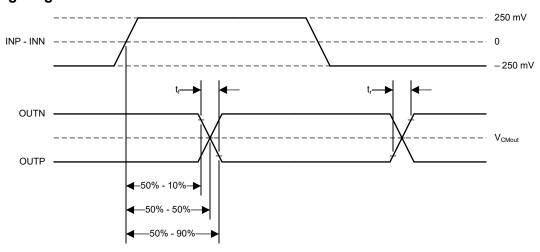
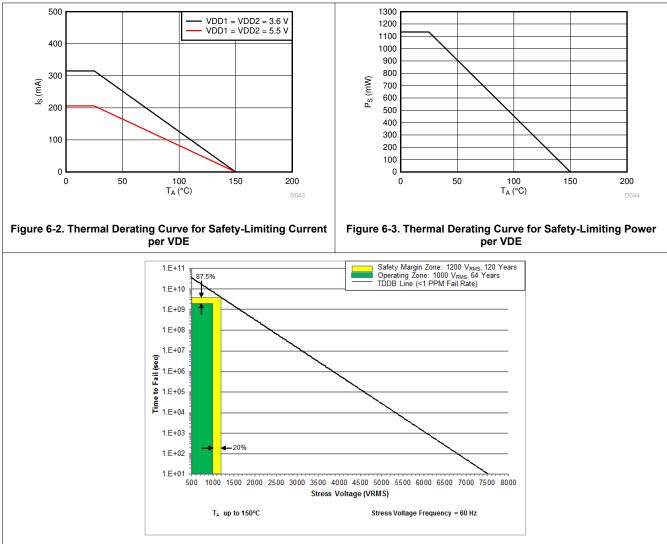


Figure 6-1. Rise, Fall, and Delay Time Definition



#### **6.12 Insulation Characteristics Curves**



T<sub>A</sub> up to 150°C, stress voltage frequency = 60 Hz

Figure 6-4. Reinforced Isolation Capacitor Lifetime Projection



#### 6.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and  $f_{IN}$  = 10 kHz (unless otherwise noted)

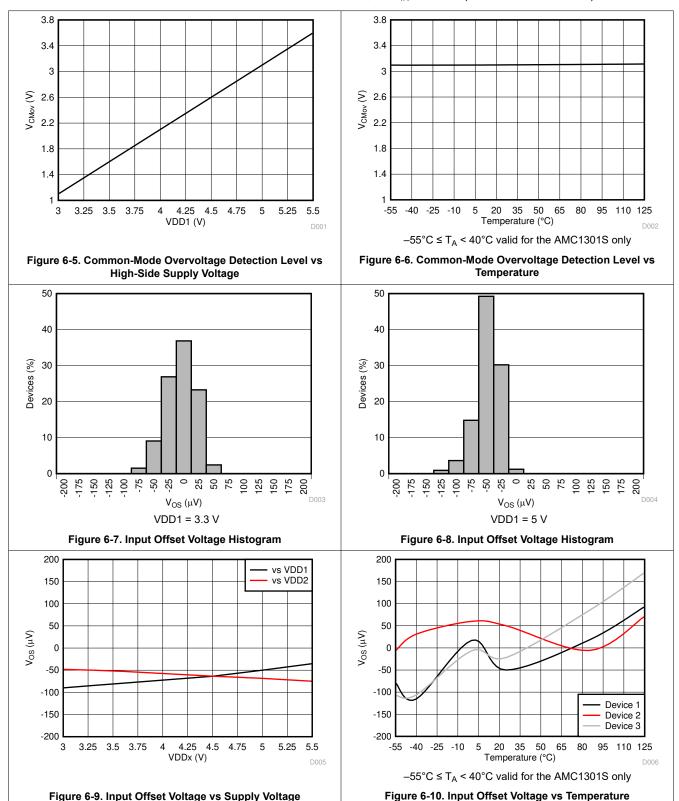
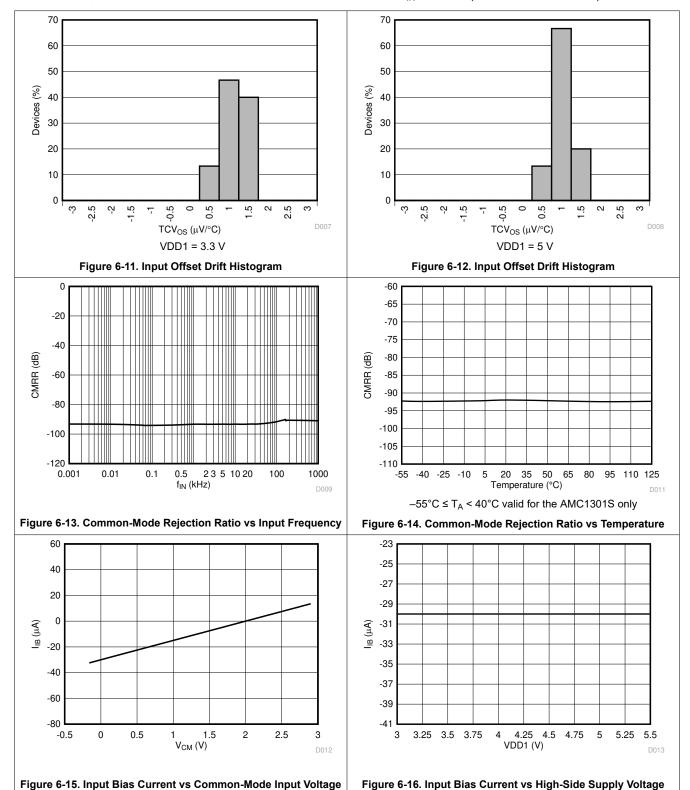
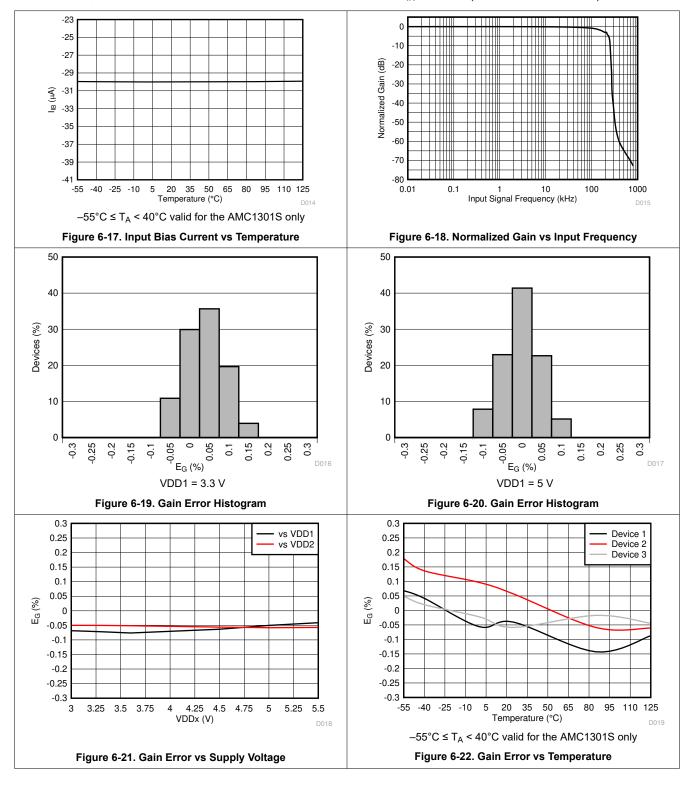


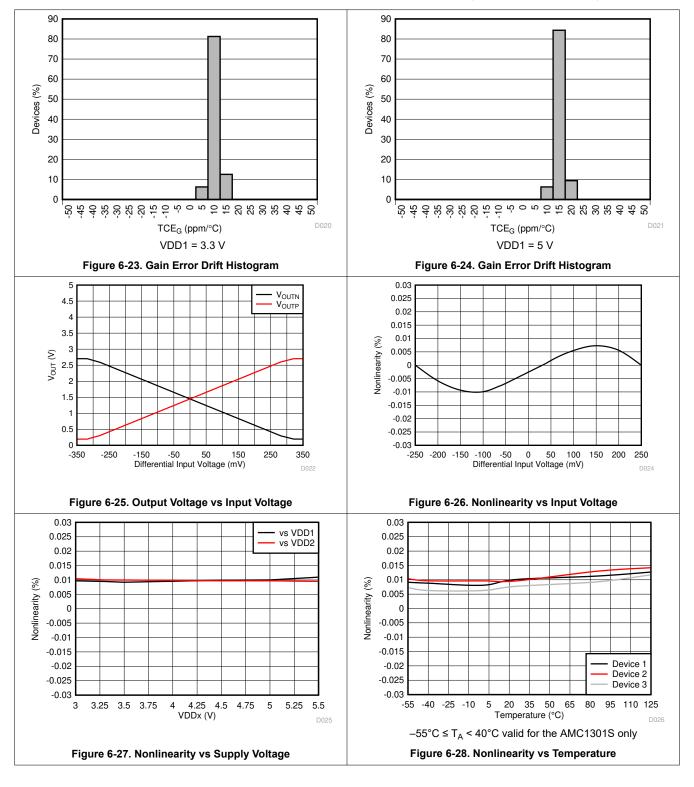
Figure 6-9. Input Offset Voltage vs Supply Voltage













at VDD1 = 5 V, VDD2 = 3.3 V, INP = -250 mV to 250 mV, INN = 0 V, and  $f_{IN}$  = 10 kHz (unless otherwise noted)

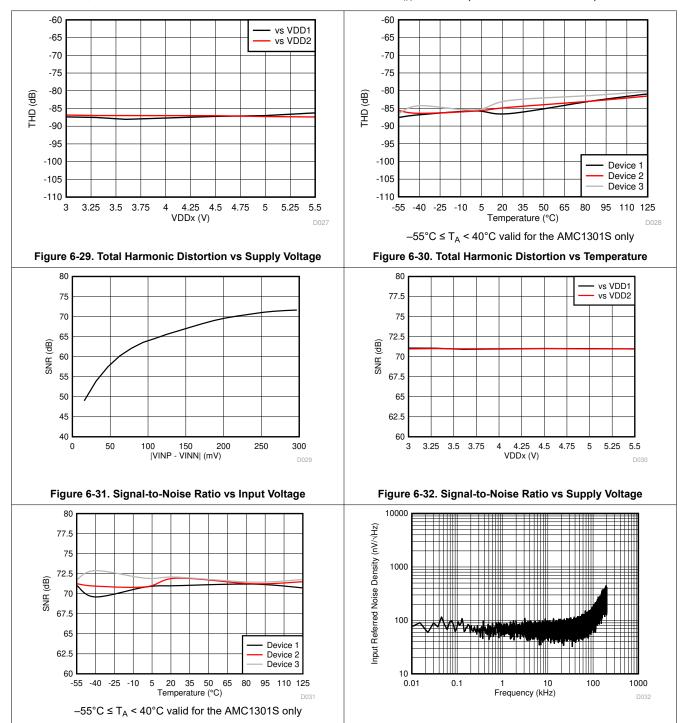
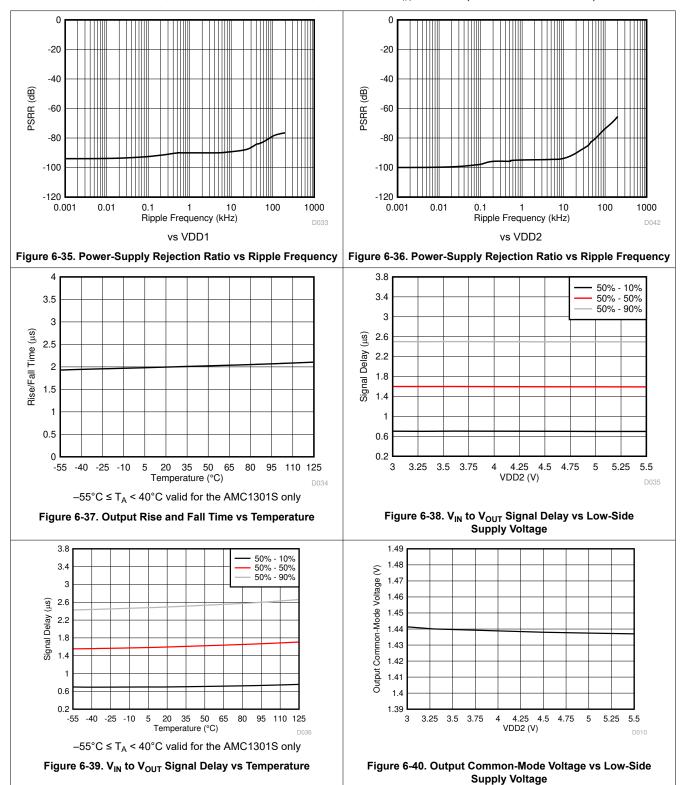
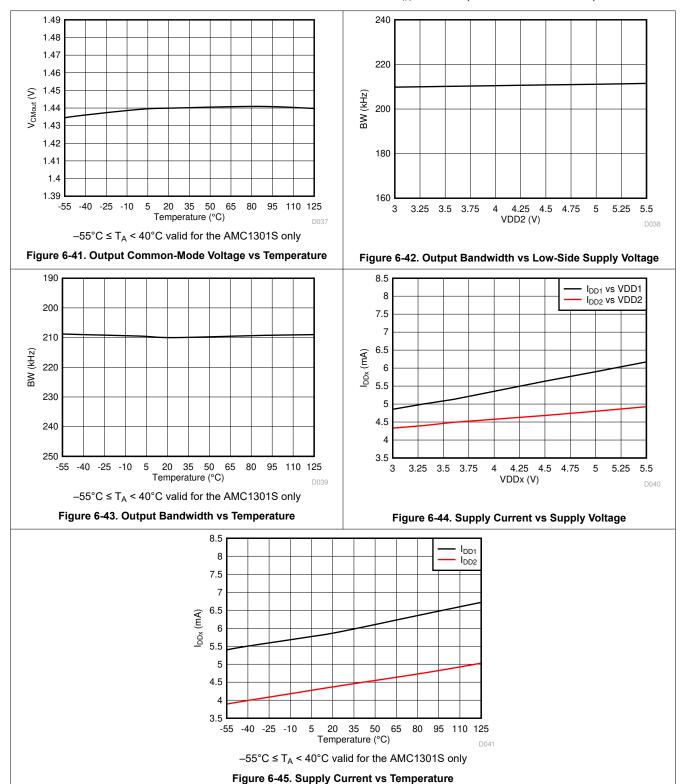


Figure 6-33. Signal-to-Noise Ratio vs Temperature

Figure 6-34. Input-Referred Noise Density vs Frequency









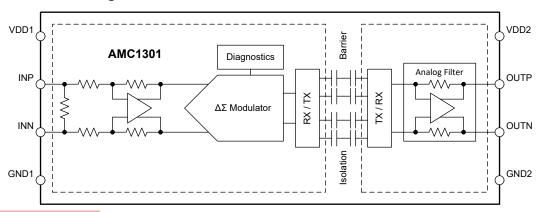
## 7 Detailed Description

#### 7.1 Overview

The AMC1301 is a fully differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma ( $\Delta\Sigma$ ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins that is proportional to the input signal.

The SiO<sub>2</sub>-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The digital modulation used in the AMC1301 to transmit data across the isolation barrier, and the isolation barrier characteristics, result in high reliability and common-mode transient immunity.

### 7.2 Functional Block Diagram



#### 7.3 Feature Description

#### 7.3.1 Analog Input

The differential amplifier input stage of the AMC1301 feeds a second-order, switched-capacitor, feed-forward  $\Delta\Sigma$  modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R<sub>IND</sub>. The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals (INP and INN). First, if the input voltages  $V_{\text{INP}}$  or  $V_{\text{INN}}$  exceed the range specified in the *Absolute Maximum Ratings* table, the input currents must be limited to the absolute maximum value, because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range ( $V_{\text{FSR}}$ ) and within the common-mode input voltage range ( $V_{\text{CM}}$ ), as specified in the *Recommended Operating Conditions* table.

#### 7.3.2 Isolation Channel Signal Transmission

The AMC1301 uses an on-off keying (OOK) modulation scheme, as shown in Figure 7-1, to transmit the modulator output bitstream across the SiO<sub>2</sub>-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1301 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC1301 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

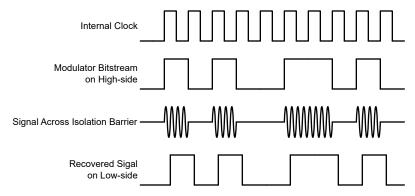


Figure 7-1. OOK-Based Modulation Scheme

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#### 7.3.3 Analog Output

The AMC1301 offers a differential analog output comprised of the OUTP and OUTN pins. For differential input voltages ( $V_{INP} - V_{INN}$ ) in the range from -250 mV to 250 mV, the device provides a linear response with a nominal gain of 8.2. For example, for a differential input voltage of 250 mV, the differential output voltage ( $V_{OUTP} - V_{OUTN}$ ) is 2.05 V. At zero input (INP shorted to INN), both pins output the same common-mode output voltage  $V_{CMout}$ , as specified in the *Electrical Characteristics* table. For absolute differential input voltages greater than 250 mV but less than 320 mV, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of  $V_{CLIPout}$ , as shown in Figure 7-2, if the differential input voltage exceeds the  $V_{Clipping}$  value.

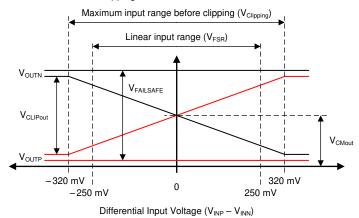


Figure 7-2. Output Behavior of the AMC1301

The AMC1301 offers a fail-safe feature that simplifies diagnostics on a system level. Figure 7-2 shows the fail-safe mode, in which the AMC1301 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in two cases:

- When the high-side supply is missing or below the VDD1<sub>LIV</sub> threshold
- When the common-mode input voltage, that is V<sub>CM</sub> = (V<sub>INP</sub> + V<sub>INN</sub>) / 2, exceeds the common-mode overvoltage detection level V<sub>CMov</sub>

Use the maximum  $V_{\text{FAILSAFE}}$  voltage specified in the *Electrical Characteristics* table as a reference value for fail-safe detection on a system level.

#### 7.4 Device Functional Modes

The AMC1301 assumes normal operation as soon as VDD1, VDD2, and the input common-mode voltage ( $V_{CM}$ ) are within the operational ranges, as specified in *Electrical Characteristics* table. In this mode, the output voltage is proportional to the input voltage.

The AMC1301 enters fail-safe mode whenever the high-side supply (VDD1) is missing or the input common-mode voltage ( $V_{CM}$ ) exceeds the specified input-overvoltage detection level  $V_{CMov}$ . In this mode, the differential output voltage is a fixed, negative value ( $V_{FAILSAFE}$ ). See the *Analog Output* section for details.



## 8 Application and Implementation

#### **Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

#### 8.1 Application Information

With a low analog input voltage range, high DC accuracy, and low temperature drift, the AMC1301 is designed for precision, shunt-based current sensing in applications requiring high voltage isolation.

## 8.2 Typical Application

Figure 8-1 shows the AMC1301 in a typical application of an AC motor drive. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop that is sensed by the AMC1301. The AMC1301 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, reconstructs the analog signal, and presents that signal as a differential voltage on the output pins.

The differential input, differential output, and the high common-mode transient immunity (CMTI) of the AMC1301 provide reliable and accurate operation even in high-noise environments.

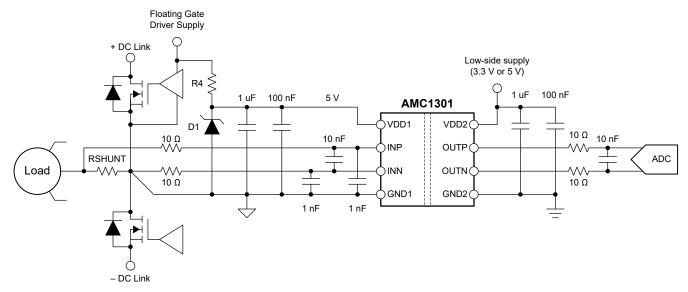


Figure 8-1. Using the AMC1301 for Current Sensing in a Typical Application

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### 8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across RSHUNT for a linear response	±250 mV (maximum)
Signal delay (50% V <sub>IN</sub> to 90% OUTP, OUTN)	3 µs (maximum)

#### 8.2.2 Detailed Design Procedure

In Figure 8-1, the high-side power supply (VDD1) for the AMC1301 is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC1301 (INN). If a four-pin shunt is used, the inputs of the AMC1301 are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the *Layout* section for more details.

#### 8.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor ( $V_{SHUNT}$ ) for the desired measured current:  $V_{SHUNT} = I \times RSHUNT$ .

Consider the following two restrictions when selecting the value of the shunt resistor, RSHUNT:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range for a linear response: |V<sub>SHUNT</sub>| ≤ |V<sub>FSR</sub>|
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes
  a clipping output: |V<sub>SHUNT</sub>| ≤ |V<sub>Clipping</sub>|

#### 8.2.2.2 Input Filter Design

Place a differential RC filter (R1, R2, C5) in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency of the  $\Delta\Sigma$  modulator (20 MHz)
- The input bias current does not generate significant voltage drop across the DC impedances (R1, R2) of the input filter
- The impedances measured from the analog inputs are equal (R1 equals R2)

Capacitors C6 and C7 are optional and improve common-mode rejection at high frequencies (>1 MHz). For best performance, C6 must match the value of C7 and both capacitors must be 10 to 20 times lower in value than C5. For most applications, the structure shown in Figure 8-2 achieves excellent performance.

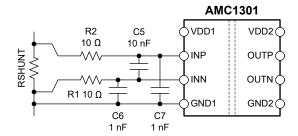


Figure 8-2. Differential Input Filter

#### 8.2.2.3 Differential to Single-Ended Output Conversion

Figure 8-3 shows an example of a TLV900x-based signal conversion and filter circuit for systems using single-ended input ADCs to convert the analog output voltage into digital. For R1 = R3 and R2 = R4, the output voltage equals (R2 / R1) × ( $V_{OUTP} - V_{OUTN}$ ) +  $V_{REF}$ . Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, R1 = R2 = R3 = R4 = 3.3 k $\Omega$  and C1 = C2 = 330 pF yields good performance.

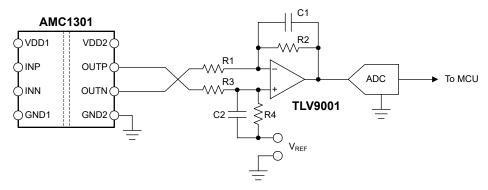


Figure 8-3. Connecting the AMC1301 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the 18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise and 18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power reference guides, available for download at www.ti.com.

#### 8.2.3 Application Curve

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. Figure 8-4 shows the typical full-scale step response of the AMC1301.



Figure 8-4. Step Response of the AMC1301

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#### 8.3 Best Design Practices

Do not leave the inputs of the AMC1301 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current can possibly drive the inputs to a positive value that exceeds the operating common-mode input voltage, thus causing the device to output the fail-safe voltage as described in the *Analog Output* section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Take care not to exceed the input common-mode range as specified in the *Recommended Operating Conditions* table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the *Layout* section for more details.

#### 8.4 Power Supply Recommendations

The AMC1301 does not require any specific power-up sequencing. The high-side power supply (AVDD) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1-μF capacitor (C2). The low-side power supply (DVDD) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1-μF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

The ground reference for the high-side (AGND) is derived from the end of the shunt resistor that is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace to make this connection instead of shorting AGND to INN directly at the device input. If a four-terminal shunt is used, the device inputs are connected to the inner leads and AGND is connected to the outer lead on the INN side of the shunt. Figure 8-5 shows a decoupling diagram of the AMC1301.

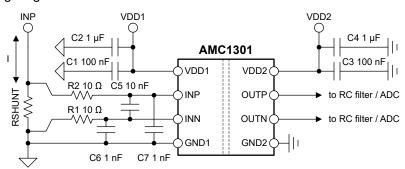


Figure 8-5. Decoupling of the AMC1301



#### 8.5 Layout

### 8.5.1 Layout Guidelines

Figure 8-6 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1301 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1301 and keep the layout of both connections symmetrical.

### 8.5.2 Layout Example

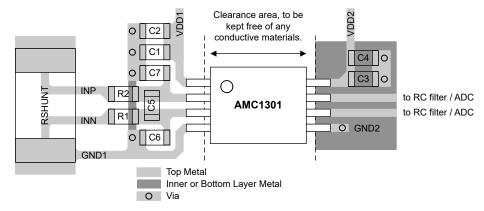


Figure 8-6. Recommended Layout of the AMC1301



## 9 Device and Documentation Support

#### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, Isolation Glossary application note
- · Texas Instruments, Semiconductor and IC Package Thermal Metrics application note
- Texas Instruments, ISO72x Digital Isolator Magnetic-Field Immunity application note
- Texas Instruments, TLV900x Low-Power, RRIO, 1-MHz Operational Amplifier for Cost-Sensitive Systems data sheet
- Texas Instruments, 18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise reference guide
- Texas Instruments, 18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power reference quide
- Texas Instruments, Isolated Amplifier Voltage Sensing Excel Calculator design tool
- Texas Instruments, Best in Class Radiated Emissions EMI Performance with the AMC1300B-Q1 Isolated Amplifier technical white paper
- Texas Instruments, Isolated Voltage-Measurement Circuit With ±250-mV Input and Differential Output application note

#### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 9.4 Trademarks

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#### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

#### 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
							(6)				
AMC1301DWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1301	Samples
AMC1301DWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1301	Samples
AMC1301SDWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1301S	Samples
AMC1301SDWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1301S	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF AMC1301:

Automotive : AMC1301-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1301DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1301DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1301DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1
AMC1301SDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1301SDWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1
AMC1301SDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1



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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1301DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1301DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1301DWVR	SOIC	DWV	8	1000	356.0	356.0	35.0
AMC1301SDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1301SDWVR	SOIC	DWV	8	1000	356.0	356.0	35.0
AMC1301SDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0

# **PACKAGE MATERIALS INFORMATION**

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### **TUBE**



#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1301DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1301SDWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6



SOIC



#### NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOIC



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



#### NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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