# OPAx320x Precision, 20-MHz, 0.9-pA, Low-Noise, RRIO, CMOS Operational Amplifier With Shutdown

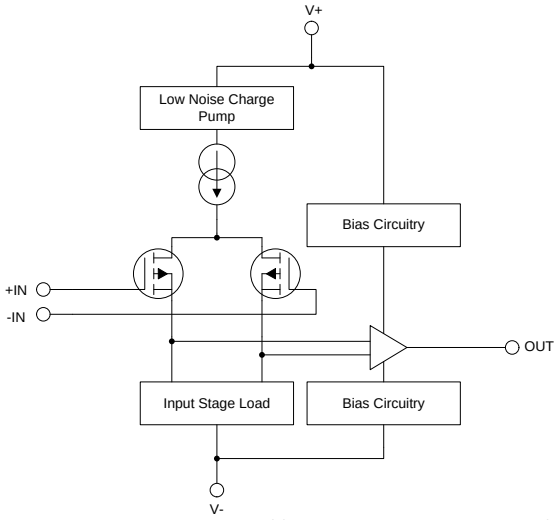
## 1 Features

- Precision with Zero-Crossover Distortion:
  - Low Offset Voltage: 150 µV (Maximum)
  - High CMRR: 114 dB
  - Rail-to-Rail I/O
- Low Input Bias Current: 0.9 pA (Maximum)
- Low Noise: 7 nV/√Hz at 10 kHz
- Wide Bandwidth: 20 MHz
- Slew Rate: 10 V/µs
- Quiescent Current: 1.45 mA/Ch
- Single-Supply Voltage Range: 1.8 V to 5.5 V
- OPA320S and OPA2320S:
  - $I_Q$ in Shutdown Mode: 0.1 µA
- Unity-Gain Stable
- Small Packages:
  - SOT-23, VSSOP, SON, and SOIC

## 2 Applications

- High-Z Sensor Signal Conditioning
- Transimpedance Amplifiers
- Test and Measurement Equipment
- Programmable Logic Controllers (PLCs)
- Motor Control Loops
- Communications
- Input/Output ADC/DAC Buffers
- Active Filters

**Block Diagram**






## 3 Description

The OPA320 (single) and OPA2320 (dual) are a new generation of precision, low-voltage CMOS operational amplifiers optimized for very low noise and wide bandwidth while operating on a low quiescent current of only 1.45 mA.

The OPA320 series is ideal for low-power, single-supply applications. Low-noise (7 nV/√Hz) and high-speed operation also make them well-suited for driving sampling analog-to-digital converters (ADCs). Other applications include signal conditioning and sensor amplification.

The OPA320 features a linear input stage with zero-crossover distortion that delivers excellent common-mode rejection ratio (CMRR) of typically 114 dB over the full input range. The input common mode range extends 100 mV beyond the negative and positive supply rails. The output voltage typically swings within 10 mV of the rails.

In addition, the OPAx320 has a wide supply voltage range from 1.8 V to 5.5 V with excellent PSRR (106 dB) over the entire supply range, making them suitable for precision, low-power applications that run directly from batteries without regulation.

The OPA320 (single version) is available in a 5-pin SOT23 package; the OPA320S shutdown single version is available in an 6-pin SOT23 package. The dual OPA2320 is offered in 8-pin SOIC, VSSOP, and SON packages, and the OPA2320S (dual with shutdown) in a 10-pin VSSOP package.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA320 | SOT-23 (5) | 2.90 mm × 1.60 mm |
| OPA320S | SOT-23 (6) | 2.90 mm × 1.60 mm |
| OPA2320 | VSSOP (8) | 3.00 mm × 3.00 mm |
| | SOIC (8) | 4.90 mm × 3.91 mm |
| | SON (10) | 3.00 mm × 3.00 mm |
| OPA2320S | VSSOP (10) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision E (June 2013) to Revision F** — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed package families throughout data sheet: DFN to SON, MSOP to VSSOP, and SO to SOIC ... 1

**Changes from Revision D (November 2011) to Revision E** — **Page**

- Deleted *Ordering Information* table ... 1
- Changed *Shutdown*, $V_{IH}$ and $V_{IL}$ parameters in Electrical Characteristics table ... 8
- Added Figure 29 and Figure 30 ... 13
- Added Figure 31 and Figure 32 ... 14

**Changes from Revision C (August 2011) to Revision D** — **Page**

- Changed status of OPA2320 SO-8 (D) to production data from product preview. ... 1

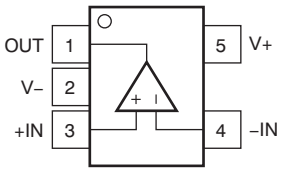
**Changes from Revision B (March 2010) to Revision C** — **Page**

- Deleted D (SO-8) package pinout drawing from *Pin Configurations and Functions* ... 4
- Changed names of pins 2 and 6 for DGS (MSOP-10) package ... 5
- Added values to *Thermal Information* tables, moved to new page, and updated format ... 6
- Added $\overline{\text{SHDN}}$ value to Electrical Characteristics condition line ... 7
- Added new test condition row for Input Bias Current Over Temperature parameter ... 7
- Changed test condition for Phase Margin parameter in Electrical Characteristics ... 8
- Added test condition to *Short-Circuit Current* parameter in Electrical Characteristics ... 8

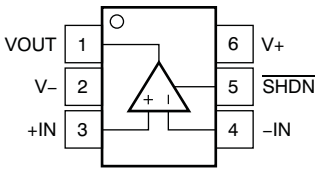
- Changed *Shutdown* subsection of Electrical Characteristics along with associated notes ..... 8
- Changed *Power Supply* subsection of Electrical Characteristics ..... 9
- Changed Figure 4 ..... 10
- Changed Figure 18 ..... 11
- Changed 100 µs to 100 ns in first paragraph of *Overload Recovery Time* section ..... 20
- Changed Figure 38 ..... 20
- Changed Figure 39 ..... 20
- Changed $R_2$ value in Figure 44 from 500Ω to 50kΩ ..... 25

# 5 Pin Configuration and Functions

**OPA320 DBV Package**
**5-Pin SOT-23**
**Top View**



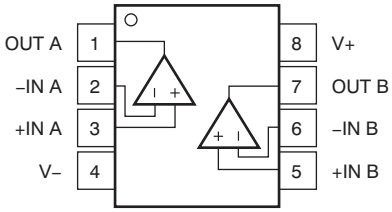

**OPA320S DBV Package**
**6-Pin SOT-23**
**Top View**



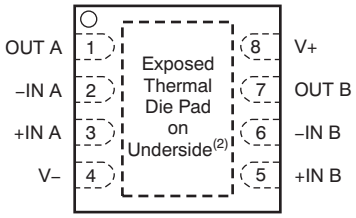

**Pin Functions: OPA320 and OPA320S**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | OPA320 | OPA320S | | |
| –IN | 4 | 4 | I | Negative (inverting) input |
| +IN | 3 | 3 | I | Positive (noninverting) input |
| OUT, VOUT | 1 | 1 | O | Output |
| $\overline{\text{SHDN}}$ | — | 5 | I | Shutdown, active low |
| V– | 2 | 2 | — | Negative (lowest) power supply |
| V+ | 5 | 6 | — | Positive (highest) power supply |

**OPA2320 D and DGK Packages**
**8-Pin SOIC and VSSOP**
**Top View**




**OPA2320 DRG Package**
**8-Pin SON With Exposed Thermal Pad**
**Top View**

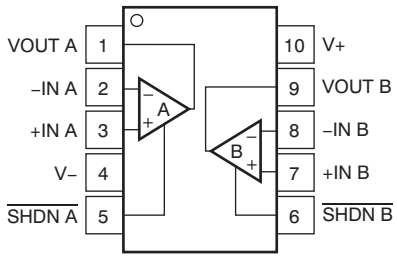



(1) No internal connection.
(2) Connect thermal pad to V–.

**Pin Functions: OPA2320**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOIC, VSSOP | SON | | |
| –IN A | 2 | 2 | I | Inverting input, channel A |
| +IN A | 3 | 3 | I | Noninverting input, channel A |
| –IN B | 6 | 6 | I | Inverting input, channel B |
| +IN B | 5 | 5 | I | Noninverting input, channel B |
| OUT A, VOUT A | 1 | 1 | O | Output, channel A |
| OUT B, VOUT B | 7 | 7 | O | Output, channel B |
| $\overline{\text{SHDN A}}$ | — | — | I | Shutdown, active low, channel A |
| $\overline{\text{SHDN B}}$ | — | — | I | Shutdown, active low, channel B |
| V– | 4 | 4 | — | Negative (lowest) power supply |
| V+ | 8 | 8 | — | Positive (highest) power supply |

**OPA2320S DGS Package**
**10-Pin VSSOP**
**Top View**




## Pin Functions: OPA2320S

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| –IN A | 2 | I | Inverting input, channel A |
| +IN A | 3 | I | Noninverting input, channel A |
| –IN B | 8 | I | Inverting input, channel B |
| +IN B | 7 | I | Noninverting input, channel B |
| OUT A, VOUT A | 1 | O | Output, channel A |
| OUT B, VOUT B | 9 | O | Output, channel B |
| $\overline{\text{SHDN A}}$ | 5 | I | Shutdown, active low, channel A |
| $\overline{\text{SHDN B}}$ | 6 | I | Shutdown, active low, channel B |
| V– | 4 | — | Negative (lowest) power supply |
| V+ | 10 | — | Positive (highest) power supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | Supply, $V_S$ = (V+) – (V–) | | 6 | V |
| | Signal input pin(2) | (V–) – 0.5 | (V+) + 0.5 | |
| Current | Signal input pin(2) | –10 | 10 | mA |
| | Output short-circuit current(3) | Continuous | | |
| Temperature | Operating range, $T_A$ | –40 | 150 | °C |
| | Junction, $T_J$ | | 150 | |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |
| | | Machine model (MM) | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Specified voltage | 1.8 | 5.5 | V |
| $T_A$ | Specified temperature | –40 | 125 | °C |

## 6.4 Thermal Information: OPA320 and OPA320S

| THERMAL METRIC | | OPA320 DBV (SOT-23) 5 PINS | OPA320S DBV (SOT-23) 6 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance(1) | 219.3 | 177.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 107.5 | 108.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 57.5 | 27.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.4 | 13.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 56.9 | 26.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the application report, *Semiconductor and IC Package Thermal Metrics*.

## 6.5 Thermal Information: OPA2320

| THERMAL METRIC(1) | | OPA2320 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | DRG (SON) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 122.6 | 174.8 | 50.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 67.1 | 43.9 | 54.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 64 | 95 | 25.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 13.2 | 2 | 0.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 63.4 | 93.5 | 25.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | — | — | 5.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the application report, *Semiconductor and IC Package Thermal Metrics*.

## 6.6 Thermal Information: OPA2320S

| THERMAL METRIC(1) | | OPA2320S | UNIT |
|---|---|---|---|
| | | DGS (VSSOP) | |
| | | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 171.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 43 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 91.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 89.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.7 Electrical Characteristics

At $V_S$ = 1.8 V to 5.5 V or ±0.9 V to ±2.75 V, $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, $V_{OUT} = V_S/2$, and $\overline{SHDN}$ x = $V_{S+}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | | | | 40 | 150 | µV |
| $dV_{OS}/dT$ | Input offset voltage vs temperature | $V_S$ = 5.5 V, $T_A$ = –40°C to 125°C | | | 1.5 | 5 | µV/°C |
| PSR | Input offset voltage vs power supply | $V_S$ = 1.8 V to 5.5 V, $T_A$ = 25°C | | | 5 | 20 | µV/V |
| | | $V_S$ = 1.8 V to 5.5 V, $T_A$ = –40°C to 125°C | | | 15 | | |
| | Channel separation | 1 kHz | | | 130 | | dB |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage | | | (V–) – 0.1 | | (V+) + 0.1 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 5.5 V, (V–) – 0.1 V < $V_{CM}$ < (V+) + 0.1 V, $T_A$ = 25°C | | 100 | 114 | | dB |
| | | $V_S$ = 5.5 V, (V–) – 0.1 V < $V_{CM}$ < (V+) + 0.1 V, $T_A$ = –40°C to 125°C | | 96 | | | |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | $T_A$ = 25°C | | | ±0.2 | ±0.9 | pA |
| | | $T_A$ = –40°C to 85°C | | | | ±50 | |
| | | $T_A$ = –40°C to 125°C | OPA2320 and OPA2320S | | | ±400 | |
| | | | OPA320 and OPA320S | | | ±600 | |
| $I_{OS}$ | Input offset current | $T_A$ = 25°C | | | ±0.2 | ±0.9 | pA |
| | | $T_A$ = –40°C to 85°C | | | | ±50 | |
| | | $T_A$ = –40°C to 125°C | | | | ±400 | |

## Electrical Characteristics (continued)

At $V_S$ = 1.8 V to 5.5 V or ±0.9 V to ±2.75 V, $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, $V_{OUT} = V_S/2$, and $\overline{SHDN}$ x = $V_{S+}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **NOISE** | | | | | | |
| | Input voltage noise | f = 0.1 Hz to 10 Hz | | 2.8 | | $\mu V_{PP}$ |
| $e_n$ | Input voltage noise density | f = 1 kHz | | 8.5 | | $nV/\sqrt{Hz}$ |
| | | f = 10 kHz | | 7 | | |
| $i_n$ | Input current noise density | f = 1 kHz | | 0.6 | | $fA/\sqrt{Hz}$ |
| **INPUT CAPACITANCE** | | | | | | |
| | Differential | | | 5 | | pF |
| | Common mode | | | 4 | | pF |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | 0.1 V < $V_O$ < (V+) – 0.1 V, $R_L$ = 10 kΩ, $T_A$ = 25°C | 114 | 132 | | dB |
| | | 0.1 V < $V_O$ < (V+) – 0.1 V, $R_L$ = 10 kΩ, $T_A$ = –40°C to 125°C | 100 | 130 | | |
| | | 0.2 V < $V_O$ < (V+) – 0.2 V, $R_L$ = 2 kΩ, $T_A$ = 25°C | 108 | 123 | | |
| | | 0.2 V < $V_O$ < (V+) – 0.2 V, $R_L$ = 2 kΩ, $T_A$ = –40°C to 125°C | 96 | 130 | | |
| PM | Phase margin | $V_S$ = 5 V, $C_L$ = 50 pF | | 47 | | ° |
| **FREQUENCY RESPONSE, $V_S$ = 5 V, $C_L$ = 50 pF** | | | | | | |
| GBP | Gain bandwidth product | Unity gain | | 20 | | MHz |
| SR | Slew rate | G = +1 | | 10 | | V/µs |
| $t_S$ | Settling time | to 0.1%, 2-V step, G = +1 | | 0.25 | | µs |
| | | to 0.01%, 2-V step, G = +1 | | 0.32 | | |
| | | to 0.0015%, 2-V step, G = +1 (1) | | 0.5 | | |
| | Overload recovery time | $V_{IN}$ × G > $V_S$ | | 100 | | ns |
| THD+N | Total harmonic distortion + noise (2) | $V_O$ = 4 $V_{PP}$, G = 1, f = 10 kHz, $R_L$ = 10 kΩ | | 0.0005% | | |
| | | $V_O$ = 2 $V_{PP}$, G = 1, f = 10 kHz, $R_L$ = 600 Ω | | 0.0011% | | |
| **OUTPUT** | | | | | | |
| $V_O$ | Voltage output swing from both rails | $R_L$ = 10 kΩ, $T_A$ = 25°C | | 10 | 20 | mV |
| | | $R_L$ = 2 kΩ, $T_A$ = 25°C | | 25 | 35 | |
| | | $R_L$ = 10 kΩ, $T_A$ = –40°C to 125°C | | | 30 | |
| | | $R_L$ = 2 kΩ, $T_A$ = –40°C to 125°C | | | 45 | |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5.5 V | | ±65 | | mA |
| $C_L$ | Capacitive load drive | | | See *Typical Characteristics* | | |
| $R_O$ | Open-loop output resistance | $I_O$ = 0 mA, f = 1 MHz | | 90 | | Ω |
| **SHUTDOWN** (3) | | | | | | |
| $I_{QSD}$ | Quiescent current per amplifier | All amplifiers disabled, $\overline{SHDN}$ = V– | | 0.1 | 0.5 | µA |
| | | OPA2320S only, $\overline{SHDN\ A}$ = $V_{S–}$, $\overline{SHDN\ B}$ = $V_{S+}$ | | 1.6 | | mA |
| | | OPA2320S only, $\overline{SHDN\ A}$ = $V_{S+}$, $\overline{SHDN\ B}$ = $V_{S–}$ | | 1.6 | | |
| $V_{IH}$ | High-level input voltage | Amplifier enabled, $V_{S–}$ + 0.7 [($V_{S+}$) + |$V_{S–}$|] | 0.7 × $V_{S+}$ | | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | Amplifier disabled, $V_{S–}$ + 0.3 [($V_{S+}$) + |$V_{S–}$|] | | | 0.3 × $V_{S+}$ | V |
| $t_{ON}$ | Amplifier enable time (4) | G = 1, $V_{OUT}$ = 0.1 × $V_S$/2, full shutdown (5) | | 20 | | µs |
| | | OPA2320S only, partial shutdown (5) | | 6 | | |
| $t_{OFF}$ | Amplifier disable time (4) | G = 1, $V_{OUT}$ = 0.1 × $V_S$/2 | | 3 | | µs |
| | $\overline{SHDN}$ pin input bias current (per pin) | $V_{IH}$ = 5 V | | 0.13 | | µA |
| | | $V_{IL}$ = 0 V | | 0.04 | | |

(1) Based on simulation.
(2) Third-order filter; bandwidth = 80 kHz at –3 dB.
(3) Specified by design and characterization; not production tested.
(4) Disable time ($t_{OFF}$) and enable time ($t_{ON}$) are defined as the time between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(5) Full shutdown refers to the dual OPA2320S having both A and B channels disabled ($\overline{SHDN\ A}$ = $\overline{SHDN\ B}$ = $V_{S–}$). For partial shutdown, only one $\overline{SHDN}$ pin is exercised; in this mode, the internal biasing and oscillator remain operational and the enable time is shorter.

## Electrical Characteristics (continued)

At $V_S$ = 1.8 V to 5.5 V or ±0.9 V to ±2.75 V, $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, $V_{OUT} = V_S/2$, and $\overline{SHDN}$ x = $V_{S+}$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Specified voltage | | 1.8 | | 5.5 | V |
| $I_Q$ | Quiescent current per amplifier, OPA320 and OPA320S | $I_O$ = 0 mA, $V_S$ = 5.5 V, $T_A$ = 25°C | | 1.5 | 1.75 | mA |
| | | $I_O$ = 0 mA, $V_S$ = 5.5 V, $T_A$ = –40°C to 125°C | | | 1.85 | |
| | Quiescent current per amplifier, OPA2320 and OPA2320S | $I_O$ = 0 mA, $V_S$ = 5.5 V, $T_A$ = 25°C | | 1.45 | 1.6 | mA |
| | | $I_O$ = 0 mA, $V_S$ = 5.5 V, $T_A$ = –40°C to 125°C | | | 1.7 | |
| | Power-on time | V+ = 0 V to 5 V, to 90% $I_Q$ level | | 28 | | µs |

## 6.8 Typical Characteristics

At $T_A$ = 25°C, $V_{CM}$ = $V_{OUT}$ = mid-supply, and $R_L$ = 10 kΩ (unless otherwise noted).

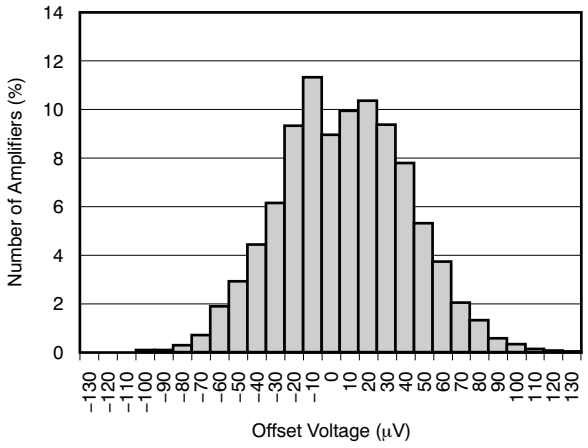



**Figure 1. Offset Voltage Production Distribution**

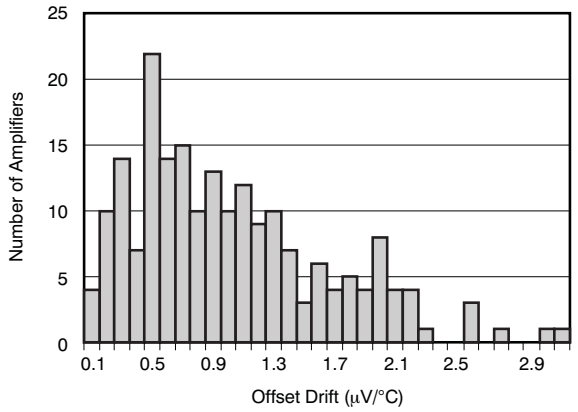



**Figure 2. Offset Voltage Drift Distribution**

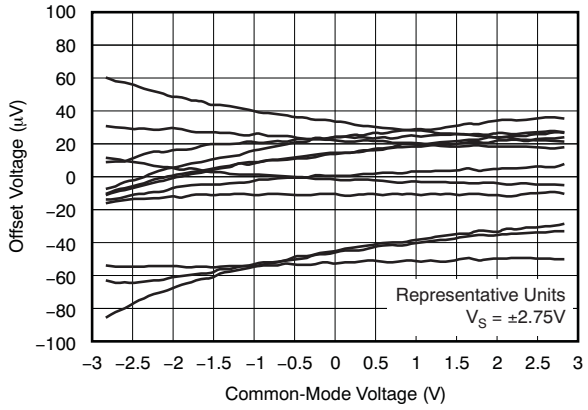



**Figure 3. Offset Voltage vs Common-Mode Voltage**

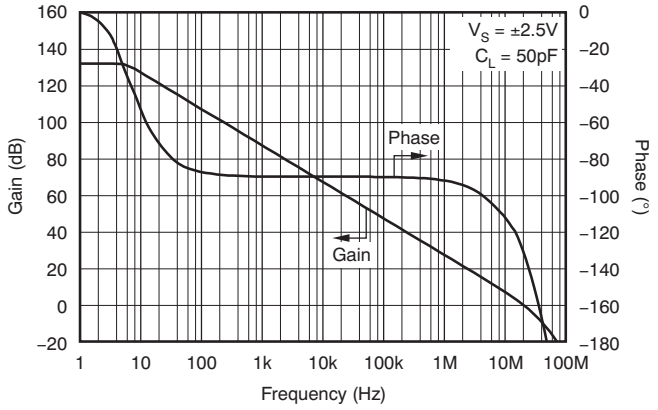



**Figure 4. Open-Loop Gain/Phase vs Frequency**

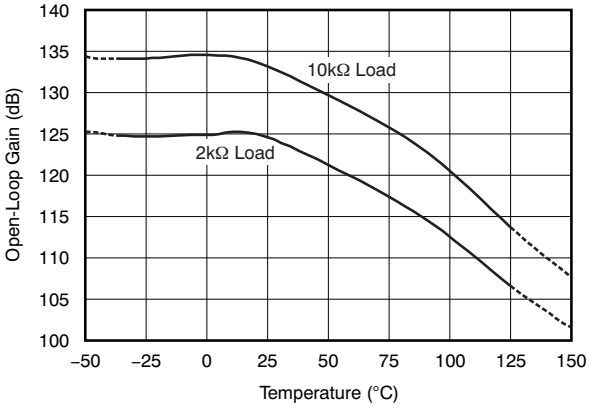



**Figure 5. Open-Loop Gain vs Temperature**

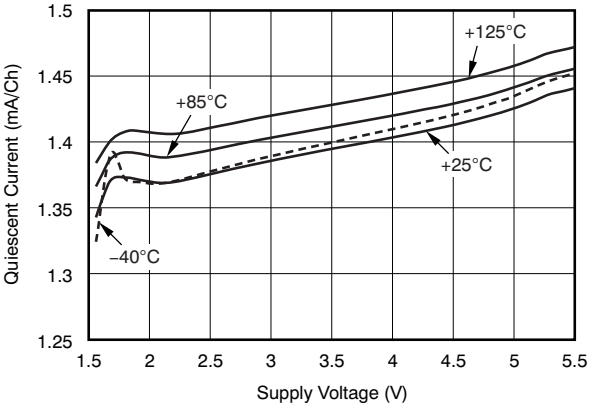



**Figure 6. Quiescent Current vs Supply Voltage**

## Typical Characteristics (continued)

At $T_A$ = 25°C, $V_{CM}$ = $V_{OUT}$ = mid-supply, and $R_L$ = 10 kΩ (unless otherwise noted).

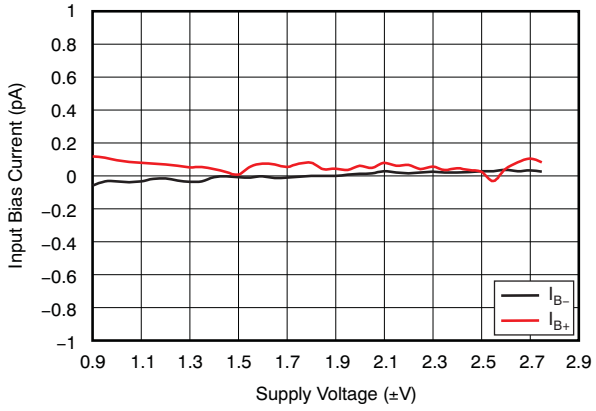



**Figure 7. Input Bias Current vs Supply Voltage**

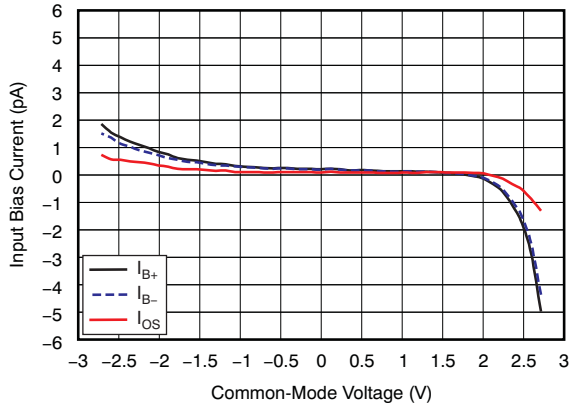



**Figure 8. Input Bias Current vs Common-Mode Voltage**

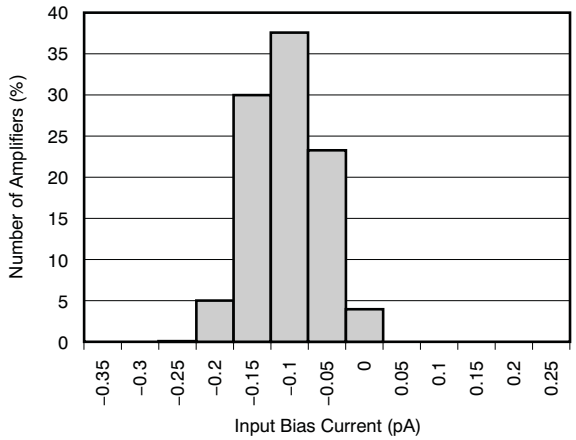



**Figure 9. Input Bias Current Distribution**

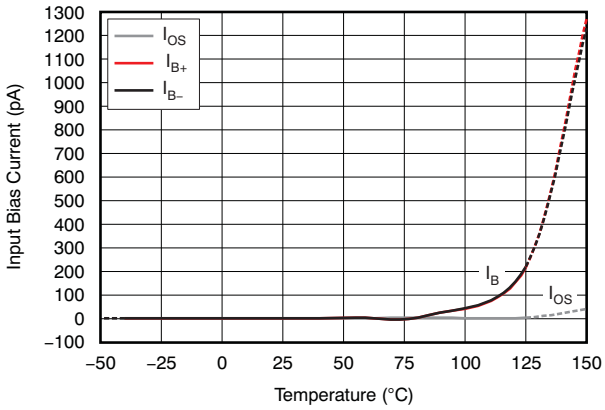



**Figure 10. Input Bias Current vs Temperature**

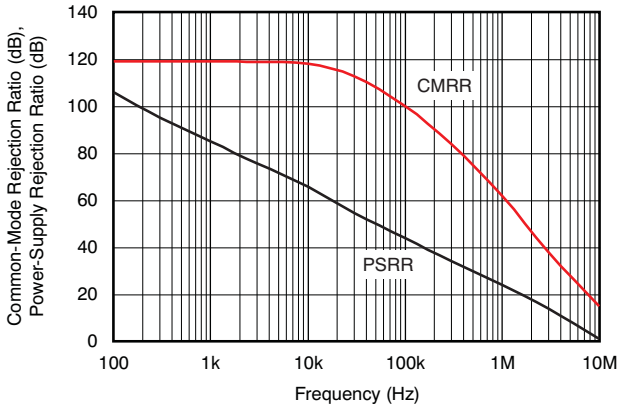



**Figure 11. CMRR and PSRR vs Frequency**

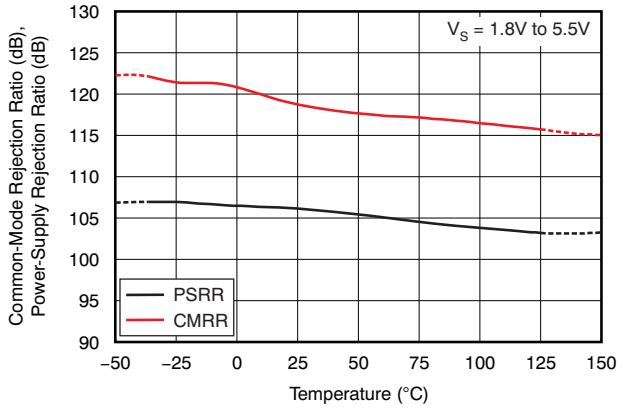



**Figure 12. CMRR and PSRR vs Temperature**

## Typical Characteristics (continued)

At $T_A$ = 25°C, $V_{CM}$ = $V_{OUT}$ = mid-supply, and $R_L$ = 10 kΩ (unless otherwise noted).

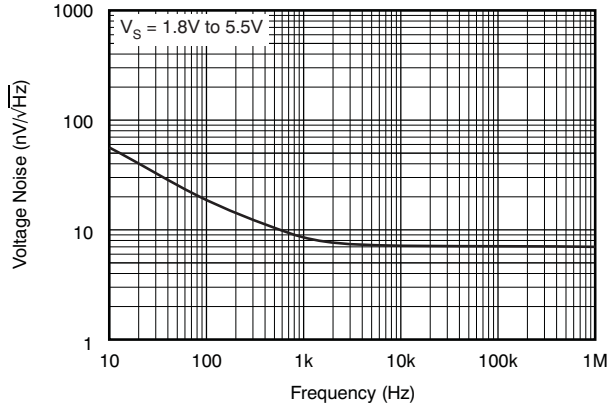



**Figure 13. Input Voltage Noise Spectral Density vs Frequency**

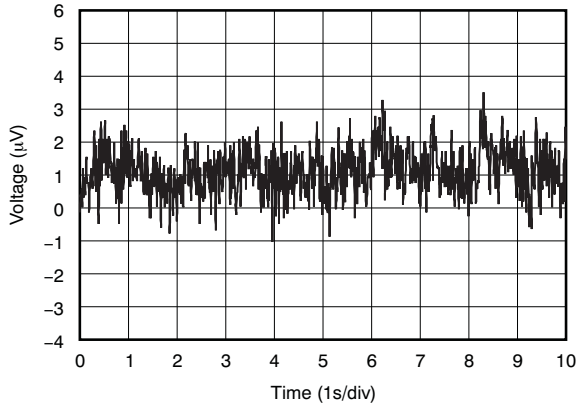



**Figure 14. 0.1-Hz to 10-Hz Input Voltage Noise**

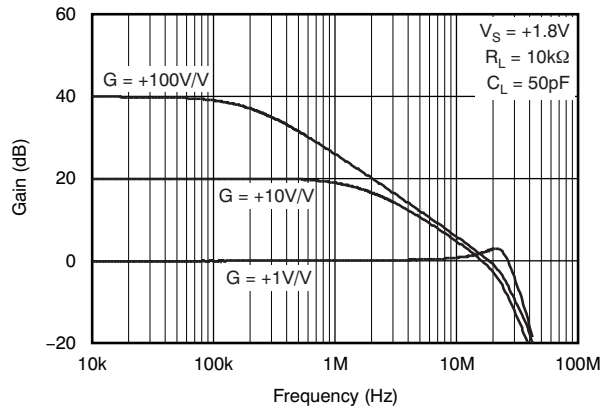



**Figure 15. Closed-Loop Gain vs Frequency**

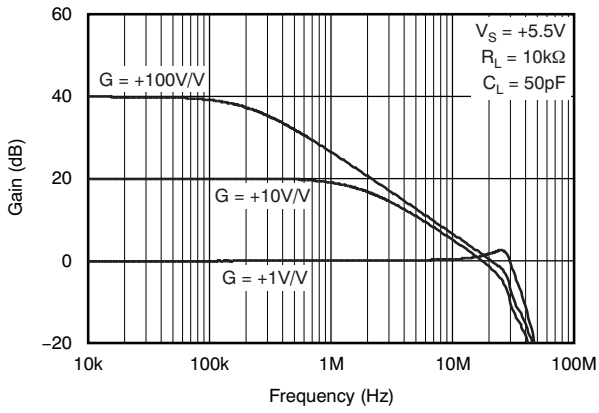



**Figure 16. Closed-Loop Gain vs Frequency**

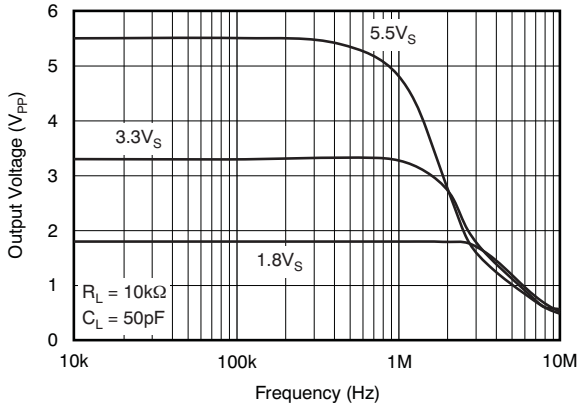



**Figure 17. Maximum Output Voltage vs Frequency**

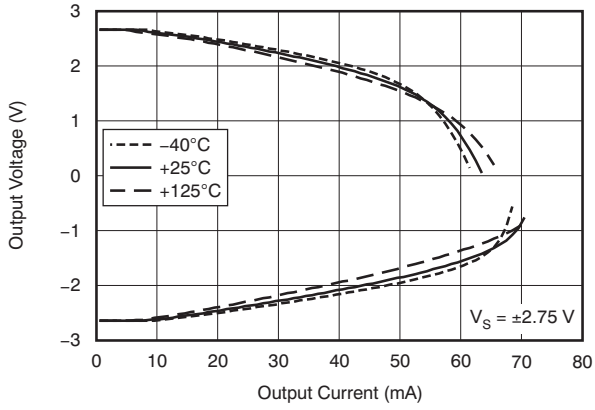



**Figure 18. Output Voltage Swing vs Output Current (8-Pin VSSOP)**

## Typical Characteristics (continued)

At $T_A$ = 25°C, $V_{CM}$ = $V_{OUT}$ = mid-supply, and $R_L$ = 10 kΩ (unless otherwise noted).

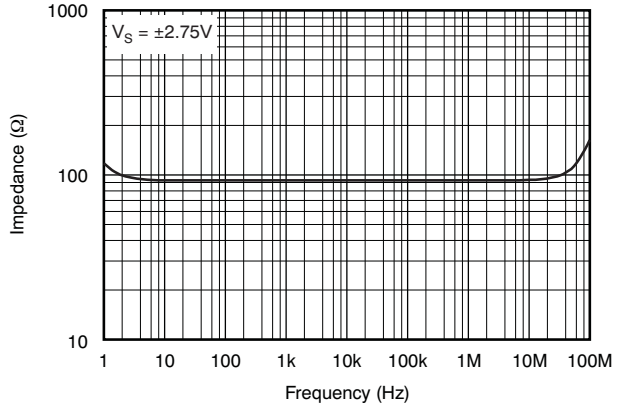



**Figure 19. Open-Loop Output Impedance vs Frequency**

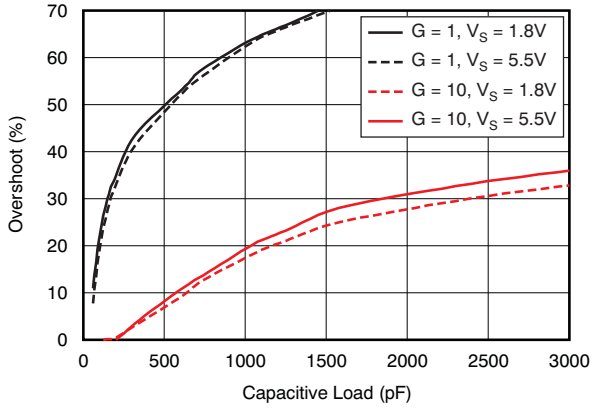



**Figure 20. Small-Signal Overshoot vs Load Capacitance**

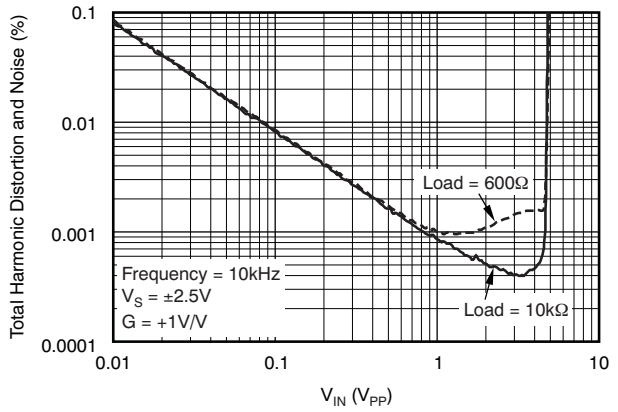



**Figure 21. THD+N vs Amplitude**

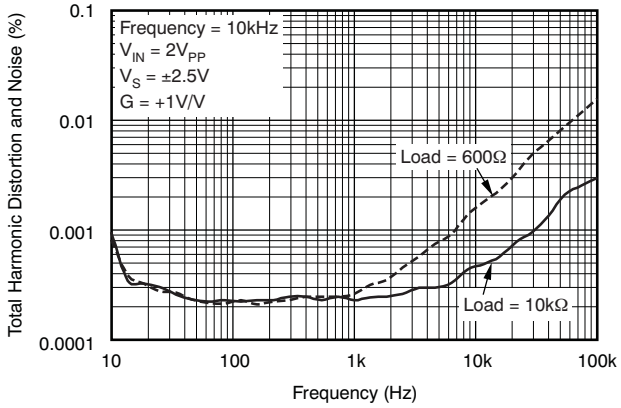



**Figure 22. THD+N vs Frequency**

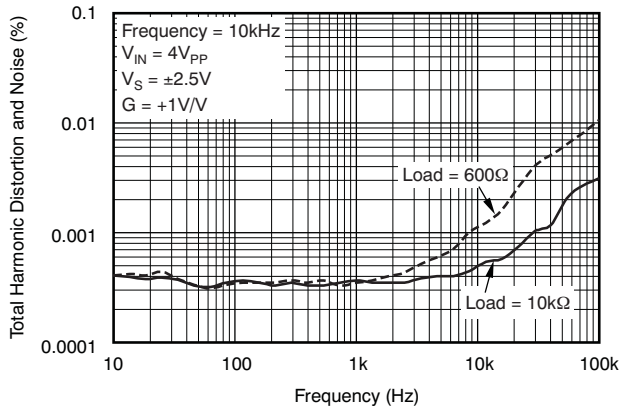



**Figure 23. THD+N vs Frequency**

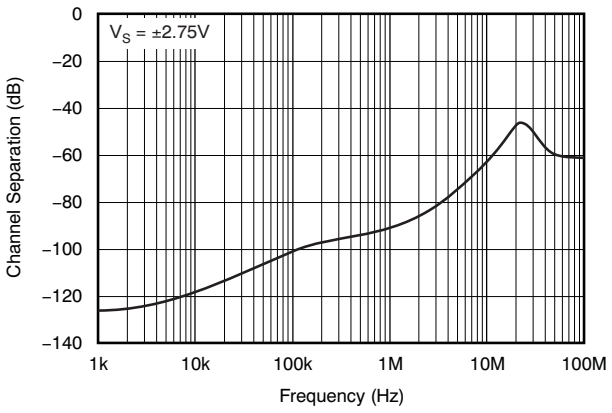



**Figure 24. Channel Separation vs Frequency (for Dual Versions)**

## Typical Characteristics (continued)

At $T_A$ = 25°C, $V_{CM}$ = $V_{OUT}$ = mid-supply, and $R_L$ = 10 kΩ (unless otherwise noted).

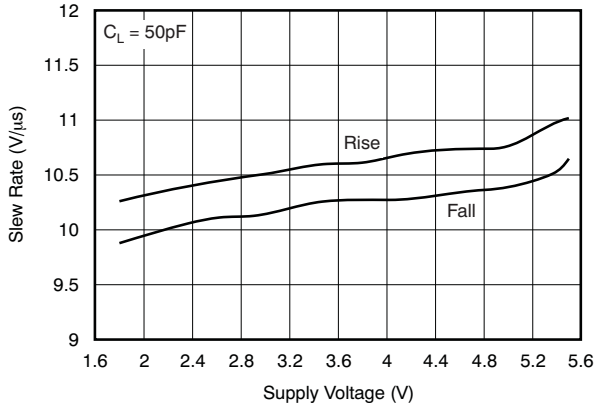



**Figure 25. Slew Rate vs Supply Voltage**

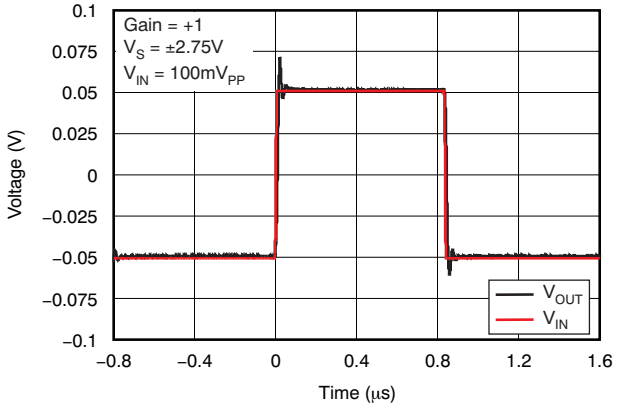



**Figure 26. Small-Signal Step Response**

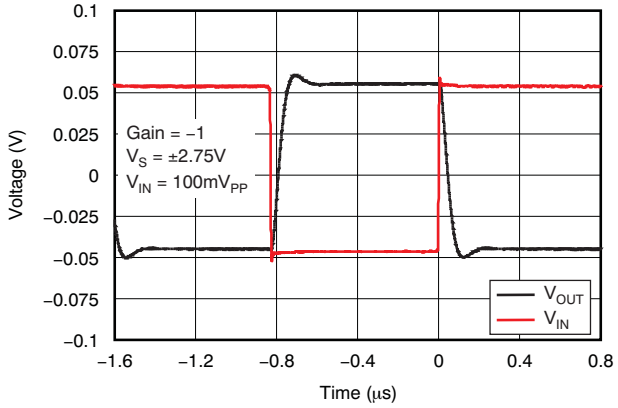



**Figure 27. Small-Signal Step Response**

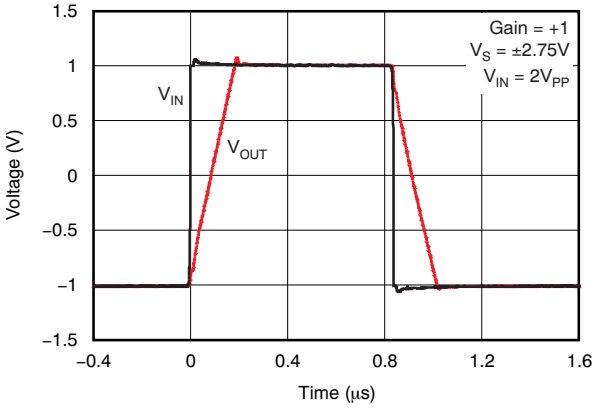



**Figure 28. Large-Signal Step Response vs Time**

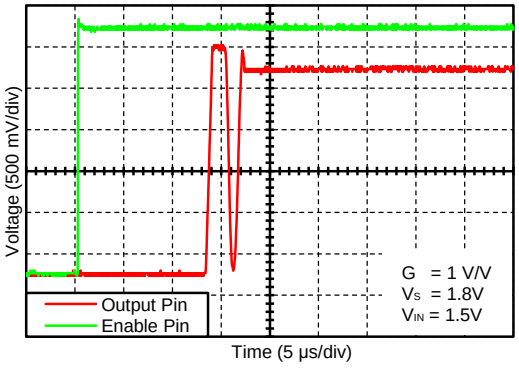



**Figure 29. Enable Start-Up**

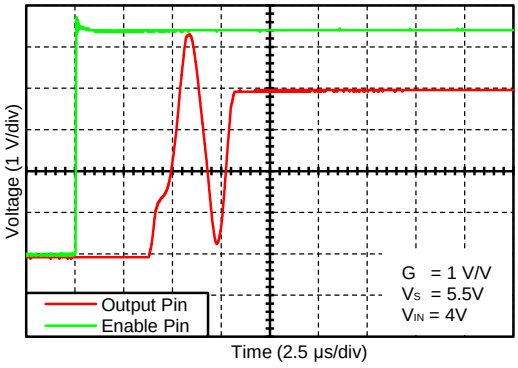



**Figure 30. Enable Start-Up**

## Typical Characteristics (continued)

At $T_A$ = 25°C, $V_{CM}$ = $V_{OUT}$ = mid-supply, and $R_L$ = 10 kΩ (unless otherwise noted).

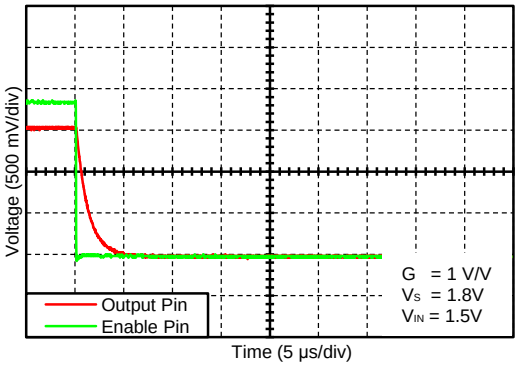



**Figure 31. Enable Shutdown**

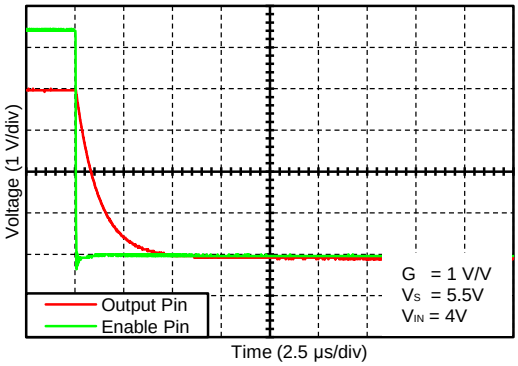


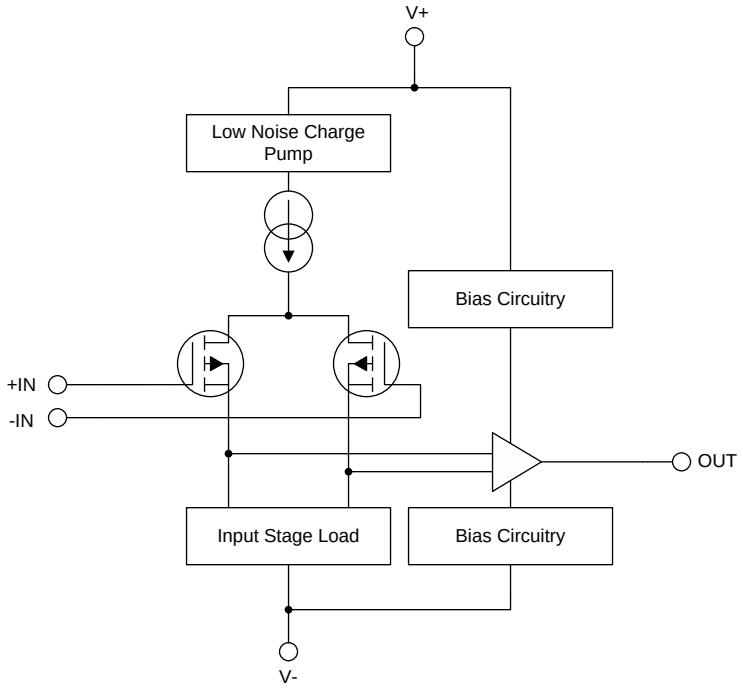

**Figure 32. Enable Shutdown**

# 7 Detailed Description

## 7.1 Overview

The OPA320 family of operational amplifiers (op amps) are high-speed, precision amplifiers, perfectly suited to drive 12-, 14-, and 16-bit analog-to-digital converters. Low output impedance with flat frequency characteristics and zero-crossover distortion circuitry enable high linearity over the full input common mode range, achieving true rail-to-rail input from a 1.8-V to 5.5-V single supply.

## 7.2 Functional Block Diagram






## 7.3 Feature Description

### 7.3.1 Operating Voltage

The OPA320 series op amps are unity-gain stable and can operate on a single-supply voltage (1.8 V to 5.5 V), or a split-supply voltage (±0.9 V to ±2.75 V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 µF to 0.1 µF). The OPA320 amplifiers are fully specified from 1.8 V to 5.5 V and over the extended temperature range of –40°C to 125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

## Feature Description (continued)

### 7.3.2 Input and ESD Protection

The OPA320 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, provided that the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 33 shows how a series input resistor ($R_S$) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to the minimum in noise-sensitive applications.

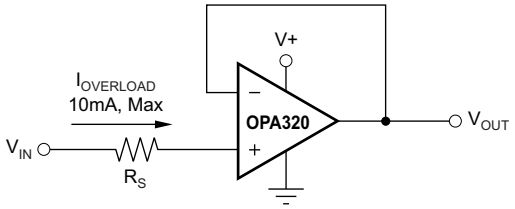





**Figure 33. Input Current Protection**

### 7.3.3 Rail-to-Rail Input

The OPA320 product family features true rail-to-rail input operation, with supply voltages as low as ±0.9 V (1.8 V). The design of the OPA320 amplifiers include an internal charge-pump that powers the amplifier input stage with an internal supply rail at approximately 1.6 V above the external supply ($V_{S+}$). This internal supply rail allows the single differential input pair to operate and remain very linear over a very wide input common mode range. A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary input stage operational amplifiers. This topology allows the OPA320 to provide superior common-mode performance (CMRR > 110 dB, typical) over the entire common-mode input range, which extends 100 mV beyond both power-supply rails. When driving analog-to-digital converters (ADCs), the highly linear $V_{CM}$ range of the OPA320 assures maximum linearity and lowest distortion.

### 7.3.4 Phase Reversal

The OPA320 op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, therefore providing further in-system stability and predictability. Figure 34 shows the input voltage exceeding the supply voltage without any phase reversal.

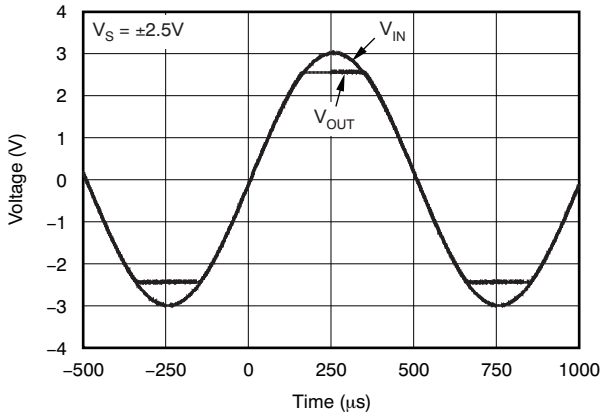
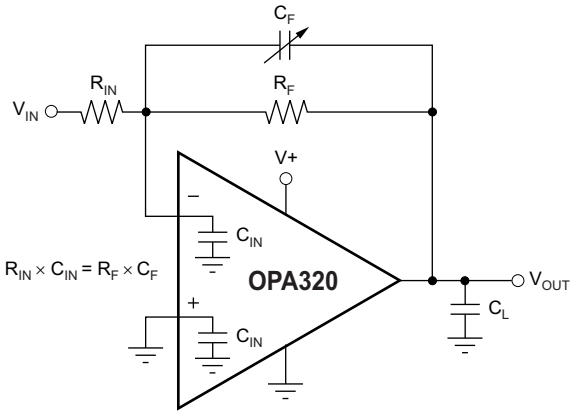



**Figure 34. No Phase Reversal**

## Feature Description (continued)

### 7.3.5 Feedback Capacitor Improves Response

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, $R_F$, as shown in Figure 35. This capacitor compensates for the zero created by the feedback network impedance and the OPA320 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.






Where $C_{IN}$ is equal to the OPA320 input capacitance (approximately 9 pF) plus any parasitic layout capacitance.

**Figure 35. Feedback Capacitor Improves Dynamic Performance**

For the circuit shown in Figure 35, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPA320 (typically 9 pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor calculated with Equation 1.

$$R_{IN} \times C_{IN} = R_F \times C_F \quad (1)$$

where

- $C_{IN}$ is equal to the OPA320 input capacitance (sum of differential and common mode) plus the layout capacitance.

The capacitor value can be adjusted until optimum performance is obtained.

### 7.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA320 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 580 MHz (–3 dB), with a roll-off of 20 dB per decade.

### 7.3.7 Output Impedance

The open-loop output impedance of the OPA320 common-source output stage is approximately 90 Ω. When the op amp is connected with feedback, this value is reduced significantly by the loop gain. For example, with 130 dB (typical) of open-loop gain, the output impedance is reduced in unity-gain to less than 0.03 Ω. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a ten-fold increase in effective output impedance. While the OPA320 output impedance remains very flat over a wide frequency range, at higher frequencies the output impedance rises as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive as a result of parasitic capacitance. This architecture in turn prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPA320 has excellent capacitive load drive capability for an op amp with its bandwidth.

## Feature Description (continued)

### 7.3.8 Capacitive Load and Stability

The OPA320 is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA320 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (1-V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA320 remains stable with a pure capacitive load up to approximately 1 nF.

The equivalent series resistance (ESR) of some very large capacitors ($C_L$ > 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 37. One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor ($R_S$), typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 36.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider may be insignificant. For instance, with a load resistance, $R_L$ = 10 kΩ and $R_S$ = 20 Ω, the gain error is only about 0.2%. However, when $R_L$ is decreased to 600 Ω, which the OPA320 is able to drive, the error increases to 7.5%.

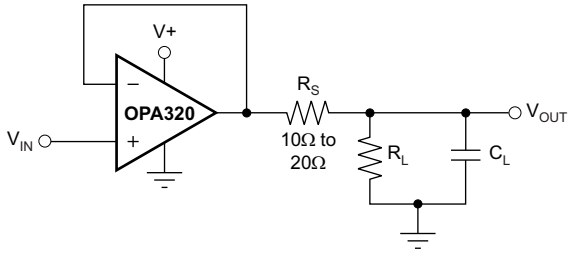





**Figure 36. Improving Capacitive Load Drive**

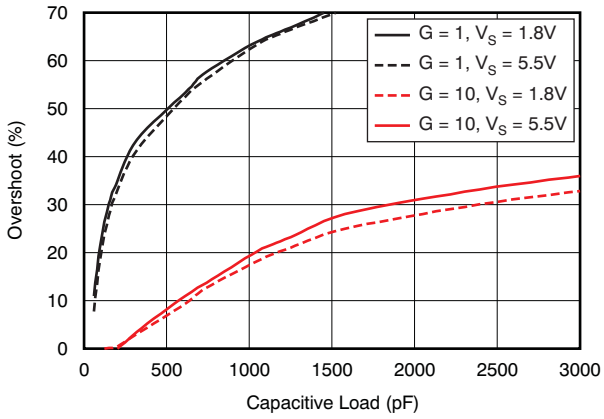



**Figure 37. Small-Signal Overshoot vs Capacitive Load (100-$mV_{PP}$ Output Step)**

## Feature Description (continued)

### 7.3.9 Overload Recovery Time

Overload recovery time is the time it takes the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications where small signals must be amplified in the presence of large transients. Figure 38 and Figure 39 show the positive and negative overload recovery times of the OPA320, respectively. In both cases, the time elapsed before the OPA320 comes out of saturation is less than 100 ns. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

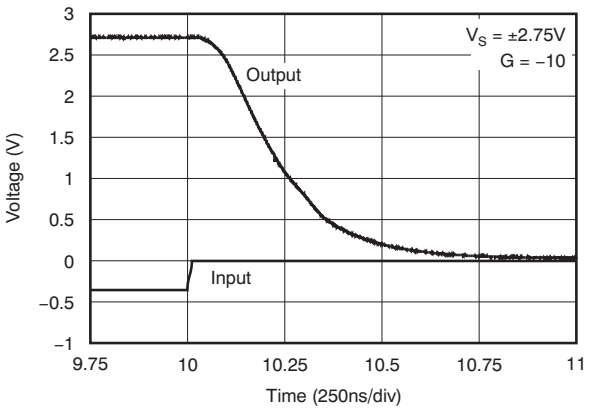



**Figure 38. Positive Recovery Time**

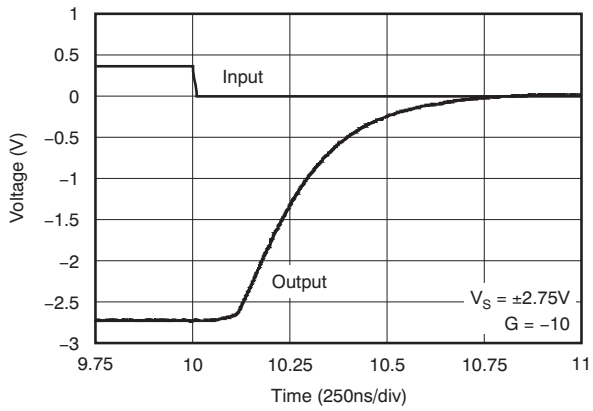



**Figure 39. Negative Recovery Time**

### 7.3.10 Shutdown Function

The SHDN (enable) pin function of the OPAx320S is referenced to the negative supply voltage of the operational amplifier. A logic level high enables the op amp. A valid logic high is defined as voltage [(V+) – 0.1 V], up to (V+), applied to the SHDN pin. A valid logic low is defined as [(V–) + 0.1 V], down to (V–), applied to the enable pin. The maximum allowed voltage applied to SHDN is 5.5 V with respect to the negative supply, independent of the positive supply voltage. This pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit.

The logic input is a high-impedance CMOS input. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 µs for full shutdown of all channels; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx320S to be operated as a *gated* amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time ($t_{OFF}$) depends on loading conditions and increases with increased load resistance. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to mid-supply ($V_S$ / 2) is required. If using the OPAx320S without a load, the resulting turn-off time is significantly increased.

### 7.3.11 Leadless SON Package

The OPA320 series uses the SON style package (also known as *SON*), which is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes printed circuit board (PCB) space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the SON package is its low height (0.8 mm).

SON packages are physically small, have a smaller routing area, improved thermal performance, reduced electrical parasitics, and a pinout scheme that is consistent with other commonly-used packages (such as SOIC and VSSOP). Additionally, the absence of external leads eliminates bent-lead issues.

The SON package can easily be mounted using standard PCB assembly techniques. See Application Report, *QFN/SON PCB Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

## Feature Description (continued)

**NOTE**

The exposed leadframe die pad on the bottom of the SON package should be connected to the most negative potential (V–).

## 7.4 Device Functional Modes

The OPA320 family of operational amplifiers are operational when power-supply voltages between 1.8 V to 5.5 V are applied. Devices with an *S* suffix have a shutdown capability. For a detailed description of the shutdown function, see *Shutdown Function*.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

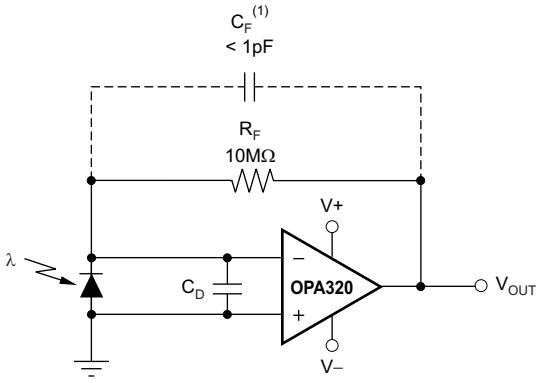
## 8.1 Application Information

The OPA320 family offers outstanding DC and AC performance. These devices operate up to a 5.5-V power supply and offer ultra-low input bias current and 20-MHz bandwidth. These features make the OPA320 family a robust operational amplifier for both battery-powered and industrial applications.

### 8.1.1 Transimpedance Amplifier

Wide gain bandwidth, low-input bias current, low input voltage, and current noise make the OPA320 an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 40, are the expected diode capacitance ($C_D$), which should include the parasitic input common mode and differential-mode input capacitance (4 pF + 5 pF for the OPA320); the desired transimpedance gain ($R_F$); and the gain-bandwidth (GBW) for the OPA320 (20 MHz). With these three variables set, the feedback capacitor value ($C_F$) can be set to control the frequency response. $C_F$ includes the stray capacitance of $R_F$, which is 0.2 pF for a typical surface-mount resistor.






(1) $C_F$ is optional to prevent gain peaking. It includes the stray capacitance of $R_F$.

**Figure 40. Dual-Supply Transimpedance Amplifier**

To achieve a maximally-flat, second-order Butterworth frequency response, the feedback pole should be set as shown in Equation 2.

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBW}{4\pi R_F C_D}} \tag{2}$$

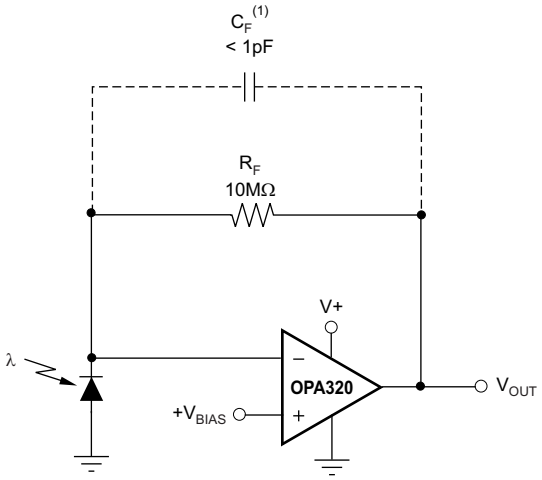
Bandwidth is calculated by Equation 3.

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi R_F C_D}} \quad \text{(Hz)} \tag{3}$$

For even higher transimpedance bandwidth, consider the high-speed CMOS OPA380 (90-MHz GBW), OPA354 (100-MHz GBW), OPA300 (180-MHz GBW), OPA355 (200-MHz GBW), or OPA656/57 (400-MHz GBW).

## Application Information (continued)

For single-supply applications, the +IN input can be biased with a positive dc voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; this configuration is shown in Figure 41. This bias voltage also appears across the photodiode, providing a reverse bias for faster operation.






(1) $C_F$ is optional to prevent gain peaking. It includes the stray capacitance of $R_F$.

**Figure 41. Single-Supply Transimpedance Amplifier**

For additional information, see the Application Bulletin *Compensate Transimpedance Amplifiers Intuitively* (SBOA055), available for download at www.ti.com.

### 8.1.2 Optimizing the Transimpedance Circuit

To achieve the best performance, components should be selected according to the following guidelines:

1. For lowest noise, select $R_F$ to create the total required gain. Using a lower value for $R_F$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_F$ increases with the square-root of $R_F$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce its capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the $R_F$ to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, refer to the Application Bulletins *Noise Analysis of FET Transimpedance Amplifiers* (SBOA060), and *Noise Analysis for High-Speed Op Amps* (SBOA066), available for download at www.ti.com.

## Application Information (continued)

### 8.1.3 High-Impedance Sensor Interface

Many sensors have high source impedances that may range up to 10 MΩ, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in Figure 42, where ($V_{IN+} = V_S – I_{BIAS} \times R_S$). The last term, $I_{BIAS} \times R_S$, shows the voltage drop across $R_S$. To prevent errors introduced to the system as a result of this voltage, an op amp with very low input bias current must be used with high impedance sensors. This low current keeps the error contribution by $I_{BIAS} \times R_S$ less than the input voltage noise of the amplifier, so that it does not become the dominant noise factor. The OPA320 series of op amps feature very low input bias current (typically 200 fA), and are therefore ideal choices for such applications.

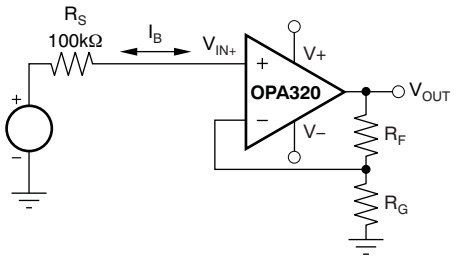



**Figure 42. Noise as a Result of $I_{BIAS}$**

### 8.1.4 Driving ADC'S

The OPA320 series op amps are well-suited for driving sampling analog-to-digital converters (ADC's) with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPA320 to drive ADC's without degradation of differential linearity and THD.

The OPA320 can be used to buffer the ADC switched input capacitance and resulting charge injection while providing signal gain. Figure 44 shows the OPA320 configured to drive the ADS8326.

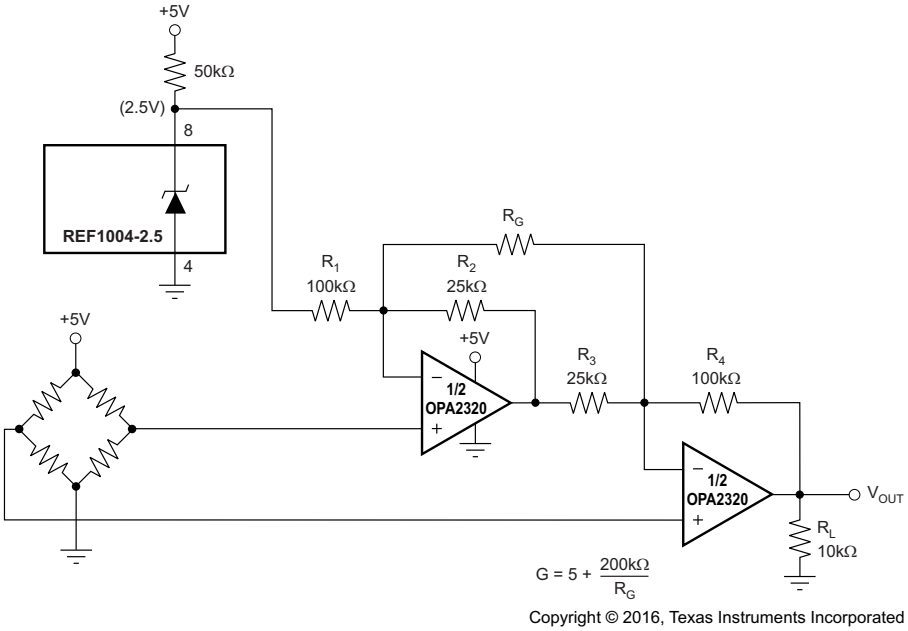
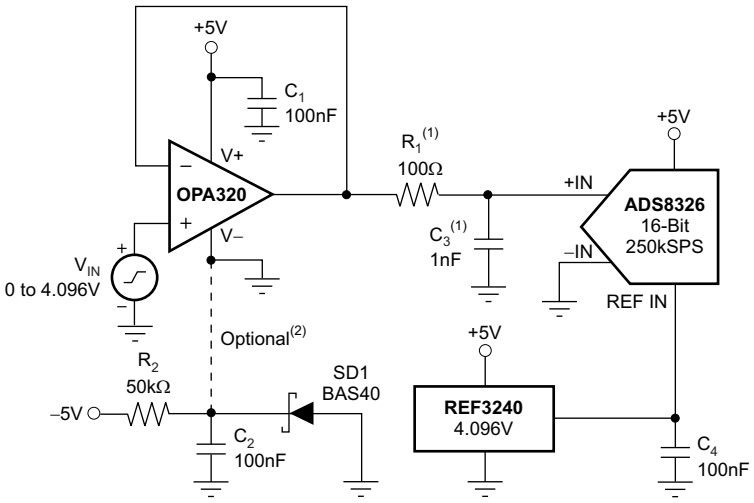





**Figure 43. Two Op Amp Instrumentation Amplifier With Improved High-Frequency Common-Mode Rejection**

## Application Information (continued)




(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a –0.3-V supply to allow output swing to true ground potential.

**Figure 44. Driving the ADS8326**

### 8.1.5 Active Filter

The OPA320 is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 45 shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is ideal for applications requiring predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options:

1. Adding an inverting amplifier;
2. Adding an additional second-order MFB stage; or
3. Using a noninverting filter topology, such as the Sallen-Key (shown in Figure 46).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.

## Application Information (continued)

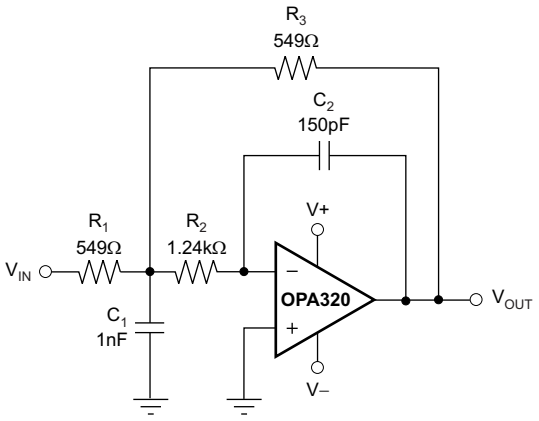





**Figure 45. Second-Order, Butterworth, 500-kHz, Low-Pass Filter**

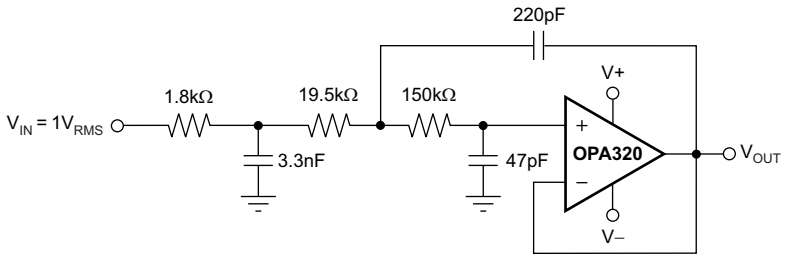





**Figure 46. OPA320 Configured as a Three-Pole, 20-kHz Sallen-Key Filter**

## 8.2 Typical Application

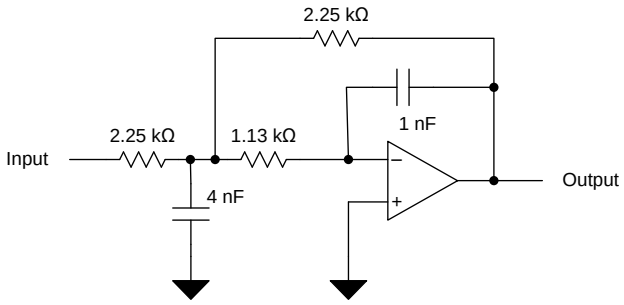



**Figure 47. Second-Order, Low-Pass Filter Schematic**

### 8.2.1 Design Requirements

- Gain = 1 V/V
- Low-pass cutoff frequency = 50 kHz
- –40-db/dec filter response
- Maintain less than 3-dB gain peaking in the gain versus frequency response

## Typical Application (continued)

### 8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in. Use Equation 4 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (4)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the lowpass cutoff frequency are calculated by Equation 5.

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (5)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

### 8.2.3 Application Curve

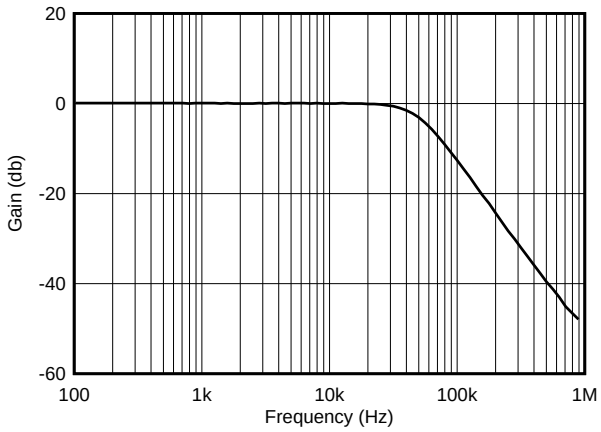



**Figure 48. OPA320 Second-Order, 50-kHz, Low-Pass Filter**

# 9 Power Supply Recommendations

The OPA320 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

**CAUTION**

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

# 10 Layout

## 10.1 Layout Guidelines

The OPA320 is a wideband amplifier. To realize the full operational performance of the device, good high-frequency PCB layout practices are required. The bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

## 10.2 Layout Example

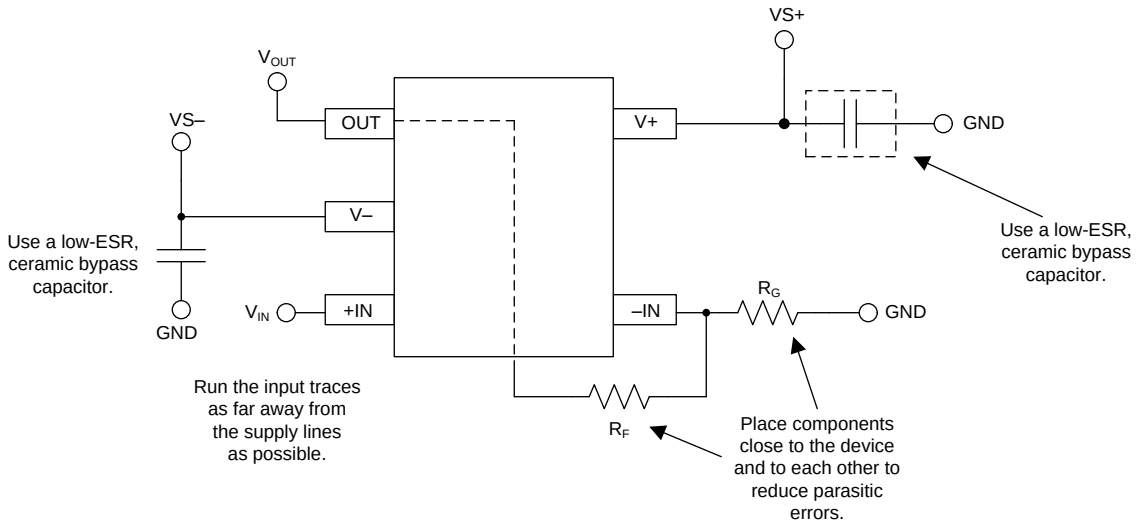





**Figure 49. Layout Example**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### *11.1.1.1 TINA-TI™ (Free Software Download)*

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

**NOTE**

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

#### *11.1.1.2 DIP Adapter EVM*

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (8-pin SOIC), PW (8-pin TSSOP), DGK (8-pin VSSOP), DBV (6-pin SOT-23, 5-pin SOT23, and 3-pin SOT-23), DCK (6-pin SC-70 and 5-pin SC-70), and DRL (6-pin SOT-563). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

#### *11.1.1.3 Universal Op Amp EVM*

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP and SOT-23 packages are all supported.

**NOTE**

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

#### *11.1.1.4 TI Precision Designs*

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

#### *11.1.1.5 WEBENCH® Filter Designer*

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

The following documents are relevant to using the OPAx320 and OPAx320S, and recommended for reference. All are available for download at www.ti.com (unless otherwise noted):

- *OPA320, OPA320S, OPA2320, OPA2320S EMI Immunity Performance* (SBOZ017)
- *Software Pacemaker Detection Design Guide* (TIDUB75)
- *TIDA-00378 Schematic and Block Diagram* (TIDRJ21)
- *PM2.5/PM10 Particle Sensor Analog Front-End for Air Quality Monitoring Design* (TIDUB65)
- *QFN/SON PCB Attachment* (SLUA271)
- *Quad Flatpack No-Lead Logic Packages* (SCBA017)
- *Compensate Transimpedance Amplifiers Intuitively* (SBOA055)
- *Noise Analysis of FET Transimpedance Amplifiers* (SBOA060)
- *Noise Analysis for High-Speed Op Amps* (SBOA066)

## 11.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| OPA320 | Click here | Click here | Click here | Click here | Click here |
| OPA2320 | Click here | Click here | Click here | Click here | Click here |
| OPA320S | Click here | Click here | Click here | Click here | Click here |
| OPA2320S | Click here | Click here | Click here | Click here | Click here |

## 11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.5 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.6 Trademarks

FilterPro, TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

## 11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2320AID | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | O2320A | Samples |
| OPA2320AIDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | Call TI \| NIPDAUAG \| NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OCLQ | Samples |
| OPA2320AIDGKT | ACTIVE | VSSOP | DGK | 8 | 250 | RoHS & Green | Call TI \| NIPDAUAG \| NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OCLQ | Samples |
| OPA2320AIDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | O2320A | Samples |
| OPA2320AIDRGR | ACTIVE | SON | DRG | 8 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OCMQ | Samples |
| OPA2320AIDRGT | ACTIVE | SON | DRG | 8 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OCMQ | Samples |
| OPA2320SAIDGSR | ACTIVE | VSSOP | DGS | 10 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPAI | Samples |
| OPA2320SAIDGST | ACTIVE | VSSOP | DGS | 10 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OPAI | Samples |
| OPA320AIDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RAC | Samples |
| OPA320AIDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RAC | Samples |
| OPA320SAIDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RAE | Samples |
| OPA320SAIDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | RAE | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF OPA2320, OPA320 :**

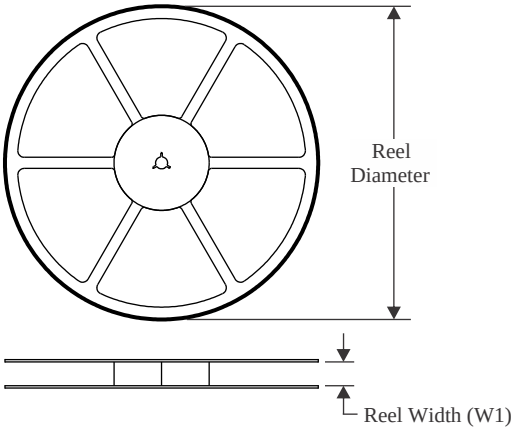
- Automotive : OPA2320-Q1, OPA320-Q1

NOTE: Qualified Version Definitions:

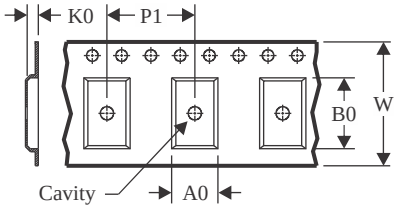
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

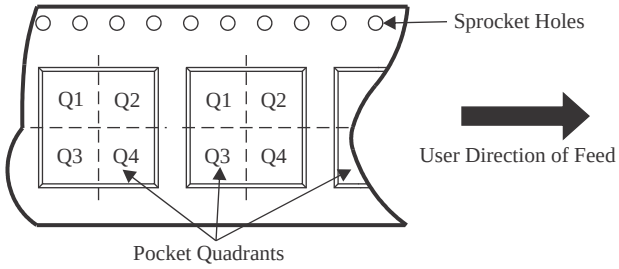



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

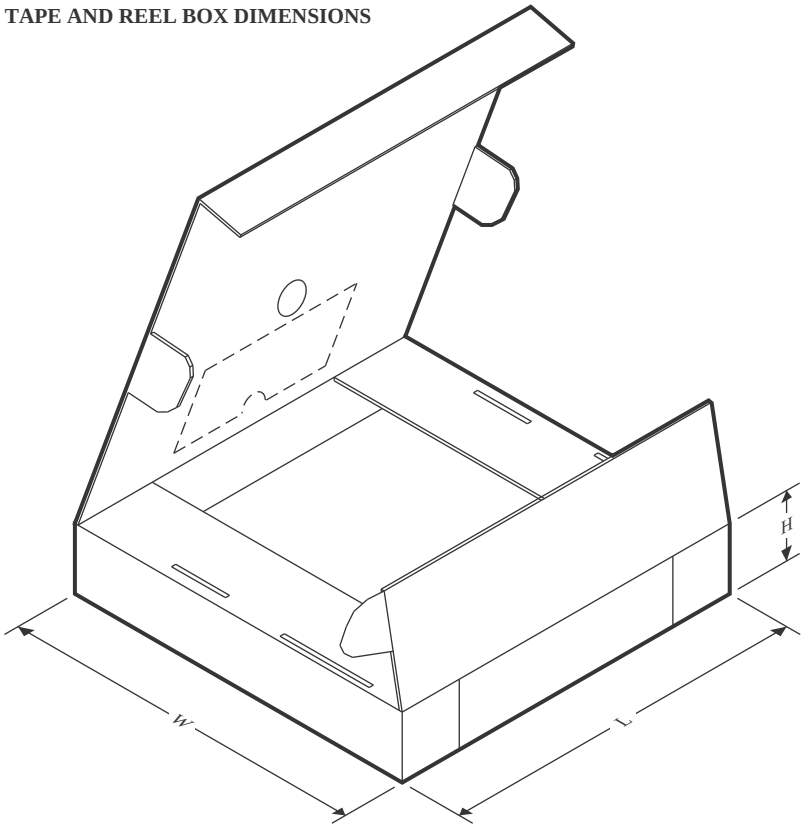
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2320AIDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2320AIDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2320AIDGKT | VSSOP | DGK | 8 | 250 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2320AIDGKT | VSSOP | DGK | 8 | 250 | 177.8 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2320AIDGKT | VSSOP | DGK | 8 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2320AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA2320AIDRGR | SON | DRG | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| OPA2320AIDRGT | SON | DRG | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| OPA2320SAIDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2320SAIDGST | VSSOP | DGS | 10 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA320AIDBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA320AIDBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA320SAIDBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 8.4 | 3.15 | 3.1 | 1.55 | 4.0 | 8.0 | Q3 |

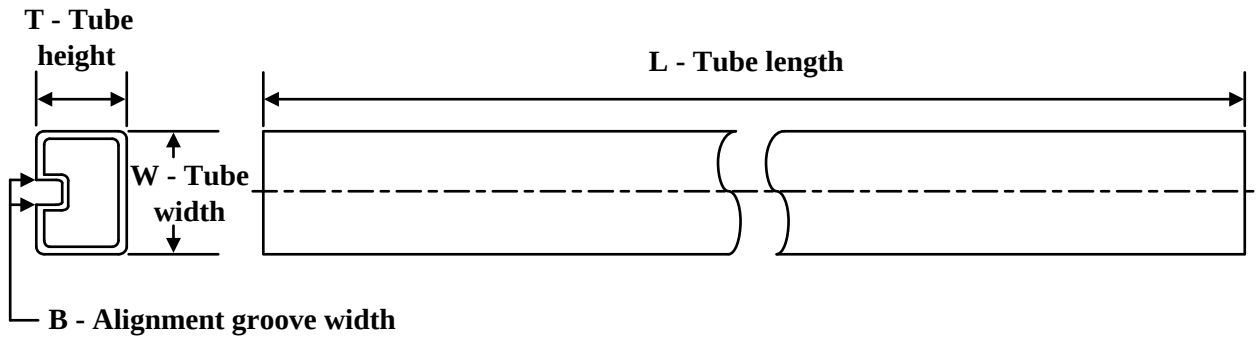
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA2320AIDGKR | VSSOP | DGK | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| OPA2320AIDGKR | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| OPA2320AIDGKT | VSSOP | DGK | 8 | 250 | 366.0 | 364.0 | 50.0 |
| OPA2320AIDGKT | VSSOP | DGK | 8 | 250 | 202.0 | 201.0 | 28.0 |
| OPA2320AIDGKT | VSSOP | DGK | 8 | 250 | 210.0 | 185.0 | 35.0 |
| OPA2320AIDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| OPA2320AIDRGR | SON | DRG | 8 | 3000 | 356.0 | 356.0 | 35.0 |
| OPA2320AIDRGT | SON | DRG | 8 | 250 | 210.0 | 185.0 | 35.0 |
| OPA2320SAIDGSR | VSSOP | DGS | 10 | 2500 | 356.0 | 356.0 | 35.0 |
| OPA2320SAIDGST | VSSOP | DGS | 10 | 250 | 210.0 | 185.0 | 35.0 |
| OPA320AIDBVR | SOT-23 | DBV | 5 | 3000 | 213.0 | 191.0 | 35.0 |
| OPA320AIDBVT | SOT-23 | DBV | 5 | 250 | 213.0 | 191.0 | 35.0 |
| OPA320SAIDBVT | SOT-23 | DBV | 6 | 250 | 210.0 | 185.0 | 35.0 |

## TUBE




*All dimensions are nominal

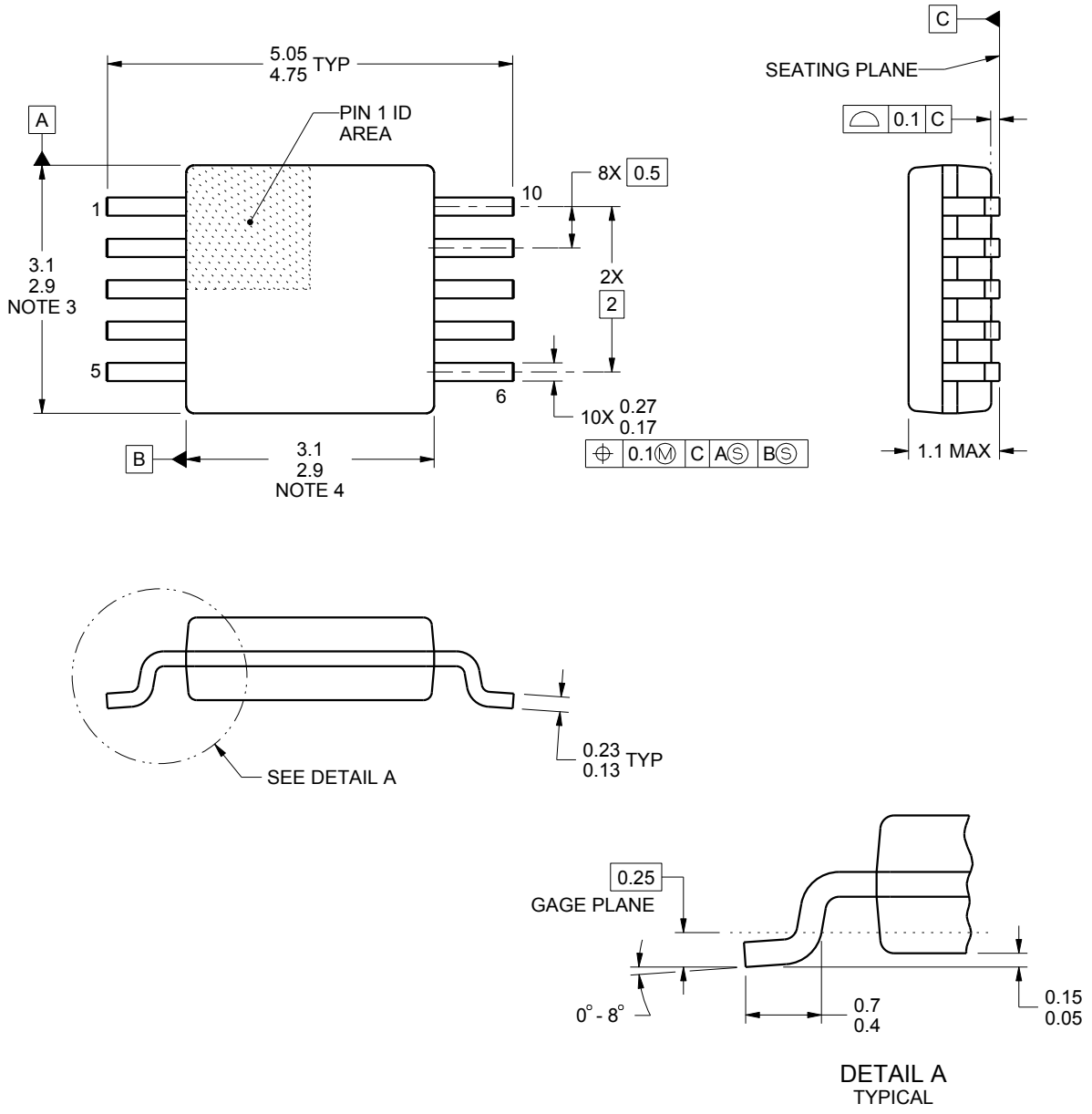
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| OPA2320AID | D | SOIC | 8 | 75 | 506.6 | 8 | 3940 | 4.32 |

# PACKAGE OUTLINE

## DGS0010A

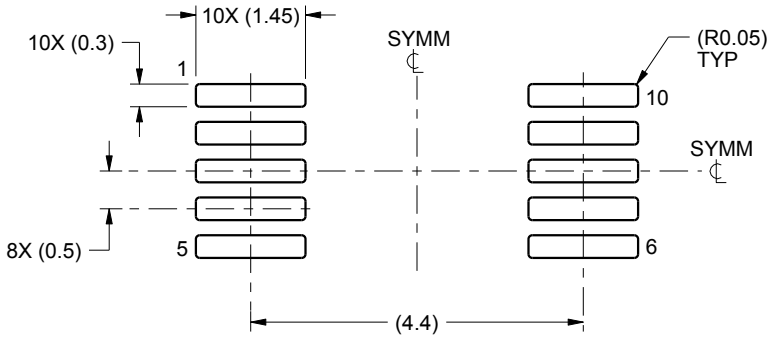
## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

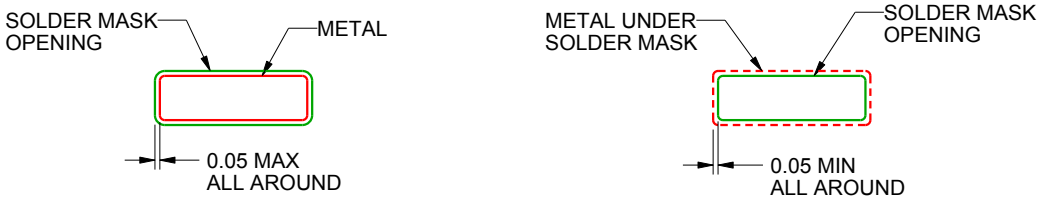



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.




LAND PATTERN EXAMPLE
SCALE:10X

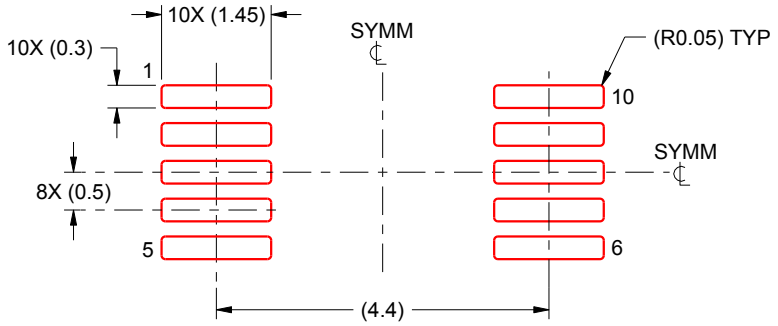



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

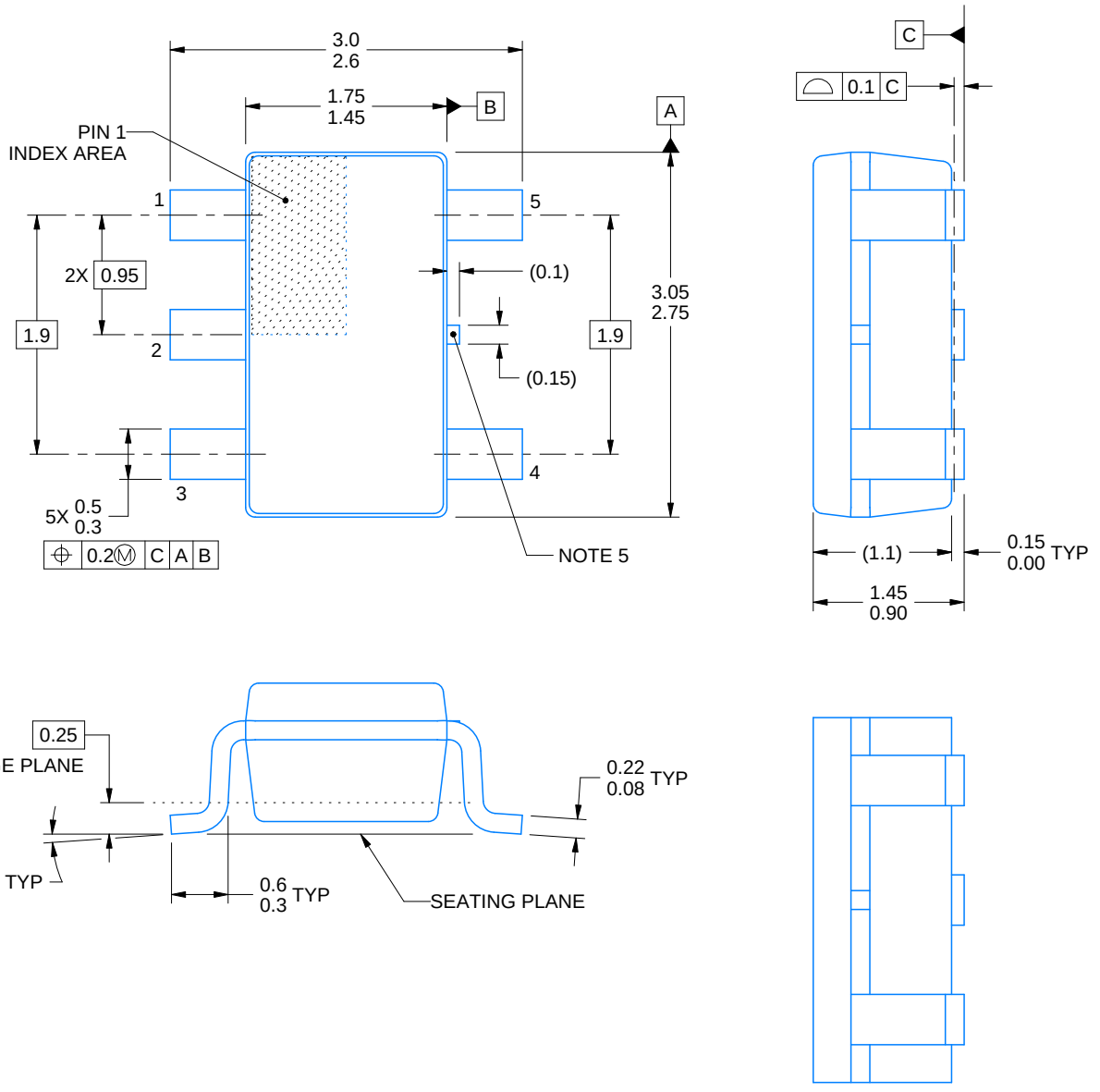
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

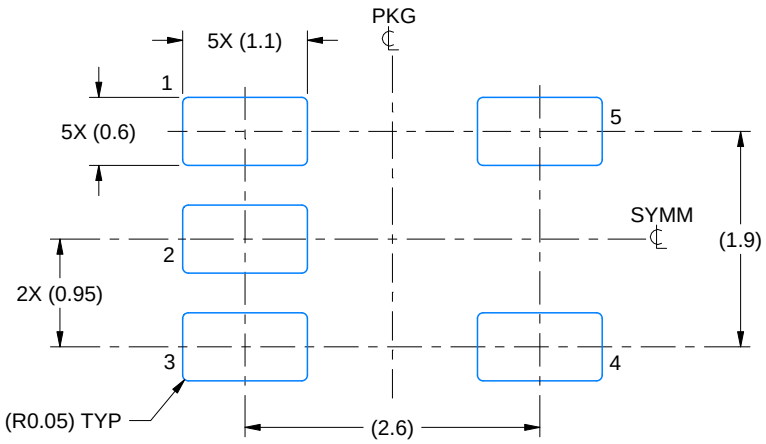



ALTERNATIVE PACKAGE SINGULATION VIEW

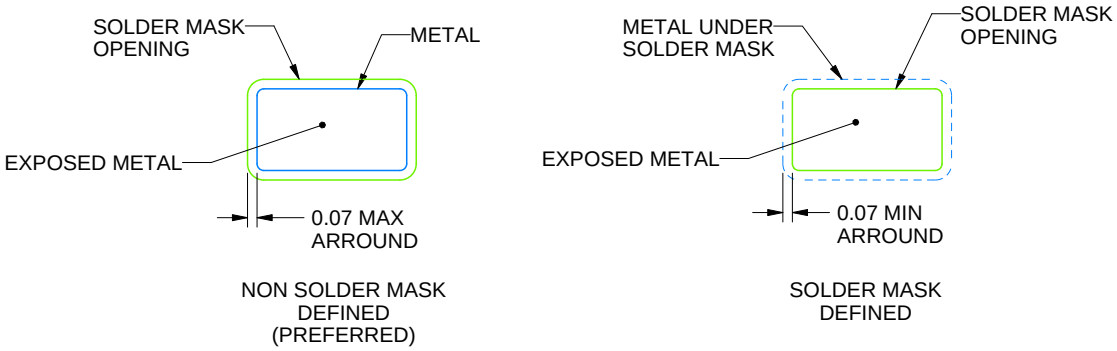
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

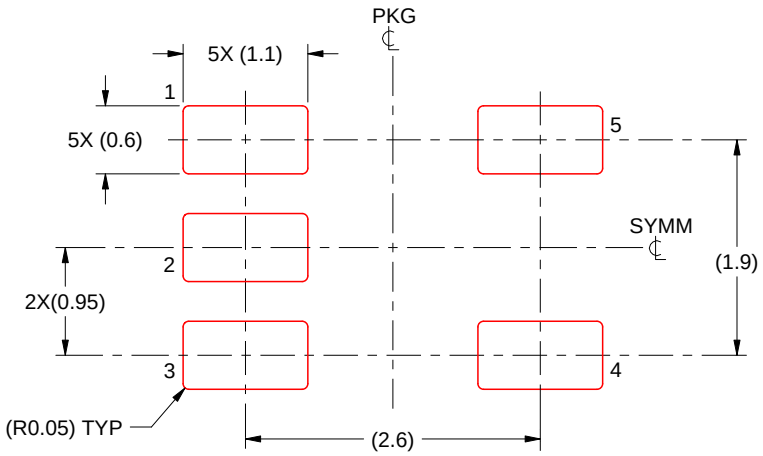



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

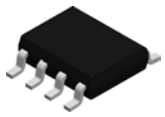



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

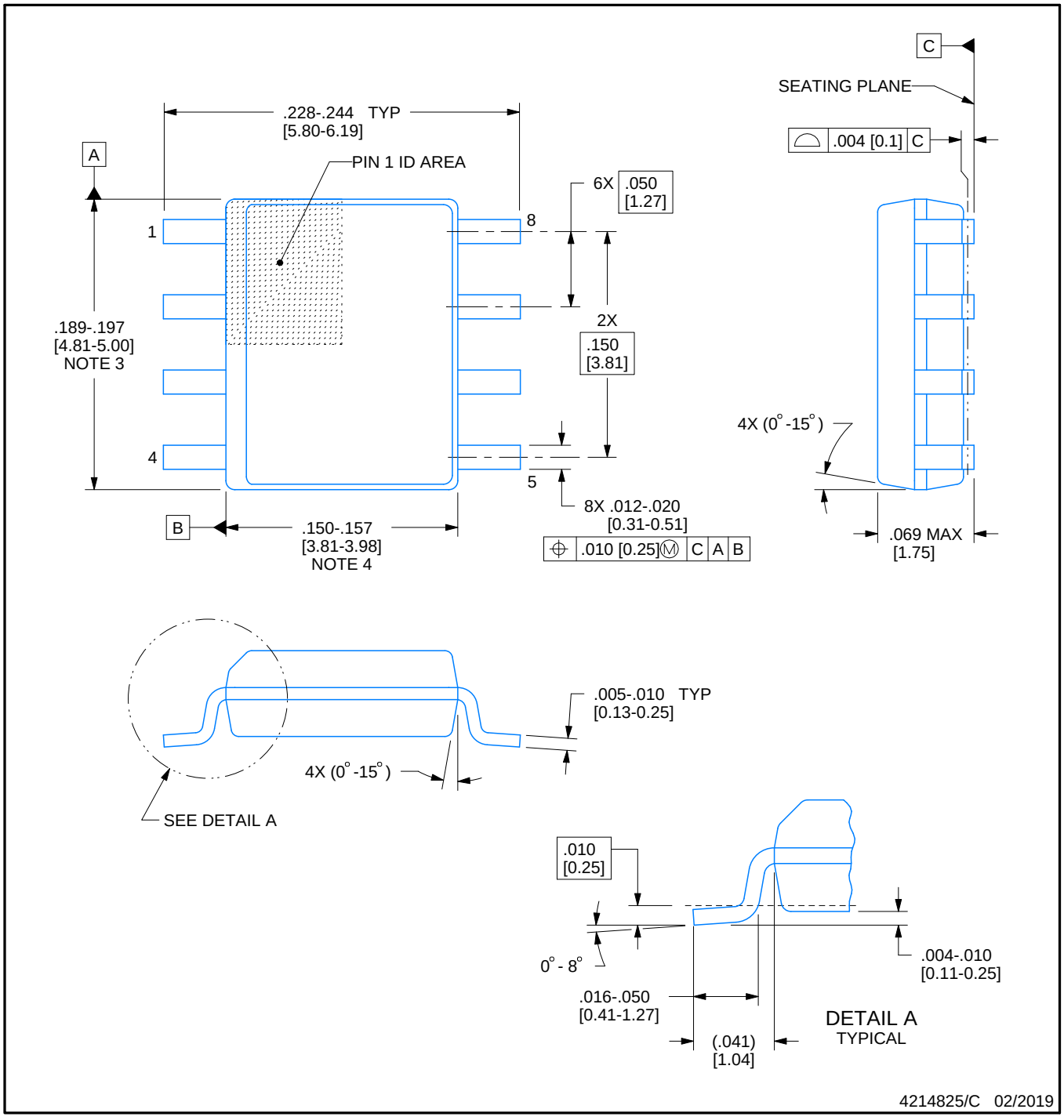


# PACKAGE OUTLINE

## D0008A

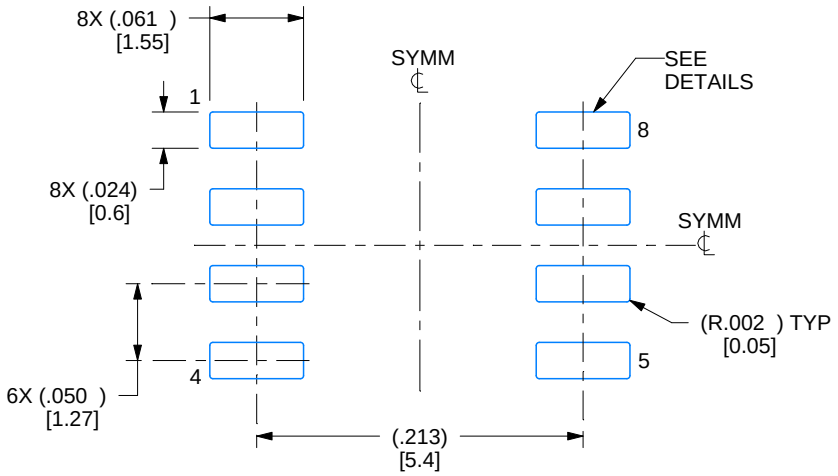
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

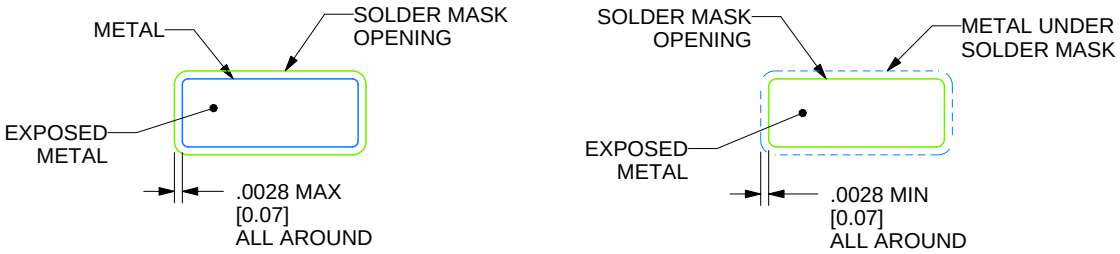



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

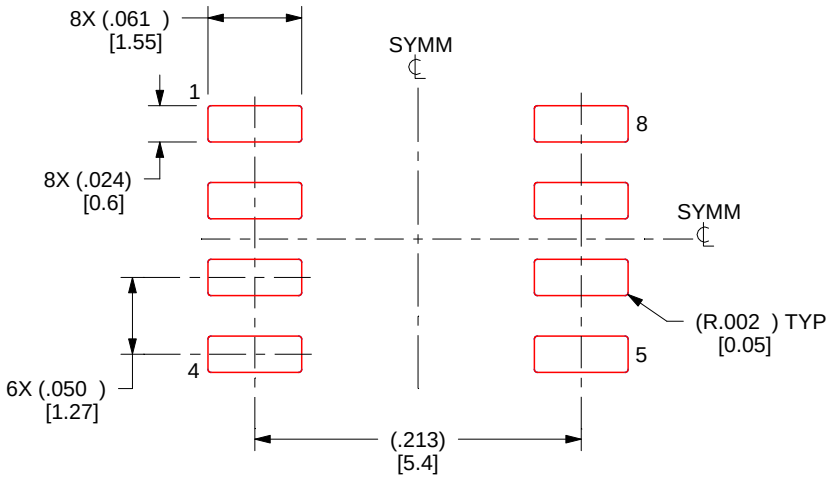
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

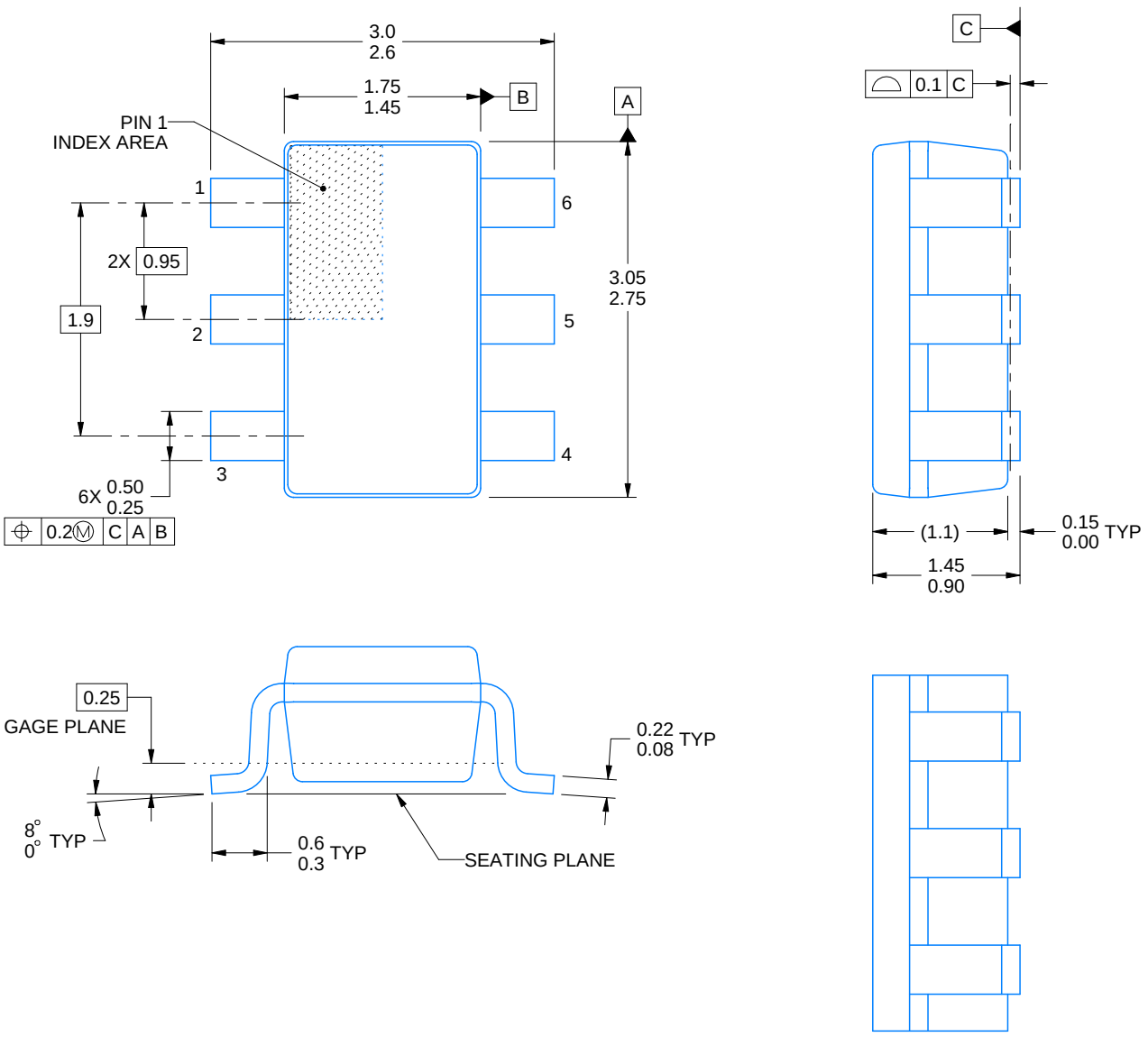
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

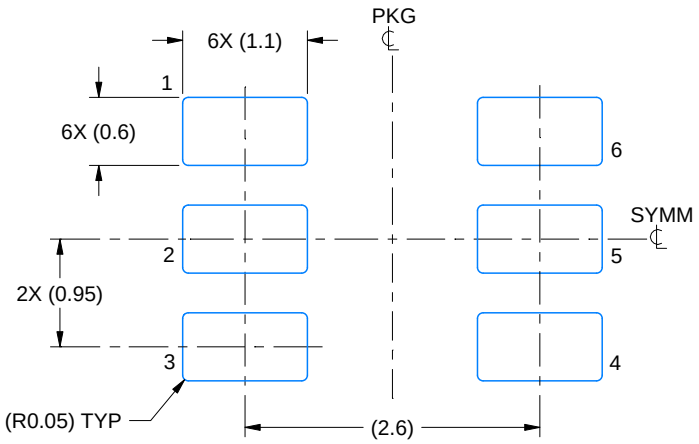



ALTERNATIVE PACKAGE SINGULATION VIEW

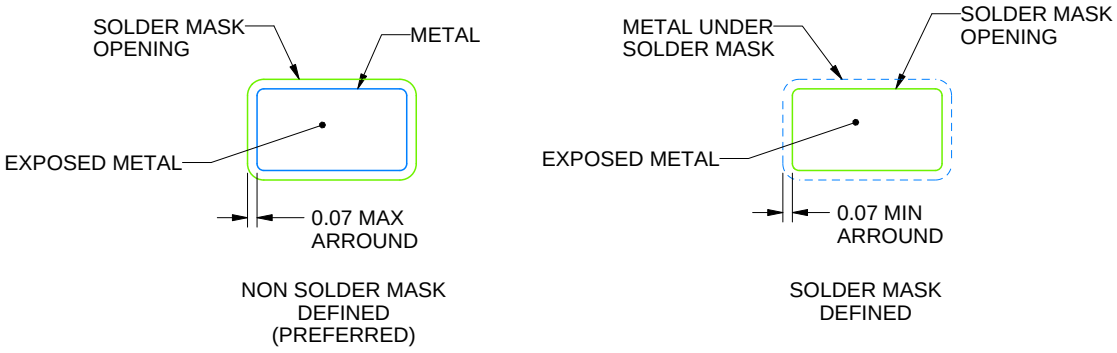
4214840/F 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

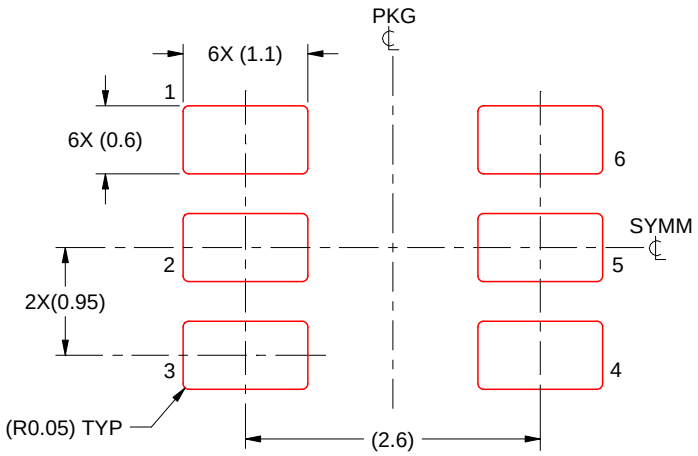



SOLDER MASK DETAILS

4214840/F 05/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



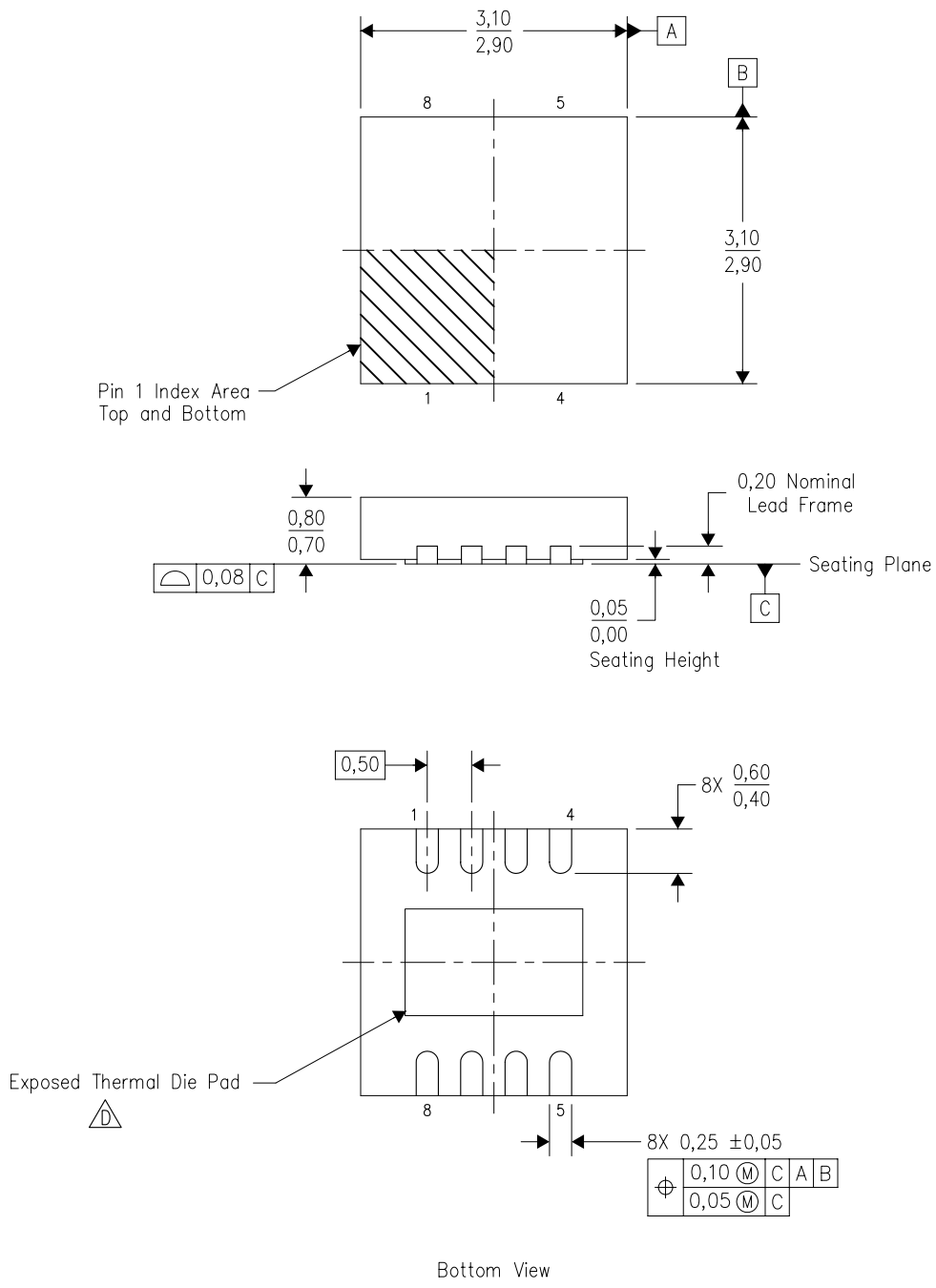

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



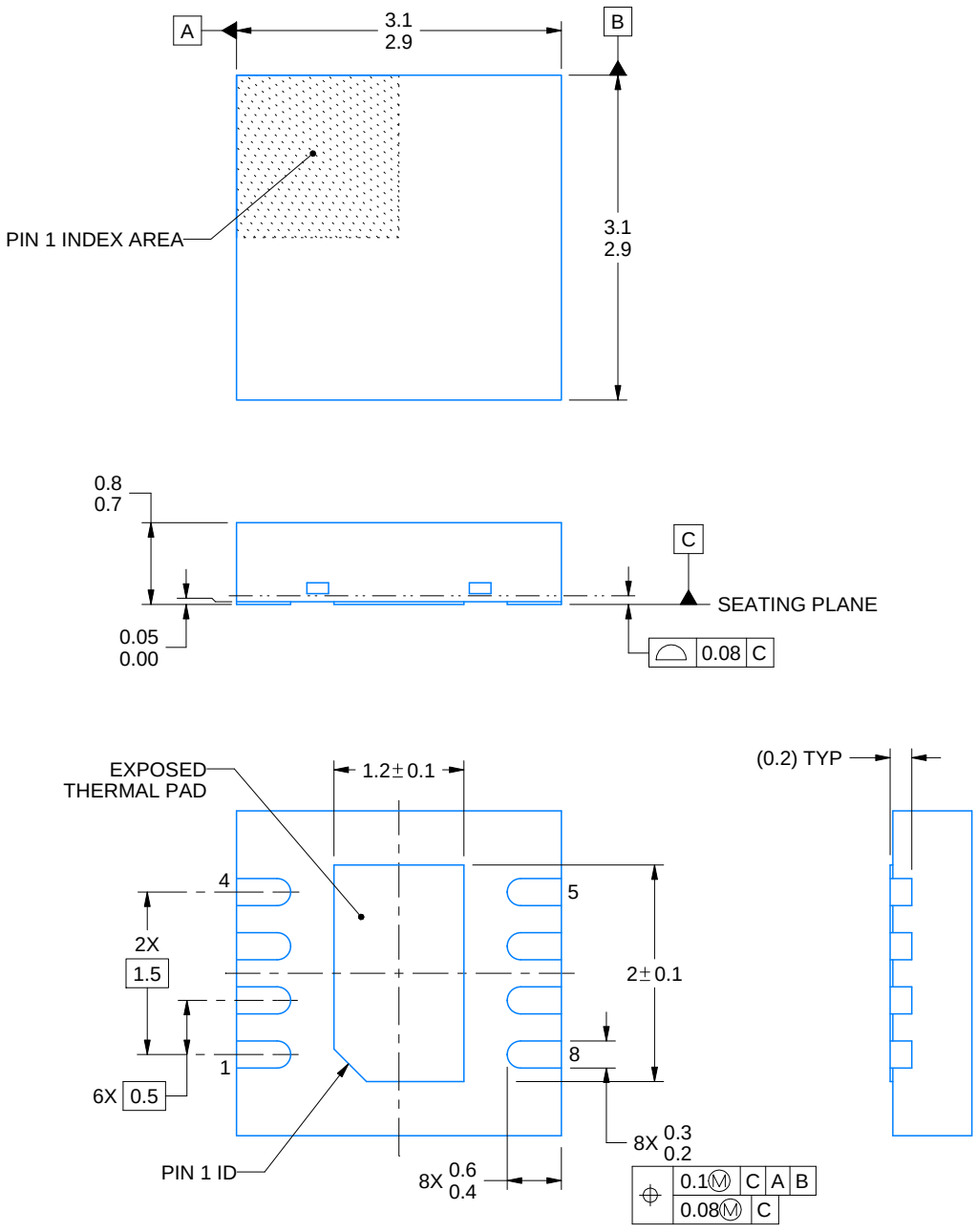

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

# PACKAGE OUTLINE

## DRG0008A

## WSON - 0.8 mm max height

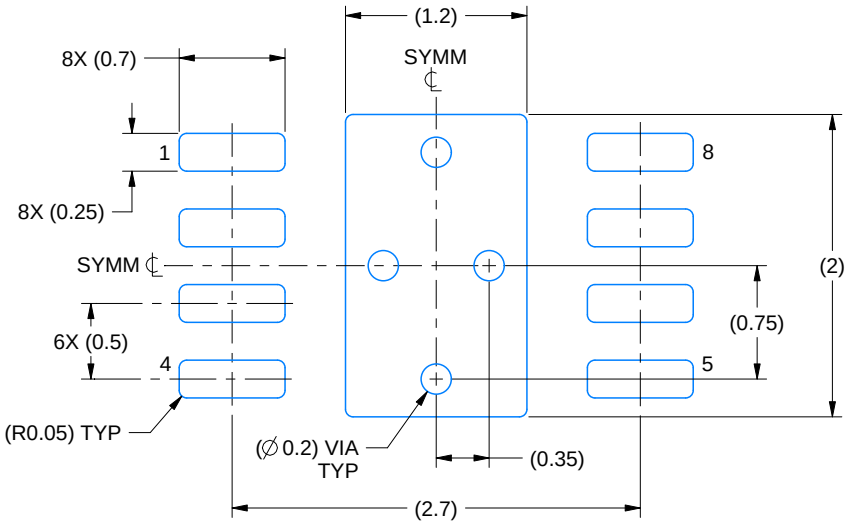
PLASTIC SMALL OUTLINE - NO LEAD



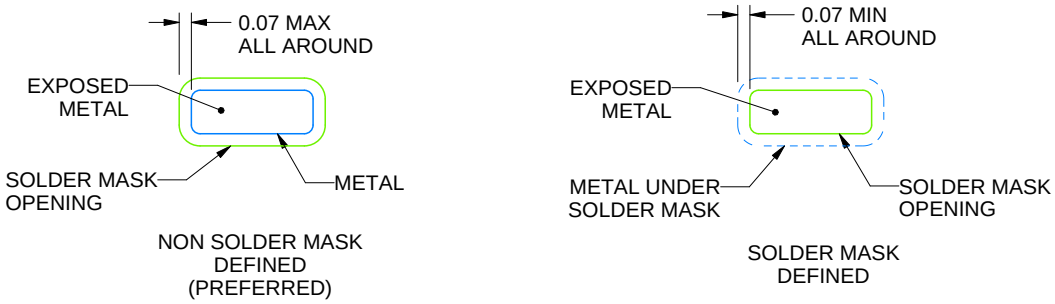

4218885/A 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

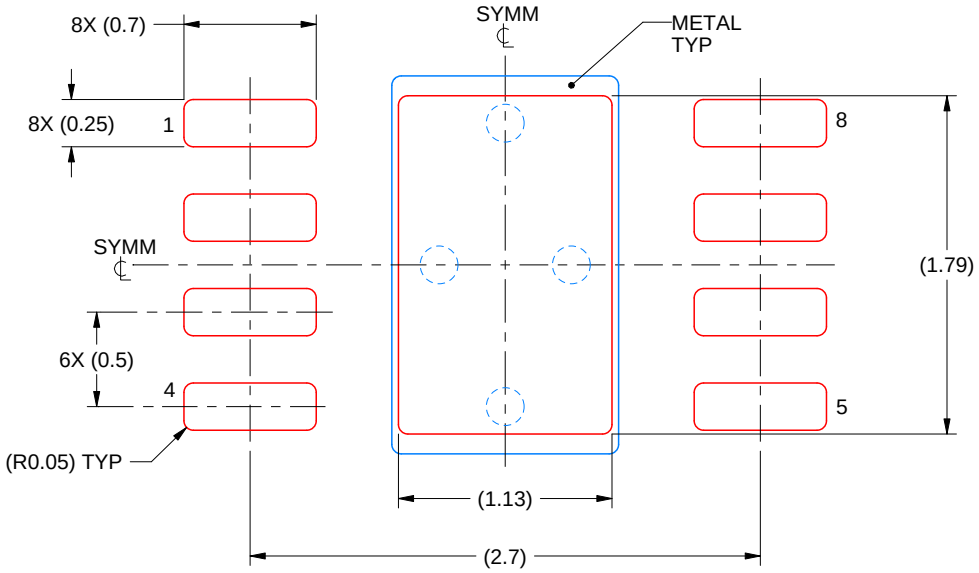



SOLDER MASK DETAILS

4218885/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

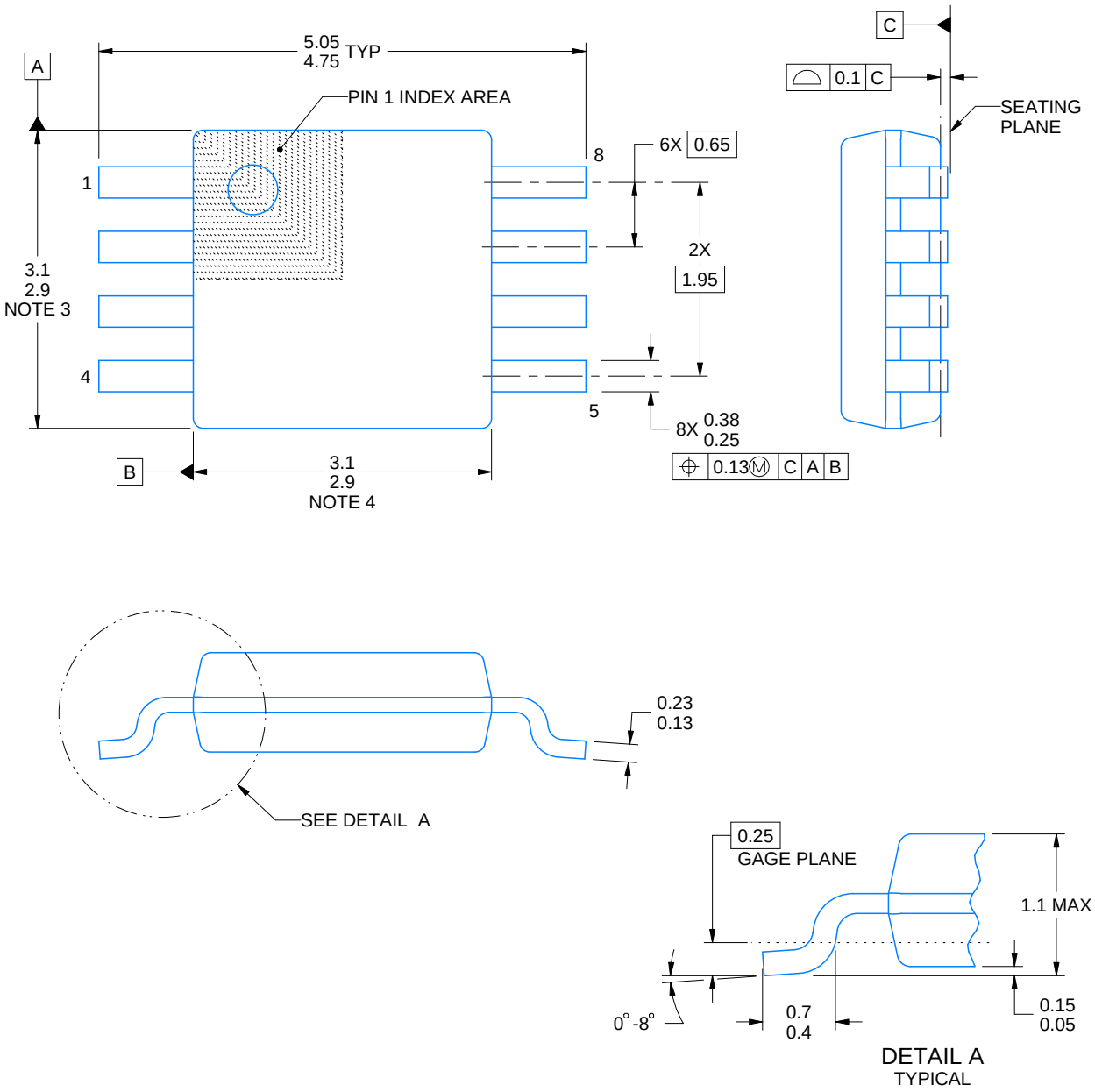
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

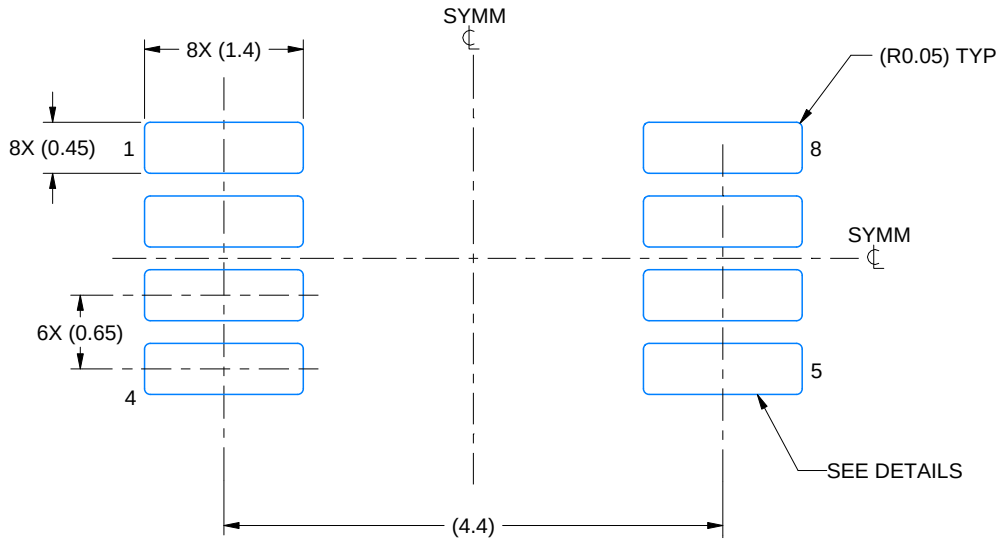
SMALL OUTLINE PACKAGE



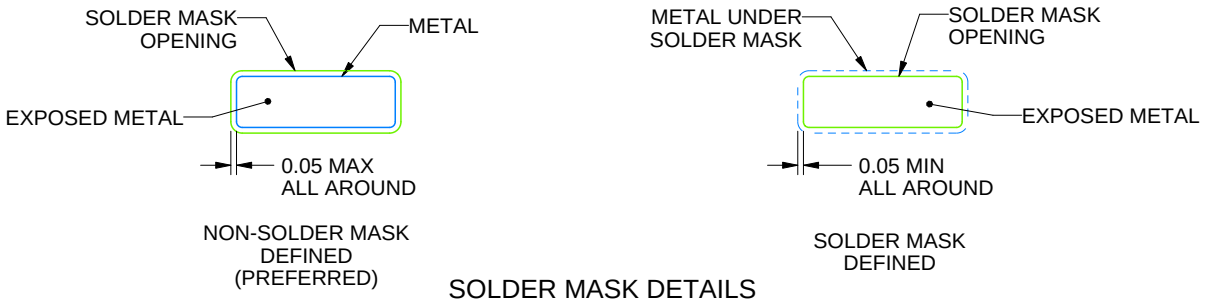

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

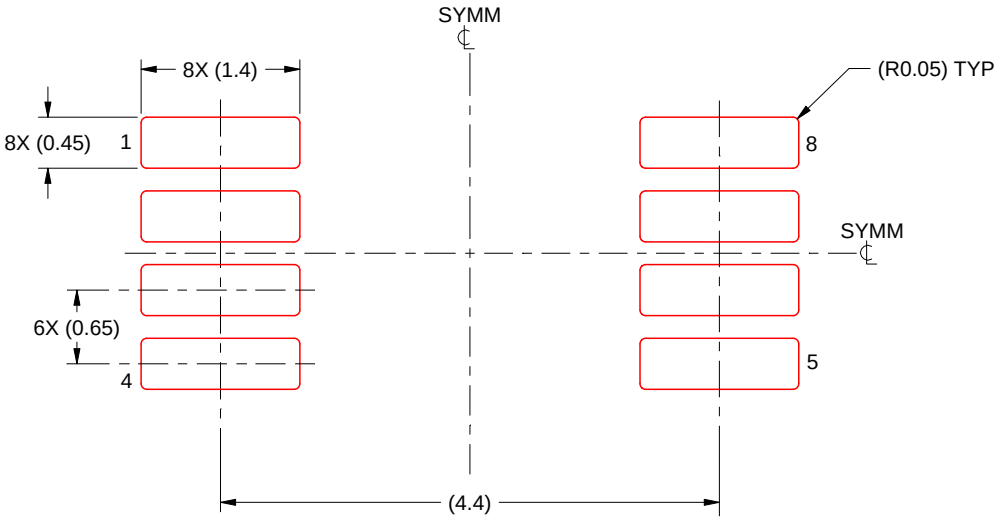



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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