

# Frequency divider using CMOS

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**Abstract**—A Frequency divider is a circuit that takes the input and divide it by specified value. It is also called clock divider. There are many circuit which use frequency dividers to generate a frequency that is a multiple of a reference frequency. It has a vital role in Phase locked loop frequency synthesizers. Frequency dividers can be implemented for both analog and digital application.

**Keywords**—synthesizers, PLL

## I. INTRODUCTION

D type flip flop is used as a frequency divider .It can be seen from the fig.1 frequency waveforms above, that by “feeding back “the output from q bar to the input terminal d, the output pulses at q have a frequency that are exactly one half ( $f/2$ ) that of the input clock frequency.The circuit function is to divide or drop the frequency of the high frequency signal to get the lower frequency signal for a given frequency signal by division. Analog frequency dividers are less common and used only at very high frequencies. Digital dividers implemented in modern IC technologies can work up to tens of GHz. An arrangement of flip flop is a classic method for integer-n division.

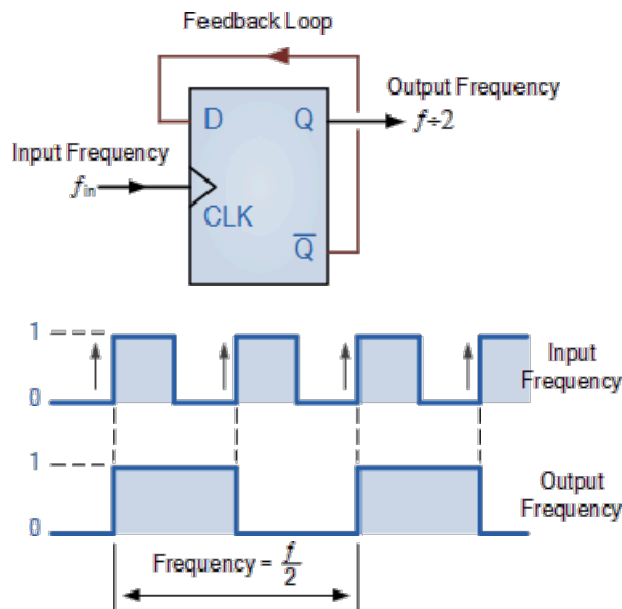


Fig.1 D-flip-flop as a frequency divider

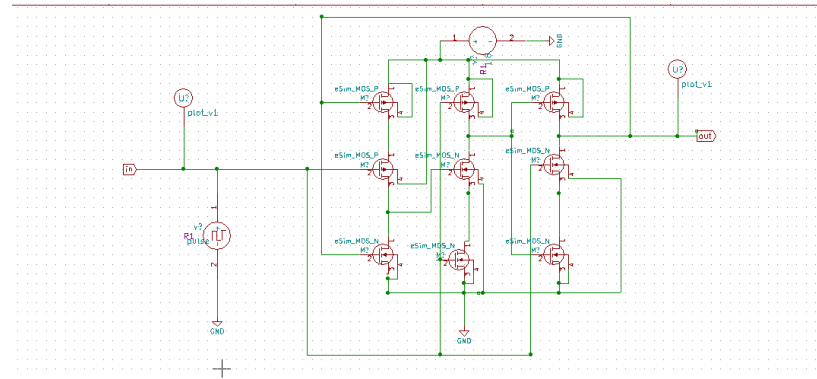


Fig.2 frequency divider

## output waveform

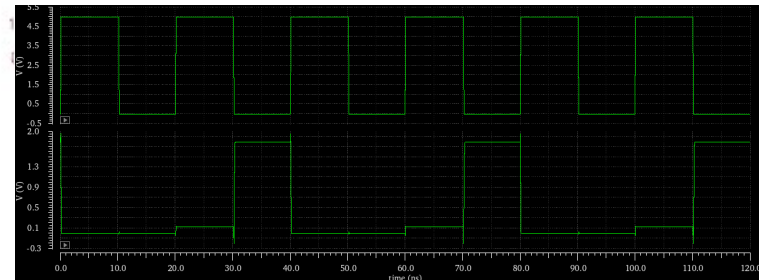


Fig. 3 waveform of frequency divider

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Fig. 1. Example of a figure caption. (*figure caption*)

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- [1] G. Eason, B. Noble, and I. N. Sneddon, “On certain integrals of Lipschitz-Hankel type involving products of Bessel functions,” *Phil. Trans. Roy. Soc. London*, vol. A247, pp. 529–551, April 1955. (*references*)
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