CITS 5506: Internet of Things

Rubric for Project Proposal

Total Marks: 100

Task Nr	Task Detail	Marks	Exemplary (100%-80%)	Proficient (80%-60%)	Satisfactory (60%-30%)	Not Satisfactory (30%-0%)
1	What is the problem ? What is benefit of its solution? What is the impact of the solution?	15	Logically fully explained and all aspects covered.	Most aspects explained with logical reasoning.	Explained but improvement possible in explanation or aspects missed or irrelevant material included.	Poorly written, lack considerable reasoning, irrelevant material, many aspects missed.
2	How comprehensive is literature research, reporting the related work?	15	A very comprehensive literature research	Good literature research and related work	Average literature research and related work.	Unsatisfactory literature research and related work.
3	How will you do the project? Explain your design approach.	15	Design Approach fully explained, steps mentioned in a chronological order.	Design approach and steps explained but some design aspects are missing.	Design approach and steps written but many aspects missing or not logically/ chronologically explained.	Approach and steps are hard to understand. Lack of logical thinking.
4	Block diagram of the proposed design.	15	Block diagram fully gives subsystems, their relationship and interdependence.	Block diagram gives most subsystems, their relationship and interdependence. Few aspects are missing.	Block diagram gives some subsystems, their relationship and interdependence OR the relationships are not fully correct.	Block diagram is hard to understand, subsystems are poorly thought, relationship among the subsystems is incorrect.
5	Explain design in terms of subsystems, their functionalities (software and Hardware) and their interdependence. Sub teams are made, and project divided into tasks for sub teams with sequential and defined timeline.	20	Subsystems, their functionalities, interdependence are fully explained, and a logical timeline made.	Most Subsystems, their functionalities, interdependence explained, and a logical timeline made.	Most Subsystems, their functionalities, interdependence explained, and logical timeline made but can be improved with effort. Some logical aspects in timeline are missed or incorrect.	Subsystems, their functionalities and interdependence are not clearly thought or poorly explained. Logical error in the approach. Timeline can considerably improve.
6	Hardware Identified	10	All hardware identified with sources and delivery time	80% hardware identified with sources and delivery time	60% hardware identified with sources and delivery time	Less than 60% Hardware identified.
7	References	10	Comprehensive list of references made regarding all aspects of project and referred in the proposal text	List of references made regarding most aspects of project and appropriately referred in project proposal text	List of references made regarding 40 % to 50% aspects of project, and not fully referred in the project proposal text.	References poorly researched, irrelevant or not correctly referred in the proposal text.