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**First Partial: Individual part.**

**a. What does FPGA mean? Why was that name given to this type of devices?**

FPGA stands for Field-Programmable Gate Array and this name was given because they can be programmable after they were manufactured.

**b. Describe the general architecture of a FPGA. Describe its main components.**

The general architecture consists on three modules: I/O blocks, Switch Matrix/ Interconnection Wires and Configurable Logic Blocks (CLB). Furthermore, they also have another general categories of components:

i. **Logic elements:** It has a configurable logic block which provides the basic logic and storage functionality for a target application design.

ii. **ALMs:** they included eight Adaptive Logic Modules (ALMs) which consists of 2 adaptive LUTs with eight inputs. ALMs allows the implementation of 2 separate 4-input Boolean function and any six input Boolean function.

iii. **Memory blocks:** They included 3 memories: a static memory, a flash memory and an anti-fuse memory.

iv. **DSP blocks:** Digital Signal Processing (DSP) blocks are used for the implementation of the full-precision multipliers. The memory blocks and DSP blocks are placed in columns at equal distance with one another.

**c. Make a detailed description of the Cyclone V FPGA/SoC**

It offers a powerful dual-core ARM* Cortex*-A9 MPCore* processor surrounded by a set of peripherals and a hardened memory controller. The FPGA fabric is connected to the hard processor system (HPS) through a high-speed >100 Gbps interconnect backbone.

i. **Variants and main features of each variant**

**Cyclone® V SE SoC FPGA**

**(5CSEA2, 5CSEA4, 5CSEA5 or 5CSEA6):**

LEs (K): 25, 40, 85 or 110

ALMs: 9 434, 15 094, 32075 or 41 509.

Registers: 37 736, 60 376, 128 300 or 166 036.

M10k memory (Kb): 1400, 2700, 3970 or 5570.

DSP blocks: 36, 84, 87 or 112.

**Cyclone® V SX SoC FPGA**

**(5CSXC2, 5CSXC4, 5CSXC5 or 5CSXC6):**

LEs (K): 25, 40, 85 or 110

ALMs: 9 434, 15 094, 32075 or 41 509.

Registers: 37 736, 60 376, 128 300 or 166 036.

M10k memory (Kb): 1400, 2700, 3970 or 5570.

DSP blocks: 36, 84, 87 or 112.

**Cyclone® V ST SoC FPGA**

**(5CSTD5 or 5CSTD6)**

LEs (K): 85, or 110

ALMs: 32075 or 41 509.

Registers: 128 300 or 166 036.

M10k memory (Kb): 3970 or 5570.

DSP blocks: 87 or 112.

**ii. Describe the programmable logic (PL) section of the SoC variants**

Look Up Table (LUT): performs logic operation.

Flip Flops: stores the result of the LUT.

Wires: Elements used to connects elements together,

I/O Blocks: Get data in an Out of the FPGA.

**iii. How many PLLs and what features they have.**

2 to 8.

| Feature | Support |
|---|---|
| C output counters | 9 |
| M, N, C counter sizes | 1 to 512 |
| Dedicated external clock outputs | 2 single-ended and 1 differential |
| Dedicated clock input pins | 4 single-ended or 4 differential |
| External feedback input pin | Single-ended or differential |
| Spread-spectrum input clock tracking | Yes (5) |
| Source synchronous compensation | Yes |
| Direct compensation | Yes |
| Normal compensation | Yes |
| Zero-delay buffer compensation | Yes |
| External feedback compensation | Yes |
| LVDS compensation | Yes |
| Phase shift resolution | 78.125 ps (6) |
| Programmable duty cycle | Yes |
| Power down mode | Yes |

**iv. Describe the Hard Processor System (HPS) and how it interconnects to the PL side of the SoC.**

It consists on processors, peripherals and memory controller. The combination of the HPS with the Intel 28 nm low-power FPGA fabric provide the performance and ecosystem of an application. They are interconnected through a highly flexible clocking network.

**References:**

*Cyclone V Device Handbook.* (2020). ALTERA & Intel. Available at: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/cyclone-v/cv_5v2.pdf

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