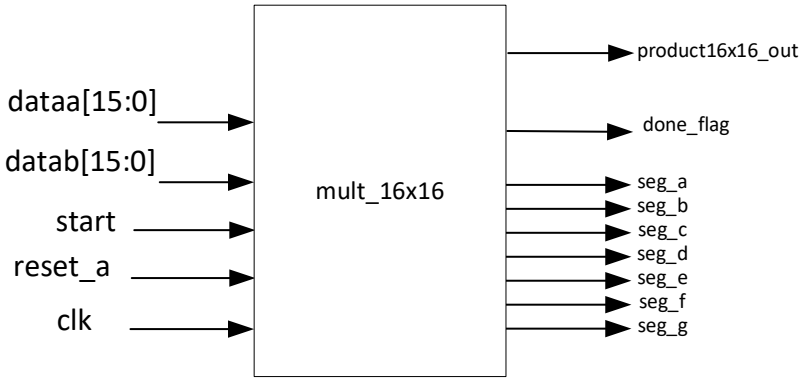
TE3060 Embedded Systems Laboratory

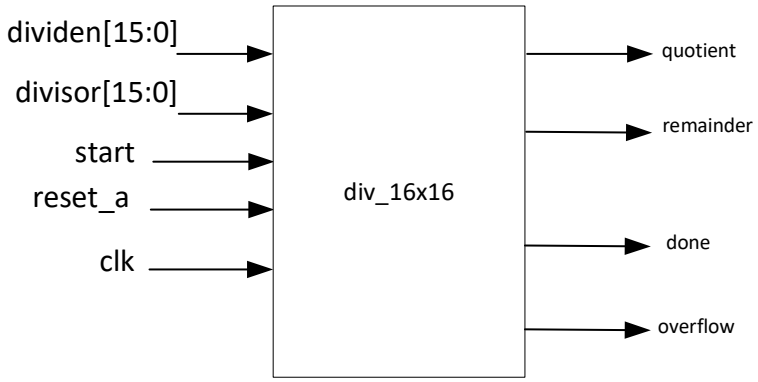
Primer Parcial

September 10, 2020

1. **(20 points)** Use the 8x8 multiplier that we implemented in class to design a 16x16 multiplier as shown below.



   a. Specifications section
      i. Goals of the project
      ii. High level block diagram
      iii. Overall functionality
   b. Design section
      i. All the intricacies of the hardware architecture
      ii. Hardware architecture at signal level
      iii. FSM controllers
      iv. Synthesis results
      v. Simulation results with different test cases
   c. HDL code and test benches runnable in Quartus Prime
2. **(30 points)** Design and implement a 16-bit divider with the shift-and-subtraction approach. The high-level diagram is shown next:



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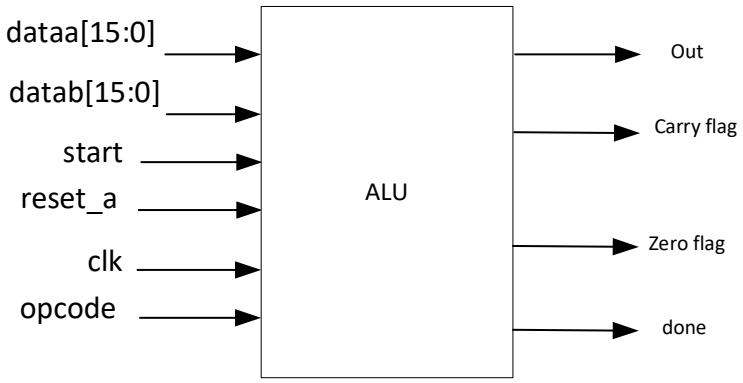
3. **(50 points)** Use the 16x16 bit multiplier and the 16-bit divider above to design and implement a clocked Arithmetic Logic Unit (ALU). The circuit is shown next:



The operations that the ALU must support are:

1. Addition/Subtracion
2. Multiplication/Division
3. Bitwise AND, OR, NAND, NOR, XOR
4. Shift left / shift right
5. Circular shift left / circular shift right
6. Greater/Smaller comparison
7. Equal comparison
8. **Carry out:** if the addition operation of the two operands gives the carry out, this flag is set
9. **Zero:** if all the bits of the result data are zero then the zero flag is set
10. **Deliverables:**
    a. Specifications section
        i. Goals of the project
        ii. High level block diagram
        iii. Overall functionality

b. Design section
    i. All the intricacies of the hardware architecture
    ii. Hardware architecture at signal level
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    iv. Synthesis results
    v. Simulation results with different test cases
c. HDL code and test benches runnable in Quartus Prime