TE2023 Microcontrollers Computer Architectures and Instructions

Luis Alfonso Maeda Núñez, PhD

Professor

Contents

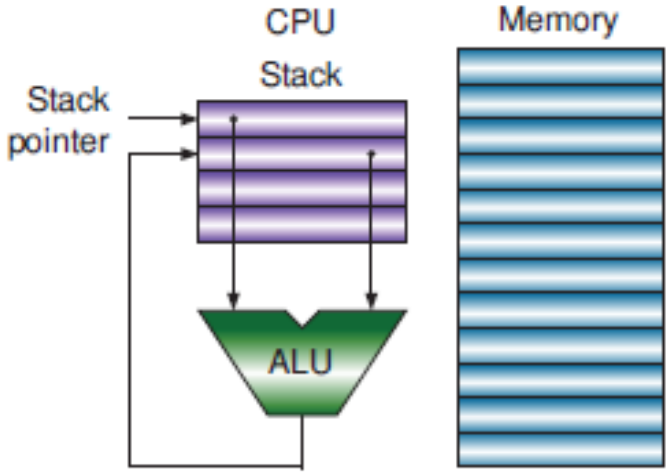
- Types of Instructions
- Types of Computer Architectures
- ARMv6 ISA
- Lifecycle of an Instruction

Types of Instructions

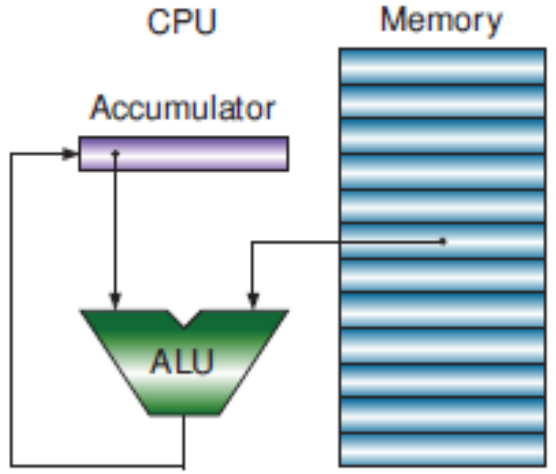
- Arithmetic Operation Type
- Logic Operation Type
- Shift Operation Type
- Memory Access Type
- Input/Output Access Type
- Control Transfer Type
- Floating-Point Calculation Type
- System Control Type

Types of Computer Architectures

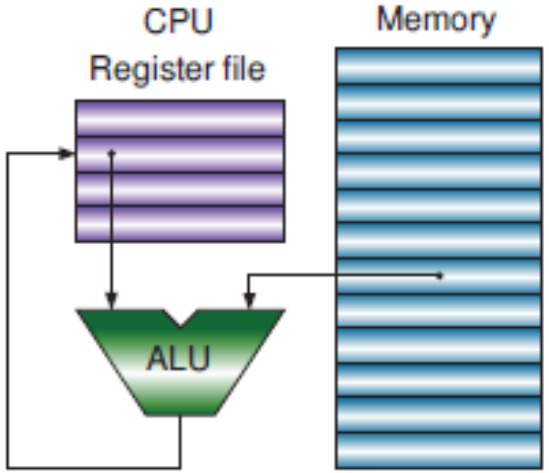
- Stack Architecture
  - (Java Virtual Machine Bytecode)
- Accumulator Architecture
  - (Z80 and 6502 ISAs)
- Register memory Architecture
  - (Intel x86)
- Register Register Architecture
  - (Most RISC processors, including ARM)



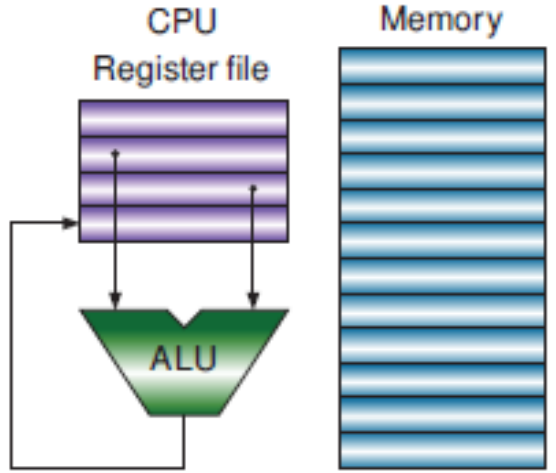
(a) Stack architecture



(b) Accumulator architecture



(c) Register memory architecture



(d) Register register architecture

ARMv6 ISA

https://developer.arm.com/ip-products/processors/cortex-m/cortex-m0-plus

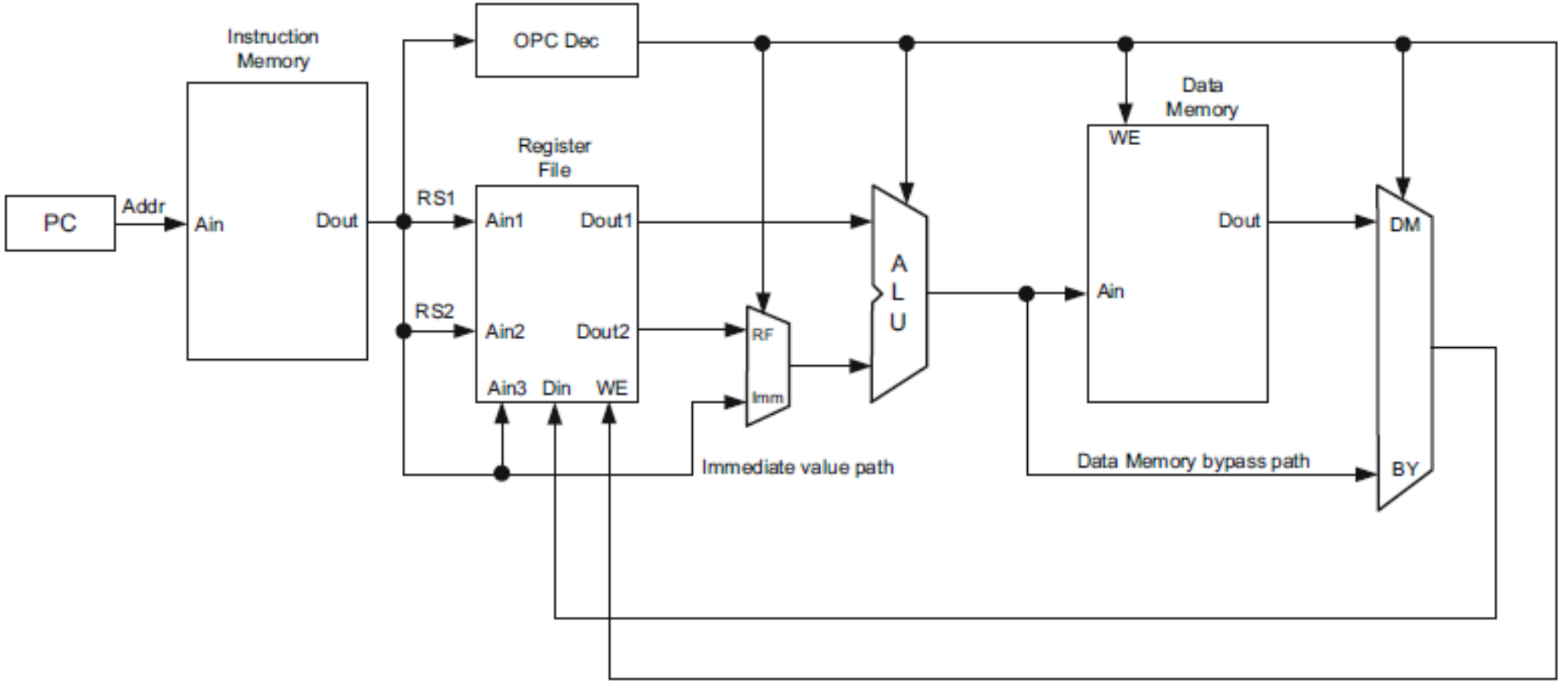
Table 5.1: 16-bit Thumb® instructions supported on the Cortex®-M0 and Cortex-M0+ processor

16-bit Thumb instructions supported on Cortex-M0/M0+ processors									
ADC	ADD	ADR	AND	ASR	B	BIC	BLX	BKPT	BX
CMN	CMP	CPS	EOR	LDM	LDR	LDRH	LDRSH	LDRB	LDRSB
LSL	LSR	MOV	MVN	MUL	NOP	ORR	POP	PUSH	REV
REV16	REVSH	ROR	RSB	SBC	SEV	STM	STR	STRH	STRB
SUB	SVC	SXTB	SXTH	TST	UXTB	UXTH	WFE	WFI	YIELD

Table 5.2: 32-bit Thumb® instructions supported on the Cortex®-M0 and Cortex-M0+ processor

32-bit Thumb instructions supported on Cortex-M0/M0+ processors					
BL	DSB	DMB	ISB	MRS	MSR

Lifecycle of an instruction



NON-PIPELINED	cycle 1					cycle 2					cycle 3				
Instruction 1	IF	RF	A	DM	WB										
Instruction 2						IF	RF	A	DM	WB					
Instruction 3											IF	RF	A	DM	WB

PC

	1st flip-flop				2nd flip-flop			3rd flip-flop			4th flip-flop					
PIPELINED	cycle 1	cycle 2	cycle 3	cycle 4	cycle 5	cycle 6	cycle 7	cycle 8	cycle 9	cycle 10	cycle 11	cycle 12	cycle 13	cycle 14	cycle 15	
Instruction 1	IF	RF	A	DM	WB											
Instruction 2		IF	RF	A	DM	WB										
Instruction 3			IF	RF	A	DM	WB									
Instruction 4				IF	RF	A	DM	WB								
Instruction 5					IF	RF	A	DM	WB							
Instruction 6						IF	RF	A	DM	WB						
Instruction 7							IF	RF	A	DM	WB					
Instruction 8								IF	RF	A	DM	WB				
Instruction 9									IF	RF	A	DM	WB			
Instruction 10										IF	RF	A	DM	WB		
Instruction 11											IF	RF	A	DM	WB	
Instruction 12												IF	RF	A	DM	WB

Topics to cover in the Exam

CONCEPTS

- Main Components of the Computer
  - CPU
  - Memory (volatile, non volatile)
  - Buses (Address, Data, Control)
  - I/O
  - Peripherals
- Components of the CPU
  - ALU, Register Set, Instruction decoder, Timing and Control Unit
- CISC vs RISC (Homework this week)
- Harvard vs Von Neumann vs Modified Harvard (Homework this week)
- What is pipelining

PRACTICE

- Lifecycle of an instruction (Homework this week)