TE2023 Microcontrollers Computer Architecture

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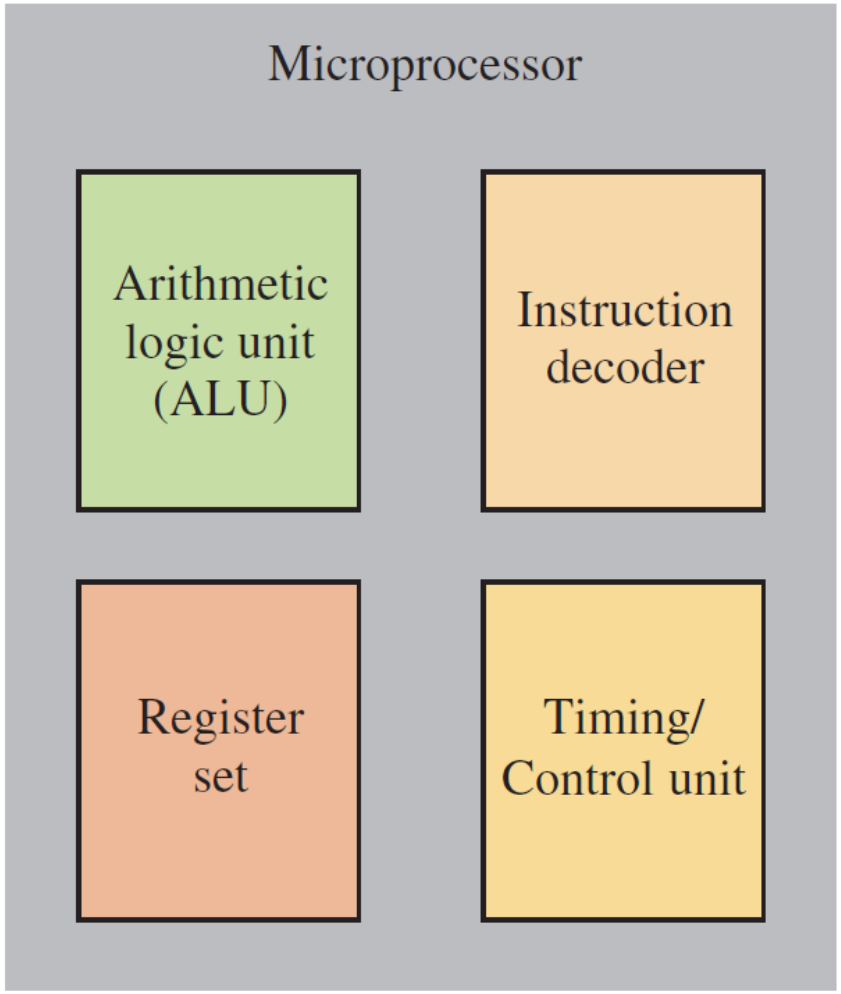
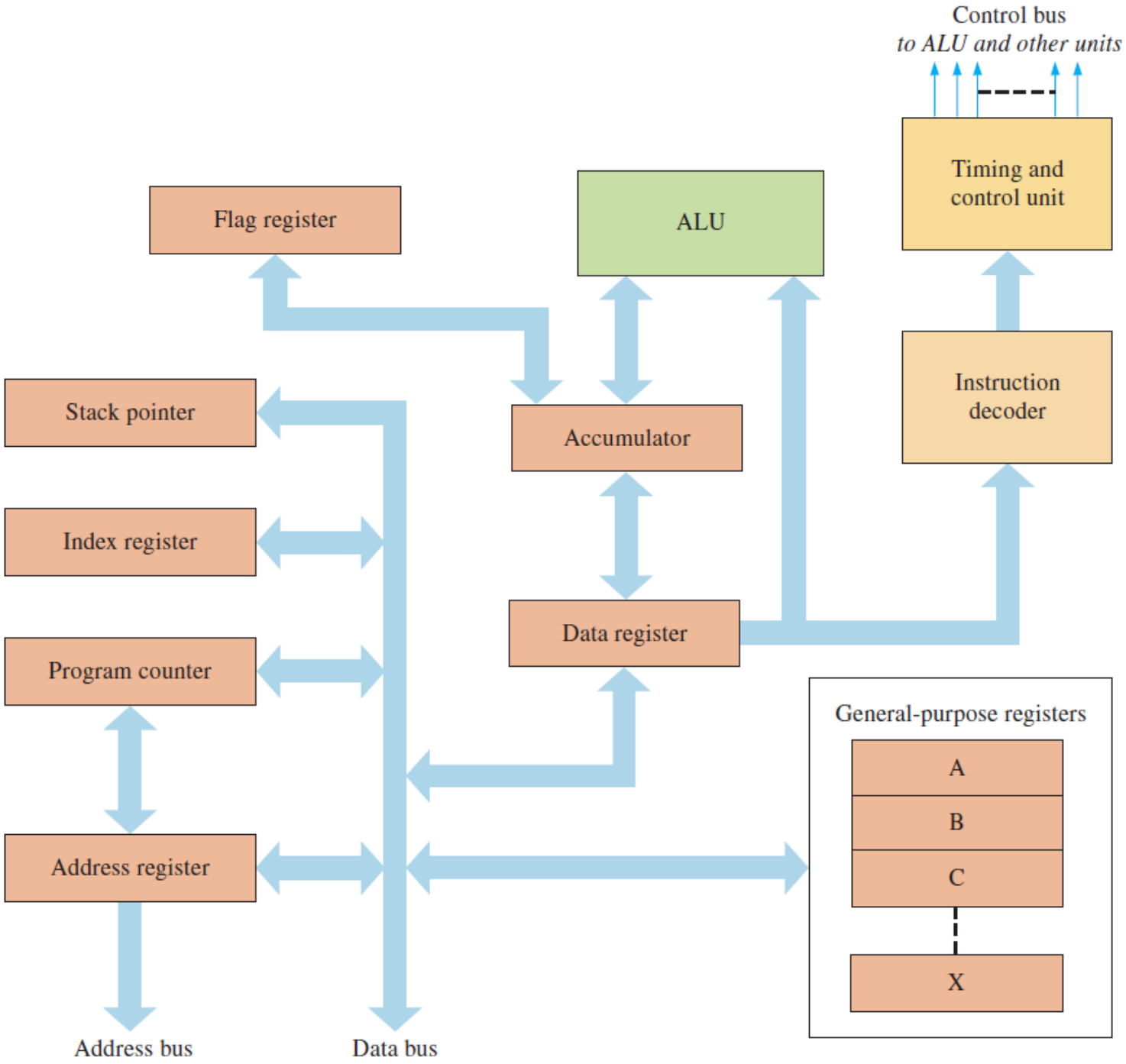
Professor

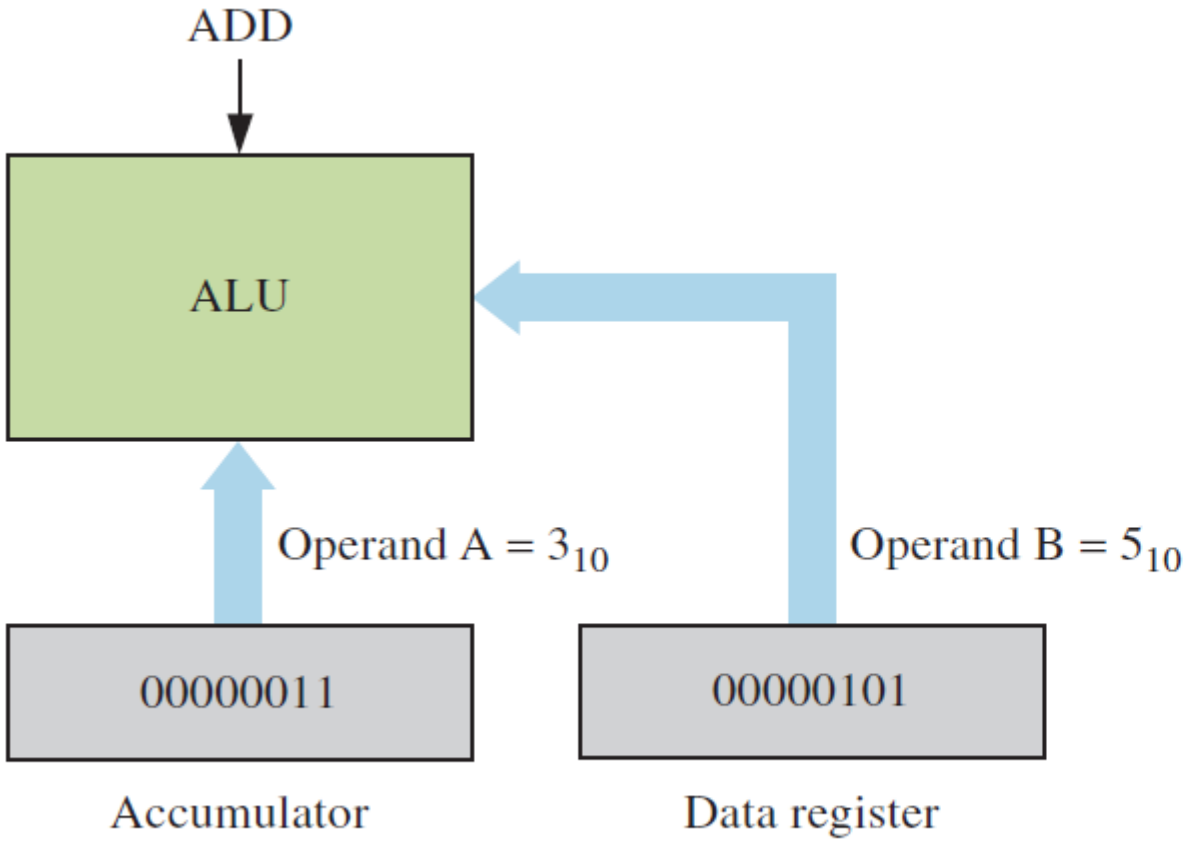
CPU

- Executes memory fetched instructions
- The basic elements of every processor are:
  - ALU (Arithmetic Logic Unit)
  - Instruction decoder
  - Register Set
  - Timing and Control Unit

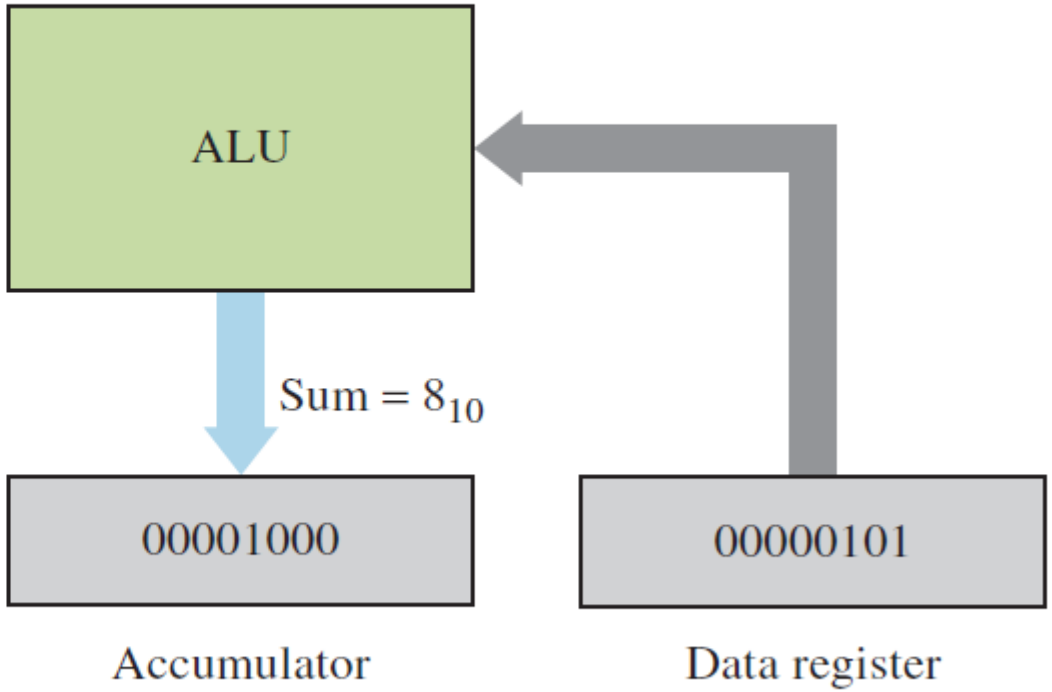



Control bus
to ALU and other units
Timing and control unit
Flag register
ALU
Instruction decoder
Stack pointer
Accumulator
Index register
Data register
Program counter
General-purpose registers
A
B
C
X
Address register
Address bus
Data bus

Arithmetic Logic Unit (ALU)

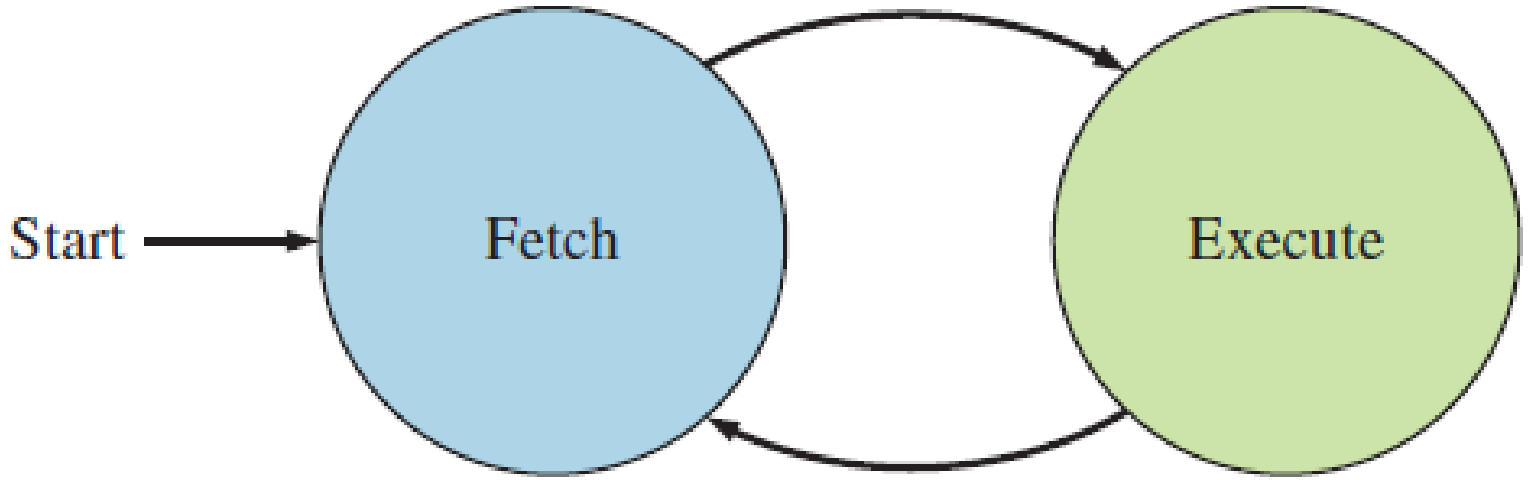


(a) ALU adds 011 and 101.

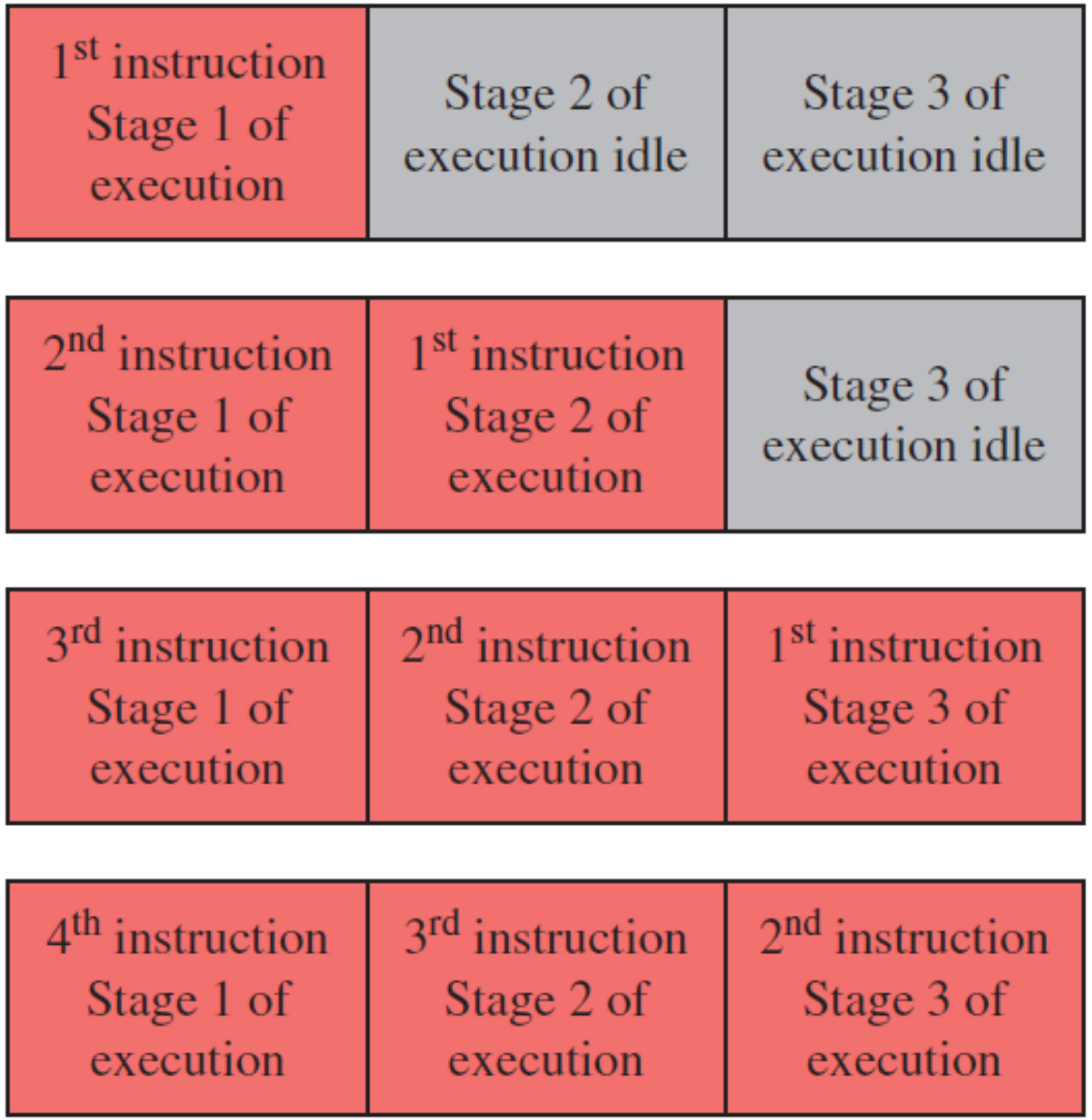


(b) The sum 1000 is put into the accumulator.

Fetch/Execute cycle



Pipelining



First instruction complete

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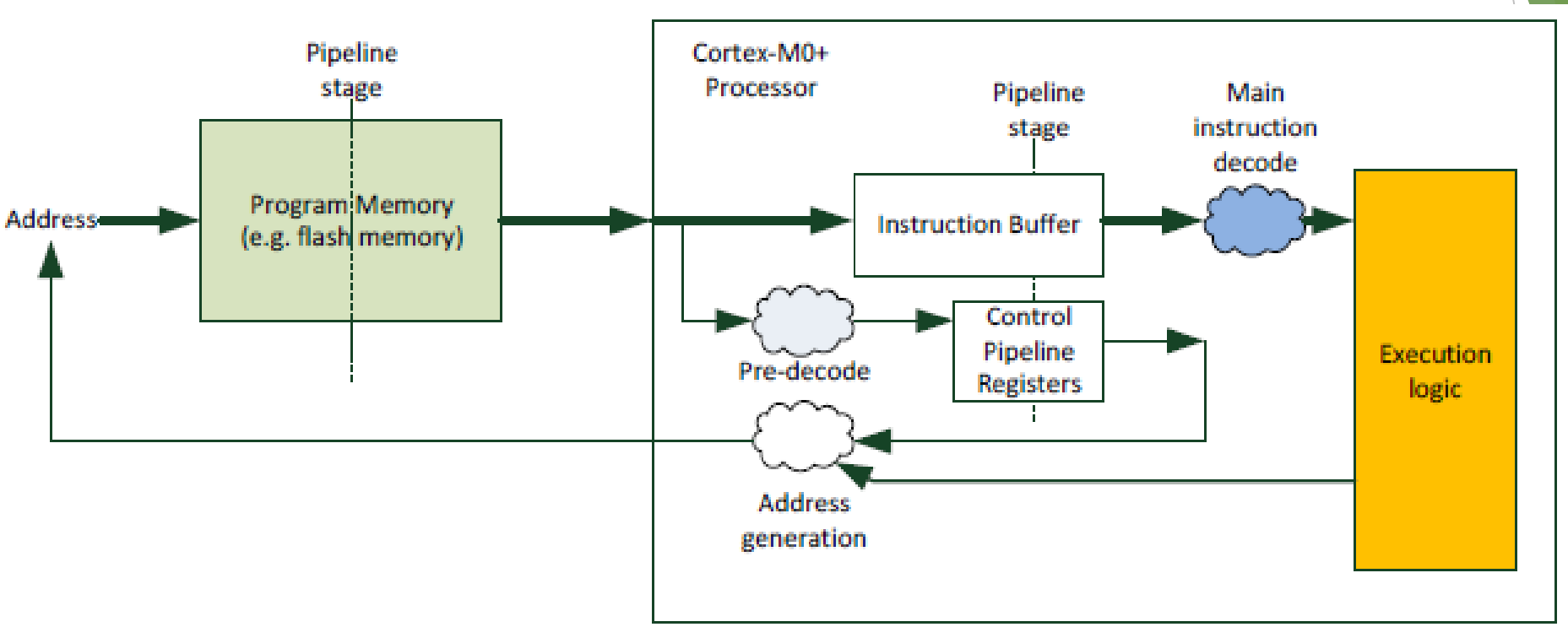
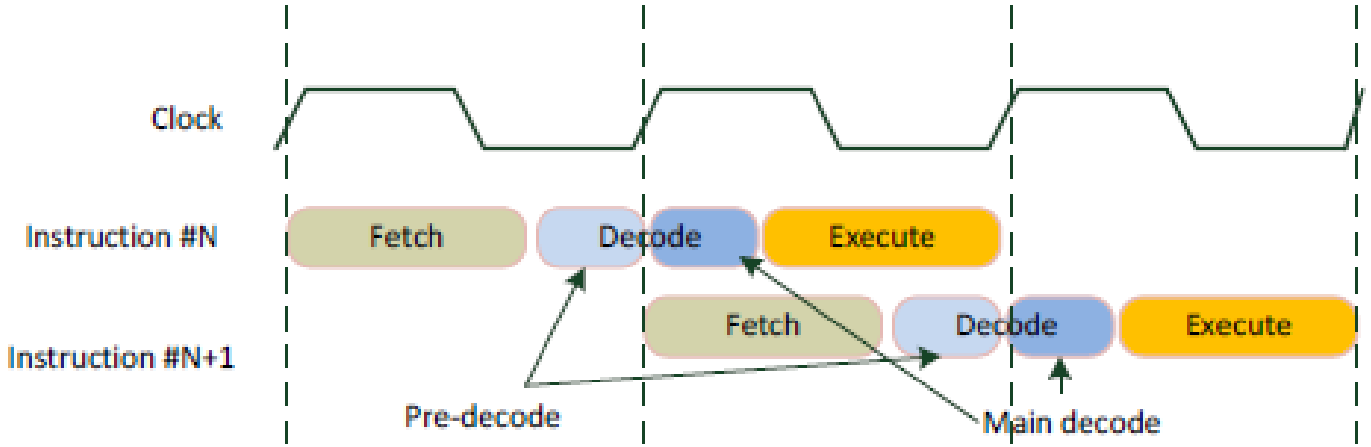
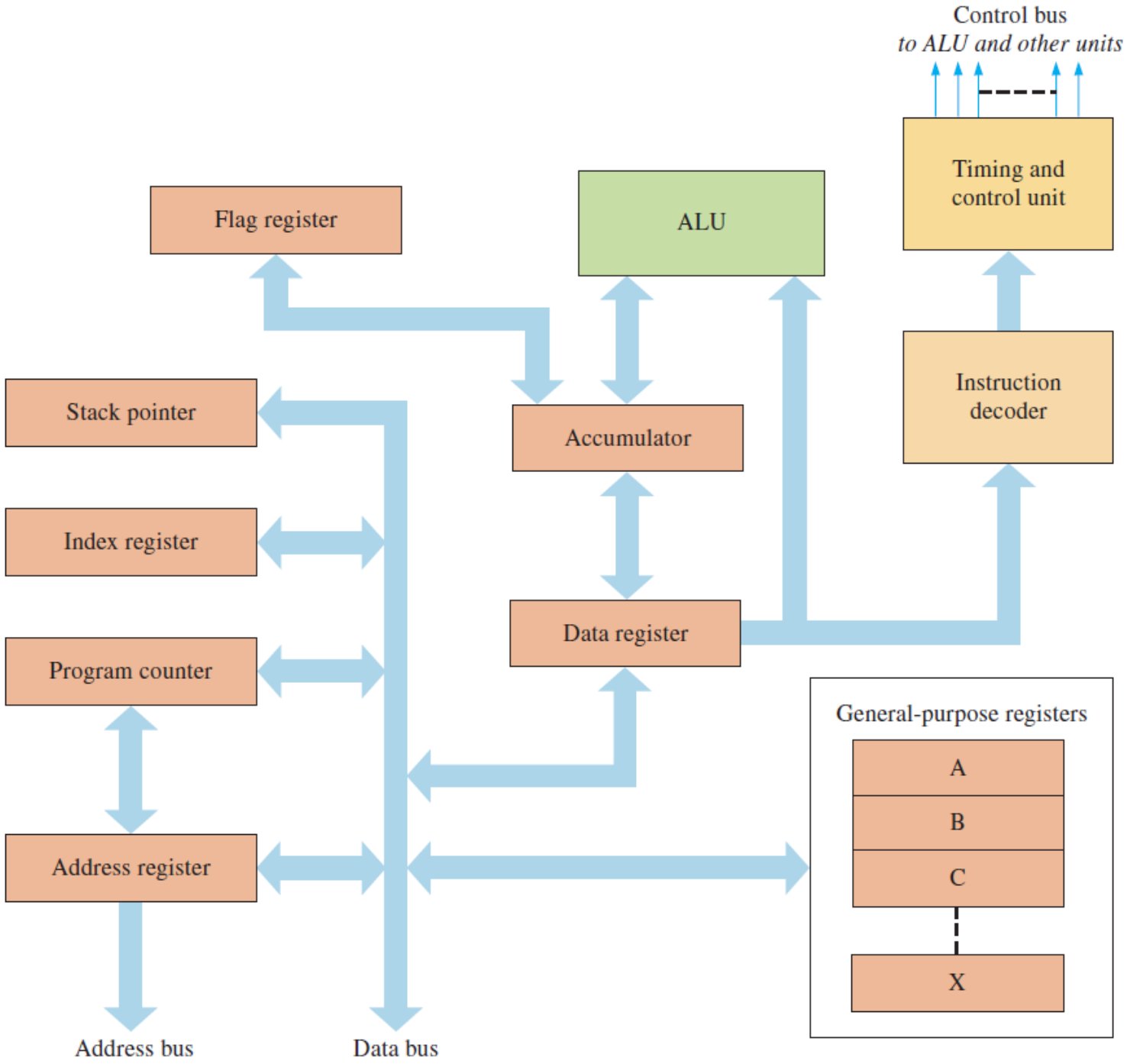
(b) Pipelined execution of a program showing three stages

Pipelining


Pipeline stage
Cortex-M0+ Processor
Pipeline stage
Main instruction decode
Address
Program Memory (e.g. flash memory)
Instruction Buffer
Pre-decode
Control Pipeline Registers
Execution logic
Address generation


Clock
Instruction #N
Fetch
Decode
Execute
Instruction #N+1
Fetch
Decode
Execute
Pre-decode
Main decode

Instructi Unit



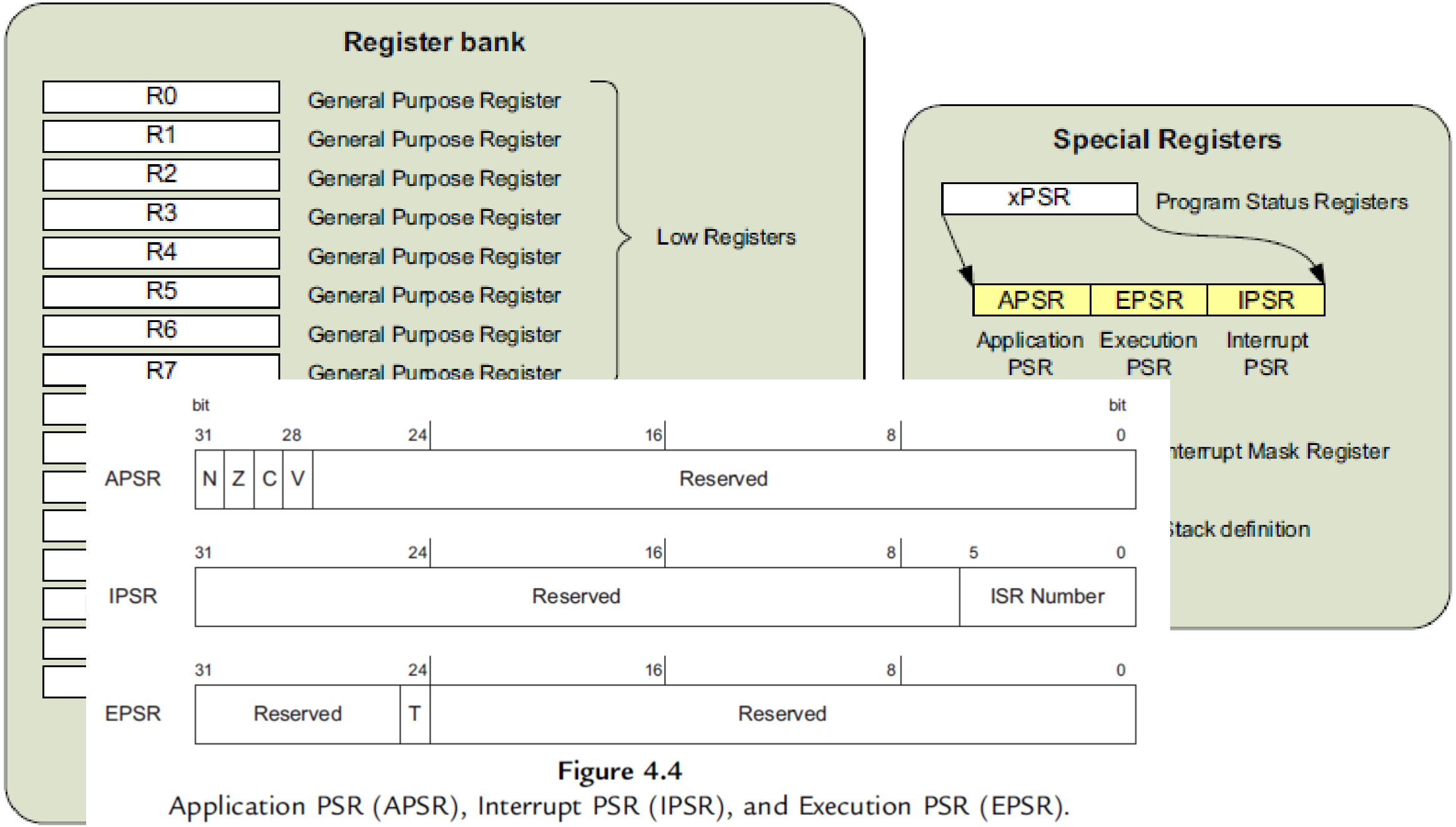
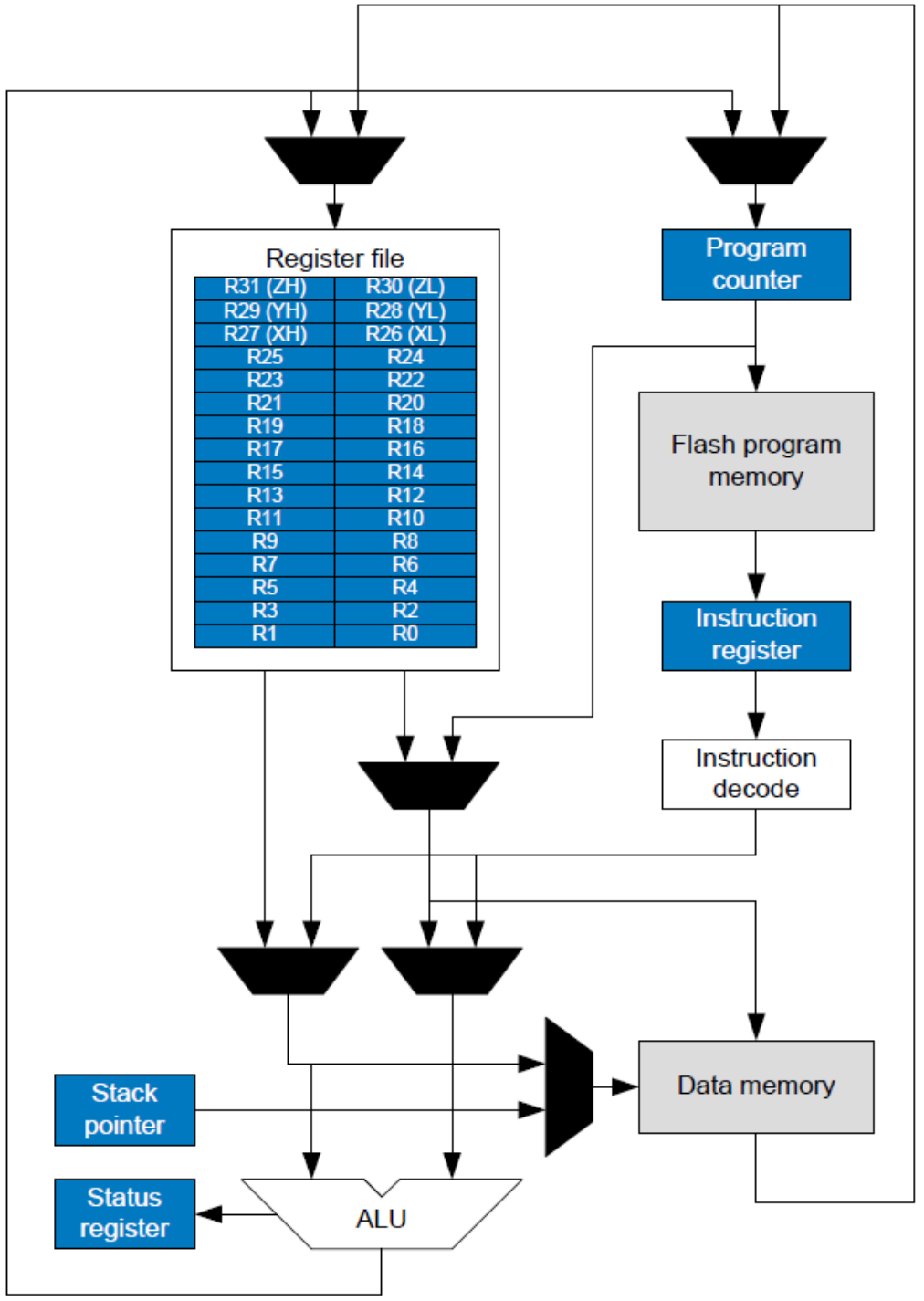


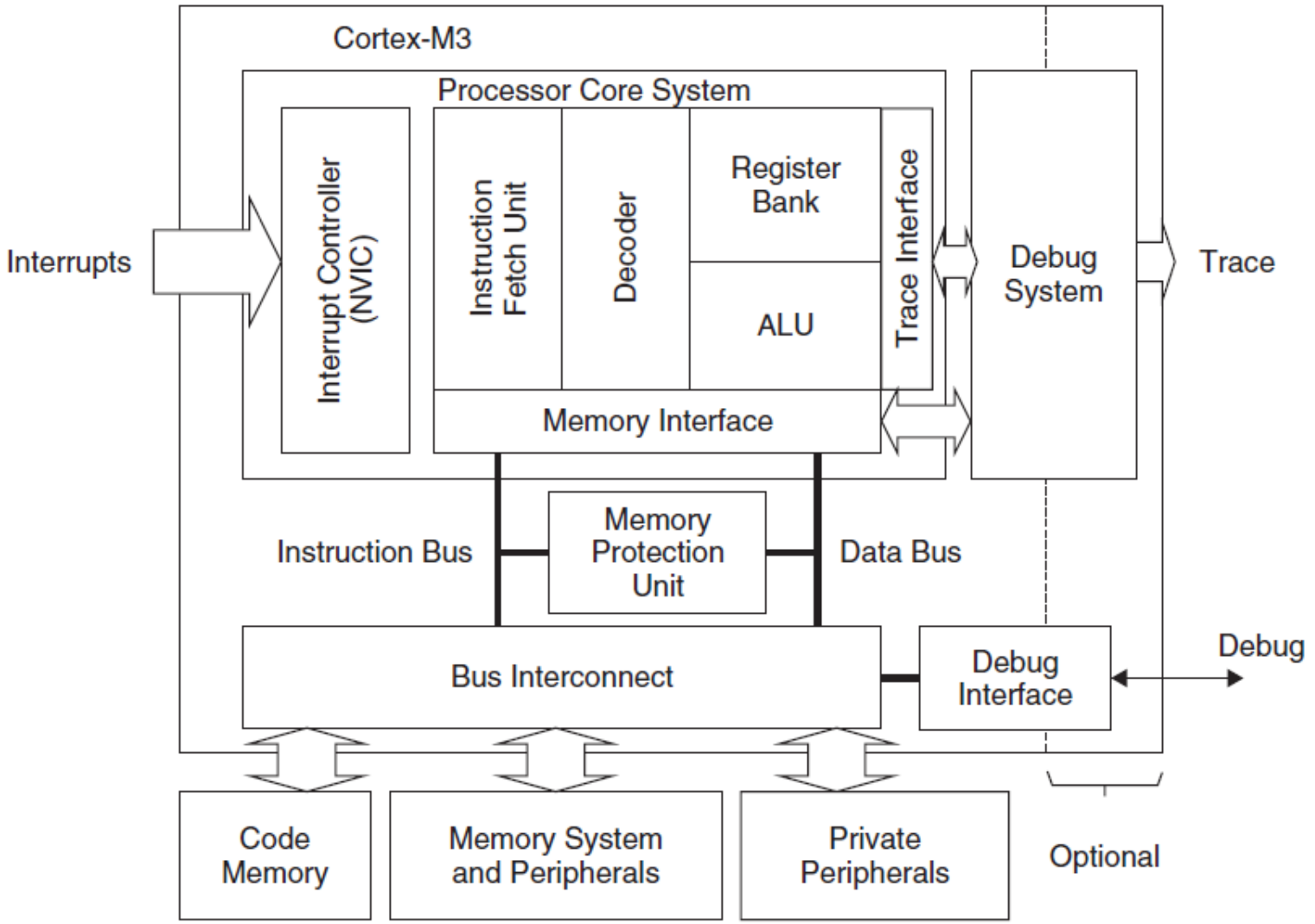
Figure 4.4

Application PSR (APSR), Interrupt PSR (IPSR), and Execution PSR (EPSR).

AVR microarc



ARM Cortex-M3 microarchitecture



ARM Cortex-A76 micro architecture