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Abstract

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Introduction

I joined this course to get a broader understanding of silicon photonics. What kind of concepts are possible to be realized. How does the fabrication process looks like and how accessible is this technology in the current phase. In more detail I am interessted in waveguide related topics. What are the mode characteristics. What similarities do we see here compared to electronics and what are the crucial differences.

Cause of time issues I only managed to implement 3 different MZIs for my design. However I would be also interested in ring resonators which I will atleast investigate simulative.

Introduction

(LaTeX version)

brief motivation for silicon photonics. Include references, e.g., [1]. objective of your course project.

Theory

Short description of the theory relevant to your project. e.g., Waveguide compact model, MZI transfer function.

Modelling and Simulation

At the beginning I concluded the waveguide analysis as described in the chapter. For the MZI the waveguide dimensions correspond to the single mode TE transmission there and the bend radi allow for a minimal mode conversion and radiation loss scenario.

The MZI were designed as following: MZ1 was designed according to the tutorial video but with randomly chosen waveguide lengths ($\Delta L = 118.577m$). For MZI2 and MZI3 the imbalance was increased. For MZI2 and MZI3 imbalances of $\Delta L = 200m$ and $\Delta L = 2100m$ has been chosen.

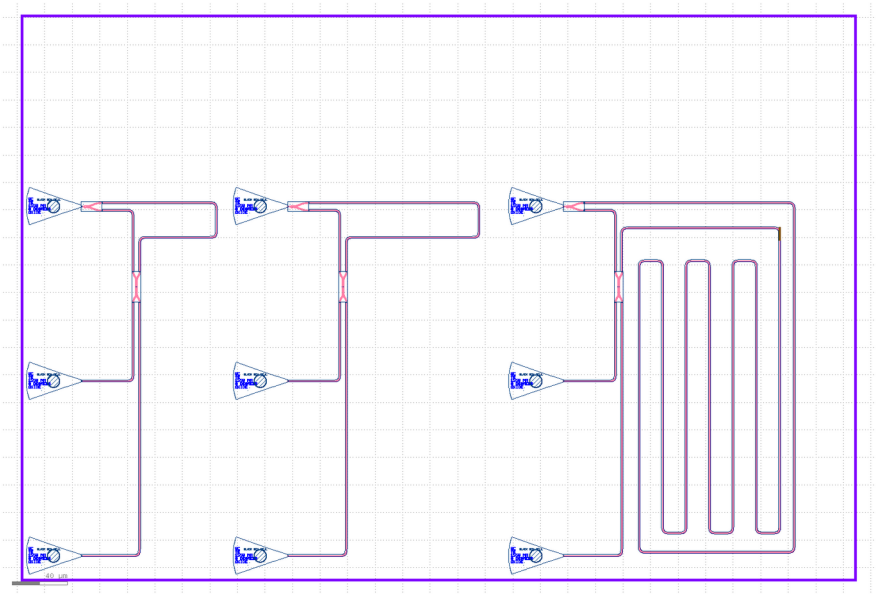

Figure 1: Design of MZ1, MZ2 and MZ3 (from left to right)

The equation for the MZI transmission is given by:
$\frac{I_{\text{out}}}{I_{\text{in}}} = \frac{1}{2}\left(1 + \cos\left(\beta \Delta L\right)\right)$
where
$\beta = \frac{2\pi n_{\text{eff}}}{\lambda}$
The FSWR is defined with:
$FSR = \frac{\lambda^2}{n_{\text{g}}\ \Delta L}$

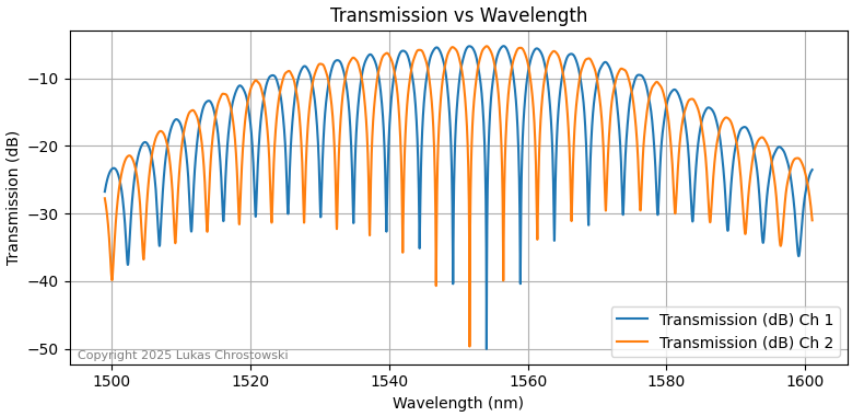

Figure 2: Transmission MZI2 with Delta L = 118.577 µm

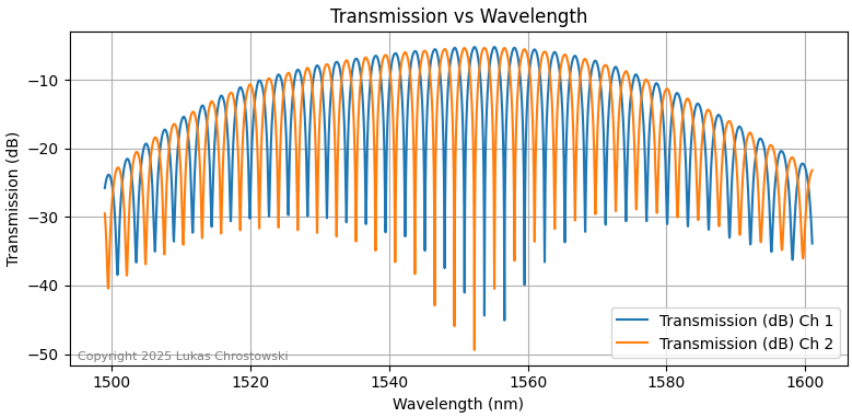

Figure 3: Transmission MZI2 with Delta L = 200 µm

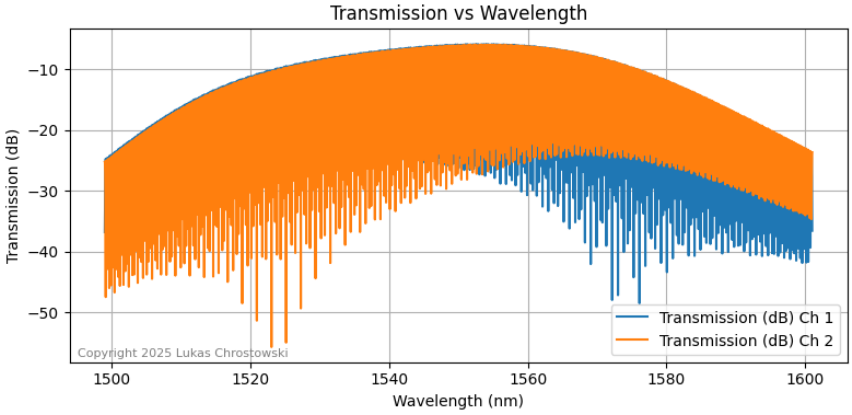

Figure 4: Transmission MZI3 with Delta L = 2100 µm

Fabrication

Two chips were fabricated in this course. Either report on one dataset, or on both. Choose the text as appropriate.

Washington Nanofabrication Facility (WNF) silicon photonics process:

The devices were fabricated using 100 keV Electron Beam Lithography [[2]]. The fabrication used silicon-on-insulator wafer with 220 nm thick silicon on 3 μm thick silicon dioxide. The substrates were 25 mm squares diced from 150 mm wafers. After a solvent rinse and hot-plate dehydration bake, hydrogen silsesquioxane resist (HSQ, Dow-Corning XP-1541-006) was spin-coated at 4000 rpm, then hotplate baked at 80 °C for 4 minutes. Electron beam lithography was performed using a JEOL JBX-6300FS system operated at 100 keV energy, 8 nA beam current, and 500 µm exposure field size. The machine grid used for shape placement was 1 nm, while the beam stepping grid, the spacing between dwell points during the shape writing, was 6 nm. An exposure dose of 2800 µC/cm2 was used. The resist was developed by

immersion in 25% tetramethylammonium hydroxide for 4 minutes, followed by a flowing deionized water rinse for 60 s, an isopropanol rinse for 10 s, and then blown dry with nitrogen. The silicon was removed from unexposed areas using inductively coupled plasma etching in an Oxford Plasmalab System 100, with a chlorine gas flow of 20 sccm, pressure of 12 mT, ICP power of 800 W, bias power of 40 W, and a platen temperature of 20 °C, resulting in a bias voltage of 185 V. During etching, chips were mounted on a 100 mm silicon carrier wafer using perfluoropolyether vacuum oil.

Applied Nanotools, Inc. NanoSOI process:

The photonic devices were fabricated using the NanoSOI MPW fabrication process by Applied Nanotools Inc. (`http://www.appliednt.com/nanosoi`; Edmonton, Canada) which is based on direct-write 100 keV electron beam lithography technology. Silicon-on-insulator wafers of 200 mm diameter, 220 nm device thickness and 2 µm buffer oxide thickness are used as the base material for the fabrication. The wafer was pre-diced into square substrates with dimensions of 25x25 mm, and lines were scribed into the substrate backsides to facilitate easy separation into smaller chips once fabrication was complete. After an initial wafer clean using piranha solution (3:1 H2SO4:H2O2) for 15 minutes and water/IPA rinse, hydrogen silsesquioxane (HSQ) resist was spin-coated onto the substrate and heated to evaporate the solvent. The photonic devices were patterned using a Raith EBPG 5000+ electron beam instrument using a raster step size of 5 nm. The exposure dosage of the design was corrected for proximity effects that result from the backscatter of electrons from exposure of nearby features. Shape writing order was optimized for efficient patterning and minimal beam drift. After the e-beam exposure and subsequent development with a tetramethylammonium sulfate (TMAH) solution, the devices were inspected optically for residues and/or defects. The chips were then mounted on a 4" handle wafer and underwent an anisotropic ICP-RIE etch process using chlorine after qualification of the etch rate. The resist was removed from the surface of the devices using a 10:1 buffer oxide wet etch, and the devices were inspected using a scanning electron microscope (SEM) to verify patterning and etch quality. A 2.2 µm oxide cladding was deposited using a plasma-enhanced chemical vapour deposition (PECVD) process based on tetraethyl orthosilicate (TEOS) at 300^{o}C. Reflectrometry measurements were performed throughout the process to verify the device layer, buffer oxide and cladding thicknesses before delivery.

Experimental Data

To characterize the devices, a custom-built automated test setup [[3]] with automated control software written in Python was used (`http://siepic.ubc.ca/probestation`). An Agilent 81600B tunable laser was used as the input source and Agilent 81635A optical power sensors as the output detectors. The wavelength was swept from 1500 to 1600 nm in 10 pm steps. A polarization maintaining (PM) fibre was used to maintain the polarization state of the light, to couple the TE polarization into the grating couplers [[4]]. A 90^{o} rotation was used to inject light into the TM grating couplers [4]. A polarization maintaining fibre array was used to couple light in/out of the chip [www.plcconnections.com].

Plots of experimental data. The following figure was generated using a built-in Python interpreter!

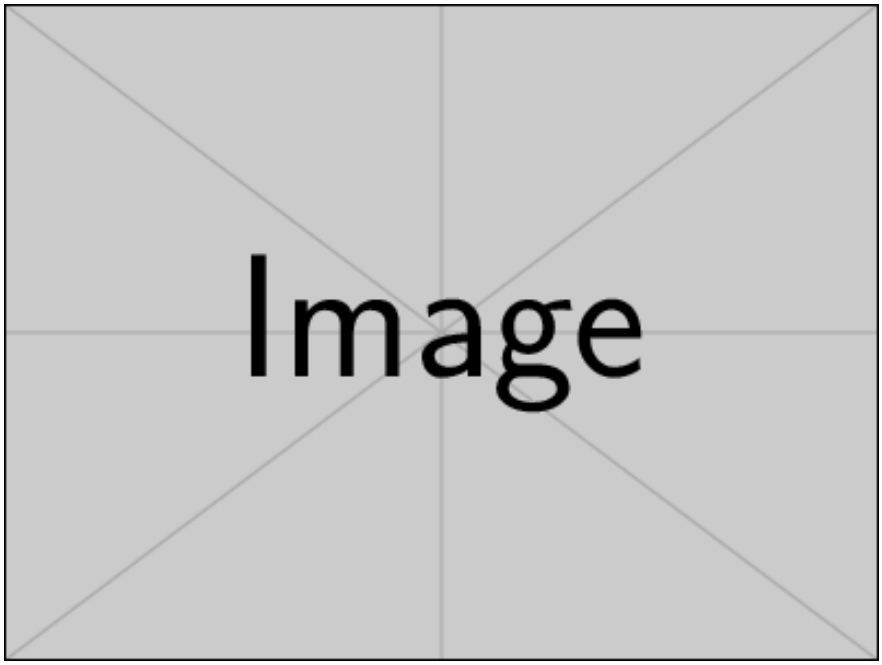

Figure 5: Measured transmission spectrum on a Mach-Zehnder Interferometer with a path length difference of x microns.

Analysis

Data analysis to extract waveguide group index, etc.

Comparison of experimental results with simulations.

Conclusion

The conclusion goes here.

Acknowledgements

(edit according to your use).

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2. Bojko RJ, Li J, He L, et al. (2011) Electron beam lithography writing strategies for low loss high confinement silicon optical waveguides. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures 29:06F309. https://doi.org/10.1116/1.3653266

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