# A Mach-Zehnder Interferometer on a Photonic Integrated Circuit

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## I. Introduction

PHOTONIC integrated circuits (PICs) leverage traditional integrated circuit fabrication technology to build high-density optical circuits. In particular, silicon PICs use CMOS-compatible fabrication to make silicon waveguides and optical components. Due to the high refractive index of silicon, these circuits can be very compact. PICs are now being used in a variety of different applications, including in high-speed data transmission.

In this report, I present a few different silicon PIC designs, including imbalanced Mach-Zehdner interferometers, Bragg gratings, Fabry-Pérot interferometers and photonic crystals. The objective of the imbalanced Mach-Zehdner interferometers is to measure the effective index of the silicon waveguides. This was achieved by measuring the interference pattern present in the transmission data. The distance between minima is known as the free spectral range, from which we can calculate the group index.

This report was written in partial fulfilment of the requirements for the *UBCx: Silicon Photonics Design, Fabrication, and Data Analysis* course taught by Lukas Chrostowski at the University of British Columbia (UBC).

### A. Silicon-on-insulator photonic integrated circuits

Silicon-on-insulator (SOI) wafers are commonly used in high-performance electronics as a result of the lower capacitance and leakage current offered by the buried oxide layer. However, they also offer an excellent platform for optical waveguides. A common SOI wafer composition for multi-project wafers (from top to bottom) is: 220 nm thick silicon, $2-3$ µm thick silicon dioxide (i.e., the *buried oxide layer* or *BOx*), and then the thick silicon handle.

To create an optical waveguide, we need a channel made from a material with a high refractive index surrounded by a material with a low refractive index. For SOI-based PICs, the waveguides are made in the top silicon layer ($n_{\mathrm{Si}} = \sqrt{\varepsilon_{\mathrm{r,Si}}} \approx 3.47$ where $\varepsilon_{\mathrm{r}}$ is the relative permittivity), which sits on top of the buried oxide layer ($n_{\mathrm{SiO_2}} = \sqrt{\varepsilon_{\mathrm{r,SiO_2}}} \approx 1.44$). After etching the waveguide, a top cladding layer is often deposited, providing a silicon channel completely surrounded by silicon dioxide. The approximate dielectric properties of silicon (Si) and silicon dioxide ($SiO_2$) are summarized in Table I. Note that $SiO_2$ has a much weaker dependence on temperature and wavelength.

## II. Strip Waveguide Modelling

For my first PIC design, I kept the waveguide parameters very simple in order to achieve at least one working circuit. I chose to use the TE polarization with a waveguide height of 220 nm and a width of 500 nm. I simulated these waveguide dimensions using a finite-difference eigenmode solver (Ansys Lumerical MODE). The simulated electric field intensity at $\lambda = 1550$ nm is plotted in Fig. 1. For the TE mode at $\lambda = 1550$ nm, the simulated effective index is $n_{\mathrm{eff}} = 2.4446$, the group index is $n_{\mathrm{g}} = 4.1967$, and the TE polarization fraction is 0.98, meaning that it is almost entirely TE. The simulated loss is 0.0004 dB/cm, but this simulation does not include the roughness of the sidewalls, which is the dominant source of loss in physical waveguides.

The simulated effective index and group index are plotted in Fig. 2 as a function of wavelength for three different waveguide widths. Note that the effective index rises with waveguide width, suggesting that more of the energy is contained within the silicon waveguide.

The effective index data were fitted with a second-order polynomial model to produce the following *compact model*.

$$n_{\mathrm{eff}} \approx n_0 + n_1 \cdot (\lambda - 1.55) + n_2 \cdot (\lambda - 1.55)^2 \qquad (1)$$

where the wavelength $\lambda$ is in units of µm. This is the Taylor series expansion about $\lambda = 1.55$ µm. The coefficient values are provided in Table II. The compact models are plotted as dashed lines in Fig. 2, but they aren't visible since they are in excellent agreement with the simulated $n_{\mathrm{eff}}$ values.

The group index is related to the effective index by:

$$n_{\mathrm{g}} = n_{\mathrm{eff}} - \lambda \frac{\mathrm{d}n_{\mathrm{eff}}}{\mathrm{d}\lambda} \qquad (2)$$

TABLE I
First-order wavelength and temperature dependence of silicon and silicon oxide.

| Property | Si | $SiO_2$ |
|---|---|---|
| $n$ | 3.47 | 1.44 |
| $\varepsilon_{\mathrm{r}}$ | 12.0 | 2.07 |
| $\mathrm{d}n/\mathrm{d}\lambda$ | $-7.6 \times 10^{-5}$ nm$^{-1}$ | $-1.2 \times 10^{-5}$ nm$^{-1}$ |
| $\mathrm{d}n/\mathrm{d}T$ | $1.87 \times 10^{-4}$ K$^{-1}$ | $8.5 \times 10^{-6}$ K$^{-1}$ |

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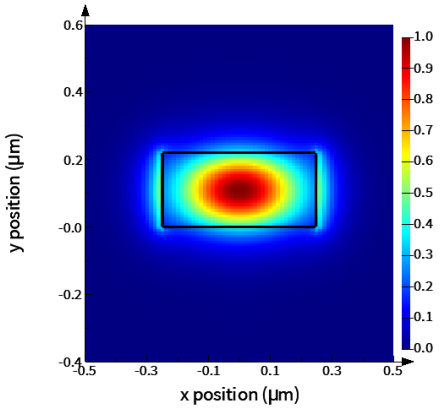


Fig. 1. The electric field intensity at $\lambda = 1550$ nm. Simulated using a finite-difference eigenmode solver (Ansys Lumerical MODE). Note that this plot is cropped to fit the waveguide. The total simulation area was 2.5 μm × 1.7 μm.

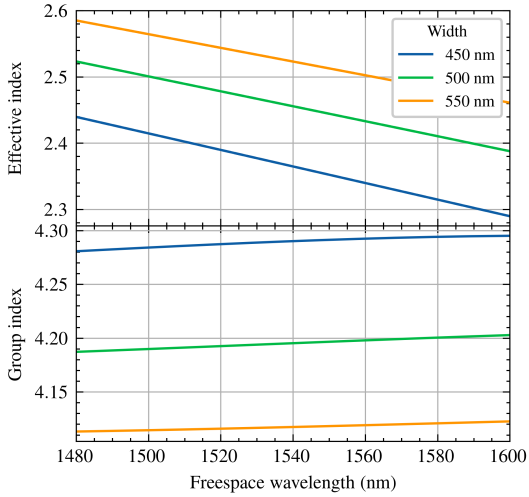


Fig. 2. Simulated properties of the TE mode for a 500 nm × 220 nm waveguide. These results were simulated using a finite-difference eigenmode solver (Ansys Lumerical MODE).

TABLE II
COMPACT MODEL FOR THE EFFECTIVE REFRACTIVE INDEX OF THE TE MODE.

| W (nm) | $n_0$ (1) | $n_1$ (μm$^{-1}$) | $n_2$ (μm$^{-2}$) |
|---|---|---|---|
| 450 | 2.35244 | -1.25065 | -0.04055 |
| 500 | 2.44457 | -1.13035 | -0.04296 |
| 550 | 2.51302 | -1.03573 | -0.02595 |

From the effective index and group index, we can calculate the phase and group velocities by:

$$v_{\mathrm{p}}(\lambda) = \frac{c}{n_{\mathrm{eff}}(\lambda)} \tag{3}$$

$$v_{\mathrm{g}}(\lambda) = \frac{c}{n_{\mathrm{g}}(\lambda)} \tag{4}$$

where $c$ is the speed of light in a vacuum. Note that silicon waveguides are dispersive, meaning that different frequencies travel at different velocities and $v_{\mathrm{p}} > v_{\mathrm{g}}$. Since the group velocity is slower than the phase velocity, in simulated time-domain animations, the phase fronts appear to travel faster than the pulse envelope.

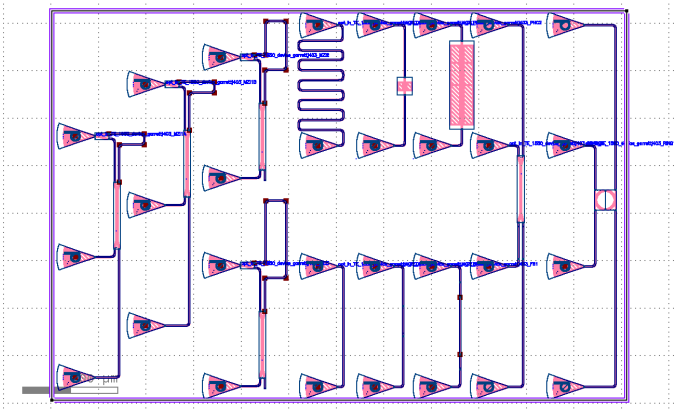

Fig. 3. Layout with various PIC designs.

## III. PIC Designs

### A. De-Embedding Circuits

Text.

### B. Imbalanced Mach-Zehdner Interferometer

Mach-Zehdner interferometers (MZI) are common optical devices used in PICs to create components like switches and filters. They are constructed using simple strip waveguides and Y-branch splitters, as well as fiber grating couplers for the input and output signals.

The transfer function of a lossless imbalanced MZI is:

$$\frac{I_{\mathrm{o}}}{I_{\mathrm{i}}} = \frac{1}{2}\left[1 + \cos\left(\beta\,\Delta\ell\right)\right] \tag{5}$$

where $I_{\mathrm{i}}$ and $I_{\mathrm{o}}$ are the input and output intensity, respectively; $\beta$ is the propagation constant and $\Delta\ell$ is the length mismatch between the two branches of the MZI.

The goal of this design is to extract the group index from the MZI transmission spectra. The distance between minima in the transmission data is known as the free spectral range (FSR) and it is approximately equal to:

$$\mathrm{FSR} \approx \frac{\lambda^2}{\Delta\ell\, n_{\mathrm{g}}} \quad [\mathrm{m}] \tag{6}$$

where $\Delta\ell$ is the length mismatch between the two legs of the MZI, $\lambda$ is the free-space wavelength, and $n_{\mathrm{g}}$ is the ground index. Therefore, by measuring the FSR, we can extract the group index.

A target of 10 minima will give us enough samples within the C-band measurement window to see the shape of the group index. Since the measurement bandwidth is 100 nm, this means that we should target an FSR of 10 nm. For a measurement centered at 1550 nm, this corresponds to a length mismatch of:

$$\Delta\ell \approx \frac{\lambda^2}{\mathrm{FSR} \cdot n_{\mathrm{g}}} = 60 \text{ nm} \tag{7}$$

TABLE III
SUMMARY OF MZI VARIATIONS.

| Number of minima | Target FSR (nm) | $\Delta\ell$ (µm) |
|---|---|---|
| 10 | 10.0 | 60 |
| 20 | 5.0 | 120 |
| 30 | 3.3 | 180 |

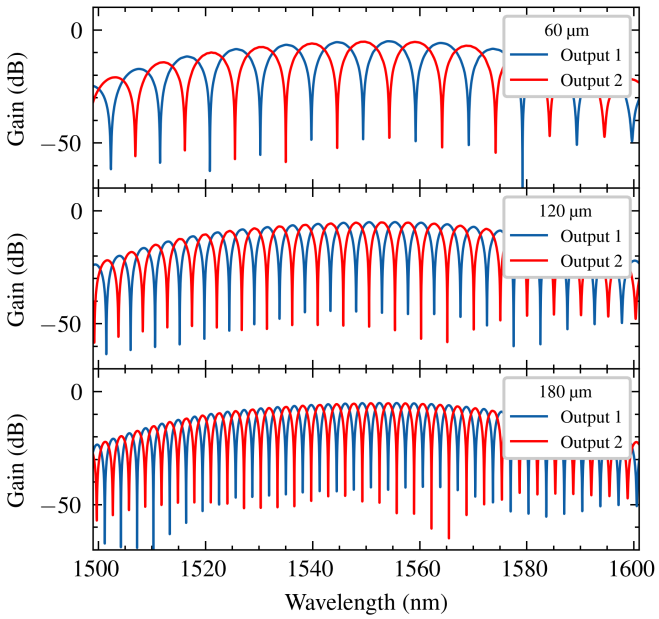


Fig. 4. Simulated gain of the imbalanced MZI with a length mismatch of 60 µm, 120 µm and 180 µm. These simulated results are from Ansys Lumerical INTERCONNECT using the SiEPIC PDK.

where I assumed $n_g \approx 4$. I can also create variants with 20 and 30 minima. These require length mismatches of $\Delta\ell \approx 120$ µm and $\Delta\ell \approx 180$ µm, respectively. These design variants are summarized in Table III.

These length mismatch values were validated using Ansys Lumerical INTERCONNECT, along with the SiEPIC E-Beam PDK. The gain of the three imbalanced MZI circuits is shown in Fig. 4. We can see 10 or 11 minima, as intended. The FSR at approximately 1556 nm is 9.2 nm. Rearranging Eq. 6, this is equivalent to a group index of:

$$n_g \approx \frac{\lambda^2}{\Delta\ell \cdot \mathrm{FSR}} = 4.35 \tag{8}$$

To measure the repeatability, I created two copies of the $\Delta\ell = 60$ µm design.

### C. Bragg Grating

Text.

### D. Fabry-Pérot Interferometer

Text.

### E. Ring Resonator

Text.

### F. Photonic Crystals

Text.

## IV. Fabrication and Testing

The PICs presented in this report were fabricated and tested through the openEBL[1] service offered by the Silicon Electronics-Photonics Integrated Circuits[2] (SiEPIC) program [1], [2]. For the February 2026 fabrication run, the PICs were fabricated using the NanoSOI MPW fabrication process by Applied Nanotools, Inc.[3] in Edmonton, Alberta, Canada. This process uses a state-of-the-art 100 keV electron-beam lithography system (*e-beam*). The typical loss for waveguides made through this process is 1.2 dB/cm for straight waveguides and 3.0 dB/cm for curved waveguides.

The process begins with a 200 mm SOI wafer. This wafer features a 220-nm-thick silicon layer on top of a 2-µm-thick buried oxide layer, which is all on top of the 725-µm-thick silicon handle. The wafer was pre-diced into square substrates with dimensions of 25 × 25 mm, and lines were scribed into the substrate backsides to facilitate easy separation into smaller chips once fabrication was complete.

After an initial wafer cleaning using piranha solution (3:1 $H_2SO_4$:$H_2O_2$) for 15 minutes and a water/IPA rinse, a negative resist (hydrogen silsesquioxane, HSQ) was spin-coated onto the substrate and heated to evaporate the solvent. The photonic devices were then patterned using a Raith EBPG 5000+ e-beam instrument using a raster step size of 5 nm. The exposure dosage of the design was corrected to account for proximity effects that result from the backscatter of electrons from the exposure of nearby features. The shape writing order was optimized for efficient patterning and minimal beam drift. After the e-beam exposure, and subsequent development with a tetramethylammonium sulfate (TMAH) solution, the devices were inspected optically for residue and/or defects. The chips were then mounted on a 4" handle wafer. The silicon not covered by the negative photoresist was then fully etched using an inductively coupled plasma (ICP) reactive-ion etching (RIE) process, using chlorine afterwards for qualification of the etch rate. The resist was removed from the surface of the devices using a 10:1 buffer oxide wet etch, and then the devices were inspected using a scanning electron microscope (SEM) to verify patterning and etch quality.

Finally, a 2.2 µm thick oxide cladding was deposited using a plasma-enhanced chemical vapour deposition (PECVD) process based on tetraethyl orthosilicate (TEOS) at 300°C. Reflectometry measurements were performed throughout the process to verify the device layer, buffer oxide and cladding thicknesses before delivery.

Each designer through openEBL program is allowed an area of 605 µm × 410 µm. This is enough room to fit approximately 5–10 simple photonic circuits, such as Mach-Zehdner or Fabry-Pérot interferometers.

The openEBL program offers automated optical measurements in the C-band, between approximately 1500 and

[1] https://siepic.ca/openebl/
[2] https://siepic.ca/
[3] http://www.appliednt.com/nanosoi

1600 nm; therefore, any spectral features that we intend to measure must fall within this range. These measurements were carried out using a custom-built automated test setup [Chrostowski] with automated control software written in Python[4]. An Agilent 81600B tunable laser was used as the input source and Agilent 81635A optical power sensors were used as the output detectors. The wavelength was swept from 1500 to 1600 nm in 10 pm steps. A polarization maintaining (PM) fibre was used to maintain the polarization state of the light, to couple the TE polarization into the grating couplers [Wang 2014]. A 90° rotation was used to inject light into the TM grating couplers [4]. A polarization maintaining fibre array was used to couple light in/out of the chip[5]. These measurements were conducted at 25°C, with the option of additional measurements at other higher temperatures.

To work with the automated testing setup, the grating couplers (GCs) must follow a specific sequence. A maximum of four grating couplers is allowed. They must be arranged in a column with a centre-to-centre spacing of 127 µm. They must be rotated such that the waveguide exits from the right-hand side. Counting from the top GC, the second GC is the input and all of the other GCs are outputs. Note that we don't need to use all four GCs, e.g., we could choose to only use 2–4, meaning that the input is actually the top GC.

## V. Measurement Results & Analysis

Work in progress.

### A. De-Embedding Circuits

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### B. Imbalanced Mach-Zehdner Interferometer

Text.

### C. Bragg Grating

Text.

### D. Fabry-Pérot Interferometer

Text.

### E. Ring Resonator

Text.

### F. Photonic Crystals

Text.

## VI. Conclusion

Work in progress.

[4] http://siepic.ubc.ca/probestation
[5] www.plcconnections.com

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