Cycle	*Instruction Retired*	*Reason*
1	nop	First instruction is in pipeline - Instruction Fetch
2	nop	First instruction is in pipeline - ID
3	nop	First instruction is in pipeline - Execute
4	nop	First instruction is in pipeline - Memory
5	lbi r0, 0	Write back and retired
6	lbi r5, 43	No stall required
7	lbi r6, 43	No stall required
8	lbi r7, 43	No stall required
9	nop	R0 is in Write back as this instruction enters
10	ld r1, r0, 0	Required one stall for first lbi instruction
11	nop	load and store are treated as unpredictable hazards so are completely avoided with stalls. This could be optimised by calculated the memory address and save a cycle on consecutive memory instructions
12	nop	“”
13	nop	“”
14	nop	“”
15	st r5, r1, 0	“” avoiding last load
16	nop	“”
17	nop	“”
18	nop	“”
19	nop	“”
20	ld r1, r0, 2	“” avoiding last store

21	nop	“”
22	nop	“”
23	nop	“”
24	nop	“”
25	st r6, r1, 1	“” avoiding last load
26	nop	“”
27	nop	“”
28	nop	“”
29	nop	“”
30	ld r1, r0, 4	“” avoiding last store
31	nop	“”
32	nop	“”
33	nop	“”
34	nop	“”
35	st r7, r1, 1	“” avoiding last load
36	halt	Only stall on branches and jumps