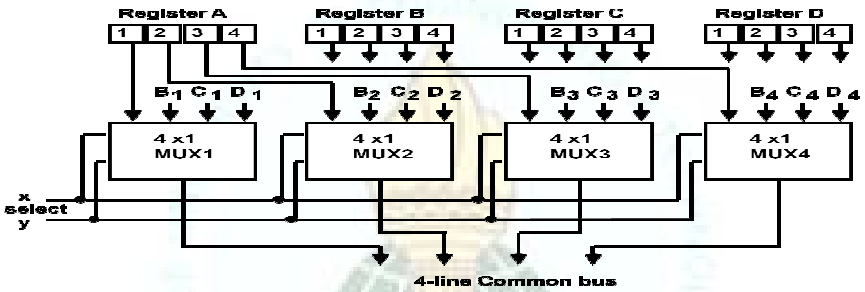
JAYPEE UNIVERSITY OF ENGINEERING & TECHNOLOGY, GUNA
DEPARMENT OF COMPUTER SCIENCE & ENGINEERING
Course: Computer Organization & Architecture Lab
Course Code: 18B17CI474
B. Tech. (CSE VI Sem.)

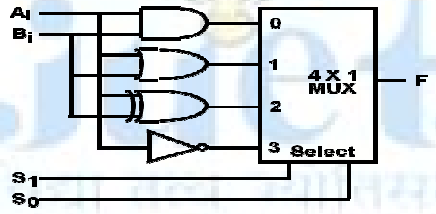
Experiment # 5

Aim: Design of multiplexer based logic circuits.

Exercise#1: Design N-bit, 4-source common bus system shown in figure below in structural style of architecture using **generic** and **for-generate** statements. Use all inputs, outputs and selection lines in the form of bus.



Exercise#2: Design N-bit logic circuit shown in figure below in structural style of architecture using **generic** and **for-generate** statements. Use all inputs, outputs and selection lines in the form of bus.



Exercise#3: Design N-bit shift circuit in using **behavioural style of architecture** which performs four operations given in table. Use all inputs, outputs and selection lines in the form of bus.

S_1S_0	Micro operations
00	shl B
01	ashr A
10	Cir B
11	Cil A