JAYPEE UNIVERSITY OF ENGINEERING & TECHNOLOGY, GUNA
DEPARMENT OF COMPUTER SCIENCE & ENGINEERING
Course: Computer Organization & Architecture Lab
Course Code: 18B17CI474
B. Tech. (CSE VI Sem.)

Experiment # 7

Aim: Design of registers and counters.

A sequential logic circuit is the digital system whose **output depends on its current combination of input values as well as previous values of the output**. All flip-flops, registers, counters are the examples of sequential circuits. Other important features of these circuits are as following:-

- Feedback connections in the circuits.
- Clock signal i.e. time independent
- Memory elements in the circuit

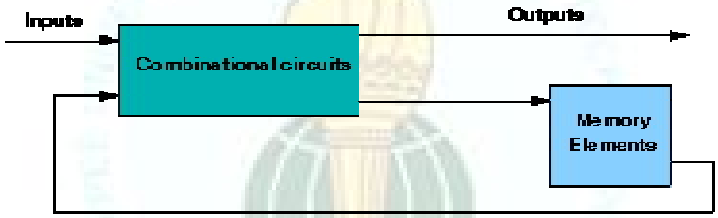

Figure 1: Block diagram of a typical sequential logic circuit

Registers: This is a group of flip-flops. Its basic function is to hold and shift the information within a digital system so as to make it available to the logic units during the computing process. This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name **Shift Register**. Data bits may be fed in or out of a shift register serially (SISO: serial in serial out), that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration (PIPO: parallel in parallel out) as shown in Figure 2. A shift register basically consists of several single bit "D-flip-flops", one for each data bit, connected together.

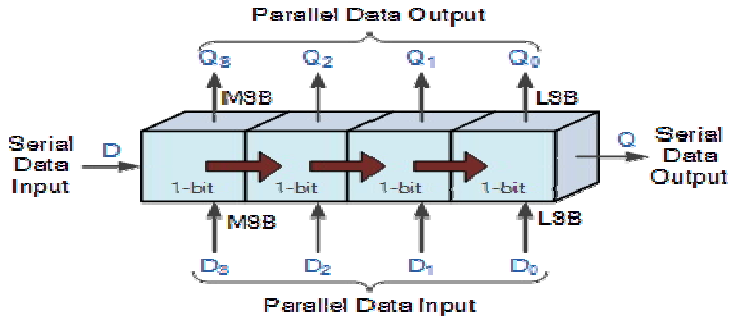

Figure 2: Four configurations (SISO, SIPO, PIPO, and PISO) of a shift register.

Counters: *Counters* are the (group of flip-flops) sequential *circuits* which "count" through a specific state of sequence. The number of flip-flops used and the way in which they are connected determine the number of states and also the specific sequence of states that the counter goes through during each complete cycle. Counters are classified according to the way they are clocked: **Asynchronous** (also called ripple counter) in which the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flip-flop and **Synchronous** counter is one in which the flip-flops within the counter changes states at exactly the same time because they do have a common clock pulse to all flip-flops.

Registers and counters can be implemented by using any type of flip-flop i.e. SR, JK, D and T. VHDL code for D flip-flop is given below which can be used for implementation of various registers and counters.

VHDL code for D flip-flop

```
entity DFF is
port( d, reset, clk : in std_logic;
        q : out std_logic);
end DFF;
architecture Behavioral of DFF is
begin
process(d, reset, clk)
begin
  if (clk'event and clk = '1') then
    if(reset = '1' ) then
      q <= '0';
    else
      q <= d;
    end if;
  end if;
end process;
end Behavioral;
```

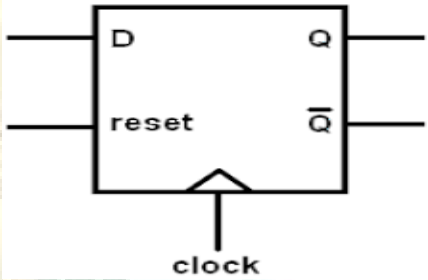

Figure:3 Block diagram of D flip-flop

Truth Table of D-flipflop

Input			Output	
D	reset	clock	Q	Q`
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

Exercise#1: Design and verify 4-bit serial-in-serial-out (SISO) shift register shown in Figure-4 in **structural style of architecture**. Use reset control line to reset the register.

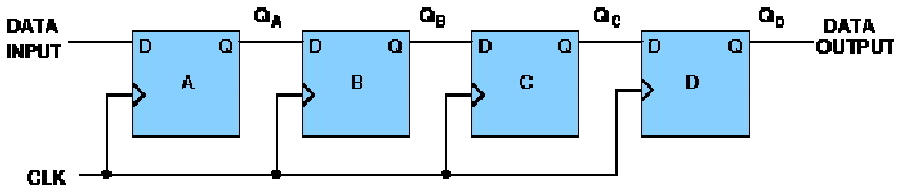

Figure 4: Block diagram of 4-bit serial-in-serial-out (SISO) shift register

Exercise#2: Design and verify MOD-6 binary counter shown in figure-5 using **structural style of architecture.**

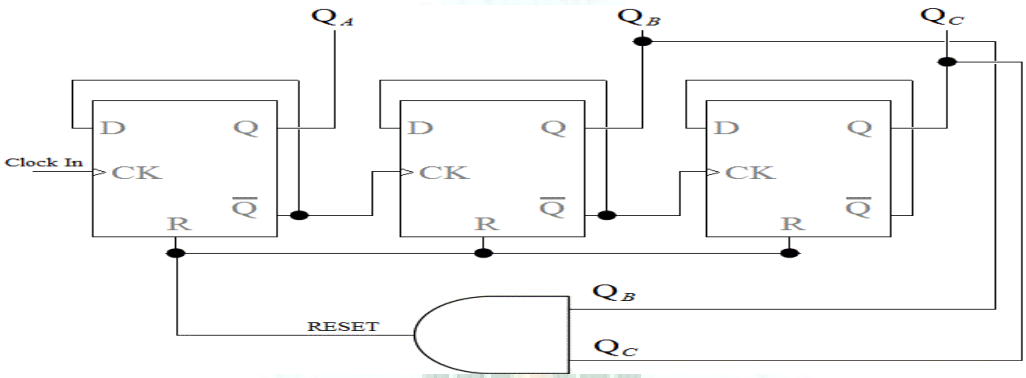

Figure 5: Block diagram of Mod-6 binary counter