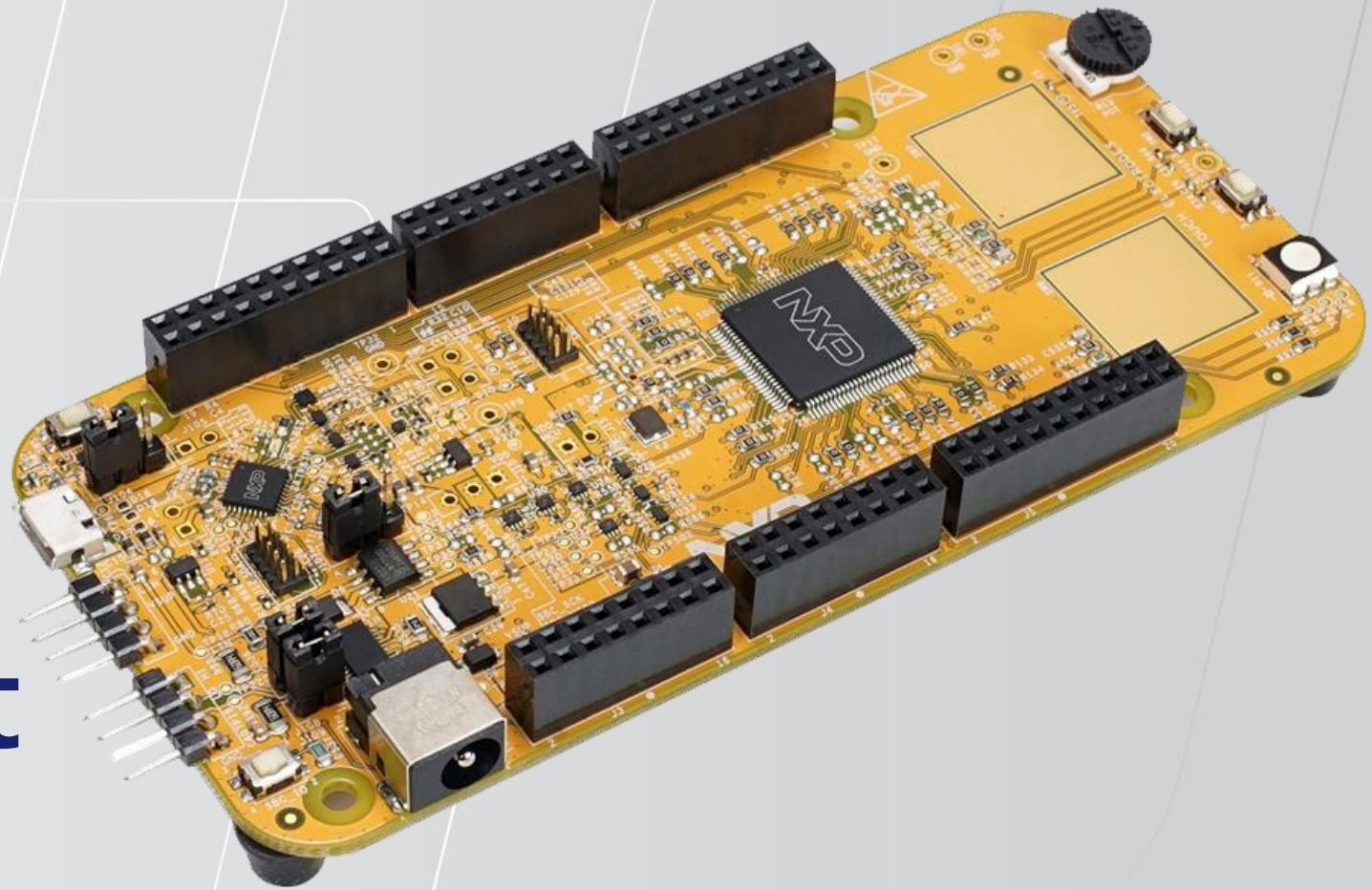
GPIO – General Purpose Input/Output



10 Oct 2022

OUTLINE

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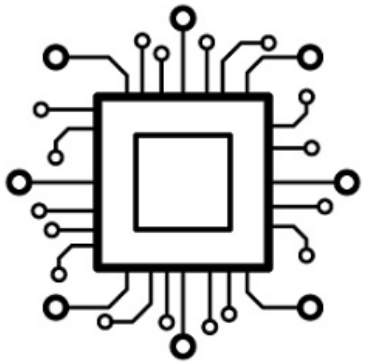
1. Introduction GPIO

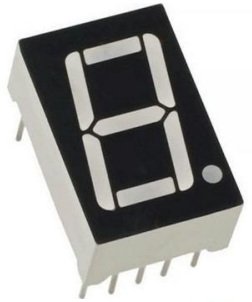
General Purpose Input/Output

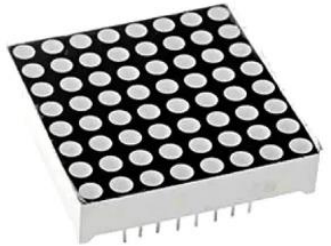
INPUT

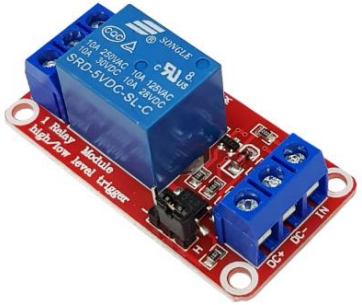
MCU



OUTPUT



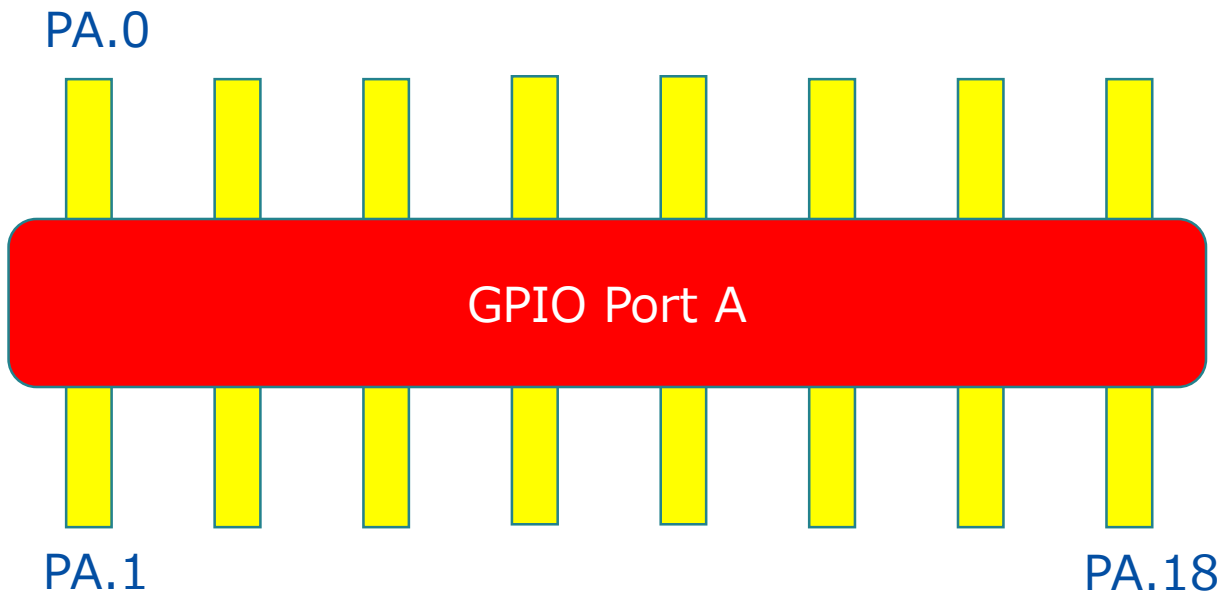




1. Introduction GPIO

PORT	S32K144
PORT A	18
PORT B	18
PORT C	18
PORT D	18
PORT E	17

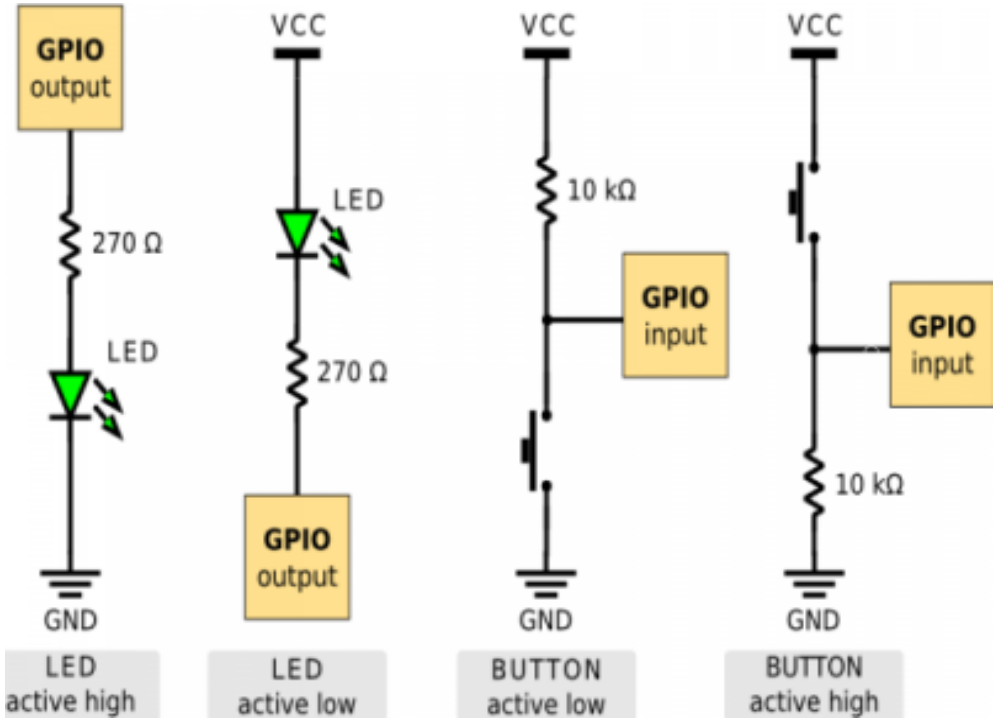
- 5 GPIO ports:
  A, B, C, D, E
- Up to 32 pins in each port



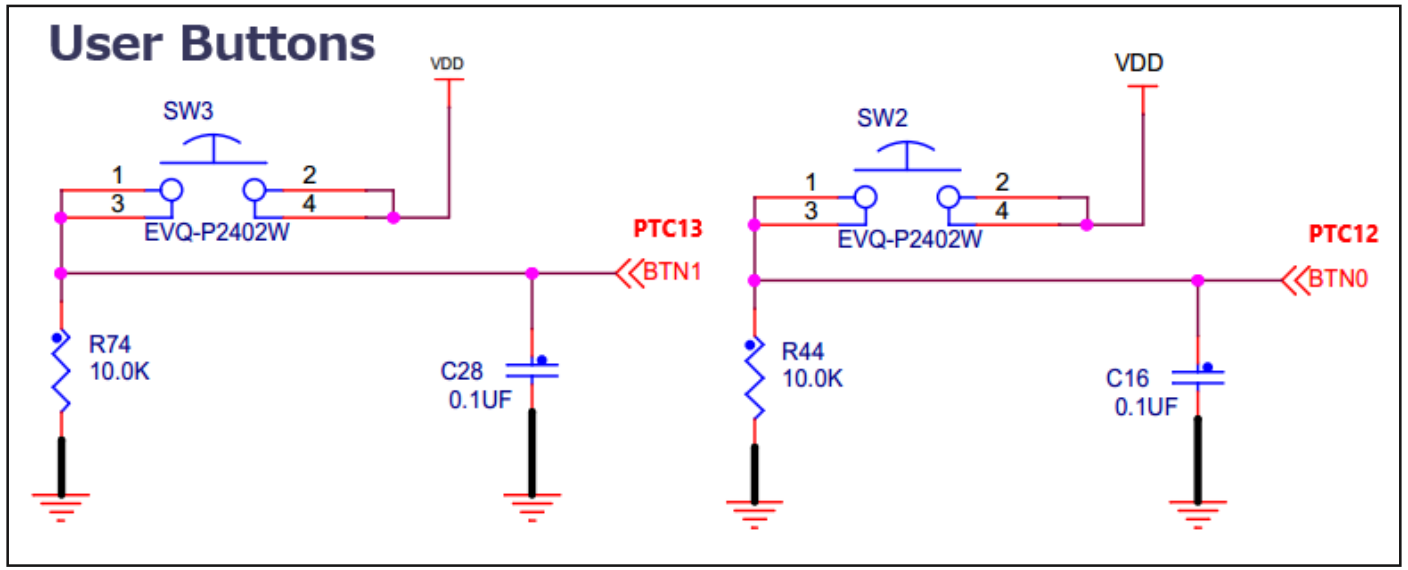
1.1. GPIO Features

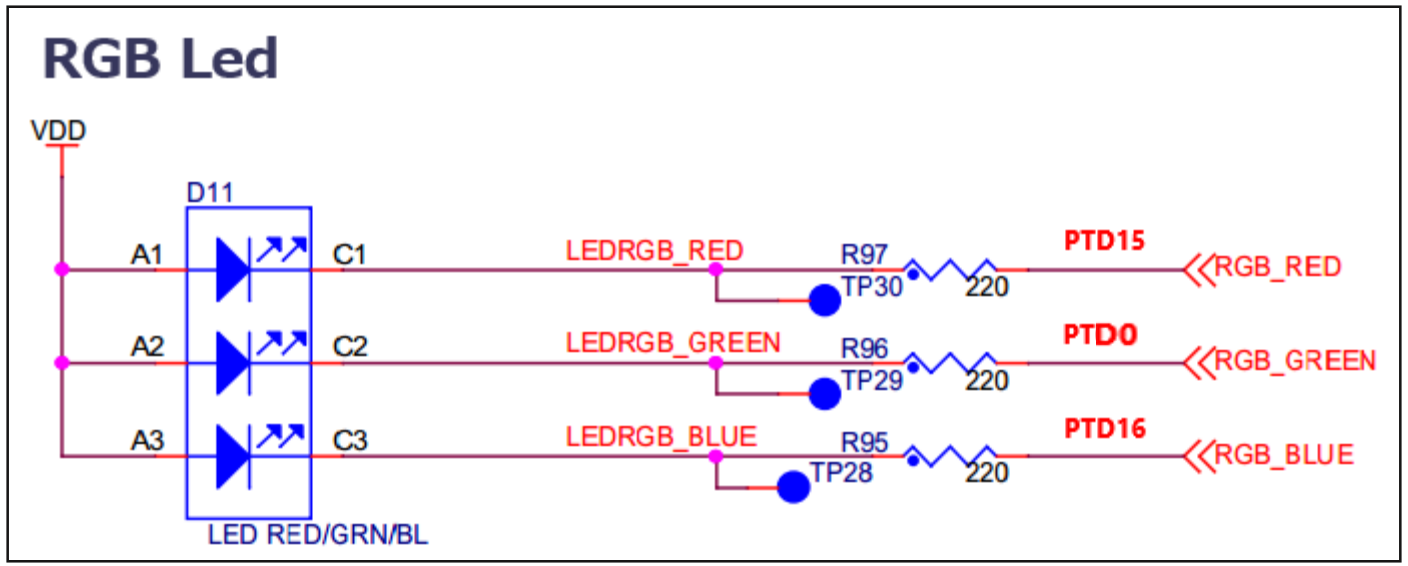
GPIO typically used for:

- Reading digital signal
- Generating triggers for external components
- Issuing interrupts
- Waking up the processor



1.2. Schematic

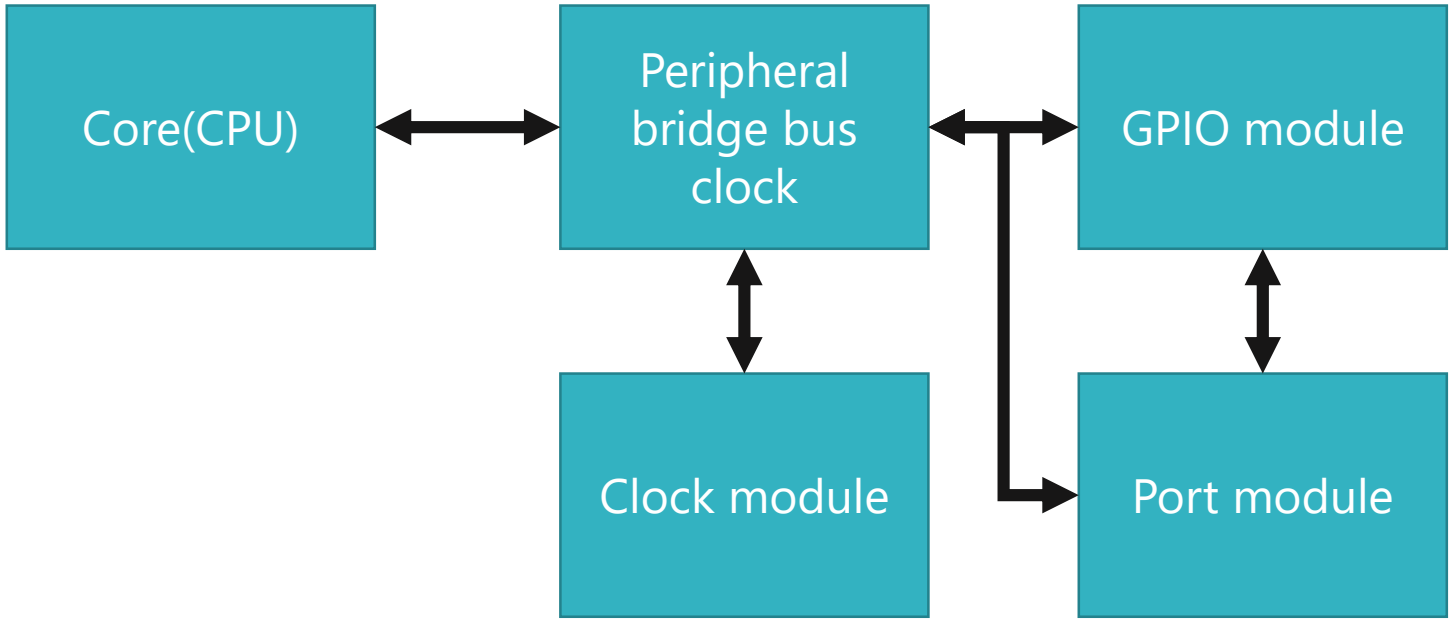




1.3. Assignment

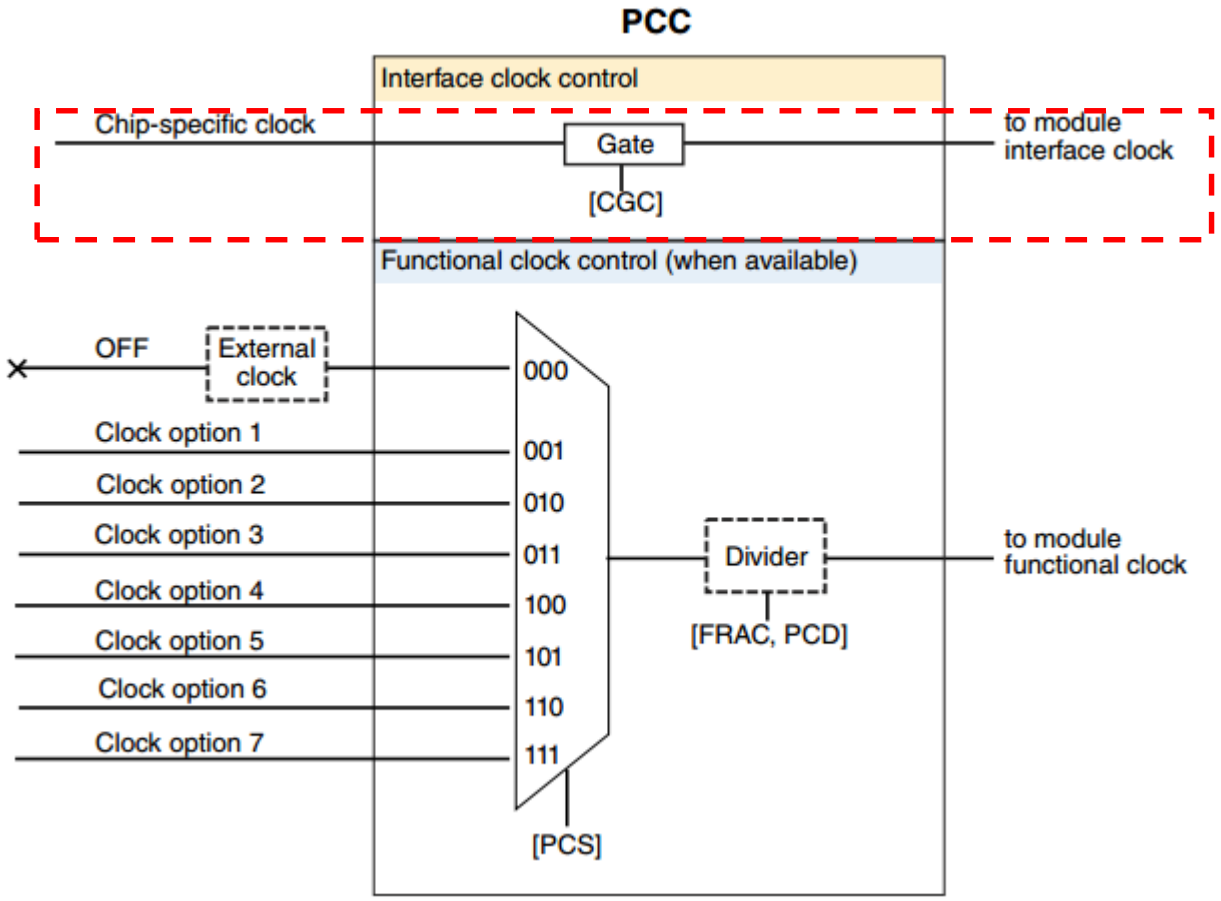
Blink Red Led

2. Modules overview



The clock signal is used to maintain the synchronicity and result validity between blocks(CPU, GPIO, Port). Allow Core(CPU) able to be access to the registers of GPIO.

2.1. Peripheral Clock Controller (PCC)



PCC Block Diagram

2.1. Peripheral Clock Controller (PCC)

PCC PORTx Register (PCC_PORTx)

- PCC PORTA Register (PCC_PORTA)
- PCC PORTB Register (PCC_PORTB)
- PCC PORTC Register (PCC_PORTC)
- PCC PORTD Register (PCC_PORTD)
- PCC PORTE Register (PCC_PORTE)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	PR	CGC	Reserved	0		0			0							
W																
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0												0	0		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Field	Function
30	Clock Gate Control
CGC	This read/write bit enables the interface clock for the peripheral, allowing access to the module's registers. It also controls whether the clock selection and divider options can be modified. 0b - Clock disabled. The current clock selection and divider options are not locked and can be modified. 1b - Clock enabled. The current clock selection and divider options are locked and cannot be modified.

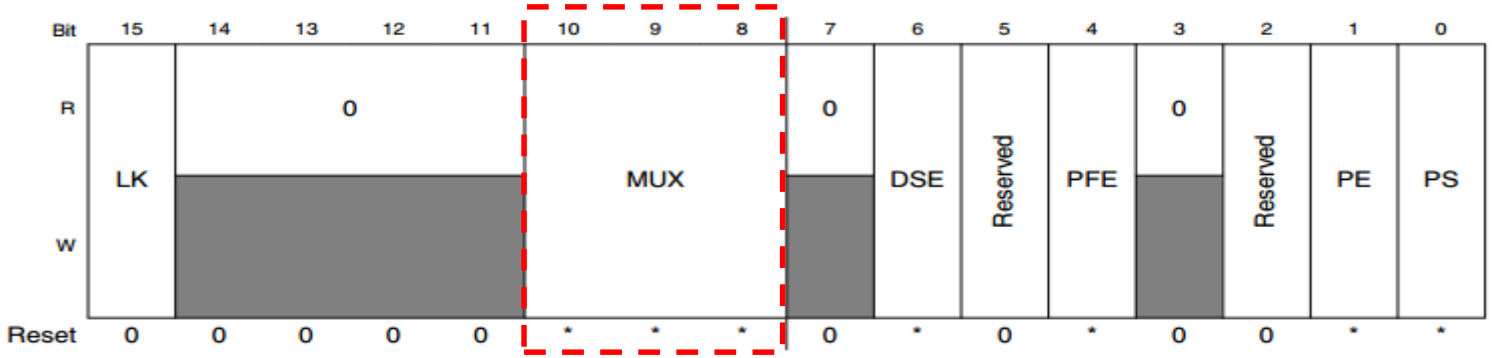
2.2. PORT module

Port Control and Interrupts (PORT) features:

- Port control
  - Pullup or pulldown enable
  - Drive strength
  - Passive input filter enable
  - Pin Muxing mode
- Digital input filter
- Pin interrupt
  - Asynchronous wake-up in low-power modes
  - Support for edge sensitive (rising, falling, both)

2.2. PORT module

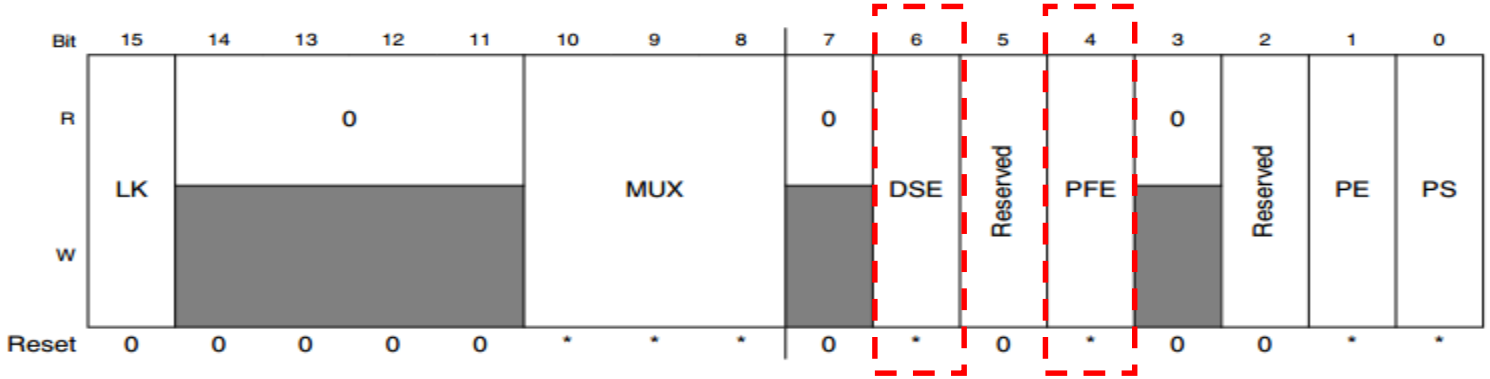
Pin Control Register n (PORT_PCR*n*)



Field	Description
10–8 MUX	Pin Mux Control Not all pins support all pin muxing slots. Unimplemented pin muxing slots are reserved and may result in configuring the pin for a different pin muxing slot. The corresponding pin is configured in the following pin muxing slot as follows: 000 Pin disabled (Alternative 0) (analog). 001 Alternative 1 (GPIO). 010 Alternative 2 (chip-specific). 011 Alternative 3 (chip-specific). 100 Alternative 4 (chip-specific). 101 Alternative 5 (chip-specific). 110 Alternative 6 (chip-specific). 111 Alternative 7 (chip-specific).

2.2. PORT module

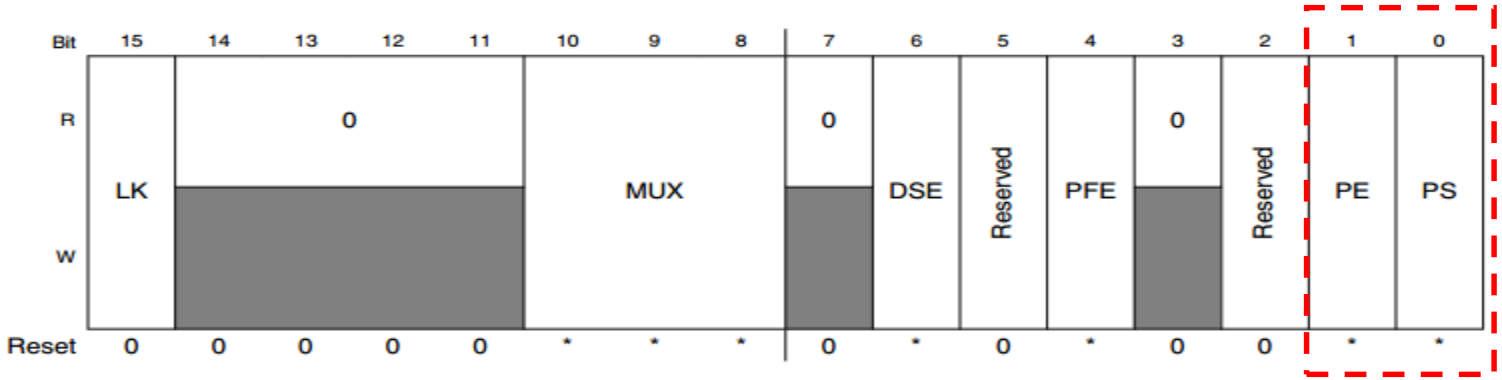
Pin Control Register n (PORT_PCR*n*)



6 DSE	Drive Strength Enable Drive strength configuration is valid in all digital pin muxing modes. 0 Low drive strength is configured on the corresponding pin, if pin is configured as a digital output. 1 High drive strength is configured on the corresponding pin, if pin is configured as a digital output.
4 PFE	Passive Filter Enable Passive filter configuration is valid in all digital pin muxing modes. 0 Passive input filter is disabled on the corresponding pin. 1 Passive input filter is enabled on the corresponding pin, if the pin is configured as a digital input. Refer to the device data sheet for filter characteristics.

2.2. PORT module

Pin Control Register n (PORT_PCR*n*)



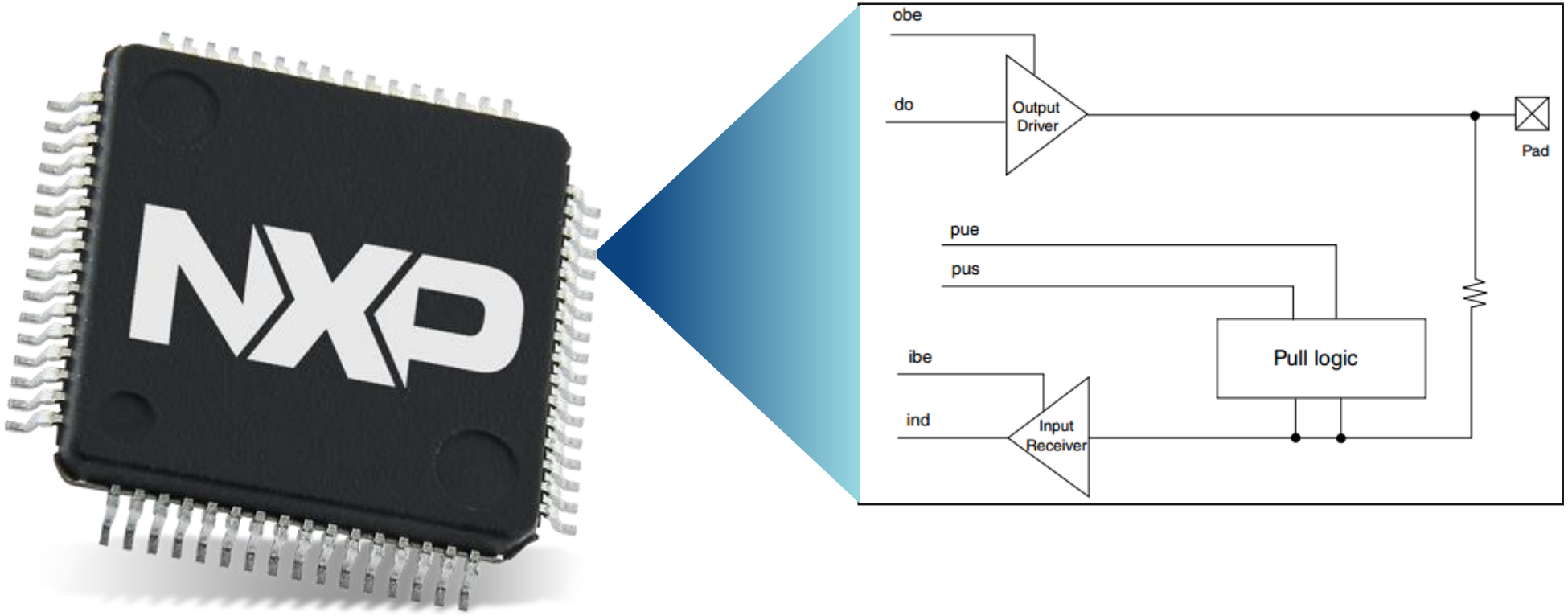
1 PE	Pull Enable Pull configuration is valid in all digital pin muxing modes. 0 Internal pullup or pulldown resistor is not enabled on the corresponding pin. 1 Internal pullup or pulldown resistor is enabled on the corresponding pin, if the pin is configured as a digital input.
0 PS	Pull Select Pull configuration is valid in all digital pin muxing modes. 0 Internal pulldown resistor is enabled on the corresponding pin, if the corresponding PE field is set. 1 Internal pullup resistor is enabled on the corresponding pin, if the corresponding PE field is set.

2.3. GPIO module

GPIO module features:

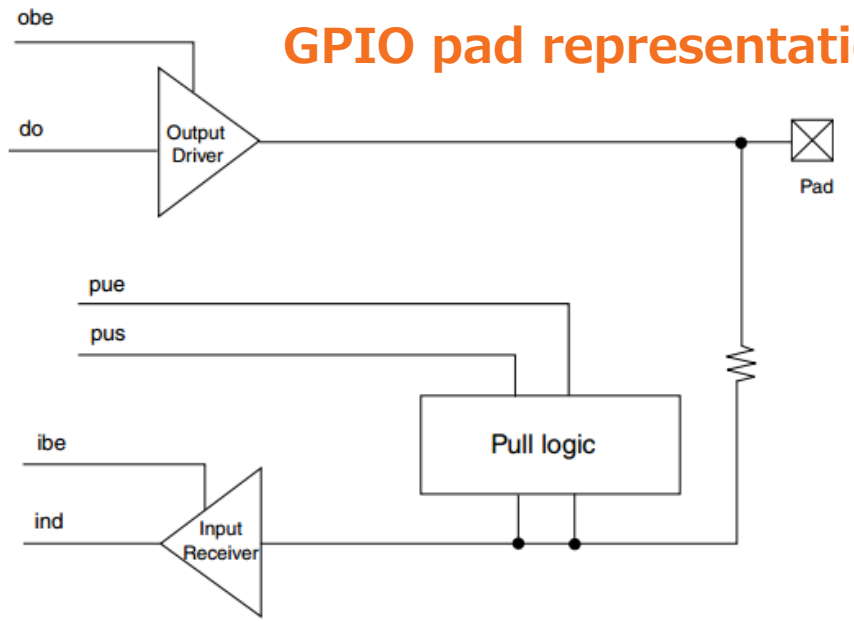
- Port Data Input register visible in all digital
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register

2.3. GPIO module



2.4. GPIO Pad

GPIO pad representation



Signal name	Direction	Description
pad	I/O	I/O to external world
do	I	Data coming from the core into the pad
obe	I	Enable output driver
pue	I	0: Disable internal pullup or pulldown resistor 1: Enable internal pullup or pulldown resistor
pus	I	0: Enable internal pulldown resistor if pue is set 1: Enable internal pullup resistor if pue is set
ibe	I	Enable input receiver
ind	O	Data coming out of the pad into the core

Pad Signal description

obe	do	pad	Description
0	X	Z	Output buffer disabled, pad hi-Z (If not configured as input)
1	0/1	0/1	Output buffer enable, pad = do

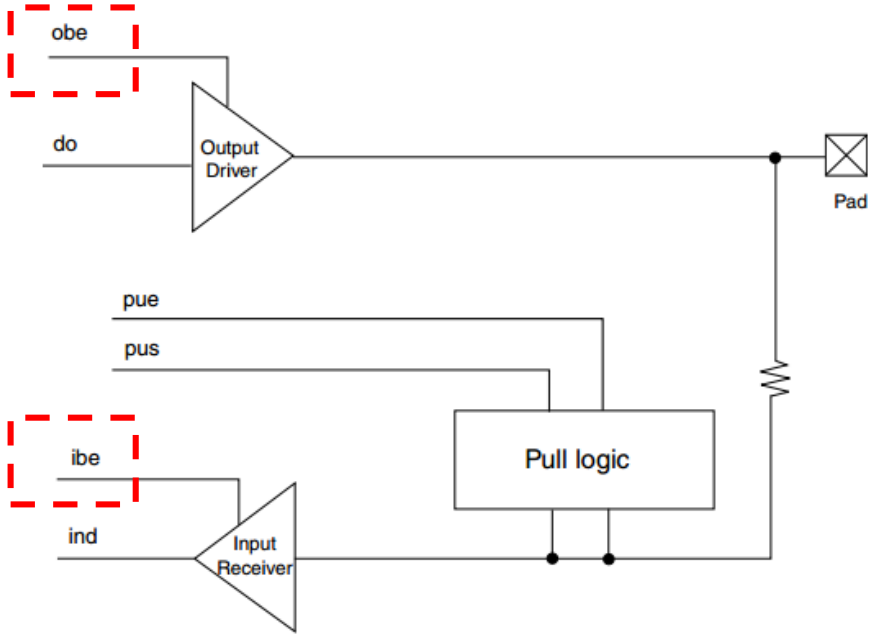
pue	pus	pad	Description
0	X	Z	Weak pull disabled. Pad retains previous state
1	0	0	Weak pull down enabled
1	1	1	Weak pull up enabled

ibe	pad	ind	Description
0	X	0	Input buffer disabled, ind gets low
1	0/1	0/1	Input buffer enabled, ind = pad

Truth table

2.4. GPIO Pad

Registers configure for ode and ibe:



GPIO pad representation

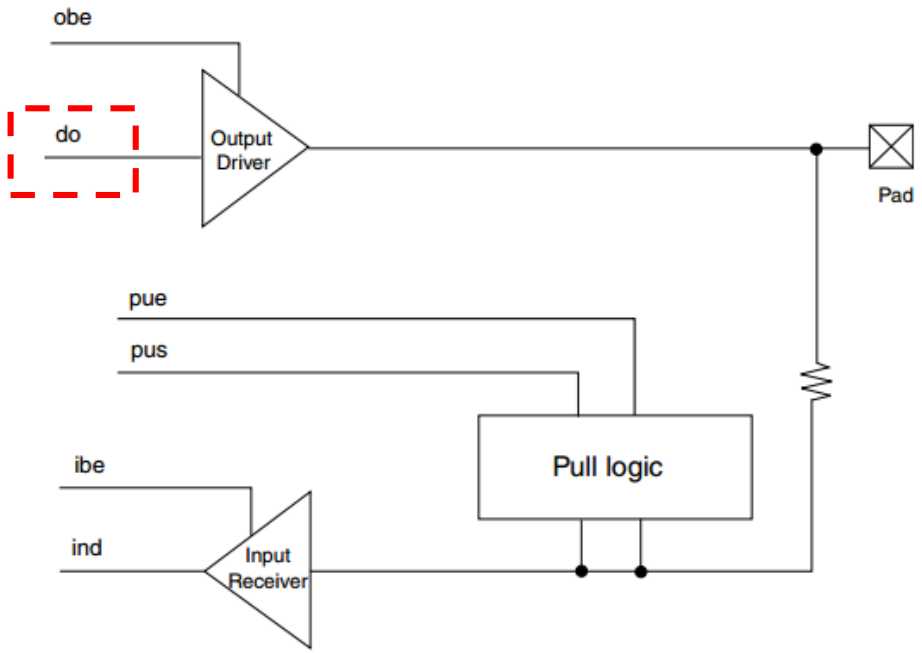
Port Data Direction Register (PDDR)

→ The PDDR configures the individual port pins for input or output.

Field	Function
31-0	Port Data Direction
PDD	Configures individual port pins for input or output. 0b - Pin is configured as general-purpose input, for the GPIO function. The pin will be high-Z if the port input is disabled in GPIOx_PIDR register. 1b - Pin is configured as general-purpose output, for the GPIO function.

2.4. GPIO Pad

Registers configure for do:



GPIO pad representation

Port Data Output Register (PDOR)

Field	Function
31-0	Port Data Output
PDO	Register bits for unbonded pins return an undefined value when read. 0b - Logic level 0 is driven on pin, provided pin is configured for general-purpose output. 1b - Logic level 1 is driven on pin, provided pin is configured for general-purpose output.

Port Set Output Register (PSOR)

Field	Function
31-0	Port Set Output
PTSO	Writing to this register updates the contents of the corresponding bit in the PDOR as follows: 0b - Corresponding bit in PDORn does not change. 1b - Corresponding bit in PDORn is set to logic 1.

Port Clear Output Register (PCOR)

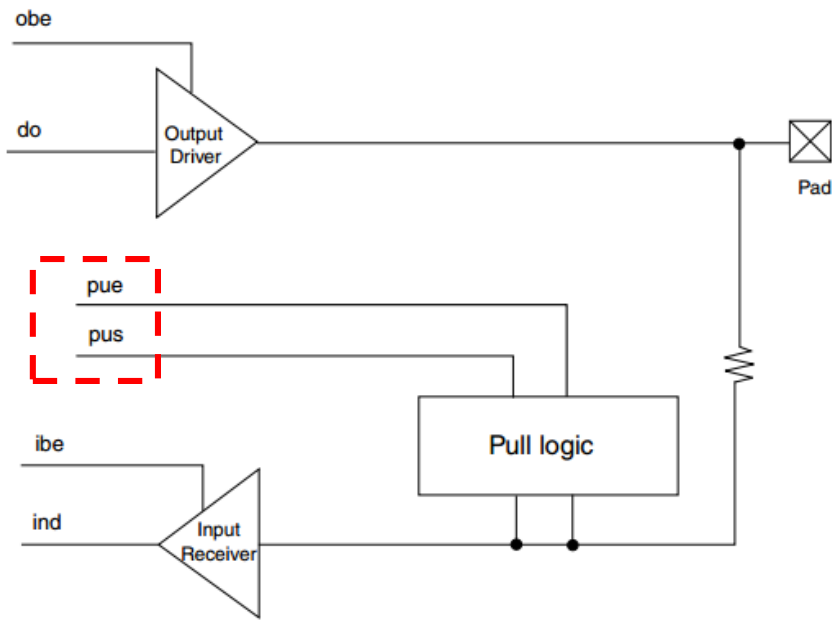
Field	Function
31-0	Port Clear Output
PTCO	Writing to this register updates the contents of the corresponding bit in the Port Data Output Register (PDOR) as follows: 0b - Corresponding bit in PDORn does not change. 1b - Corresponding bit in PDORn is cleared to logic 0.

Port Toggle Output Register (PTOR)

Field	Function
31-0	Port Toggle Output
PTTO	Writing to this register updates the contents of the corresponding bit in the PDOR as follows: 0b - Corresponding bit in PDORn does not change. 1b - Corresponding bit in PDORn is set to the inverse of its existing logic state.

2.4. GPIO Pad

Registers configure for pue and pus:



GPIO pad representation

Pin Control Register n (PORT_PCRn)

→ This register configures Pullup or pulldown enable

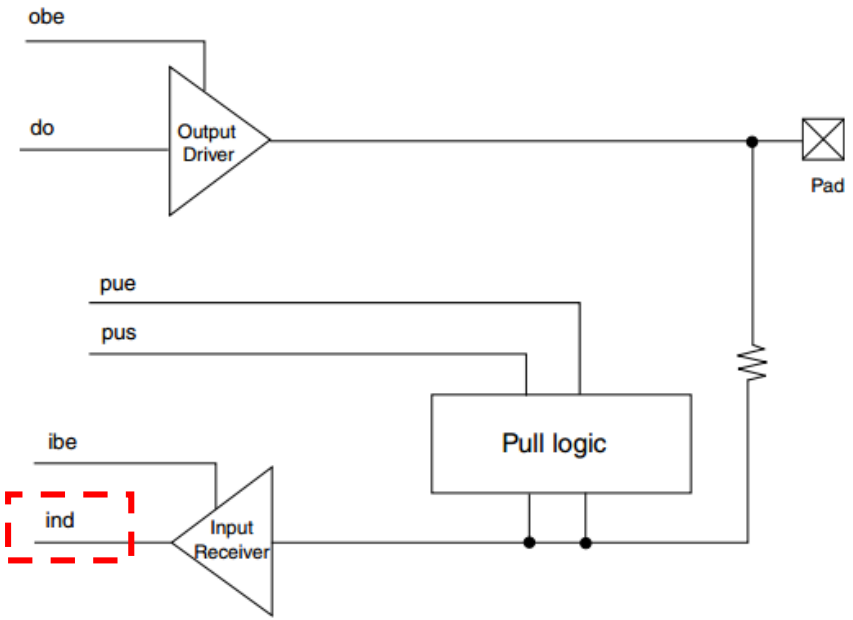
Field	Description
1 PE	Pull Enable Pull configuration is valid in all digital pin muxing modes. 0 Internal pullup or pulldown resistor is not enabled on the corresponding pin. 1 Internal pullup or pulldown resistor is enabled on the corresponding pin, if the pin is configured as a digital input.
0 PS	Pull Select Pull configuration is valid in all digital pin muxing modes. 0 Internal pulldown resistor is enabled on the corresponding pin, if the corresponding PE field is set. 1 Internal pullup resistor is enabled on the corresponding pin, if the corresponding PE field is set.

Pull-Up: Small internal resistor to Vcc

Pull-Down: Small internal resistor to Gnd

2.4. GPIO Pad

Registers configure for ind:



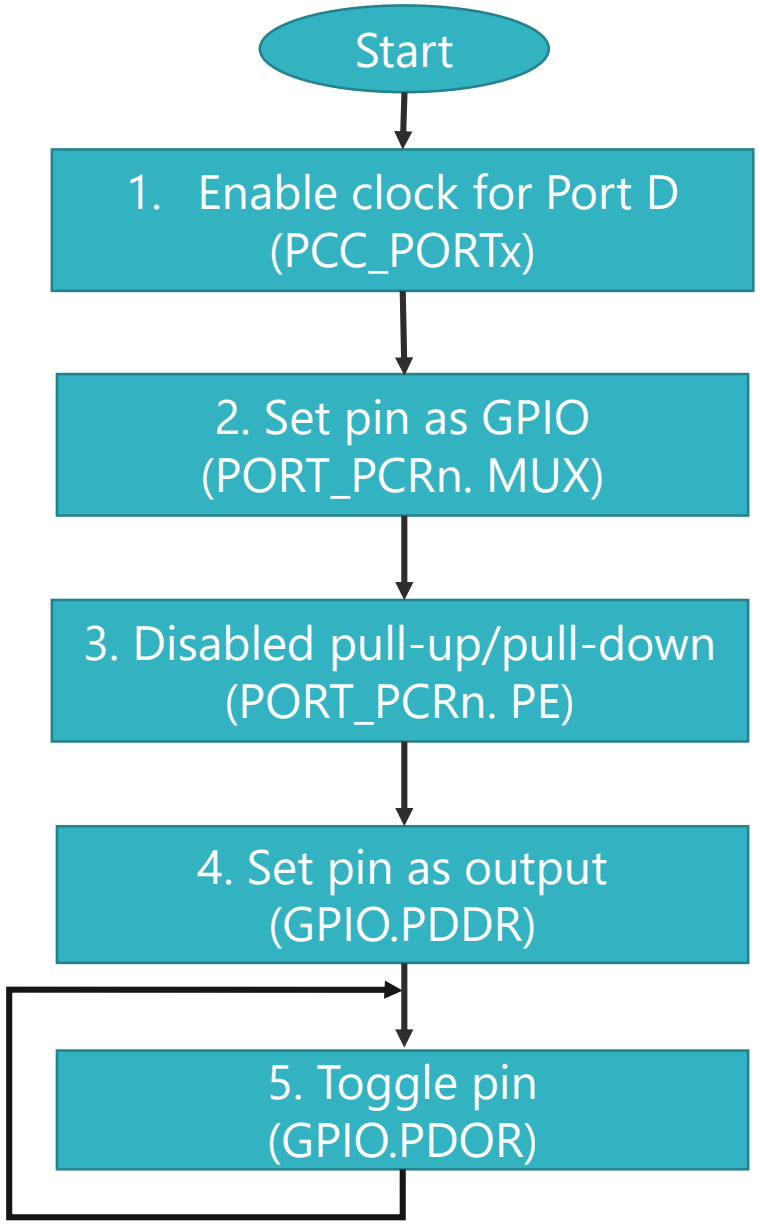
GPIO pad representation

Port Data Input Register (PDIR)

→ This register captures the logic levels that are driven into each general-purpose input pin.

Field	Function
31-0	Port Data Input
PDI	Reads 0 at the unimplemented pins for a particular device. Pins that are not configured for a digital function read 0. If the Port Control and Interrupt module is disabled, then the corresponding bit in PDIR does not update. 0b - Pin logic level is logic 0, or is not configured for use by digital function. 1b - Pin logic level is logic 1.

2.5. Configure GPIO pin to output



2.5.1. Finding address register

No.	Register	Address
1	PCC_PORTD	
2	PORT_PCR15	
3	GPIOD.PDDR	
4	GPIOD. PDOR	

2.5.2. Practice

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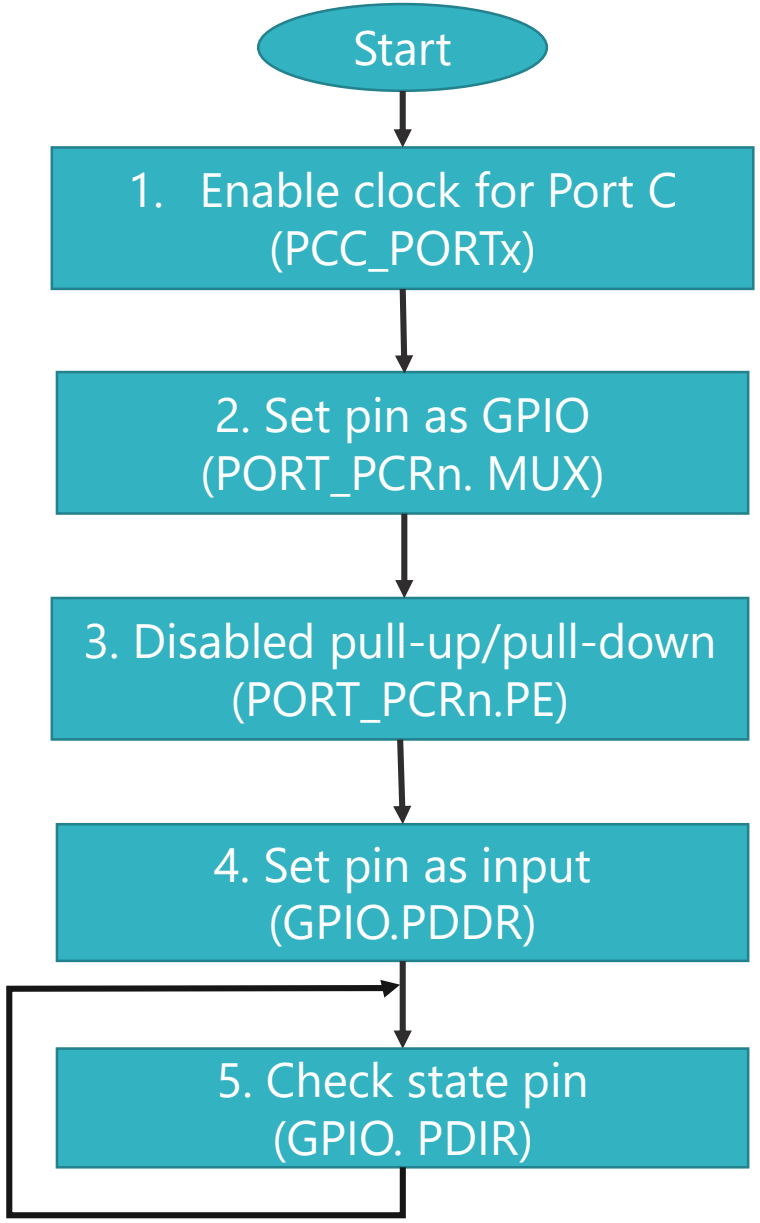
2.6. Configure GPIO pin to input



2.6.1. Finding address register

No.	Register	Address
1	PCC_PORTC	
2	PORT_PCR13	
3	GPIOC.PDDR	
4	GPIOC.PDIR	

Read state SW3 (PTC13)


Thank you