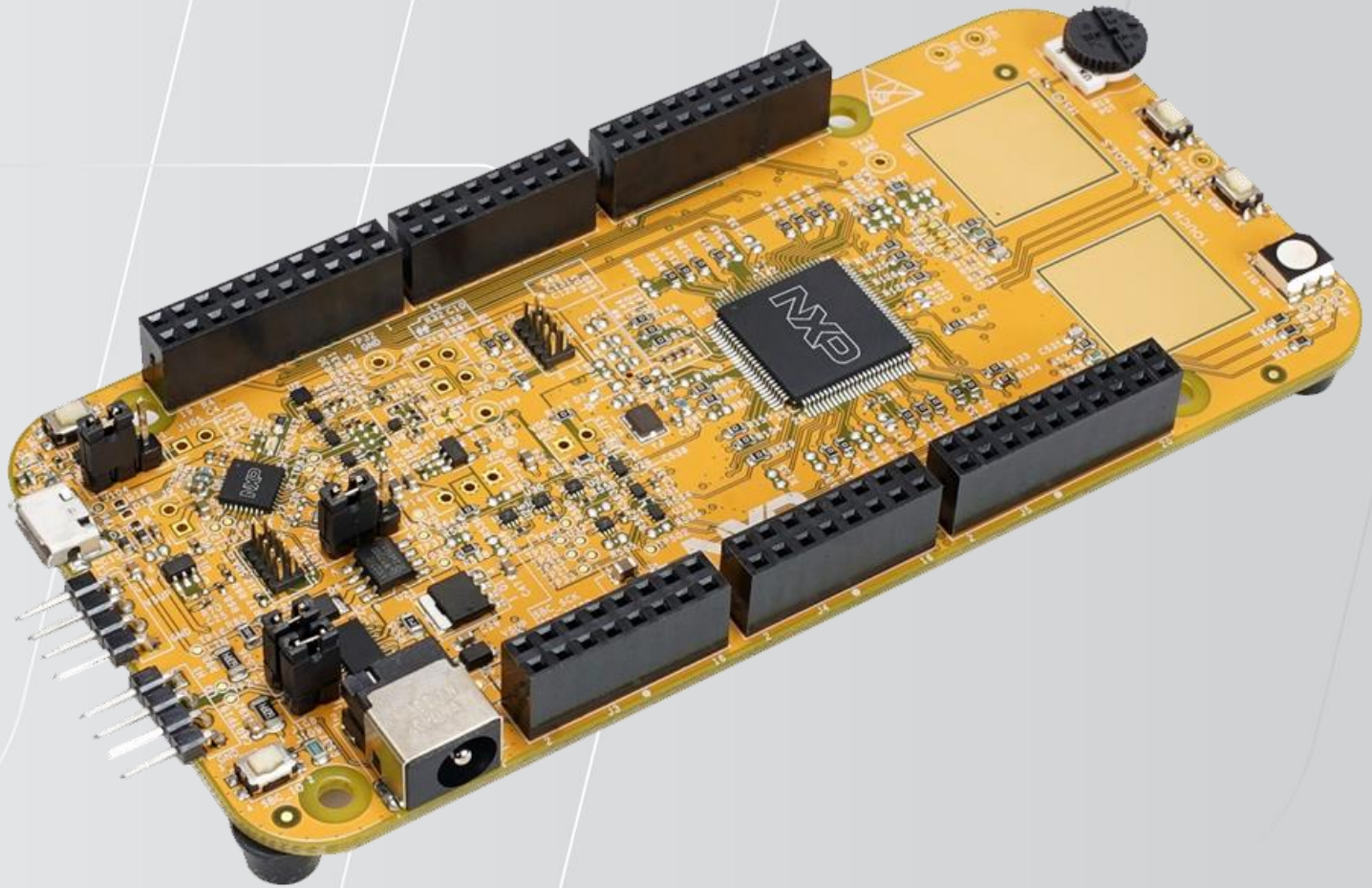
Clocking



24 Aug 2024

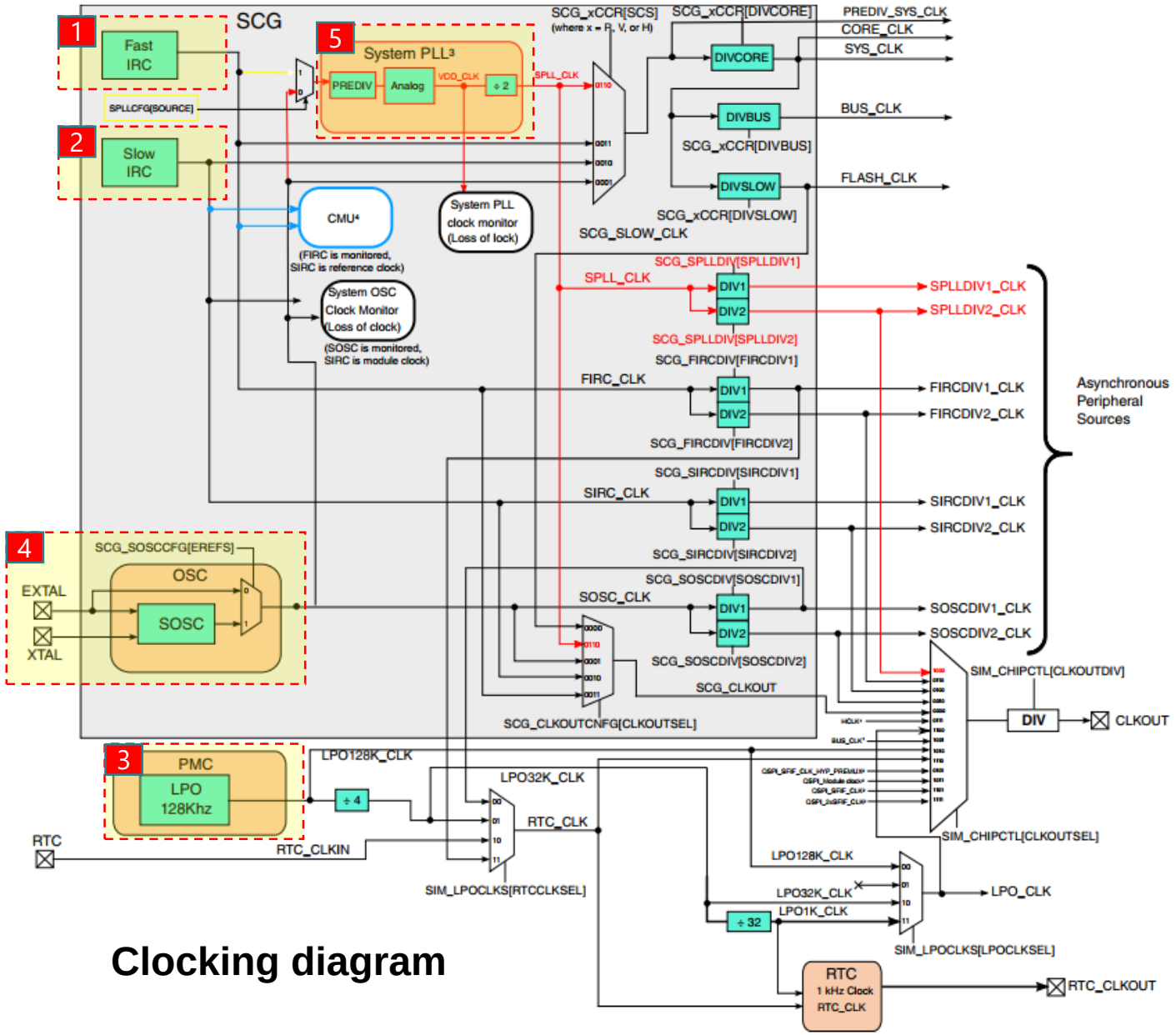
OUTLINE

1. Clock Distribution
2. Power Management
3. Internal clocking requirements
4. Clock Gating
5. System Clock Generator (SCG)
6. Peripheral Clock Controller (PCC)
7. Configuration

1. Clock Distribution

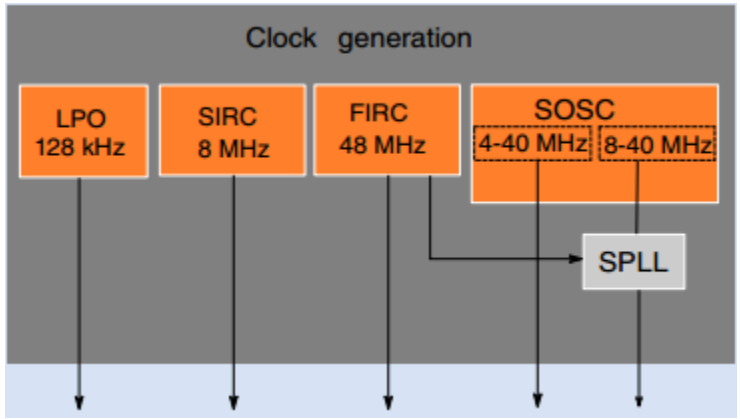
- The **System Clock Generator (SCG)** module is used to **generate** most of the **clocks used by the device**.
- The SCG module **controls** which **clock source** (internal references, external crystals, external clocks) is used to **derive system clocks**.
- The SCG also divides the selected clock source into a variety of clock domains, including clocks for system bus masters, system bus slaves, and flash memory.
- Clock selection for most **modules** is controlled by the **PCC module**.
- The **default** configuration out of **reset** has the CPU clocked by the **Fast IRC** (FIRC_CLK). The clocks (for example, CORE_CLK, FLASH_CLK, and BUS_CLK) are configured in the SCG module.

1. Clock Distribution



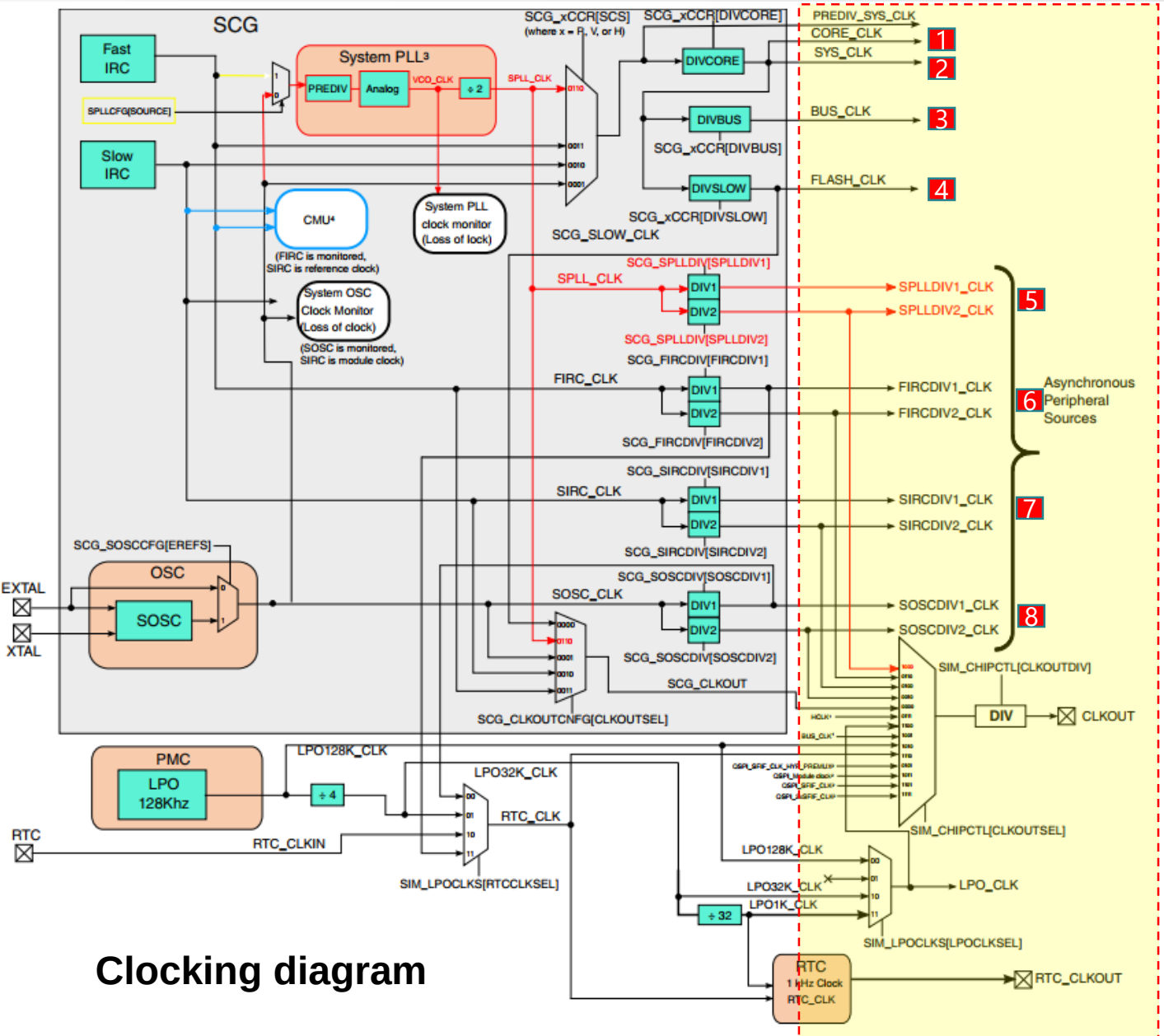
Clocking diagram

Clock Source :



No	Clock
1	FIRC-Fast Internal Reference Clock
2	SIRC-Slow Internal Reference Clock
3	LPO-Low Power Oscillator
4	***SOSC- System OScillator Clock***
5	***SPLL-System Phase-Locked Loop***

1. Clock Distribution



Clocking diagram

No.	Clock	Description
1	CORE_CLK	Clocks the Arm core
2	SYS_CLK	Clocks the Crossbar, NVIC, Flash controller, FTM, PDB
3	BUS_CLK	Clocks the chip peripherals.
4	FLASH_CLK	Clocks the flash module.
5	SPLLDIV1_CLK, SPLLDIV2_CLK	Divided SPLL_CLK
6	FIRCDIV1_CLK, FIRCDIV2_CLK	Divided FIRC_CLK
7	SIRCDIV1_CLK, SIRCDIV2_CLK	Divided SIRC_CLK
8	SOSCDIV1_CLK, SOSCDIV2_CLK	Divided SOSC_CLK

Table of Clock descriptions

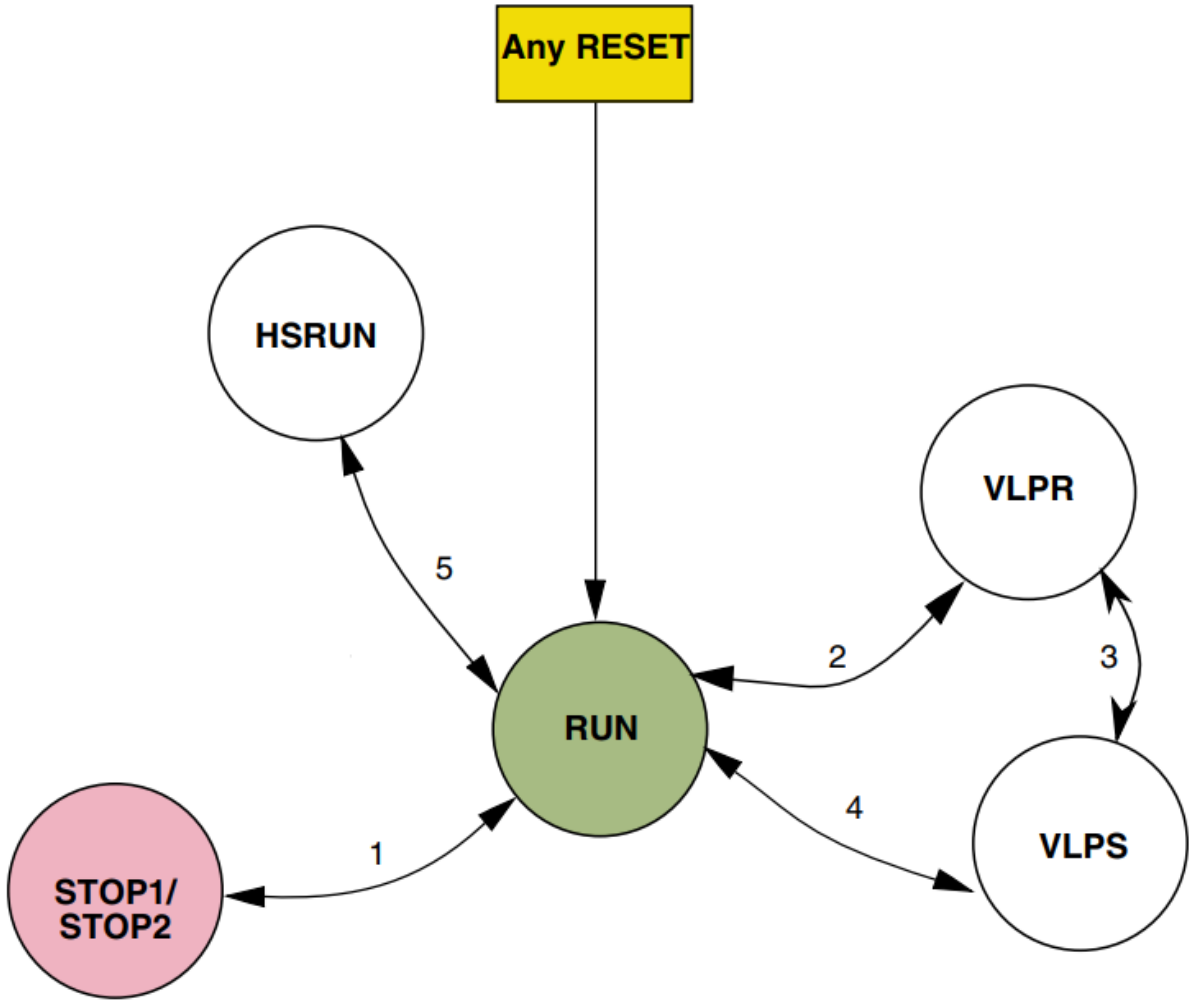
2. Power Management

Power modes:

No.	Mode	Description
1	RUN	The **MCU** can be **run at full speed and the internal supply is fully regulated**, that is, in run regulation. This mode is also referred to as Normal Run mode.
2	HSRUN	The **MCU** can be run at a **faster frequency** compared with RUN mode and the internal supply is fully regulated. See the Power Management chapter for details about the maximum allowable frequencies.
3	STOP	The **core clock** is gated **off**. There are two variants of stop mode - STOP1 and STOP2 . In **STOP1 system clock** as well as **bus clocks** are **gated** . In **STOP2** bus clocks keep running whereas **system clocks** are **gated**.
4	VLPR Very Low Power Run	**The core, system, bus, and flash clock maximum frequencies** are **restricted** in this mode. See the Power Management chapter for details about the maximum allowable frequencies.
5	VLPS Very Low Power Stop	The **core clock** is gated **off**. System clocks to other masters and bus clocks are gated off after all stop acknowledge signals from supporting peripherals are valid.

2. Power Management

Power mode state transition diagram:



Power Mode Status register (SMC_PMSTAT)

Field	Description
31–8 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
PMSTAT	Power Mode Status **NOTE:** When debug is enabled, the PMSTAT will not update to STOP or VLPS **NOTE:** When a STOP mode is enabled, the PMSTAT will not update to STOP 0000_0001 Current power mode is RUN. 0000_0010 Reserved. 0000_0100 Current power mode is VLPR. 0000_1000 Reserved. 0001_0000 Current power mode is VLPS. 0010_0000 Reserved 0100_0000 Reserved 1000_0000 Current power mode is HSRUN

3. Internal clocking requirements

The **clock dividers** are **programmed** via the **SCG module's clock divider registers**.

The following **requirements** must be met when **configuring** the clocks for this chip:

- **CORE_CLK** and **SYS_CLK** clock frequency must be **112 MHz or less** in **HSRUN** mode and **80 MHz or less than** in **normal RUN** mode (but not configured to be less than BUS_CLK).

- **BUS_CLK** frequency must be programmed to **56 MHz or less** in **HSRUN**, **48 MHz or less** in **RUN**(when using PLL as system clock source maximum bus clock frequency is 40 MHz), and an integer divide of the CORE_CLK.

- **FLASH_CLK** frequency must be programmed to **28 MHz or less** in **HSRUN**, **26.67 MHz or less** in **RUN**, and an integer divide of the CORE_CLK. The core clock to flash clock ratio is limited to a max value of 8.

3. Internal clocking requirements

Following table summarizes the maximum frequencies:

No.	Clock	HSRUN	RUN	VLPR	Notes
1	CORE_CLK, SYS_CLK	112 MHz	80 MHz	4 MHz	Must be configured to be more than or equal to BUS_CLK.
2	BUS_CLK	56 MHz	48 MHz (40 MHz when using PLL as system clock source)	4 MHz	Must be integer divide of the CORE_CLK.
3	FLASH_CLK	28 MHz	28 MHz	1 MHz	Must be integer divide of the CORE_CLK. The core clock to flash clock ratio is limited to a max value of 8.

4. Clock Gating

- The **clock** to each **module** can be individually **gated** on and **off** using the **PCC** module.
- After any **reset**, **PCC disables** the **clock** to the corresponding **module** to conserve power.
- Prior to **initializing** a module, **set** the corresponding **clock gating control bits** in **PCC register** to **enable** the **clock**. **Before** turning **off** the clock, make sure to **disable** the **module**.
- **Any bus access** to a **peripheral** that has its **clock disabled** generates an **error** termination.

Module name	Bus interface clock [1]	Bus interface clock[1] gating	Peripheral functional clock	Additonal clocks	Comments and maximum frequencies
		Gated by [CGC] of PCC	Clocks controlled by [PCS] of PCC		
Communications					
LPUART	BUS_CLK	Yes	SPLLDIV2_CLK, FIRCDIV2_CLK, SIRCDIV2_CLK, SOSCDIV2_CLK	—	Maximum frequency governed by BUS_CLK

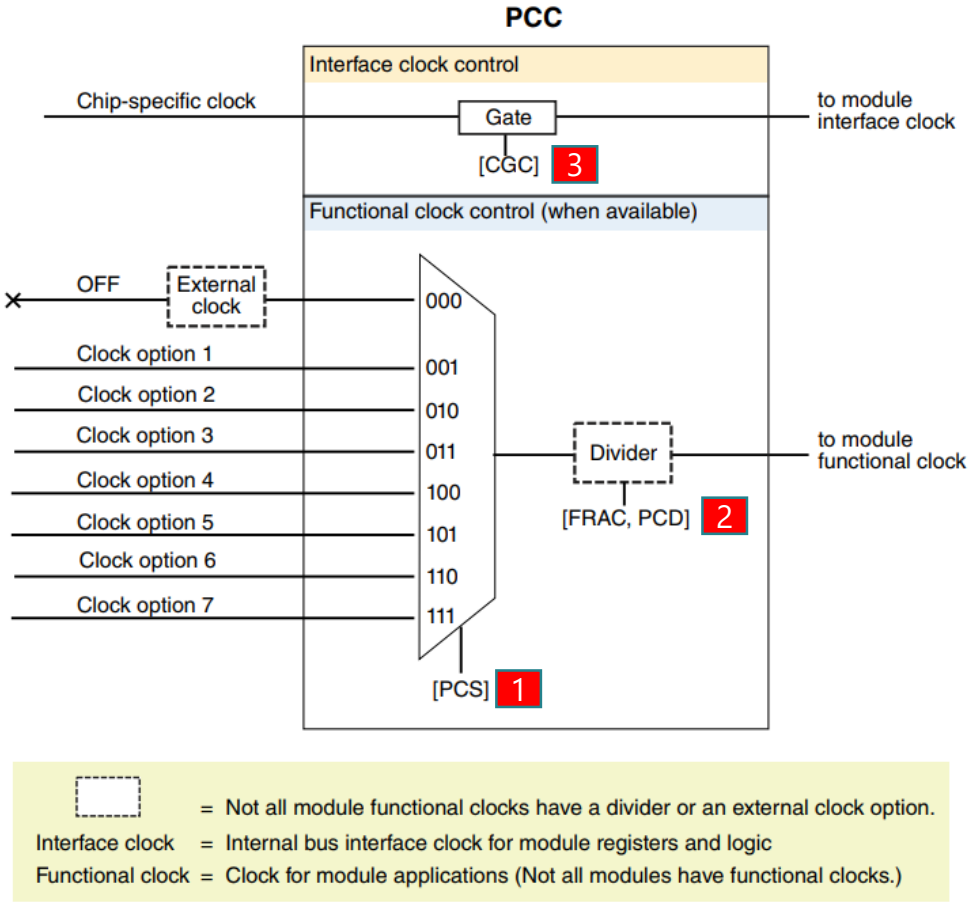
5. System Clock Generator (SCG)

- The **system clock generator (SCG)** module provides the **system clocks** of the MCU.
- The **SCG** can select either the output clock of the **SPLL** or a **SCG reference clock** (SIRC, FIRC, and SOSC) as the source for the MCU system clocks.
- The SCG also supports operation with **crystal oscillators**, which allows an external crystal, ceramic resonator, or another external clock source to produce the external reference clock.

Address offset (hex)	Register name	Description
10	Clock Status Register (SCG_CSR)	System Clock Source, DIVCORE, DIVBUS, DIVSLOW
14	Run Clock Control Register (SCG_RCCR)	Run mode
18	VLPR Clock Control Register (SCG_VCCR)	VLPR mode
1C	HSRUN Clock Control Register (SCG_HCCR)	HSRUN mode
20	SCG CLKOUT Configuration Register (SCG_CLKOUTCNFG)	CLKOUT pin.
100	System OSC Control Status Register (SCG_SOSCCSR)	SOSC
104	System OSC Divide Register (SCG_SOSCDIV)	
108	System Oscillator Configuration Register (SCG_SOSCCFG)	
200	Slow IRC Control Status Register (SCG_SIRCCSR)	SIRC
204	Slow IRC Divide Register (SCG_SIRCDIV)	
208	Slow IRC Configuration Register (SCG_SIRCCFG)	
300	Fast IRC Control Status Register (SCG_FIRCCSR)	FIRC
304	Fast IRC Divide Register (SCG_FIRCDIV)	
308	Fast IRC Configuration Register (SCG_FIRCCFG)	
600	System PLL Control Status Register (SCG_SPLLCSR)	SPLL
604	System PLL Divide Register (SCG_SPLLDIV)	
608	System PLL Configuration Register (SCG_SPLLCFG)	

6. Peripheral Clock Controller (PCC)

- The **Peripheral Clock Control** (**PCC**) module **provides clock** control and **configuration** for on-chip **peripherals**.
- Each peripheral has its own clock control and configuration register.
- The PCC module enables software to configure the following clocking options for each peripheral:
  - Interface clock gating
  - Functional clock source selection
  - Functional clock divide values



7. Configuration

7.1. Configuration SOSC

7.2. Configuration SPLL

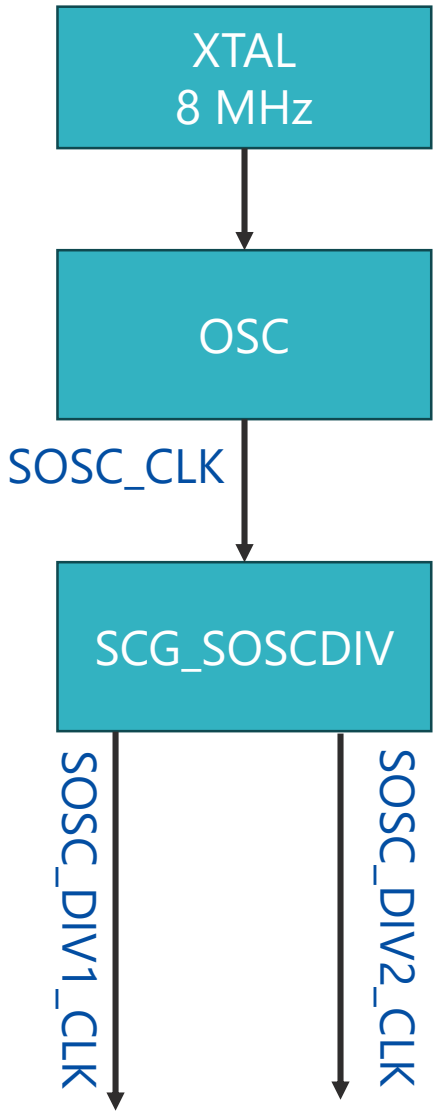
7.3. Configuration normal RUN mode

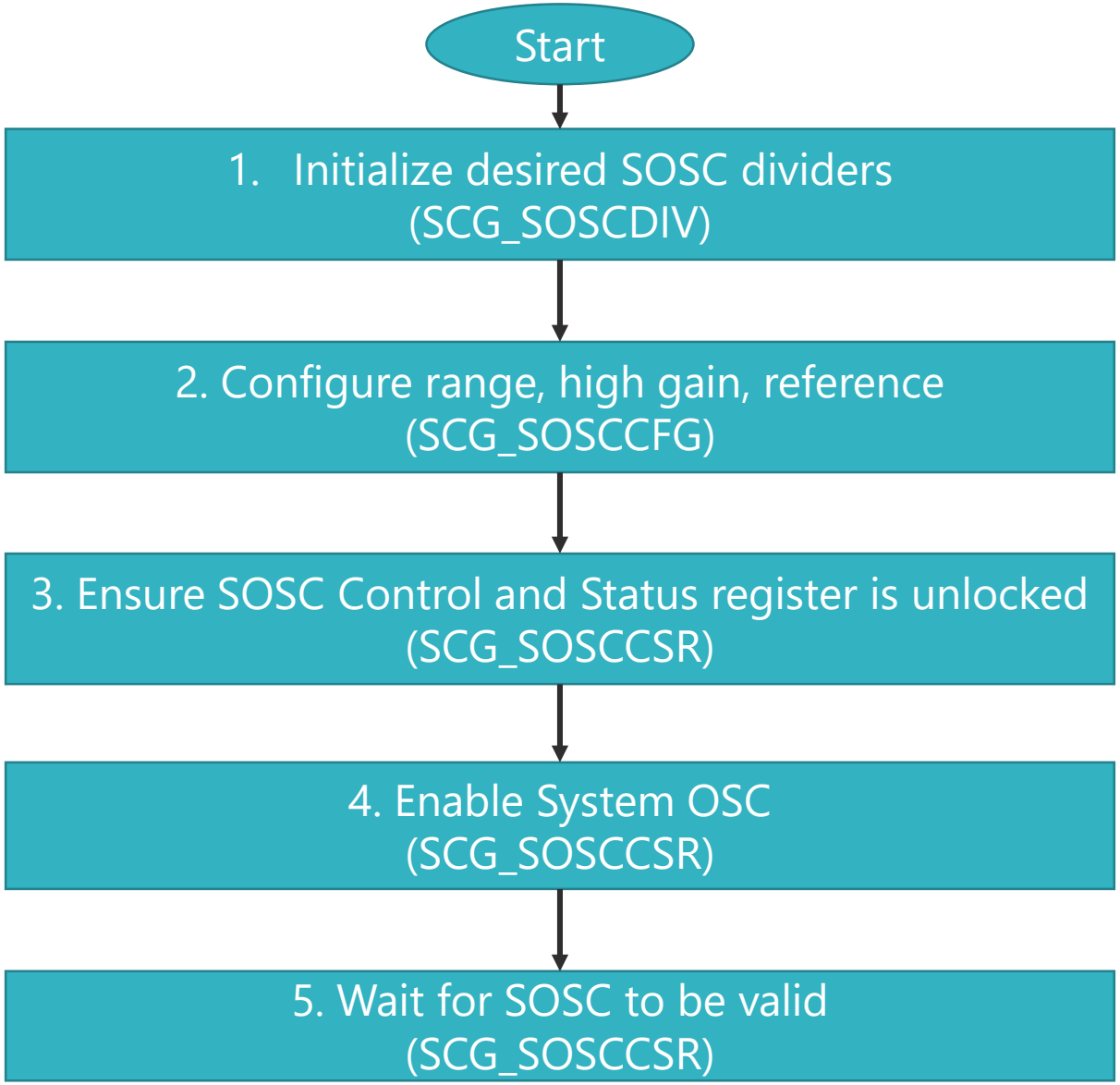
7.4. Transition to High Speed RUN mode

7.5. Configuration CLKOUT pin

7.1. Configuration SOSC

Initialize system oscillator (SOSC):





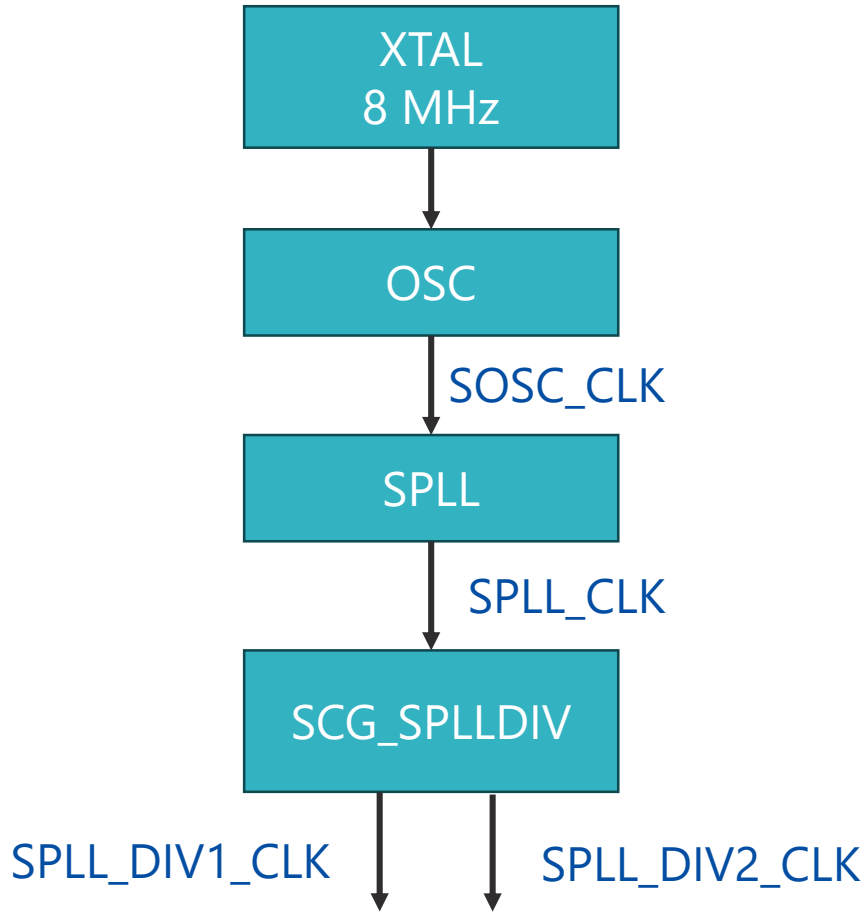
7.1. Assignment 1

Initialize system oscillator (SOSC):

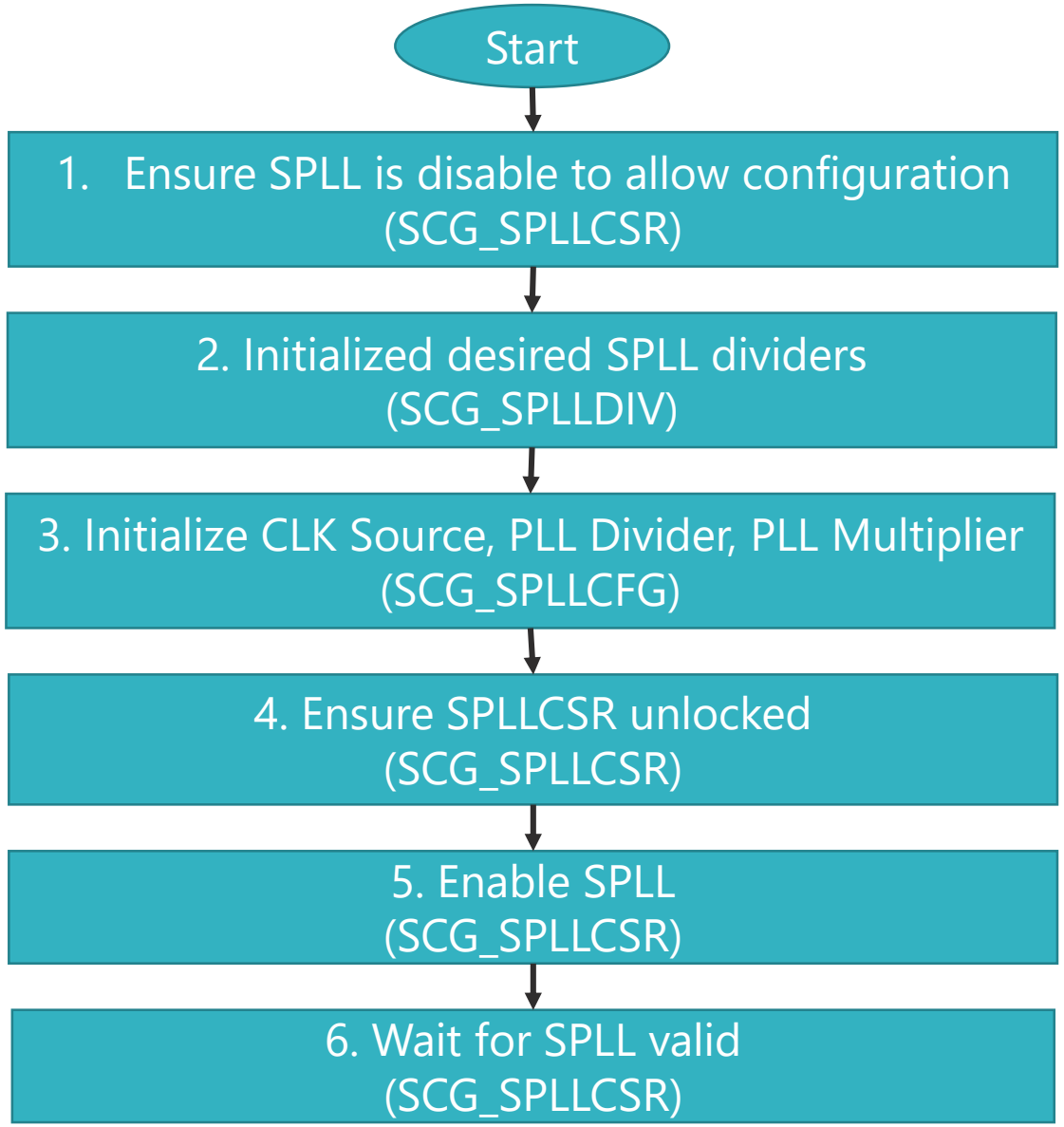
- Initialize system oscilator for 8 MHz xtal
- SOSC_DIV1_CLK: 4MHz
- SOSC_DIV2_CLK: 1MHz

7.2. Configuration SPLL

Initialize SPLL using SOSC:



SPLL_CLK =(VCO_CLK)/2
VCO_CLK = SPLL_SOURCE/(PREDIV+1) X (MULT+16)



7.2.1. Assignment 2

Initialize SPLL using SOSC:

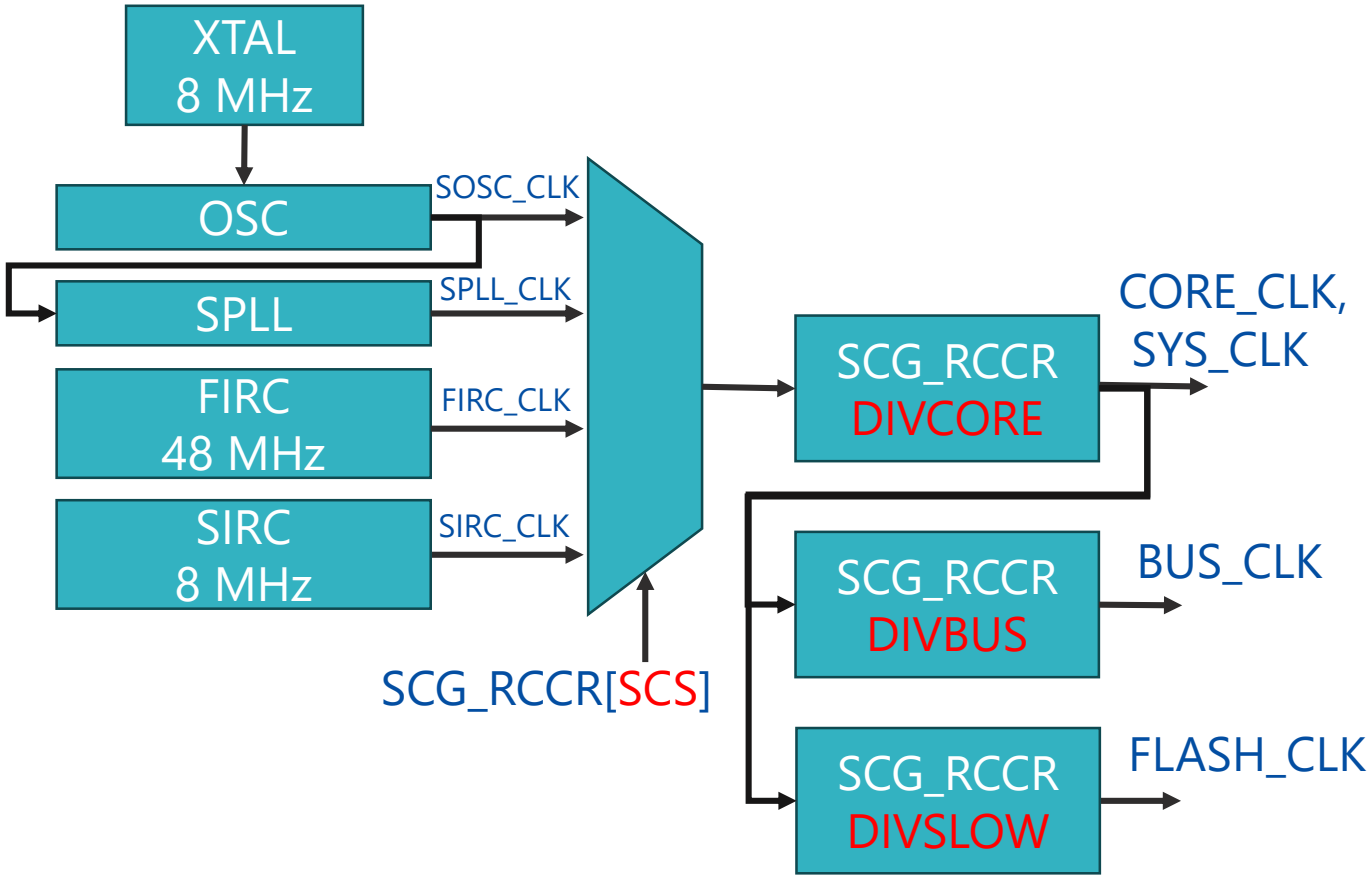
- Initialize SPLL to 160 MHz
- SPLL_DIV1_CLK: 80MHz
- SPLL_DIV2_CLK: 10MHz

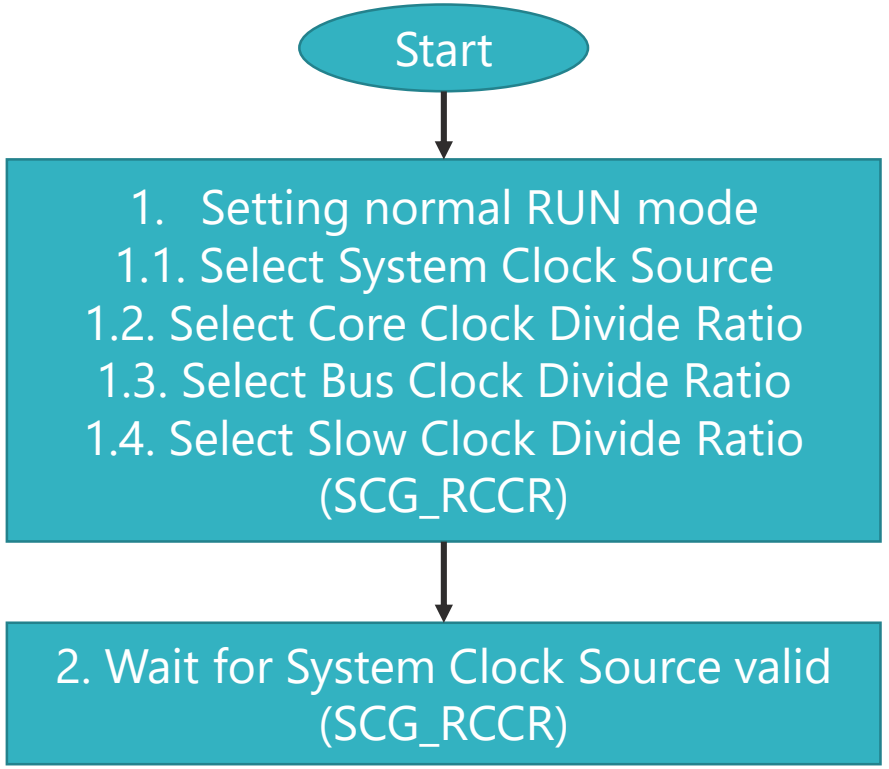
7.2.2. Assignment 3

Initialize SPLL using FIRC:

- Initialize SPLL to 160 MHz
- SPLL_DIV1_CLK: 80MHz
- SPLL_DIV2_CLK: 10MHz

7.3. Configuration normal RUN mode





Note: **Run Clock Control Register (SCG_RCCR)**
This register can only be written using a 32-bit write.

7.3.1. Assignment 4

Initialize normal RUN mode:

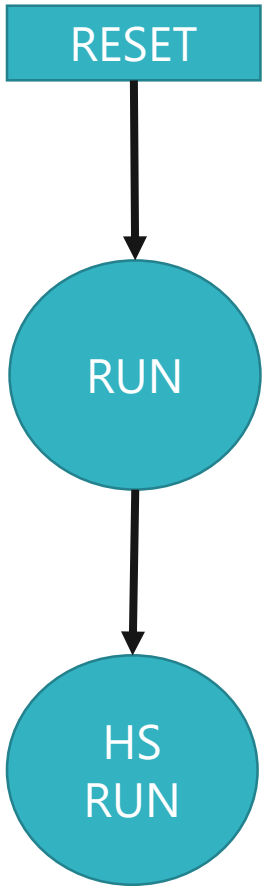
- Select SOSC as System clock source
- Core clock = 8 MHz
- Bus clock = 4 MHz
- Flash clock = 2 MHz

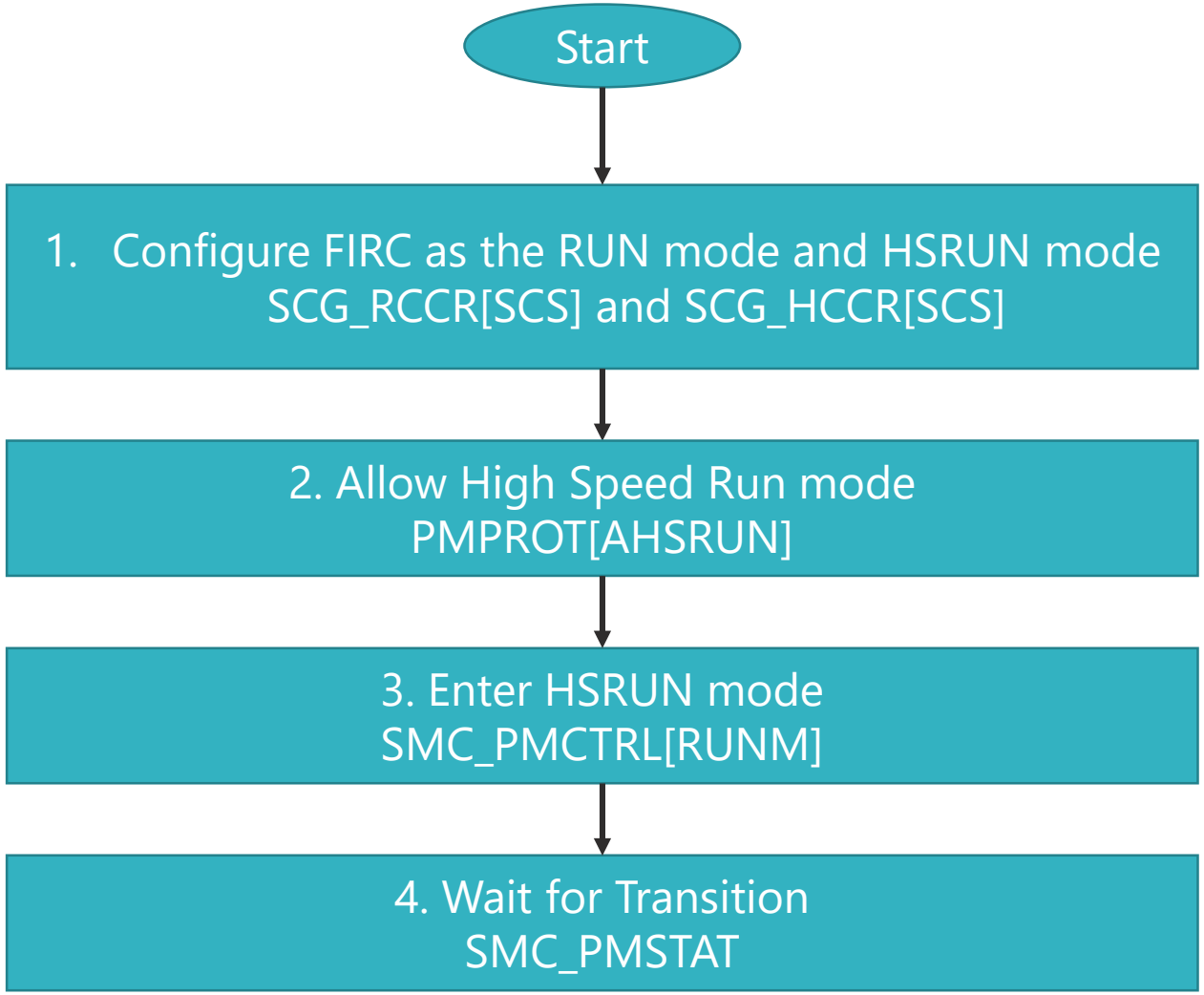
7.3.2. Assignment 5

Initialize normal RUN mode:

- Select SPLL as System clock source
- Core clock = 40 MHz
- Bus clock = 20 MHz
- Flash clock = 10 MHz

7.4. Transition to High Speed RUN mode



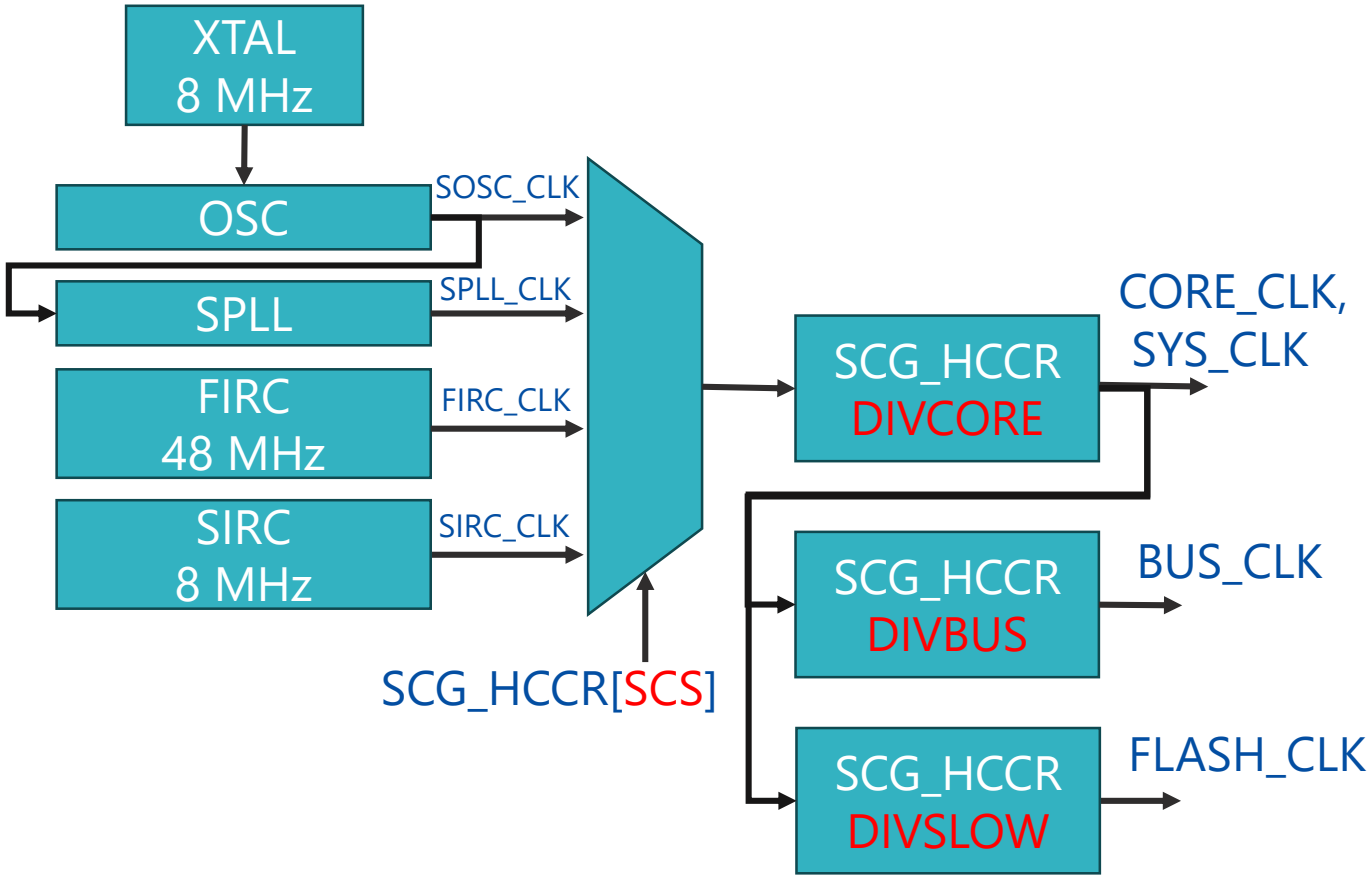


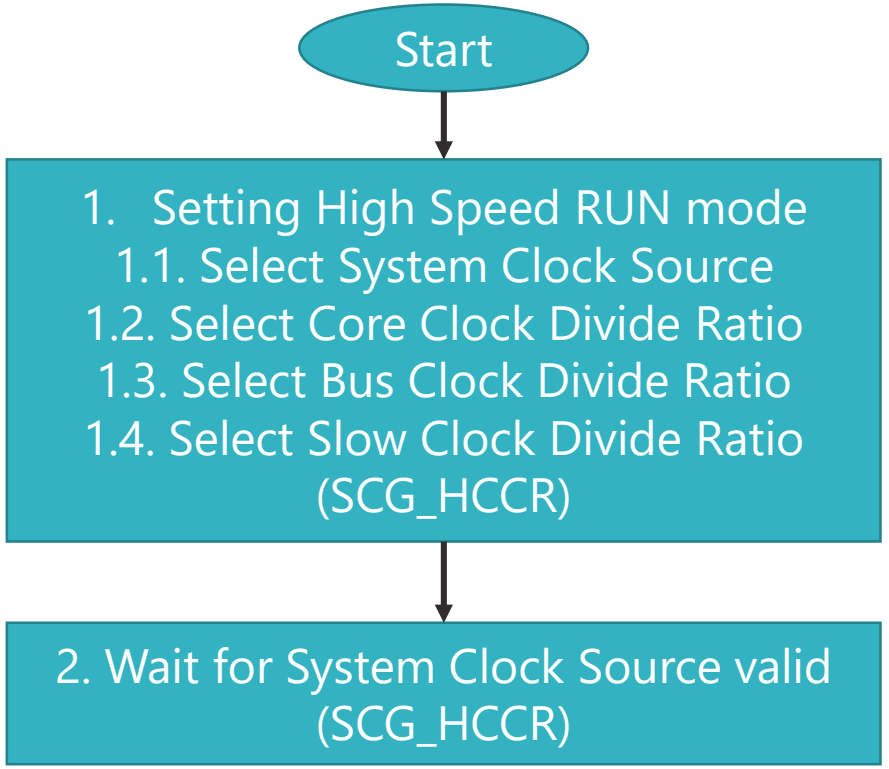
7.4.1. Assignment 6

Transition to High Speed RUN mode:

- Select FIRC as System clock source

7.4.2. Configuration High Speed RUN mode





Note: **HSRUN Clock Control Register (SCG_HCCR)**
This register can only be written using a 32-bit write.

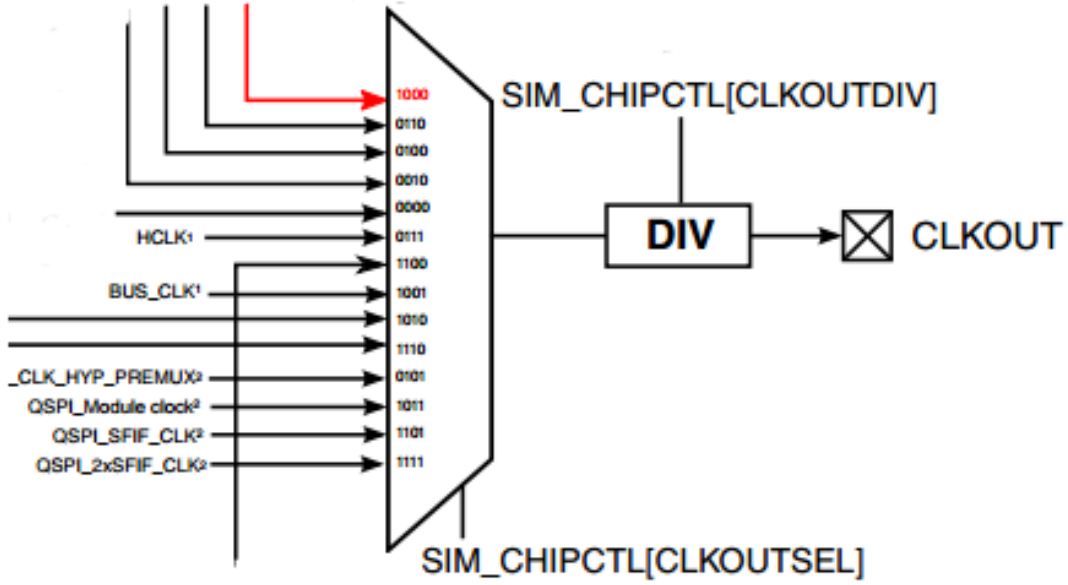
7.4.3. Assignment 6

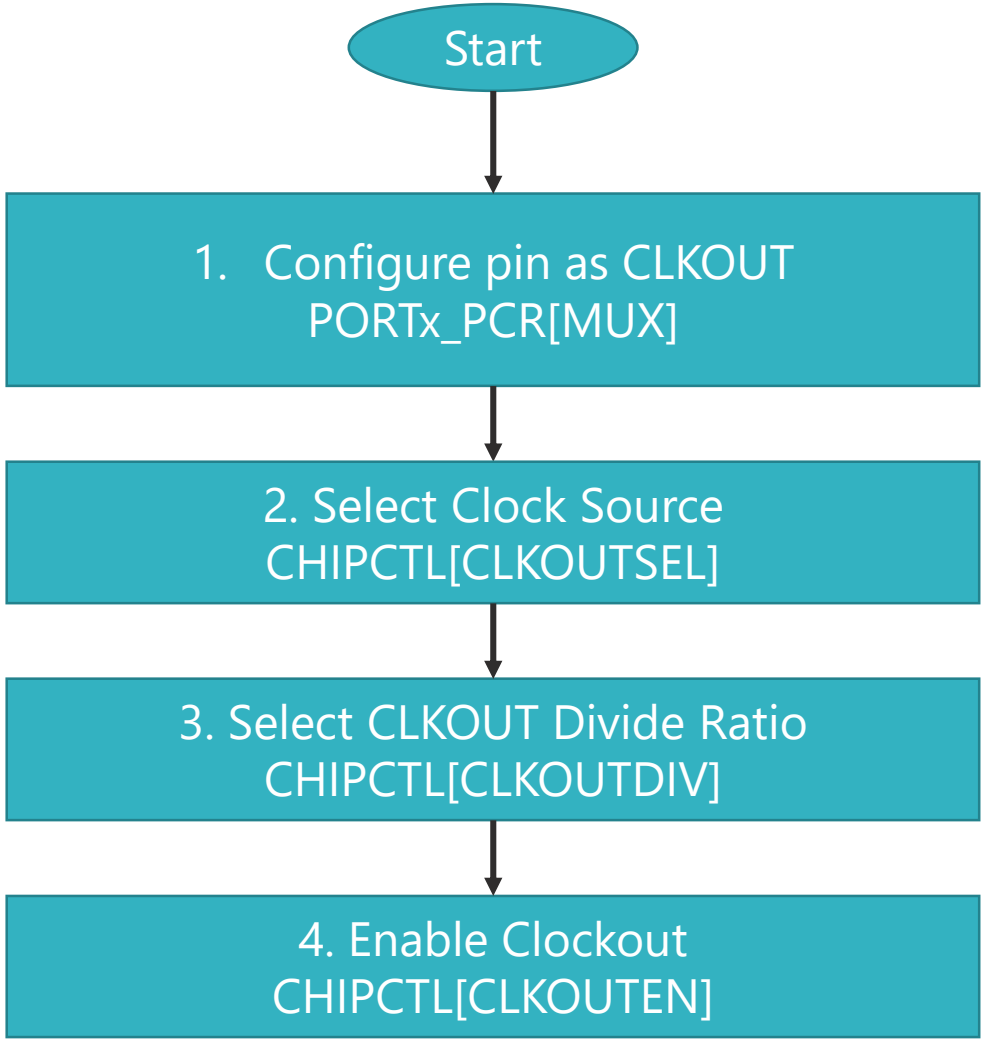
Initialize High Speed RUN mode:

- Select SPLL as System clock source
- Core clock = 112 MHz
- Bus clock = 56 MHz
- Flash clock = 28 MHz

7.5. Configuration CLKOUT pin

Initialize CLKOUT pin:





7.5.1. Assignment 6

Initialize CLKOUT pin:

- CLKOUT pin = 2MHz


Thank you