COA Assignment-4

Q1→

The logical address has two parts:

a 7-bit segment (since $2^7 = 128$ segments) and 15-bit offset within the segment (since each segment has $32 \times 2^{12} = 2^{17}$ words, requiring $\log_2(2^{17}) = 17$ bits, but the Question states 32 pages of 4K words, so $\log_2(32) = 5$ bits for the page number and $\log_2(4K) = 12$ bits for the word within the page, totaling $5 + 12 = 17$ bits.

The physical address format depends on the memory management unit and isn't directly derivable from the given information about physical memory blocks.

The logical address is 7 bits (segment) + 17 bits (offset).

Q2 Hardware interrupts are triggered by hardware devices and handled by the OS kernel. Software interrupts (traps) are inhibited by software instructions (eg. system calls, exceptions like division by zero) also handled by the Kernel.

Q3 Tag bits: $16 - (\log 9)$

$(1k/4) + \log 9$

(4)) - 16 - (8+2) = 6 bits. Index bits : log of

(1K/4) = 8 bits . Block offset bits : log

(4) = 2 bits. Word offset bits : log

(16) = 4 bits

II. Each cache word has 16 bits. They are divided into data bits and a valid bit (1 bit). The data bits serve to store a portion of a memory block.

III. The cache can accomodate 1K words / 4 words/block = 256 blocks.

Q4 Semiconductor memory technologies include SRAM (Static RAM), which is fast and used for cache due to its low latency and DRAM (Dynamic RAM) which is denser and cheaper, making it suitable for main memory. Technologies differ in their cell structure, speed, power consumption and cost. Non volatile memories like ROM, PROM, EPROM, EEPROM and flash are used for persistent storage.

Q5 →

FIFO

string	frame1	frame2	frame3	frame4	Faults?
1	1				yes
2	1	2			yes
3	1	2	3		yes
4	1	2	3	4	yes
1	1	2	3	4	No
5	5	2	3	4	yes
6	5	6	3	4	yes
2	5	6	2	4	yes
1	1	6	2	4	No
2	1	6	2	4	yes
3	3	6	2	4	yes
7	3	7	2	4	yes
6	3	7	6	4	yes
3	3	7	6	4	No
2	2	7	6	4	yes
1	2	1	6	4	yes
2	2	1	6	4	yes
6	2	1	6	4	yes

Total FIFO faults = 13

block offset bits: log

LRU

String	Frame1	Frame2	Frame3	Frame4	Fault?
1	1				Yes
2	1	2			Yes
3	1	2	3		Yes
4	1	2	3	4	Yes
1	1	2	3	4	NO
5	5	2	3	4	Yes
6	5	6	3	4	Yes
2	5	2	3	4	Yes
1	1	2	3	4	Yes
2	1	2	3	4	NO
3	1	2	3	4	NO
7	7	2	3	4	Yes
6	7	6	3	4	Yes
3	7	6	3	4	NO
2	7	6	2	4	Yes
1	1	6	2	4	Yes
	1	2	6	4	No
2		2	6	4	NO
6	1				

LRU faults = 12