



# INTERNATIONAL INSTITUTE OF INFORMATION TECHNOLOGY

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## Analog Electronic Circuits

Course Project

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# Abstract

In modern communication systems, signals are transmitted at high frequencies and then converted to lower frequencies at the receiver. The Quadrature Down Converter (QDC) is a crucial component in mobile communication, widely used in Bluetooth, Wi-Fi, and WLAN receivers. This project focuses on implementing a basic QDC. The design involves utilizing operational amplifiers, a quadrature oscillator, and a mixer to achieve the down-conversion process effectively.

## Introduction

Quadrature Down Converters (QDCs) are integral components in modern wireless receivers, including Bluetooth, WiFi, and WLAN systems. They play a critical role in enhancing communication quality by mitigating interference. Before transmission, signals are typically frequency modulated to reduce antenna size and transmission costs. This modulation, however, can introduce interference from other waves during transmission. QDCs address this challenge by converting the high-frequency modulated signal, comprising the carrier and original message frequencies, into its baseband frequency using two quadrature components.

The size of the transmitting antenna is directly related to the wavelength of the signal, with higher frequencies corresponding to shorter wavelengths and smaller antenna sizes. Its effective to build antennas with smaller size. This relationship underscores the importance of effective interference mitigation in wireless communication systems. QDCs utilize quadrature signals, which are 90° phase-shifted signals, to convert high-frequency input signals into low-frequency output signals. This process involves three main components:

1. Quadrature Oscillator: Used for generating two sinusoids having phase difference of 90 degrees between them.
2. Mixer: It acts a switch and used to multiply two signals .i.e. Input signal and sinusoid coming from Quadrature Oscillator.
3. )Low Pass Filter(LPF): It is used to filter

our required Vin signal and remove the unwanted carrier signal.

## Quadrature Oscillator

### Working of Oscillator

The circuit consists of an op amp connected in the noninverting configuration, with a closed-loop gain of

$$1 + \frac{R_2}{R_1}$$

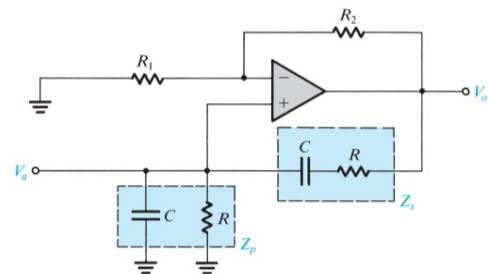
. In the feedback path of this positive-gain amplifier, an RC network is connected. The loop gain can be easily obtained by multiplying the transfer function

$$\frac{V_a s}{V_o S}$$

of the feedback network by the amplifier gain, To ensure that oscillations will start, one chooses

$$\frac{R_2}{R_1}$$

slightly greater than 2. The oscillator's output lacks stabilization in its amplitude, thus introducing the need for the Limiter Circuit.



Wein Bridge Oscillatot

$$L(s) = \left[1 + \frac{R_2}{R_1}\right] \frac{Z_p}{Z_p + Z_s} = \frac{1 + \frac{R_2}{R_1}}{1 + Z_s Y_p}$$

Thus,

$$L(s) = \frac{1 + \frac{R_2}{R_1}}{3 + sCR + \frac{1}{sCR}}$$

Substituting  $s = j\omega$  results in

$$L(j\omega) = \frac{1 + \frac{R_2}{R_1}}{3 + j(\omega CR - \frac{1}{\omega CR})}$$

The loop gain will be a real number (i.e., the phase will be zero) at one frequency given by

$$\omega_0 CR = \frac{1}{\omega_0 CR}$$

That is,

$$\omega_0 = \frac{1}{CR}$$

Oscillations will start at this frequency if the loop gain is at least unity. This can be achieved by selecting

$$\frac{R_2}{R_1} = 2$$

## Limiter

The amplitude of oscillation can be determined and stabilized using a nonlinear control network, specifically a Limiter circuit. This circuit incorporates a symmetrical feedback limiter comprising diodes D1 and D2 with resistors R3, R4, R5, and R6. Here's how the limiter operates: At the positive peak of the output voltage  $V_O$ , the voltage at node b exceeds the voltage  $V_1$  (approximately one-third of  $V_O$ ), causing diode D2 to conduct. This action clamps the positive peak to a value determined by R5, R6, and the negative power supply. The positive output peak value can be calculated by setting  $V_b = V_1 + V_{D2}$  and writing a node equation at node b while neglecting the current through D2. Similarly, the negative peak of the output sine wave is clamped to the value that causes diode D1 to conduct. The

value of the negative peak can be determined by setting  $V_a = V_1 - V_{D1}$  and writing an equation at node a while neglecting the current through D1. To ensure a symmetrical output waveform, R3 is chosen to be equal to R6, and R4 is equal to R5

## Working of Limiter

The Limiter circuit, shown in Fig 1, has a transfer characteristic depicted in Fig 2. To understand how this characteristic is derived, let's first consider a small input signal  $v_I$  and a small output voltage  $v_O$ , such that  $v_A$  is positive and  $v_B$  is negative. In this scenario, both diodes D1 and D2 are off.

Thus, all of the input current  $v_I/R_1$  flows through the feedback resistance  $R_f$ , and the output voltage is given by:

$$v_O = -\left(\frac{R_f}{R_1}\right)v_I \dots eq1$$

This represents the linear segment of the limiter transfer characteristic as shown in Fig 2. Using superposition, we can now express the voltages at nodes A and B in terms of  $\pm V$  and  $v_O$ .

$$V_A = v \frac{R_3}{R_2 + R_3} + V_o \frac{R_2}{R_2 + R_3} \dots eq2$$

$$V_B = v \frac{R_4}{R_4 + R_5} + V_o \frac{R_5}{R_5 + R_4} \dots eq3$$

As the input voltage  $v_I$  increases positively, the output voltage  $v_O$  decreases (as per Eq. 1). According to Eq. (3), the voltage at node B ( $v_B$ ) becomes more negative, which keeps diode D2 off. However, Eq. (2) shows that the voltage at node A ( $v_A$ ) becomes less positive. Continuing to increase  $v_I$ , a point is reached where  $v_O$  becomes negative enough that  $v_A$  drops to around -0.7 V, at which point diode D1 starts conducting. Assuming a constant-voltage-drop model for D1 with a voltage drop denoted as  $V_D$ , the value of  $v_O$  at which D1 conducts can be determined from Eq. (2). This value is known as the negative limiting level, denoted as  $L_-$ .

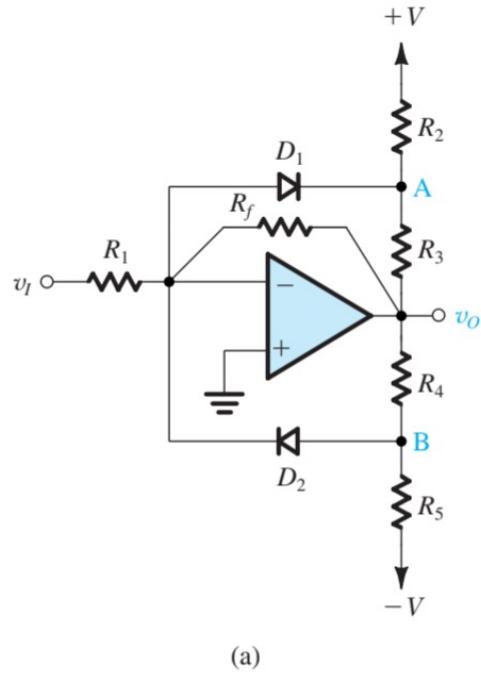
$$L_- = -V \frac{R_3}{R_2} - V_D \left(1 + \frac{R_3}{R_2}\right) \dots \text{eq4}$$

To find the corresponding value of  $v_I$ , divide  $L_-$  by the limiter gain  $-R_f/R_1$ . If  $v_I$  is increased beyond this value, more current is directed into D1, causing  $v_A$  to remain at approximately  $-V_D$ . Consequently, the current through  $R_2$  stays constant, and the additional diode current flows through  $R_3$ . This effectively places  $R_3$  in parallel with  $R_f$ , resulting in an incremental gain (ignoring the diode resistance) of  $-(R_f||R_3)/R_1$ . To ensure a small slope of the transfer characteristic in the limiting region, a low value should be chosen for  $R_3$ . The transfer characteristic for negative  $v_I$  can be derived using a method similar to the one just described. It's evident that for negative  $v_I$ , diode D2 plays the same role as D1 does for positive  $v_I$ . Using Eq. (3), we can determine the positive limiting level  $L_+$ .

$$L_+ = V \frac{R_4}{R_5} + V_D \left(1 + \frac{R_4}{R_5}\right) \dots \text{eq5}$$

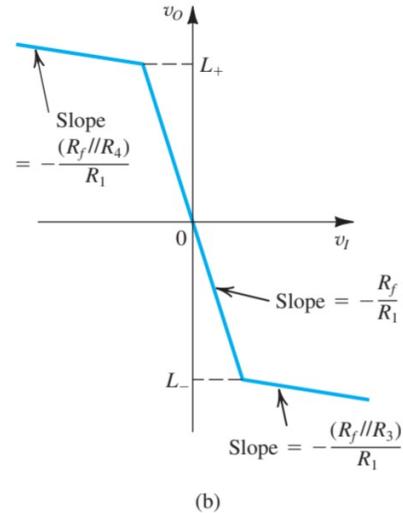
The slope of the transfer characteristic in the positive limiting region is  $-(R_f||R_4)/R_1$ . This implies that the circuit in Fig. 5 acts as a soft limiter, with independently adjustable limiting levels  $L_+$  and  $L_-$ , and limiting gains determined by the selection of appropriate resistor values.

Increasing  $R_f$  leads to a higher gain in the linear region while keeping  $L_+$  and  $L_-$  unchanged. Removing  $R_f$  altogether results in the transfer characteristic shown in Fig. 5, which behaves like a comparator.



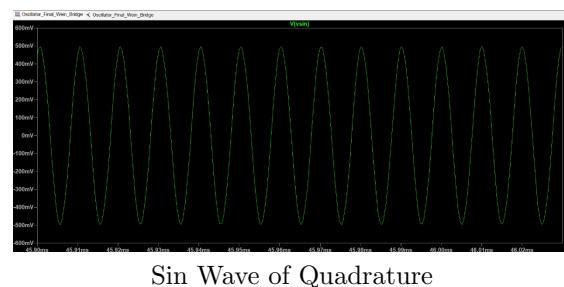
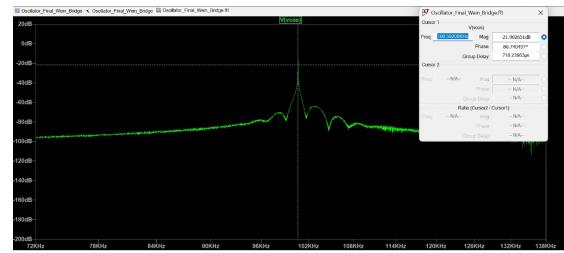
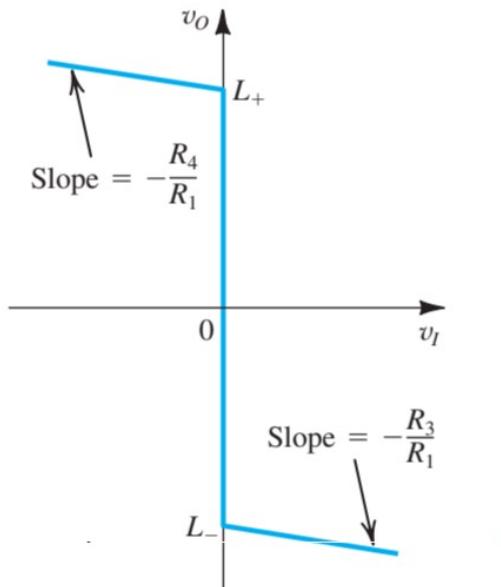
(a)

Fig 1

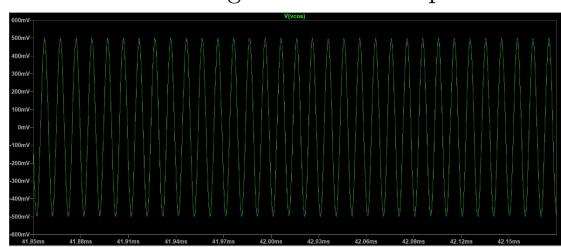
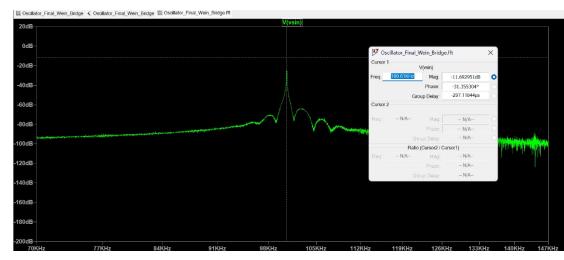
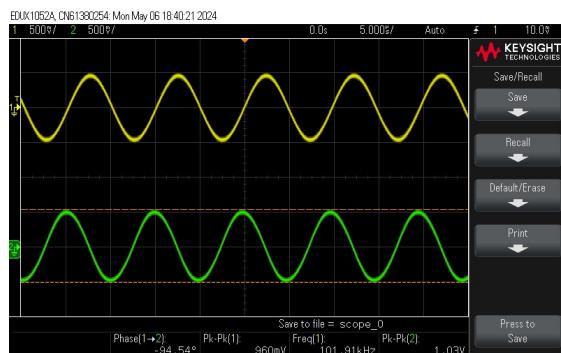


(b)

Fig 2

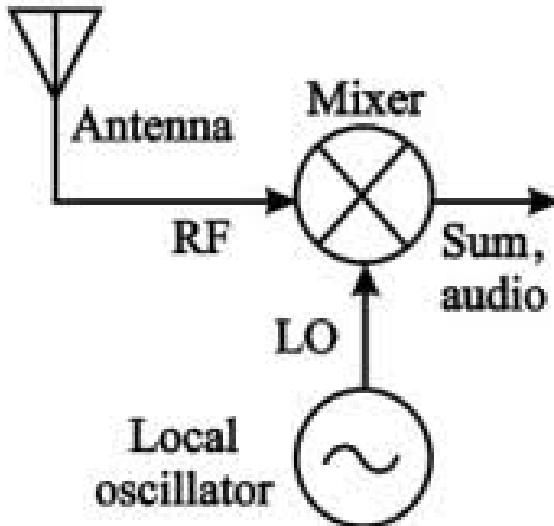


## LTSpice and Lab simulation

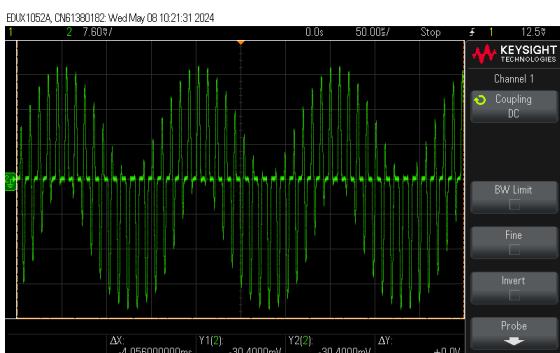
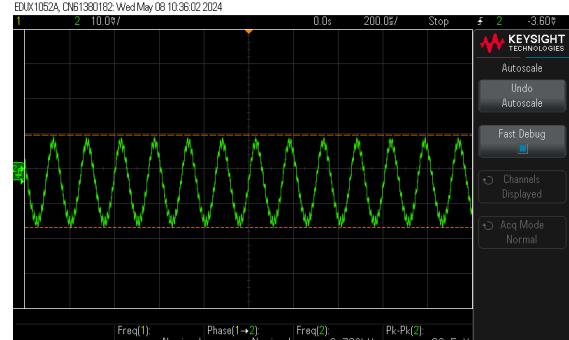
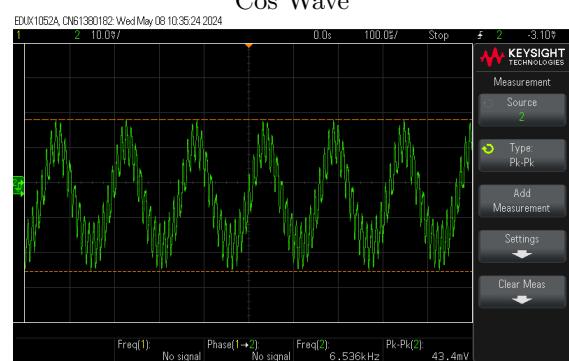
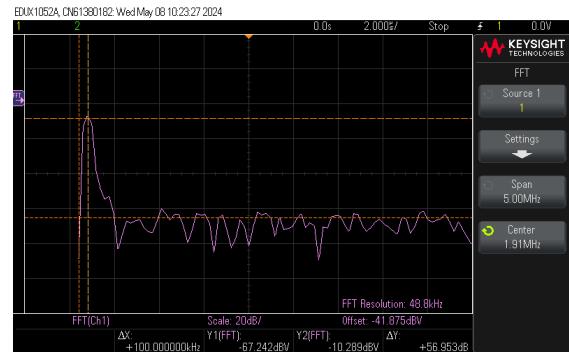


## Mixer

A major part of mixer's working is based on how mosfet behaves in circuit. Hence a major part of mixer's working lies in analyzing the working of mosfet.



Circuit depiction of Mixer



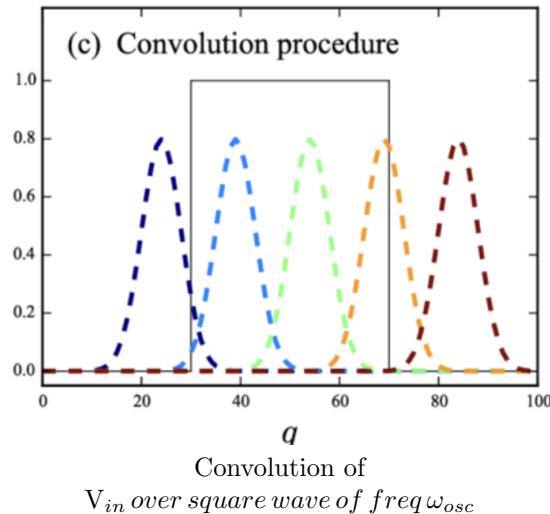
## MOSFETS:

MOSFETs are commonly used as voltage-controlled switches. To differentiate between the positive and negative halves of our Quadrature's incoming sinusoid, we bias the gate voltage close to the threshold voltage of

the MOSFET ( $V_{gs}=V_{th}$ ). During the positive half-cycle, when  $V_{osc}$  greater than equal to 0, the condition  $V_{gs} + V_{osc} - V_t$  greater than equal to 0 is met, and the MOSFET operates in the linear mode. However, during the negative half-cycle ( $V_{osc}$  less than 0), the condition  $V_{gs} + V_{osc} - V_t$  less than 0 is true, and the MOSFET is in cutoff mode, resulting in no signal being detected at the source end.

In summary, the MOSFET acts as a switch that turns on and off with a frequency of  $\omega_{osc}$ . This behavior can be represented as a square wave with a frequency of  $\omega_{osc}$  and an amplitude of 1 Vpp. When we apply  $V_{in}$  at the drain of the MOSFET, we essentially pass  $V_{in}$  over the switch, which can be understood as convolution in the time domain, equivalent to multiplication in the frequency domain. These mathematical expressions are given as below. The purpose of capacitor here is to block any DC signal coming from  $V(Bias)$ , ensuring that it doesn't give any offset to  $V_{osc}$  signal. Resistor is required for two purposes: 1) To ensure the gate of Mosfet is not connected directly to ground in small signal model. 2)To avoid the flow of small signal current through the bias resistance.

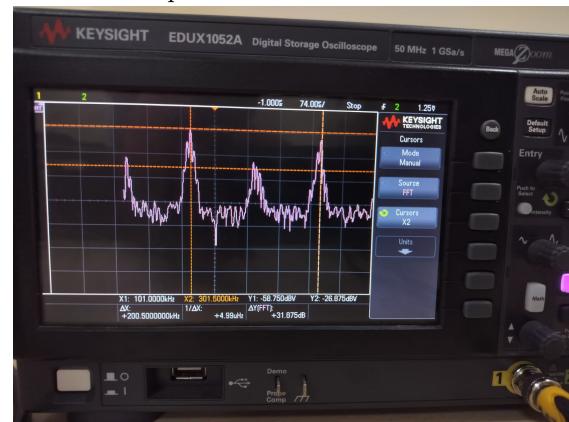
As seen from the schematic of the circuit behaves as a high pass filter, so value of Capacitance  $C_c$  shall be high enough to pass conveniently.



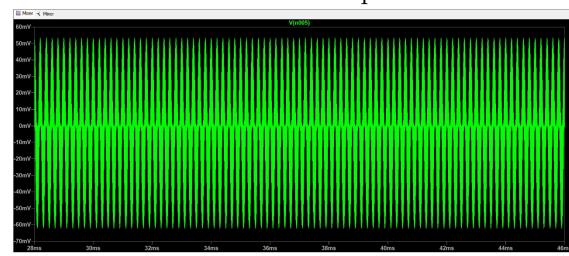
## LTSpice and Lab simulation



Output of MOSFET on DSO



FFT of the output



Mixer LT spice Simulation

## Analysis of Mixer Circuit:

- 1) Large Signal Analysis: During the large signal analysis, the oscillator voltage  $V_{osc}$  is set to 0, and the input voltage  $V_{in}$  is also set to 0.

The capacitor is considered open as the frequency tends to 0. The bias voltage ( $V_{Bias}$ ) is set equal to the threshold voltage ( $V_{th}$ ) to bias the MOSFET into the linear mode.

2) Small Signal Analysis: Small signal analysis is crucial in mixer design. During this analysis, the bias voltage ( $V_{Bias}$ ) is set to 0. During the positive cycle of  $V_{osc}$ , the MOSFET operates in the linear mode, and during the negative cycle of  $V_{osc}$ , the MOSFET operates in the cutoff mode. This operation results in the production of a square wave with a uniform frequency  $\omega_{osc}$  on which  $V_{in}$  is convolved.

The output is then taken across the load resistor ( $R_L$ ).

## Low Pass Filter

A low pass filter is a circuit that can be designed to reject all unwanted high frequencies. We know that our mixer output consists of output frequencies  $w_{in} + w_{osc}$ ,  $w_{in} - w_{osc}$  by the formula The area of interest of our frequency is  $w_{in} - w_{osc}$ , hence we need to filter out high frequency of  $w_{in} + w_{osc}$ .

$$V_{OUT} = X_c \cdot \left( \frac{V_{IN}}{X_C + X_R} \right)$$

here,

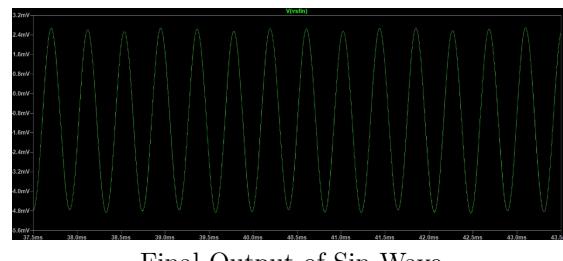
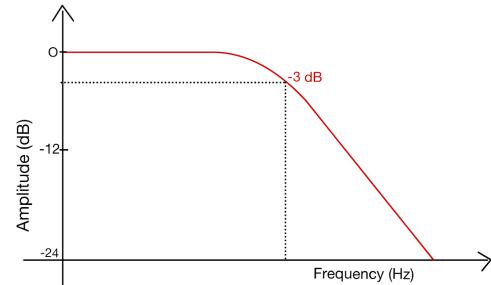
$X_C$  and  $X_R$   
are impedance of capacitor and resistor

To obtain the -3dB frequency,

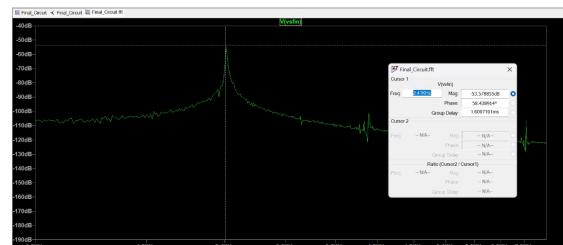
From eq(1),

Solving eq (2) and (3)

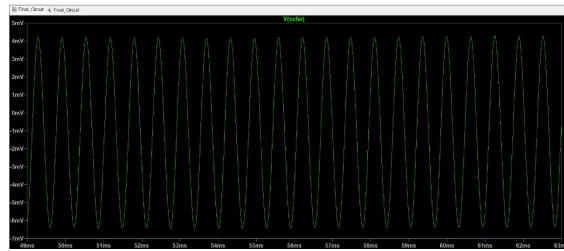
$$\omega = \frac{1}{RC}$$



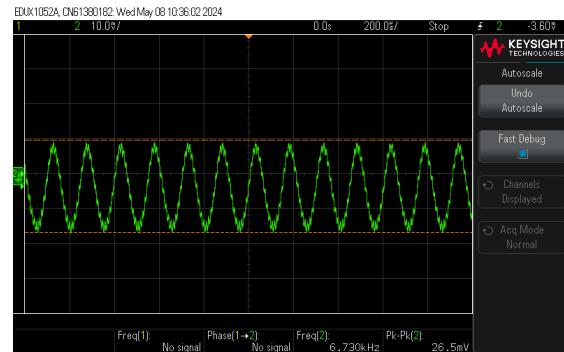
## Final Output of Sin Wave



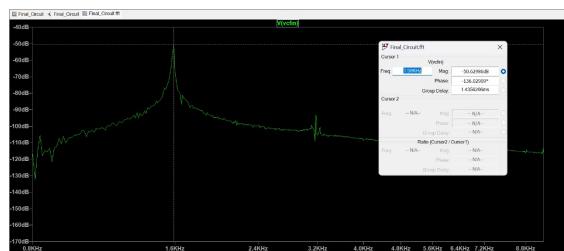
## FFT on LTSpice with cursor



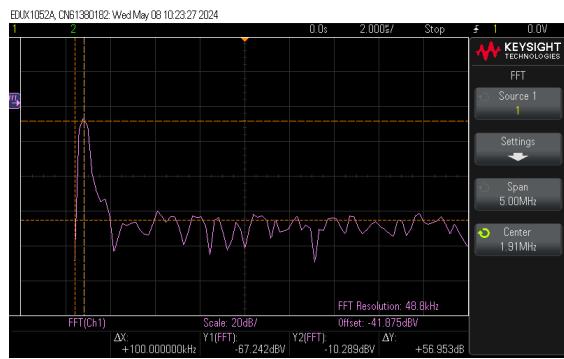
Final Output of Cos Wave



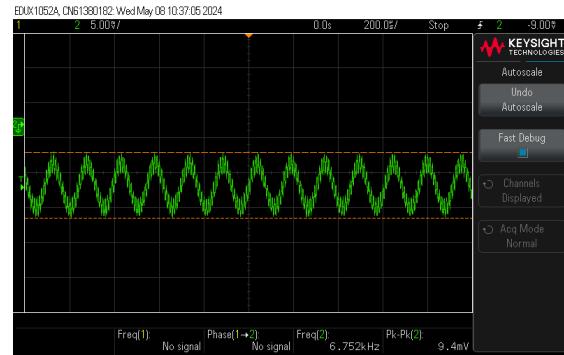
Cos wave after first cascading



FFT on LTSpice with cursor



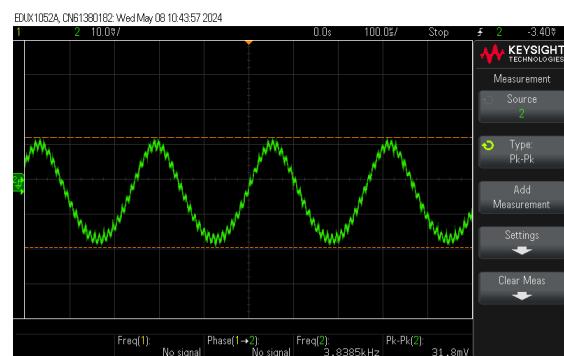
Cos Wave



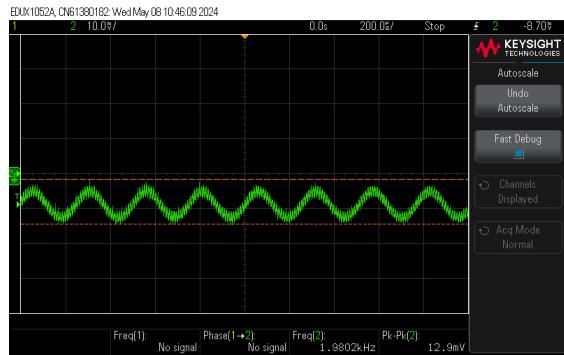
Cos wave after first cascading



Cos Wave after LPF



Final Output Cos



Final Output Sin

## References

1. Sedra Simth
2. Direct-Conversion Radio Transceivers for Digital Communications by Asad A. Abidi
3. Design of op amp sine wave oscillators by Ron Macini
4. Wikipedia

## Contribution

1. LTSpice - Vansh and Jainil
2. Hardware - Vansh and Jainil
3. Project Report - Vansh and Jainil