MCA/DX   **5562**

COMPUTER ARCHITECTURE AND
PARALLEL PROCESSING
Paper : MCA-503

Time : Three Hours]   [Maximum Marks : 80

Note : Attempt *five* questions in all, selecting *one* question from each unit and Q. No. 1 which is compulsory.

1.   Answer the following questions in brief :

   (a)   Compare Horizontal and Vertical microinstruction formats.

   (b)   Why Booth's multiplication is faster ?

   (c)   What are the disadvantages of VLIW architecture ?

   (d)   Differentiate between Vector computer and SIMD computer.

   (e)   What is the purpose of pre-decode unit in a superscalar processor ?

   (f)   Discuss any *two* techniques to detect branch early.

   (g)   Distinguish between Write-update and Write-invalidate policy of cache coherence.

   (h)   Draw the diagram of Chordal ring of degree 4 with 8 nodes and compute its network diameter.   8×3=24

UNIT–I

2. (a) Derive an algorithm in flow chart form for the restoring method of fixed-point binary division. Explain how division by zero and divide overflow conditions are handled. Also describe the necessary hardware needed to implement this algorithm. 7

   (b) Derive an algorithm in flow chart form for adding and subtracting two floating-point binary numbers. 7

3. (a) What is the purpose of Control unit ? Explain the classical method of hardwired control design. 7

   (b) What is Microprogrammed control unit ? Explain Microinstruction addressing scheme. 7

UNIT–II

4. (a) What is Instruction level parallelism (ILP) ? Explain loop-scheduling technique used in ILP processors. 7

   (b) Explain true and false data dependencies with examples. Also explain how you can remove false dependencies. 7

5. (a) Explain the following : Scalar pipeline, Dynamic pipeline, Super pipeline and Speed-up factor of the pipeline. 7

   (b) Explain the concept of computer architecture as a multilevel hierarchical framework. 7

UNIT–III

6. (a) What is Superscalar processor ? Why superscalar issue is more complex than scalar issue ? Explain blocking and shelved issue, in-order and out-of-order issue. 7

   (b) How can you preserve sequential consistency of execution of instruction ? Explain. 7

7. (a) What is Branch penalty ? How is it introduced ? Explain with an example. Discuss different ways to reduce branch penalty. 7

   (b) What are implicit, static and dynamic branch prediction schemes ? Explain *one* method in each category. 7

UNIT–IV

8. (a) What are *three* generations of buses used in multiprocessor systems ? Compare their read and write bandwidths. 7

   (b) What is Bus arbiter ? Explain Daisy chain based centralized arbiter. Discuss its advantages and disadvantages. 7

9. (a) What is Cache coherence problem in multiprocessor system ? Discuss S/W based protocol to solve this problem. 7

   (b) What are memory and synchronization latencies in multicomputers ? How can you reduce these latencies ? Explain. 7