Roll No. ……. Total Pages: 2

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MCA/D-08
COMPUTER ARCHITECTURE AND PARALLEL PROCESSING
Paper-MCA-303

Time Allowed: 3 Hours] [Maximum Marks: 80

Note: Attempt five questions in all, selecting at least one question from each unit.

UNIT-I

1. (a) Explain the following terms with respect to linear pipeline: speedup factor, efficiency, throughput, clock skewing and reservation table.

(b) What do you mean by computational model? Discuss the evaluation of this concept.

2. What is non-linear pipeline? Explain the following concepts associated with a non-linear pipeline with the help of an example: reservation table, forbidden latency, simple cycle, greedy cycle and minimum average latency.

3. (a) What is the interpretation of the concept of computer architecture? Discuss.

(b) Distinguish between SPMD and SIMD execution model.

UNIT-II

4. (a) What is superscalar pipeline? Discuss the data dependencies in superscalar pipeline processing.

(b) What do you mean by register renaming? Discuss different implementations for renaming used in superscalar processing.

5. (a) Draw a schematic diagram of VLIW processor and explain its working. Also discuss pros and cons of VLIW.

(b) Explain the reordering of memory accesses of load/store instructions.

6. (a) What is branch problem? Discuss the basic delayed branching scheme to handle this problem. Also discuss the possible extensions of this scheme.

(b) Explain the global scheduling scheme used in the ILP compilers.

UNIT-III

7 (a) what are the performance parameters of cache memories? Discuss the various cache performance issues.

(b) Discuss the principle of locality of reference and coherence used in memory hierarchy.

8. (a) What is paging? Distinguish between demand page and swapping scheme of paging.

(b) What are private and shared virtual memory models? What are the pros and cons of these models?

9. (a) Discuss the models for virtual caches. What is the aliasing problem in these models?

(b) Compare and contrast set associative and sector mapping schemes used in cache memories.

10 (a) what is coherence problem? Discuss hierarchical cache coherence protocol.

(b) Compare and contrast NUMA and CC-NUMA models.