MCA/D07
Computer Architecture and Parallel Processing
MCA -303

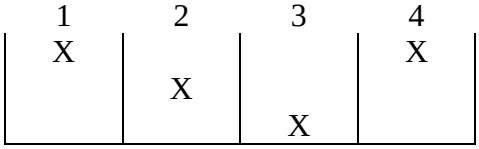
Time : 3 Hours MM:50
Note:- Attempt Five questions in all, selecting One question from each unit.

UNIT-I

1 Distinguish between the following concepts:
(a) Data-driven and Demand-driven Execution Control.
(b) Procedural and Declarative description of problems.
(c) Abstract and concrete architectures.
(d) Concurrent and Data-Parallel Languages.
(e) Vector and SIMD computers 10

2(a) What are the flow dependency and control dependency? How do they affect pipeline processing? Explain with the help of space-time diagrams. 6
(b) Define the following terms associated with the synchronous pipeline: Clock Cycle, Clock Skewing, Speed up factor and Efficiency. 4

3 Consider the following three stage pipeline reservation table:



(a) What are the forbidden latencies?
(b) Draw the state transition diagram.
(c) List all the simple cycles and greedy cycles.
(d) Determine the optimal constant latency cycle and the minimal average latency.
(e) Let the pipeline clock period be 20ns. Determine the throughput of the pipeline.

UNIT-II

4(a) What is superscalar pipeline? What are the factors that affect superscalar pipeline processing? Explain 5
(b) Compare and contrast VLIW and superscalar processor. 5

5(a) Explain software pipelining and global code scheduling techniques. Which one is better and why? 6
(b) How can you minimize the loss incurred due to mispredictions in branch

processing? 4

6 Distinguish between the following:

(a) Aligned and Non-aligned issue. 2
(b) Precise and Imprecise consistency models. 3
(c) Static and Dynamic branch prediction techniques 5

UNIT - III

7(a) What is locality of reference? Discuss its importance with respect to memory hierarchy. 5

(b) What are Write Through (WT) and Copy Back(CB) approaches to design Cache memory? Discuss relative advantages and disadvantages of these approaches. 5

8(a) Consider a paged virtual memory system with a two level hierarchy. There are eight pages numbered from 0 to 7 and three page frames. Initially all page frames are empty. Given the following page trace : 0, 1, 2, 4, 2, 3, 7, 2, 1, 3, 1. compare the relative performance of FIFO, LRU and OPT page replacement policies for the given page trace 5

(b) What are three generations of buses used in multiprocessor systems? Compare their read and write bandwidths using time space diagrams. 5

9(a) Consider the main memory size of 4MB and cache size of 4KB. If block size is 64 bytes and sector size is 4 blocks then write the address formats for direct, associative and sectored mapping schemes, compute the number of bits required for each address field. 5

(b) How do you classify distributed shared memory MIMD computers? Explain any one of them in detail. 5

10(a) What is cache coherence problem? Discuss snoopy cache coherence protocol.

(b) Discuss 4-way low –ordered interleaved memory with the help of suitable diagram taking memory size 32 words. Also explain C-Access for this memory. 5