MCA/D11

4562

Computer Architecture and Parallel Processing

Paper: MCA-503

Time: Three Hours]

[Maximum Marks: 80

Note: - Attempt FIVE questions in all. Question No.1 is compulsory.

Attempt FOUR more questions, selecting ONE question from each Unit.

- 1. Answer the following questions in brief:
 - (a) What are the limitations of sign-magnitude addition and subtraction algorithm?
 - (b) Define microoperation, microinstruction and microprogram.
- (c) Explain the relationship between computer architecture and programming language.
 - (d) What is granularity? How is it related to levels of parallelism?
 - (e) Distinguish between in-order and out-of-order issue in superscalar processors.
 - (f) What is branch penalty? Explain any two ways in brief to reduce them.
 - (g) What is barrel shifter? Draw the diagram of 8 node barrel shifter interconnection network.
 - (h) What is split transaction bus? How is it better than pended bus?
 8×3=24

UNIT-I

2.	(a)	Derive an algorithm in flowchart form for non-restoring method	
		of fixed-point binary division. Also describe the necessary	
		hardware needed to implement this algorithm. 7	
	(b)	Derive an algorithm in flowchart form for multiplying two	
		floating-point binary numbers.	
3.	(a)	What is hardwired control? Discuss one-hot method of hardwired control design.	
	(b)	What are vertical and horizontal microinstructions? Discuss the	
	(0)	pros and cons of each.	
		UNIT-II	
4.	(a)	What is computational model ? Compare von Neumann,	
		object-based and applicative computational models.	
	(b)	Explain the following parallel architectures in brief: vector, array	
		and systolic.	
5.	(a)	What is pipeline processing? Explain data hazardous in pipeline	
		processing.	
	(b)	Explain global scheduling technique used in ILP processors. 7	
		UNIT-III	
6.	Diff	ferentiate between the following:	
	(a)	Processor consistency and memory consistency 4	
	(b)	Blocking issue and shelved issue 4	
	(c)	VLIW and Superscalar processor. 6	
	(b) Diff (a) (b)	Explain global scheduling technique used in ILP processors. 7 UNIT-III ferentiate between the following: Processor consistency and memory consistency 4 Blocking issue and shelved issue 4 VLIW and Superscalar processor. 6	

2

7.	(a)	What is speculative branch processing? Discuss dynamic branch
		prediction schemes. 7
	(b)	Explain different techniques for early detect of branches. 7
		UNIT—IV
8.	(a)	What is multicomputer? How is it different from NUMA
		model ? Explain. 7
	(b)	Explain the characteristics of Star, Chordal ring of degree 3 and
		2D Torus interconnection networks. 7
9.	(a)	What are multi-stage dynamic interconnection network? Explain
		construction and working of 8×8 omega network.
	(b)	What is cache coherence problem? Discuss snoopy cache
		coherence protocol. 7