MCA-14-42 ADVANCED COMPUTER ARCHITECTURE

Maximum marks: 100 (External: 80, Internal: 20) Time: 3 hours

Note: Examiner will be required to set NINE questions in all. Question Number 1 will consist of objective type/short-answer type questions covering the entire syllabus. In addition to question no. 1, the examiner is required to set eight more questions selecting two from each unit. Student will be required to attempt FIVE questions in all. Question Number 1 will be compulsory. In addition to compulsory question, student will have to attempt four more questions selecting one question from each Unit. All questions will carry equal marks.

UNIT – I

Computational Model: Basic computational models, evolution and interpretation of computer architecture, concept of computer architecture as a multilevel hierarchical framework. Classification of parallel architectures, Relationships between programming languages and parallel architectures

Parallel Processing:: Types and levels of parallelism, Instruction Level Parallel (ILP) processors, dependencies between instructions, principle and general structure of pipelines, performance measures of pipeline, pipelined processing of integer, Boolean, load and store instructions, VLIW architecture, Code Scheduling for ILP-Processors - Basic block scheduling, loop scheduling, global scheduling

UNIT – II

Superscalar Processors: Emergence of superscalar processors, Tasks of superscalar processing – parallel decoding, superscalar instruction issue, shelving, register renaming, parallel execution, preserving sequential consistency of instruction execution and exception processing, comparison of VLIW & superscalar processors

Branch Handling: Branch problem, Approaches to branch handling – delayed branching, branch detection and prediction schemes, branch penalties and schemes to reduce them, multiway branches, guarded execution

UNIT – III

MIMD Architectures: Concepts of distributed and shared memory MIMD architectures, UMA, NUMA, CC-NUMA & COMA models, problems of scalable computers.

Direct Interconnection Networks: Linear array, ring, chordal rings, star, tree, 2D mesh, barrel shifter, hypercubes.

UNIT – IV

Dynamic interconnection networks: single shared buses, comparison of bandwidths of locked, pended & split transaction buses, arbiter logics, crossbar, multistage networks – omega, butterfly

Cache coherence problem, hardware based protocols – snoopy cache protocol, directory schemes, hierarchical cache coherence protocols, software based protocols.

Text Books:

1. Sima, Fountain, Kacsuk, Advanced Computer Architecture, Pearson Education, 2006.
2. D. A. Patterson and J. L. Hennessey, Computer Architecture – A Quantitative Approach, Fifth Edition, Morgan Kaufmann, 2012.

Reference Books:

1. Kai Hwang, Advanced Computer Architecture, Tata McGraw Hill, 2005
2. Nicholas Carter, Computer Architecture, McGraw Hill, 2006
3. Harry F. Jordan, Gita Alaghband, Fundamentals of Parallel Processing, Pearson Education, 2003.