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MCA/D06 6231

Computer Architecture and Parallel Processing

Paper : MCA-303(New)

Time : Three Hours] [Maximum Marks : 50

Note :– Attempt **FIVE** questions in all, selecting **ONE** question from each unit.

UNIT–I

1. Analyse the data dependence of the statements of the following code segment :

   S1 : Load R1, 1000

   S2 : Load R2, M[10]

   S3 : Add R1, R2

   S4 : Store M[1000], R1

   S5 : Store M[R2], 1000.

   Assume that the location M[10] contains value 100. Also draw the dependency graph to show all the dependencies. 10

2. What is meant by inclusion, coherence and locality in a memory hierarchy ? 10

3. Discuss following terms in context of advanced computer architecture :

   (i) Grain size and latency

   (ii) NUMA

   (iii) Hypercube routing

   (iv) Software parallelism. 2.5×4=10

UNIT–II

4. What do you understand by memory interleaving ? How is it different from cache memory ? 10

5. What is VLIW architecture ? How is pipelining performed in VLIW processors ? 10

6. Describe following in respect to multiprocessor system interconnection :

   (i) Hierarchical bus system

   (ii) Cross bar system with multiport memory. 5×2=10

UNIT–III

7. Describe the desirable and necessary language features for parallel processing. 10

8. Write short notes on the following :

   (i) Snoopy protocols

   (ii) Distributed arbitration. 5×2=10

9. What do you understand by superpipelining ? How is it different from superscaler pipeline ? Illustrate. 10

10. Describe following concepts :

    (i) Static and dynamic data flow machines

    (ii) Multivector computing and use. 5×2=10