MCA/D06
Computer Architecture and Parallel Processing
MCA -303

Time : 3 Hours MM:50
Note:- Attempt Five questions in all, selecting One question from each unit.

UNIT-I

1 Analyse the data dependency of the statements of the following code segments:
S1 : Load R1, 1000
S2 : Load R2, M[10]
S3 : Add R1, R2
S4 : Store M[1000], r1
S5 : Store M[R2], 1000
Assume that the location M[10] contains value 100. Also draw the dependency graph to show all the dependencies. 10

2 What is meant by inclusion, coherence and locality in a memory hierarchy? 10

3 Discuss following terms in context of advanced computer architecture:
(i) Grain size and latency
(ii) NUMA
(iii) Hypercube routing
(iv) Software parallelism. 10

UNIT- II

4 What do you understand by memory interleaving? How is it different from cache memory? 10

5 What is VLIW architecture? How is pipelining performed in VLIW processors? 10

6 Describe following in respect to multiprocessor system interconnection:
(i) Hierarchical bus system
(ii) Cross bar system with multiport memory 10

UNIT – III

7 Describe the desirable and necessary language features for parallel processing. 10

8 Write short notes on the following:
(i) Snoopy protocols
(ii) Distributed arbitration 10

9 What do you understand by superpipelining? How is it different from superscalar pipeline? Illustrate. 10

10 Describe following concepts:

(i) Static and dynamic data flow machines
(ii) Multivector computing and use. 10