MCA/D08

Computer Architecture and Parallel Processing

MCA -303

Time : 3 Hours MM:50

Note:- Attempt Five questions in all, selecting One question from each unit.

UNIT-I

1(a) Explain the following terms with respect to linear pipeline:
Speedup factor, efficiency, throughput, clock skewing and reservation table. 5

(b) What do you mean by computational model? Discuss the evolution of this concept. 5

2 What is non-linear pipeline? Explain the following concept associated with a non-linear pipeline with the help of an example : reservation table, forbidden latency, simple cycle, greedy cycle and minimum average latency. 10

3(a) What is the latest interpretation of the concept of computer architecture? Discuss. 5

(b) Distinguish between SPMD and SIMD execution model. 5

UNIT-II

4(a) What is superscalar pipeline? Discuss the data dependencies in superscalar pipeline processing. 5

(b) What do you mean by register renaming? Discuss different implementations for renaming used in superscalar processing. 5

5(a) Draw a schematic diagram of VLIW processor and explain its working. Also discuss pros and cons of VLIW. 5

(b) Explain the reordering of memory accesses of load/store instructions. 5

6(a) What is branch problem? Discuss the basis delayed branching scheme to handle this problem. Also discuss the possible extensions of this scheme. 5

(b) Explain the global scheduling scheme used in the ILP compilers 5

UNIT-III

7(a) What are the performance parameters of cache memories? Discuss the various cache performance issues. 5

(b) Discuss the principle of locality of reference and coherence used in memory hierarchy. 5

8(a) What is paging? Distinguish between demand page and swapping schemes of paging. 5

(b) What are private and shared virtual memory models? What are the pros and cons of these models? 5

9(a) Discuss the models for virtual address caches. What is the aliasing problem in these models? 5

(b) Compare and contrast set associative and sector mapping schemes used in cache memories. 5

10(a) What is coherence problem? Discuss hierarchical cache coherence protocol. 5

(b) Compare and contrast NUMA and CC-NUMA models. 5