

Roll No.

Total Pages : 3

6335

MCA/D07

COMPUTER ARCHITECTURE & PARALLEL PROCESSING

MCA-303

Time : Three Hours]

[Maximum Marks : 50

Note : Attempt *five* questions in all, selecting *one* question from each Unit.

UNIT-I

1. Distinguish between the following concepts :

- (a) Data-driven and Demand-driven Execution Control.
- (b) Procedural and Declarative description of problems.
- (c) Abstract and Concrete architectures.
- (d) Concurrent and Data-parallel languages.
- (e) Vector and SIMD computers.

10

2. (a) What are flow dependency and control dependency ?
How do they affect pipeline processing ? Explain with
the help of space-time diagrams.

6

(b) Define the following terms associated with the
synchronous pipeline :

Clock Cycle, Clock Skewing, Speed-up factor and
Efficiency.

4

3. Consider the following three-stage pipeline reservation table :

1	2	3	4
X			X
	X		
		X	

- What are the forbidden latencies ?
- Draw the state transition diagram.
- List all the simple cycles and greedy cycles.
- Determine the optimal constant latency cycle and the minimal average latency.
- Let the pipeline clock period be 20 ns. Determine the throughput of the pipeline.

UNIT-II

- What is superscalar pipeline ? What are the factors that affect superscalar pipeline processing ? Explain. 5
 - Compare and contrast VLIW and superscalar processor. 5
- Explain software pipelining and global code scheduling techniques. Which one is better and why ? 6
 - How can you minimize the loss incurred due to mispredictions in branch processing ? 4
- Distinguish between the following :

 - Aligned and Non-aligned issue. 2
 - Precise and Imprecise consistency models. 3
 - Static and Dynamic branch prediction techniques. 5

UNIT-III

7. (a) What is locality of reference ? Discuss its importance with respect to memory hierarchy. 5
- (b) What are Write Through (WT) and Copy Back (CB) approaches to design Cache memory ? Discuss relative advantages and disadvantages of these approaches. 5
8. (a) Consider a paged virtual memory system with a two-level hierarchy. There are eight pages numbered from 0 to 7 and three page frames. Initially all page frames are empty. Given the following page trace : 0, 1, 2, 4, 2, 3, 7, 2, 1, 3, 1. Compare the relative performance of FIFO, LRU and OPT page replacement policies for the given page trace. 5
- (b) What are three generations of buses used in multiprocessor systems ? Compare their read and write bandwidths using time-space diagrams. 5
9. (a) Consider the main memory size of 4MB and cache size of 4KB. If block size is 64 bytes and sector size is 4 blocks then write the address formats for direct, associative and sectorized mapping schemes, compute the number of bits required for each address field. 5
- (b) How do you classify distributed shared memory MIMD computers ? Explain any one of them in detail. 5
10. (a) What is Cache coherence problem ? Discuss Snoopy cache coherence protocol. 5
- (b) Discuss 4-way low-ordered interleaved memory with the help of suitable diagram taking memory size 32 words. Also explain C-access for this memory. 5