Roll No…… Total Pages: 3

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OMCA/D-17

COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

Paper: MCA-503

Time: Three Hours Maximum Marks: 80

Note: Attempt five questions in all. Question No. 1 is compulsory. In addition to compulsory question, attempt four more questions selecting one question from each unit. All questions carry equal marks.

Compulsory Question

1. Answer the following questions in brief :

   (a) What is cache coherence problem? Distinguish between write invalidate and write update policies.

   (b) What is branch penalty? Discuss different schemes to reduce them in brief.

   (c) Explain the general structure of a pipeline.

   (d) Explain Booth's algorithm of multiplication with the help of flowchart.

UNIT-I

2. (a) Derive an algorithm in flowchart form for adding and subtracting numbers represented in sign-magnitude representation. Also show the hardware needed for its implementation.

   (b) Drive an algorithm in flowchart form for multiplication when numbers are represented in sign-magnitude form. Also show the hardware needed for its implementation.

3. (a) Derive an algorithm in flowchart form for multiplication when numbers are represented in floating-point form. Also show the hardware needed for its implementation.

   (b) What is hardwired control? Explain one-hot method of its design.

UNIT-II

4. (a) What is the concept of computational model? Differentiate between von Neumann and Data Flow computational models.

(b) What is computer architecture? Give its interpretation at different levels of abstraction.

5. (a) Explain the pipelined processing of load and store instructions.

(b) What is VLIW architecture? Explain the architecture of VLIW processor with the help of block diagram.

UNIT-III

6. (a) What is shelving? Discuss layouts of shelving buffers used in superscalar processor.

(b) Explain different types of operand fetch policies used in superscalar processor.

7. (a) What is delayed branch technique? Explain its various extensions.

(b) Explain multiway branch handling technique to reduce branch penalty.

UNIT-IV

8. Write short note on the following :
   (a) CC-NUMA Model.
   (b) Hypercube.

9. (a) Compare the read and write bandwidths of locked, pended and split transaction buses.

(b) Explain software-based cache coherence protocol.