**Basic Functional Verification Fundamentals**

Q1. What prevents verification engineers from creating test benches for every possible scenario in a DUV?

Q2. Describe the role of functional verification within the chip design process based on your investigation.

Q3. Why do verification engineers must find design bugs as soon as possible?

Q4. From which stage (or stages) of the verification cycle are these activities?

(a) Write code to drive and check the DUV

(b) Understand the interesting scenarios and corner cases in the DUV

(c) Contemplate what improvements need to be made to the verification environment based on hardware results

(d) Contemplate what improvements need to be made to the verification environment as the bug rate drops

(e) Find bugs by using a simulation engine

(f) Find bugs by using an oscilloscope

(g) Discuss design intent and specification with designer and architect

(h) Discuss a miscompare between the HDL and the reference model with the designer

(i) List the tools needed for verification

(j) Create a reference model to check the design’s behavior

Q5. Which of the following should verification engineers do, and which should they avoid? Please explain your answers.

(a) Talk to designers about the function and understand the design

(b) Rely on the DUV designer’s description for input/output specification

(c) When creating checkers and reference models, look at the HDL implement (RTL) for hard-to-predict cases

(d) Try to think of situations the designer might have missed

(e) Focus on exotic scenarios and situations

(f) After receiving a bug fix, move on to the next job in the test plan

(g) Try to fill all queues during simulation

(h) Focus on multiple events at the same time

(i) Move on to the next product after the initial tape-out because the work is complete

(k) Inform a bug to designer as soon as possible, then move to next jobs right after without explanation of the bug and fixing proposals.

(l) When a test-vector is failed in simulation, put it aside and do next job. Check it again when possible.

Q6. In a project, should random verification or directed verification be processed firstly? Why?