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MAX77658

Ultra-Low Power PMIC Featuring Single-Inductor, 3-Output Buck-Boost, 2-LDOs, Power-Path Charger, and Fuel Gauge for Small Li+

General Description

The MAX77658 provides highly-integrated battery charging and power supply solutions for low-power applications where size and efficiency are critical. The IC features a SIMO buck-boost regulator that provides three highly-efficient and independently programmable power rails from a single inductor to minimize total solution size. Two 150mA LDOs provide ripple rejection for audio and other noise-sensitive applications. The LDOs can also be configured as load switches to manage power consumption by disconnecting external blocks when not required. A highly-configurable linear charger supports a wide range of Li+ battery capacities and includes battery temperature monitoring for additional safety (JEITA). The fuel-gauge implements the Maxim ModelGauge m5 EZ algorithm with ultra-low power. The IC provides best performance for batteries with 10mAhr to 1Ahr capacity.

This device includes three GPIOs and an analog multiplexer that selects between several internal voltage and current signals to an external node for monitoring with an external ADC. A bidirectional I^2C serial interface allows for configuring and checking the status of the devices. An internal on/off controller provides a controlled startup sequence for the regulators and provides supervisory functionality while they are on. Numerous factory programmable options allow the device to be tailored for many applications, enabling faster time to market.

Applications

- Bluetooth Headphones, Hearables
- Wireless Speakers
- Wearables
- Safety and Security Monitors
- Sensor Nodes
- Internet of Things (IoT)

Benefits and Features

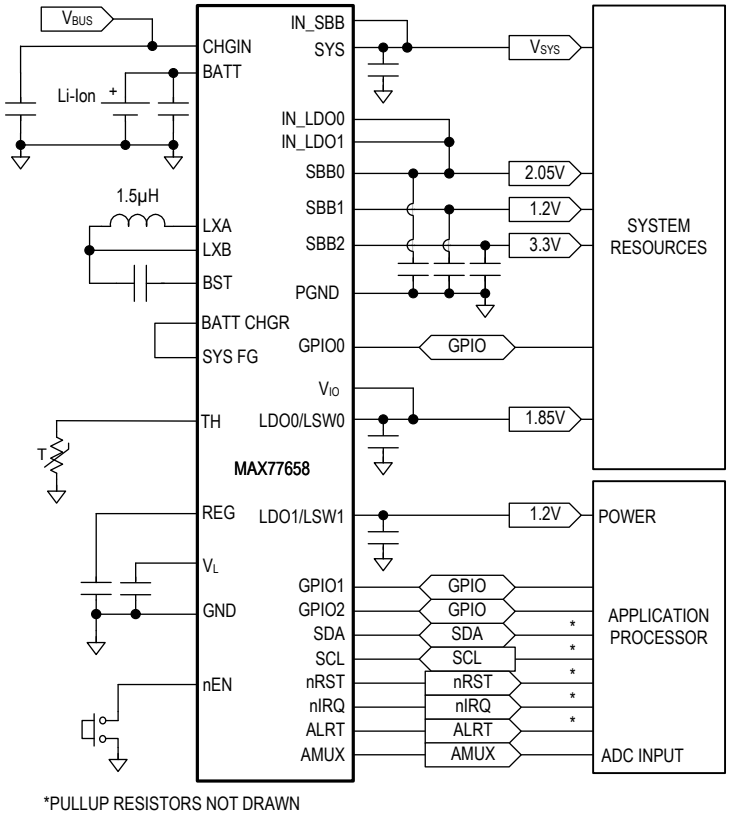
- Highly Integrated
  - 3x Output, Single-Inductor Multiple-Output (SIMO) Buck-Boost Regulator
    - Supports Wide Output Voltage Range from 0.5V to 5.5V for all SIMO Channels
    - Delivers Up to Total 750mA Load Current
    - SBB2 can be Configured to 1.5A Peak Inductor Current Limit to Support a Heavily Loaded Rail.
  - 2x 150mA LDO/LSW
  - Smart Power Selector™ Li+/Li-Poly Charger
  - 3x GPIO Resources
  - Analog MUX Output for Power Monitoring
  - Lowest Power mode < 700nA I_Q
  - Watchdog Timer
- Low Power
  - 1µA Shutdown Current
  - 11.2µA Operating Current (3 SIMO Channels + 2 LDOs + Fuel Gauge)
- Charger Optimized for Small Li-Ion Battery Size
  - Programmable Fast-Charge Current from 7.5mA to 300mA
  - Programmable Battery Regulation Voltage from 3.6V to 4.6V
  - Programmable Termination Current from 0.375mA to 45mA
  - JEITA Battery Temperature Monitors Adjust Charge Current and Battery Regulation Voltage for Safe Charging
- Fuel Gauge M5 ModelGauge EZ
  - No Calibration Required for EZ Performance
  - Robust Against Battery Variation
  - Die-Temperature or External Thermistor Measurement Capability
  - Integrated Internal Current Sensing Using Internal Sense Resistor
  - Compensates for Age, Current, Temperature
  - Does Not Require Empty, Full, Idle States
- Flexible and Configurable
  - I^2C-Compatible Interface and GPIO
- Small Size
  - 9.55mm^2 Wafer-Level Package (WLP)
  - 36-Bump, 0.5mm Pitch, 6x6 Array

***Ordering Information* appears at end of data sheet.**

PRELIMINARY

Datasheet Document ID; Rev 1; 5/21

Simplified Block Diagram



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Absolute Maximum Ratings

nEN, nIRQ, nRST to GND ..... -0.3V to V_{SYS} + 0.3V
SCL, SDA, GPIO to GND ..... -0.3V to V_{IO} + 0.3V
CHGIN to GND ..... -0.3V to +30.0V
SYS, BATT CHGR, SYS FG to GND ..... -0.3V to +6.0V
SYS to IN_SBB ..... -0.3V to +0.3V
V_L to GND ..... -0.3V to +6.0V
AMUX to GND ..... -0.3V to +6.0V
nIRQ, nRST, SDA, AMUX, GPIO, ALRT Continous Current ..... ±20mA
CHGIN Continuous Current ..... $1.2A_{RMS}$
SYS Continuous Current ..... $1.2A_{RMS}$
BATT CHGR Continuous Current (Note 1) ..... $1.2A_{RMS}$
IN_LDO0, IN_LDO1 to GND ..... -0.3V to 6.0V
LDO0, LDO1 to GND ..... -0.3V to V_{IN_LDO} + 0.3V
V_{IO} to GND ..... -0.3V to V_{SYS} + 0.3V
IN_SBB to PGND ..... -0.3V to +6.0V
LXA Continuous Current (Note 2) ..... $1.2A_{RMS}$
LXB Continuous Current (Note 2) ..... $1.2A_{RMS}$
SBB0, SBB1, SBB2 to PGND ..... -0.3V to +6.0V
BST to IN_SBB ..... -0.3V to +6.0V
BST to LXB ..... -0.3V to +6.0V
SBB0, SBB1, SBB2 Short-Circuit Duration ..... Continuous
PGND to GND ..... -0.3V to +0.3V
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C
Continuous Power Dissipation (Multilayer Board, T_A = +70°C, derate 20.4mW/°C above +70°C) 1632mW
ALRT to GND ..... -0.3V to +17V
REG to GND ..... -0.3V to +2.2V
TH to GND ..... -0.3 V to V_{BATT} + 0.3 V
Continuous Source Current for TH 1mA
Lead Temperature (soldering 10s) ..... +300ºC
Current Limit of Sense Resistor (Continuous current at 100% utilization (Note 3)) 0.8A
Current Limit of Sense Resistor (Continuous current at 10% utilization (Note 3)) 1.2A

Note 1: Do not repeatedly hot-plug a source to the BATT CHGR terminal at a rate greater than 10Hz. Hot plugging low impedance sources results in an ~8A momentary (~2µs) current spike.

Note 2: Do not externally bias LXA or LXB. LXA has internal clamping diodes to PGND and IN_SBB. LXB has an internal low-side clamping diode to PGND and an internal high-side clamping diode that dynamically connects to a selected SIMO output. It is normal for these diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to V_{SBB0} + 0.3V.

Note 3: Guaranteed by design and not production tested. Total available utilization is 100,000 hours. Utilization is proportionately cumulative. See the *Current Measurement* section for a detailed explanation of the current limit under different utilization patterns.

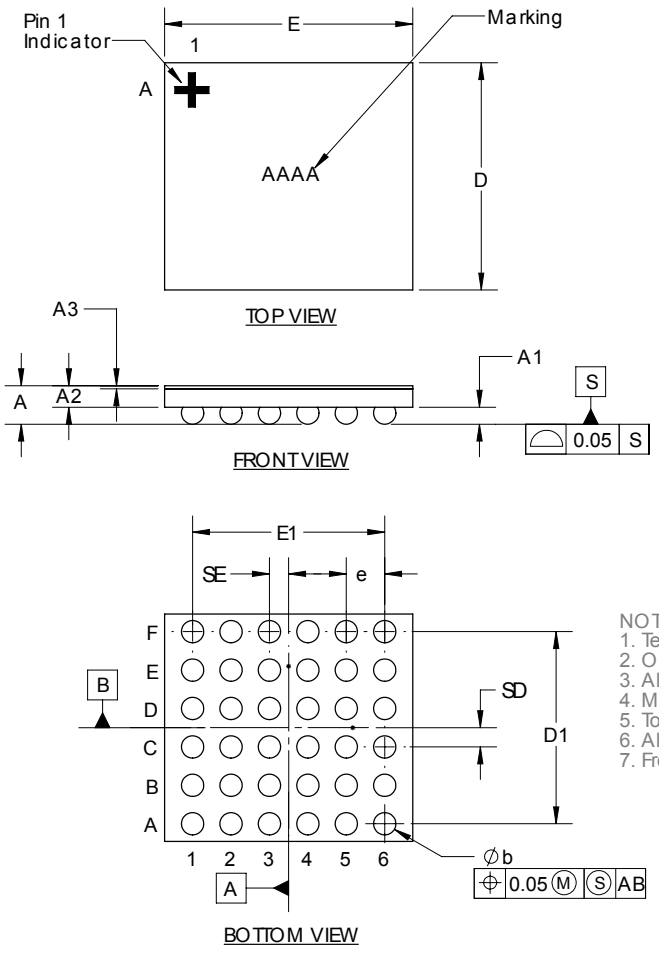
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	N362A3+1
Outline Number	21-100490
Land Pattern Number	*Refer to Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49ºC/W (2s2p board)

PRELIMINARY



COMMON DIMENSIONS	
A	0.50 MAX
A1	0.19 ±0.03
A2	0.28 REF
A3	0.04 BASIC
b	∅0.29 ±0.03
D	2.958 ±0.025
E	3.228 ±0.025
D1	2.50 BASIC
E1	2.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to Pb Free (+) package codes only.
7. Front - side finish can be either Black or Clear.

maxim integrated™

TITLE: PACKAGE OUTLINE 36 BUMPS THIN WLP PKG. 0.5 mm PITCH, N362A3+1

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-100490	A	1/1

PRELIMINARY

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{IN_SBB} = V_{IN_LDOx} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TOP-LEVEL						
Operating Voltage Range	V_{SYS}		2.7		5.5	V

Electrical Characteristics (continued)

(V_{CHGIN} = 0V, V_{SYS} = V_{BATT} = V_{IN_SBB} = V_{IN_LDOx} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Supply Current	I_{SHDN}	Current measured into BATT and SYS and IN_SBB and IN_LDOx, all resources are off (LDO0, LDO1, SBB0, SBB1, SBB2), T_A = +25°C	FG is in shutdown mode		1.0	1.9	µA
			Fuel gauge is in hibernate mode		6.0	8.0	
			Fuel gauge is in active mode		16.5	23	
Main Bias Quiescent Current	I_Q	Main bias is in normal-power mode (CNFG_GLBL.SBIA_LPM = 0)			28		µA
Quiescent Supply Current	I_Q	Main bias is in low-power mode, current measured into BATT and SYS and IN_SBB and IN_LDOx; LDO0, LDO1, SBB0, SBB1, SBB2 are enabled with no load watchdog timer disabled, fuel gauge is in hibernate mode, T_A = -40°C to 85°C			11.2	25	µA
BATT Factory-Ship Mode Current	$I_{BATT-FSM}$	Factory-ship mode (BATT to SYS switch open), T_A = +25°C, V_{BATT} = 3.7V, V_{SYS} = V_{INLDO0} = V_{INLDO1} = 0V, fuel gauge in shutdown mode			0.7	1.5	µA

Electrical Characteristics—Global Resources

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS						
Main Bias Enable Time	t_{SBIAS_EN}			0.5		ms
VOLTAGE MONITORS / POWER-ON RESET (POR)						
POR Threshold	V_{POR}	V_{SYS} falling		1.55		V
POR Threshold Hysteresis				150		mV
VOLTAGE MONITORS / UNDERVOLTAGE LOCKOUT (UVLO)						
UVLO Threshold	$V_{SYSUVLO}$	V_{SYS} falling	2.45	2.6	2.73	V
UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$			200		mV
VOLTAGE MONITORS / OVERVOLTAGE LOCKOUT (OVLO)						
OVLO Threshold	$V_{SYSOVLO}$	V_{SYS} rising	5.70	5.85	6.00	V
THERMAL MONITORS						
Overtemperature-Lockout Threshold	T_{OTLO}	T_J rising		145		°C
Thermal Alarm Temperature 1	T_{JAL1}	T_J rising		80		°C
Thermal Alarm Temperature 2	T_{JAL2}	T_J rising		100		°C

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Thermal Alarm Temperature Hysteresis					15		°C
ENABLE INPUT (nEN)							
nEN Input Leakage Current	I_{nEN_LKG}	V_{nEN} = V_{CCINT} = 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +125°C		±0.01		
nEN Input Falling Threshold	$V_{TH\_nEN\_F}$	nEN Falling		V_{CCINT} - 1.4	V_{CCINT} - 1.0		V
nEN Input Rising Threshold	$V_{TH\_nEN\_R}$	nEN Rising			V_{CCINT} - 0.9	V_{CCINT} - 0.6	V
V_{CC} Internal	V_{CCINT}	(*Note 4*)	V_{CHGIN} = 0V, battery is present (V_{BATT} is valid)		V_{BATT}		V
			V_{CHGIN} = 5V, not suspended (CNFG_CHG_G.USBS = 0)		V_L		
Debounce Time	t_{DBNC_nEN}	CNFG_GLBL.DBEN_nEN = 0			500		µs
		CNFG_GLBL.DBEN_nEN = 1			30		ms
Manual Reset Time	t_{MRST}	CNFG_GLBL.T_MRT = 1		3	4	5	s
		CNFG_GLBL.T_MRT = 0		7	8	10.5	
nEN Internal Pullup	R_{nEN-PU}	Pullup to V_{CCINT}	PU_DIS = 0		200		kΩ
			PU_DIS = 1		10000		
OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Falling Edge Time	t_{f_nIRQ}	$C_{\overline{IRQ}}$ = 25pF			2		ns
Leakage Current	I_{nIRQ_LKG}	V_{SYS} = V_{IO} = 5.5V nIRQ is high impedance (no interrupts) V_{nIRQ} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +125°C		±0.01		
OPEN-DRAIN RESET OUTPUT (nRST)							
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Falling Edge Time	t_{f_nRST}	C_{RST} = 25pF			2		ns
nRST Deassert Delay Time	t_{RSTODD}	See Figure 11 and Figure 12 for more information			5.12		ms
nRST Assert Delay Time	t_{RSTOAD}				10.24		ms

PRELIMINARY

Electrical Characteristics—Global Resources (continued)

(V_{SYS} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Leakage Current	I_{nRST_LKG}	V_{SYS} = V_{IO} = 5.5V nRST is high impedance (no reset) V_{nRST} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +125°C		±0.01		
GENERAL PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage Low	V_{IL}	V_{IO} = 1.8V				0.3 x V_{IO}	V
Input Voltage High	V_{IH}	V_{IO} = 1.8V		0.7 x V_{IO}			V
Input Leakage Current	I_{GPI_LKG}	CNFG_GPIOx.DIR = 1 V_{IO} = 5.5V V_{GPIO} = 0V and 5.5V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +125°C		±0.01		
Output Voltage Low	V_{OL}	I_{SINK} = 2mA				0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA		0.8 x V_{IO}			V
Input Debounce Time	t_{DBNC_GPI}	CNFG_GPIOx.DBEN_GPI = 1			30		ms
Output Falling Edge Time	t_{f_GPIO}	C_{GPIO} = 25pF			3		ns
Output Rising Edge Time	t_{r_GPIO}	C_{GPIO} = 25pF			3		ns
FLEXIBLE POWER SEQUENCER							
FPS Startup Delay	t_{FPS_DLY}				1.43		ms
Power-Up Event Periods	t_{EN}	See Figure 10			1.28		ms
Power-Down Event Periods	t_{DIS}	See Figure 10			2.56		ms

PRELIMINARY

Electrical Characteristics—Smart Power Selector Charger

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC INPUT							
CHGIN Valid Voltage Range	V_{CHGIN}	Initial CHGIN voltage before enabling charging		4.1		7.25	V
CHGIN Standoff Voltage Range	$V_{STANDOFF}$	DC rising			28		V
CHGIN Overvoltage Threshold	V_{CHGIN_OVP}	DC rising		7.25	7.50	7.75	V
CHGIN Overvoltage Hysteresis					100		mV
CHGIN Undervoltage Lockout	V_{CHGIN_UVLO}	DC rising	HYST_CHGINUVLO_100 = 0	4.0	4.1	4.2	V
			HYST_CHGINUVLO_100 = 1		3.6		

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN Undervoltage-Lockout Hysteresis		HYST_CHGINUVLO_100 = 0		600		mV
		HYST_CHGINUVLO_100 = 1		100		
Input Current-Limit Range	$I_{CHGIN-LIM}$	V_{SYS} = $V_{SYS-REG}$ - 100mV, programmable in 95mA steps	95		475	mA
Input Current-Limit Accuracy		$I_{CHGIN-LIM}$ = 95mA, V_{SYS} = $V_{SYS-REG}$ - 100mV	90	95	100	mA
		$I_{CHGIN-LIM}$ = 475mA, V_{SYS} = $V_{SYS-REG}$ - 100mV		475	500	
Minimum Input Voltage Regulation Range	$V_{CHGIN-MIN}$	V_{CHGIN} falling due to loading conditions and/or high-impedance charge source, programmable in 100mV increments with CNFG_CHG_B.VCHGIN_MIN[2:0]	4.0		4.7	V
Minimum Input Voltage Regulation Accuracy		$V_{CHGIN-MIN}$ = 4.5V (CNFG_CHG_B.VCHGIN_MIN[2:0] = 0b101), I_{CHGIN} reduced by 10%	4.32	4.50	4.68	V
Charger Input Debounce Timer	$t_{CHGIN-DB}$	V_{CHGIN} = 5V, time before CHGIN is allowed to deliver current to SYS or BATT	100	120	140	ms
SUPPLY AND QUIESCENT CURRENTS						
CHGIN Supply Current	I_{CHGIN}	V_{CHGIN} = 5V, charger is not in USB suspend (CNFG_CHG_G.USBS = 0), charging is finished (STAT_CHG_B.CHG_DTLS[3:0] indicates done), I_{SYS} = 0mA		1.0	1.8	mA
		V_{CHGIN} = 0V to 1V, V_{BATT} = 3.3V, I_{SYS} = 0mA			50	µA
CHGIN Suspend Supply Current	$I_{CHGIN-SUS}$	V_{CHGIN} = 5V, charger in USB suspend (CNFG_CHG_G.USBS = 1)			50	µA
BATT Bias Current	$I_{BATT-BIAS}$	V_{CHGIN} = 5V, charger is not in USB suspend (CNFG_CHG_G.USBS = 0), charging is finished (STAT_CHG_B.CHG_DTLS[3:0] indicates done), I_{SYS} = 0mA		5		µA
PREQUALIFICATION						
Prequalification Voltage Threshold Range	V_{PQ}	Programmable in 100mV steps with CNFG_CHG_C.CHG_PQ[2:0]	2.3		3.0	V
Prequalification Voltage Threshold Accuracy		V_{PQ} = 3.0V	-3		+3	%
Prequalification Mode Charge Current	I_{PQ}	V_{BATT} = 2.5V, V_{PQ} = 3.0V, Expressed as a percentage of $I_{FAST-CHG}$, CNFG_CHG_B.I_PQ = 0		10		%
		V_{BATT} = 2.5V, V_{PQ} = 3.0V, Expressed as a percentage of $I_{FAST-CHG}$, CNFG_CHG_B.I_PQ = 1		20		
Prequalification Safety Timer	t_{PQ}	V_{BATT} < V_{PQ} = 3.0V	27	30	33	minutes

PRELIMINARY

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAST-CHARGE							
Fast-Charge Voltage Range	$V_{FAST-CHG}$	I_{BATT} = 0mA, programmable in 25mV steps with CNFG_CHG_G.CHG_CV[5:0]		3.6		4.6	V
Fast-Charge Voltage Accuracy		I_{BATT} = 0mA	$V_{FAST-CHG}$ = 4.3V, V_{SYS} = 4.5V, T_A = +25°C	-0.5		+0.5	%
			$V_{FAST-CHG}$ = 3.6V to 4.6V, V_{SYS} = 4.8V			1.0	
Fast-Charge Current Range	$I_{FAST-CHG}$	Programmable in 7.5mA steps with CNFG_CHG_E.CHG_CC[5:0]		7.5		300	mA
Fast-Charge Current Accuracy		T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV	$I_{FAST-CHG}$ = 15mA	-1.5		+1.5	%
			$I_{FAST-CHG}$ = 300mA	-2.0		+2.0	
Fast-Charge Current Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV, T_A = -40°C to +125°C		-10		+10	%
Fast-Charge Safety Timer Range	t_{FC}	Programmable in 2 hour increments or disabled with CNFG_CHG_E.T_FAST_CHG[1:0], time measured from prequal. done to timer fault		3		7	hours
Fast-Charge Safety Timer Accuracy		t_{FC} = 3 hours		-10		+10	%
Fast-Charge Safety Timer Suspend Threshold		Fast-charge CC mode, fast-charge safety timer paused when charge current drops below this threshold, expressed as a percentage of $I_{FAST-CHG}$			20		%
Junction Temperature Regulation Setting Range	T_{J-REG}	Programmable in 10°C steps with CNFG_CHG_D.TJ_REG[2:0]		60		100	°C
Junction Temperature Regulation Loop Gain	G_{TJ-REG}	Rate at which $I_{FAST-CHG}/I_{PQ}$ is reduced to maintain T_{J-REG}, expressed a percentage of $I_{FAST-CHG}/I_{PQ}$ per degree centigrade rise			-5.4		%/°C
Charge Current Soft-Start Slew Time		Zero to full-scale			1		ms
TERMINATION AND TOP-OFF							
End-of-Charge Termination Current	I_{TERM}	CNFG_CHG_C.I_TERM[1:0] = 0b00 expressed as a percentage of $I_{FAST-CHG}$			5		%
		CNFG_CHG_C.I_TERM[1:0] = 0b01 expressed as a percentage of $I_{FAST-CHG}$			7.5		
		CNFG_CHG_C.I_TERM[1:0] = 0b10 expressed as a percentage of $I_{FAST-CHG}$		8.5	10	11.5	
		CNFG_CHG_C.I_TERM[1:0] = 0b11 expressed as a percentage of $I_{FAST-CHG}$			15		

Electrical Characteristics—Smart Power Selector Charger (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Top-Off Timer Range	t_{TO}	I_{BATT} < I_{TERM}, programmable in 5 minute steps with CNFG_CHG_C.T_TOPOFF[2:0]		0		35	minutes
Top-Off Timer Accuracy		t_{TO} = 10 minutes		-10		+10	%
Charge Restart Threshold	$V_{RESTART}$	Charging is finished (STAT_CHG_B.CHG_DTLS[3:0] indicates done and CNFG_CHG_H.CHR_TH_EN = 1) Charging resumes when V_{BATT} < $V_{FAST-CHG}$ - $V_{RESTART}$		65	150		mV
End-of-Charge Termination Current Accuracy		$I_{FAST-CHG}$ = 15mA, I_{TERM} = 1.5mA (10% of $I_{FAST-CHG}$), T_A = +25°C		1.35	1.5	1.65	mA
		$I_{FAST-CHG}$ = 300mA, I_{TERM} = 30mA (10% of $I_{FAST-CHG}$), T_A = +25°C		27	30	33	
End-of-Charge Termination Current Glitch Filter					60		µs
DEVICE ON-RESISTANCE AND LEAKAGE							
BATT CHGR to SYS On-Resistance		V_{BATT} = 3.7V, I_{BATT} = 300mA, V_{CHGIN} = 0V, battery is discharging to SYS			100	150	mΩ
Charger FET Leakage Current		V_{SYS} = 4.5V, V_{BATT} = 0V, charger disabled	T_A = +25°C		0.1	1.0	µA
			T_A = +125°C		1		
CHGIN to SYS On-Resistance					600		mΩ
Input FET Leakage Current		V_{CHGIN} = 0V, V_{SYS} = 4.2V, body-switched diode reverse biased	T_A = +25°C		0.1	1.0	µA
			T_A = +125°C		1		
SYSTEM NODE							
System Voltage Regulation Range	$V_{SYS-REG}$	Programmable in 50mV steps with CNFG_CHG_D.VSYS_REG[4:0]		3.4		4.8	V
System Voltage Regulation Accuracy	V_{SYS}	$V_{SYS-REG}$ = 4.5V, I_{SYS} = 1mA	T_A = +25°C	4.41	4.50	4.59	V
			T_A = -40°C to +125°C	4.365	4.5	4.635	
Minimum System Voltage Regulation Loop Setpoint	$V_{SYS-MIN}$	V_{CHGIN} = 5V, $V_{SYS-REG}$ = 4.5V, V_{SYS} < $V_{SYS-REG}$ due to I_{CHGIN} = $I_{CHGIN-LIM}$ (input in current limit), battery charging, I_{BATT} reduced to 50% of $I_{FAST-CHG}$ (minimum system voltage regulation active)		4.34	4.4	4.45	V
Supplement Mode System Voltage Regulation		I_{SYS} = 150mA			V_{BATT} - 0.15V		V
Active Discharge Resistance	R_{AD_SYS}	When CNFG_GLBL.SFT_CTRL[1:0] = 0b11 and CHGIN is disconnected		80	140	260	Ω

PRELIMINARY

Electrical Characteristics—Adjustable Thermistor Temperature Monitors

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JEITA TEMPERATURE MONITORS						
Temperature Threshold Hysteresis		Temperature hysteresis set on each JEITA threshold		3		°C
JEITA Modified Fast-Charge Voltage Range	$V_{FAST-CHG\_JEITA}$	I_{BATT} = 0mA, programmable in 25mV steps, battery is either cool or warm	3.6		4.6	V
JEITA Modified Fast-Charge Current Range	$I_{FAST-CHG\_JEITA}$	Programmable in 7.5mA steps, battery is either cool or warm	7.5		300	mA

Electrical Characteristics—Analog Multiplexer

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG MULTIPLEXER							
Full-Scale Voltage	V_{FS}				1.25		V
Channel Switching Time					0.3		µs
Off Leakage Current		V_{AMUX} = 0V, AMUX is high impedance	T_A = +25°C		1	500	nA
			T_A = +125°C		1		µA
CHGIN POWER MEASUREMENT							
CHGIN Current Monitor Gain	G_{ICHGIN}	V_{FS} corresponds to maximum $I_{CHGIN-LIM}$ setting			2.632		V/A
CHGIN Voltage Monitor Gain	G_{VCHGIN}	V_{FS} corresponds to V_{CHGIN_OVP}			0.167		V/V
BATT AND SYS POWER MEASUREMENT							
Battery Charge Current Monitor Gain	$G_{IBATT-CHG}$	V_{FS} corresponds to 100% of $I_{FAST-CHG}$ setting (CNFG_CHG_E.CHG_CC[5:0])			12.5		mV/%
Charge Current Monitor Accuracy		$I_{FAST-CHG}$ = 15mA, T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	%
		$I_{FAST-CHG}$ = 300mA, T_A = +25°C, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-3.5		+3.5	
Charge Current Monitor Accuracy over Temperature		Across all current settings, V_{BATT} = $V_{FAST-CHG}$ - 300mV		-10		+10	%
Battery Discharge Monitor Full-Scale Current Range	$I_{DISCHG-SCALE}$	Programmable with CNFG_CHG_I.IMON_DISCHG_SCALE[3:0]		8.2		300	mA
Battery Discharge Current Monitor Accuracy		15mA to 300mA battery discharge current, $I_{DISCHG-SCALE}$ = 300mA		-15		+15	%
Battery Discharge Current Monitor Offset		I_{BATT} = 0mA		-0.5		+0.8	mA
Battery-Voltage Monitor Gain	G_{VBATT}	V_{FS} corresponds to maximum $V_{FAST-CHG}$ setting			0.272		V/V

PRELIMINARY

Electrical Characteristics—Analog Multiplexer (continued)

(V_{CHGIN} = 5.0V, V_{SYS} = 4.5V, V_{BATT} = 4.2V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS Voltage Monitor Gain	G_{VSYS}	V_{FS} corresponds to maximum $V_{SYS-REG}$ setting		0.26		V/V

Electrical Characteristics—SIMO Buck-Boost

(V_{IN} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS / OUTPUT VOLTAGE RANGE (SBB0/1/2)							
Programmable Output Voltage Range	V_{SBBx}			0.5		5.5	V
Output DAC Bits					8		bits
Output DAC LSB Size		0.5V to 5.5V			25		mV
OUTPUT VOLTAGE ACCURACY							
Output Voltage Accuracy		V_{SBBx} falling, threshold where LXA switches high. Specified as a percentage of target output voltage.	T_A = -40°C to +125°C	-2.0		+2.0	%
OUT Over-Regulation Threshold	V_{OV}	T_A = +25°C			1.7	3	%
TIMING CHARACTERISTICS							
Enable Delay		Delay time from the SIMO receiving its first enable signal to when it begins to switch in order to service that output.			10		µs
Soft-Start Slew Rate	dV/dt_{SS}	I_{PK} = 1A, C_{OUT} = 10µF			5.0		mV/µs
POWER STAGE CHARACTERISTICS							
LXA Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V, or 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +125°C		±1.0		
LXB Leakage Current		SBB0, SBB1, SBB2 are disabled, V_{IN_SBB} = 5.5V, V_{LXA} = 0V or 5.5V, all V_{SBBx} = 5.5V	T_A = +25°C	-1.0	±0.1	+1.0	µA
			T_A = +125°C		±1.0		
BST Leakage Current		V_{IN_SBB} = 5.5V, V_{LXB} = 5.5V, V_{BST} = 11V,	T_A = +25°C		+0.01	+1.0	µA
			T_A = +125°C		+0.1		

PRELIMINARY

Electrical Characteristics—SIMO Buck-Boost (continued)

(V_{IN} = 3.7V, C_{SBBx} = 10µF, L = 1.5µH, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Disabled Output Leakage Current		SBB0, SBB1, SBB2 are disabled, active-discharge disabled (ADE_SBBx = 0), V_{SBBx} = 5.5V, V_{LXB} = 0V, V_{SYS} = V_{IN_SBB} = V_{BST} = 5.5V,	T_A = +25°C		+0.1	+1.0	µA
			T_A = +125°C		+0.2		
Active Discharge Resistance	R_{AD_SBBx}	SBB0, SBB1, SBB2 are disabled, active discharge enabled (CNFG_SBBx_B.ADE_SBBx = 1)		60	120	180	Ω
CONTROL SCHEME							
Peak Current Limit	I_{P_SBB} (*Note 5*)	CNFG_SBBx_B.IP_SBBx[1:0] = 0b11		-18%	0.335	+18%	A
		CNFG_SBBx_B.IP_SBBx[1:0] = 0b10		-14%	0.500	+14%	
		CNFG_SBBx_B.IP_SBBx[1:0] = 0b01		-8%	0.750	+8%	
		CNFG_SBBx_B.IP_SBBx[1:0] = 0b00		-7%	1.000	+7%	

Electrical Characteristics—Low Dropout Linear Regulator (LDO)/Load Switch (LSW)

(V_{SYS} = V_{IN_LDO} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO0/1						
Input Voltage Range	V_{IN_LDOx}	LDO mode	1.71		5.5	V
		Switch mode	1.2		5.5	
Quiescent Supply Current	I_{IN_LDOx}	I_{OUT_LDOx} = 0		1.4	2.4	µA
		I_{OUT_LDOx} = 0, switch mode		0.5	1.2	
Quiescent Supply Current In Dropout	$I_{IN\_DRP\_LDOx}$	I_{OUT_LDOx} = 0, V_{IN_LDOx} = 2.9V, V_{LDOx} = 3V		2.1	4.6	µA
Maximum Output Current	I_{OUT_LDOx}	V_{IN_LDOx} > 1.8V	150			mA
		V_{IN_LDOx} = 1.8V or lower	100			
Output Voltage	V_{OUT_LDOx}		0.5		5.0	V
Output Accuracy		V_{IN_LDOx} = (V_{OUT_LDOx} + 0.5V) or higher, I_{OUT_LDOx} = 1mA	-3.1		+3.1	%
Dropout Voltage	V_{DRP_LDOx}	V_{IN_LDOx} = 3V, LDOx programmed to 3V, I_{OUT_LDOx} = 100mA			100	mV
Line Regulation		V_{IN_LDOx} = (V_{OUT_LDOx} + 0.5 V) to 5.5V	-0.5		+0.5	%/V
Load Regulation		V_{IN_LDOx} = 1.8V or higher, I_{OUT_LDOx} = 100µA to 100mA		0.001	0.005	%/mA
Line Transient		V_{IN_LDOx} = 4V to 5V, 5µs rise time		± 35		mV

Electrical Characteristics—Low Dropout Linear Regulator (LDO)/Load Switch (LSW) (continued)

(V_{SYS} = V_{IN_LDO} = 3.7V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Load Transient		I_{OUT_LDOx} = 100µA to 10mA, 200ns rise time		100		mV
		I_{OUT_LDOx} = 100µA to 100mA, 200ns rise time		200		
Active Discharge Resistance	R_{AD_LDOX}		42	80	200	Ω
Switch Mode On-Resistance	R_{ON_LDOx}	V_{IN_LDOx} = 2.7V, I_{OUT_LDOx} = 100mA			0.5	Ω
		V_{IN_LDOx} = 1.8V, I_{OUT_LDOx} = 50mA			0.8	
		V_{IN_LDOx} = 1.2V, I_{OUT_LDOx} = 5mA			1.2	
Slew Rate		I_{OUT_LDOx} = 0mA, time from 10% to 90% of final register value		2.2		V/ms
		I_{OUT_LDOx} = 0mA, time from 10% to 90% of final register value, switch mode		2.2		
Short Circuit Current Limit		V_{IN_LDOx} = 2.7V, V_{OUT_LDOx} = GND	230	550	880	mA
		V_{IN_LDOx} = 2.7V, V_{OUT_LDOx} = 2.55V, switch mode	230	550		
Output Noise		10Hz to 100kHz, V_{IN_LDOx} = 5V, V_{OUT_LDOx} = 3.3V		150		μV_{RMS}
		10Hz to 100kHz, V_{IN_LDOx} = 5V, V_{OUT_LDOx} = 2.5V		125		
		10Hz to 100kHz, V_{IN_LDOx} = 5V, V_{OUT_LDOx} = 1.2V		90		
		10Hz to 100kHz, V_{IN_LDOx} = 5V, V_{OUT_LDOx} = 0.9V		80		
Output DAC Bits				8		bits
Output DAC LSB Size				25		mV

Electrical Characteristics—FUEL GAUGE

(V_{BATT} = 2.3V to 4.9V, T_A = -40ºC to +125ºC, typical value for T_A is +25ºC. Limits are 100% tested at T_A = +25°C. The operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{BATT}		2.3		4.9	V
Shutdown Supply Current	I_{DD0}	T_A ≤ +50ºC		0.5	0.9	µA
Hibernate Supply Current	I_{DD1}	T_A ≤ +50ºC, average current		5.2	12	µA
Active Supply Current	I_{DD2}	T_A ≤ +50ºC, average current not including thermistor measurement current		16	30	µA
Regulation Voltage	V_{REG}			1.8		V

Electrical Characteristics—FUEL GAUGE (continued)

(V_{BATT} = 2.3V to 4.9V, T_A = -40ºC to +125ºC, typical value for T_A is +25ºC. Limits are 100% tested at T_A = +25°C. The operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Startup Voltage with Charge Pump	V_{PCKPSU}			1.9	2.6	V
ANALOG-TO-DIGITAL CONVERSION						
BATT Measurement Error	V_{GERR}	T_A = +25ºC	-7.5		+7.5	mV
		-40ºC ≤ T_A ≤ +125ºC	-20		+20	
BATT Measurement Resolution	V_{LSB}			78.125		µV
BATT Measurement Range	V_{FS}		2.3		4.9	V
Sense Resistance	R_{SNS}	T_A = +25°C		35		mΩ
Current Measurement Offset Error	I_{OERR}	Zero current, long term average		±1		mA
Current Measurement Resolution	I_{LSB}			0.03125		mA
Current Measurement Gain Error	I_{GERR}	(*Note 6*)		±2.5		% of Reading
Current Measurement Error	I_{ERR}	T_A ≤ +50ºC, 0.15A and 0.3A (*Note 6*)	-3	±0.5	+3	% of Reading
		T_A ≤ +50ºC, 0.5A (*Note 6*)		±1		
Internal Temperature Measurement Error	TI_{GERR}	-40ºC ≤ T_A ≤ +125ºC		±1		ºC
Internal Temperature Measurement Resolution	TI_{LSB}			0.00391		ºC
INPUT/OUTPUT						
External Thermistance Resistance	R_{EXT10}	Config.R100 = 0		10		kΩ
	R_{EXT100}	Config.R100 = 1		100		
Output Drive Low, ALRT	V_{OL}	I_{OL} = 4mA, V_{BATT} = 2.3V			0.4	V
Input Logic High, ALRT, SCL, SDA	V_{IH}		1.5			V
Input Logic Low, ALRT, SCL, SDA	V_{IL}				0.5	V
Battery-Detach Detection Threshold	V_{DET}	Measured as a fraction of V_{BATT} on TH rising	91	96.2	99	%
Battery-Detach Detection Threshold Hysteresis	$V_{DET-HYS}$	Measured as a fraction of V_{BATT} on TH falling		1		%
Battery-Detach Comparator Delay	t_{TOFF}	TH step from 70% to 100% of V_{BATT} (Alrtp = 0, EnAIN = 1, FTHRM = 1)			100	µs
LEAKAGE						
Leakage Current, CSN, ALRT	I_{LEAK}	V_{ALRT} < 15V	-1		+1	µA
Input Pulldown Current	I_{PD}	V_{SDA} = 0.4V, V_{SCL} = 0.4V	0.05	0.2	0.4	µA

Electrical Characteristics—FUEL GAUGE (continued)

(V_{BATT} = 2.3V to 4.9V, T_A = -40ºC to +125ºC, typical value for T_A is +25ºC. Limits are 100% tested at T_A = +25°C. The operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING						
Time-Base Accuracy	t_{ERR}	T_A = +25°C	-1		+1	%
TH Precharge Time	t_{PRE}		8.48			ms

Electrical Characteristics—I²C Serial Communication

(V_{IN} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage Range	V_{IO}		1.7	1.8	3.6	V
V_{IO} Bias Current		V_{IO} = 3.6V, V_{SDA} = V_{SCL} = 0V or 3.6V, T_A = +25°C	-1	0	+1	µA
		V_{IO} = 1.7V, V_{SDA} = V_{SCL}= 0V or 1.7V	-1	0	+1	
SDA AND SCL I/O STAGE						
SCL, SDA Input High Voltage	V_{IH}	V_{IO} = 1.7V to 3.6V	0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}	V_{IO} = 1.7V to 3.6V			0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Leakage Current	I_I	V_{IO} = 3.6V, V_{SCL} = V_{SDA} = 0V and 3.6V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL}	t_{OF} (*Note 6*)				120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST AND FAST-MODE PLUS) (*Note 6*)						
Clock Frequency	f_{SCL}		0		400	kHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		0.6			µs
SCL Low Period	t_{LOW}		1.3			µs
SCL High Period	t_{HIGH}		0.6			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.6			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		100			ns
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs

Electrical Characteristics—I²C Serial Communication (continued)

(V_{IN} = 3.7V, V_{IO} = 1.8V, limits are 100% production tested at T_A = +25°C, limits over the operating temperature range (T_A = -40°C to +125°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Free Time between STOP and START Condition	t_{BUF}		1.3			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C_B = 400pF) (*Note 6*)						
SCL Fall Time	t_{FCL}	T_A = +25°C	20		80	ns

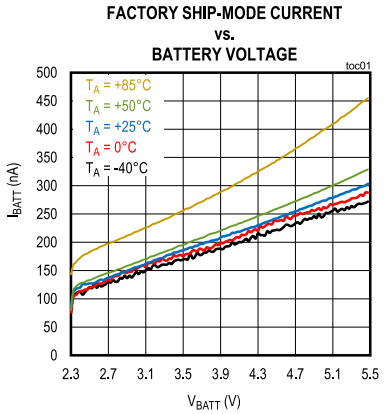
Note 4: See the *nEN Internal Pullup Resistors to VCCINT* section for more details

Note 5: Typical values align with bench observations using the stated conditions with an inductor. Minimum and maximum values are tested in production with DC currents without an inductor. See the *Typical Operating Characteristics* SIMO switching waveforms to gain more insight on this specification.

Note 6: Design guidance only. Not production tested.

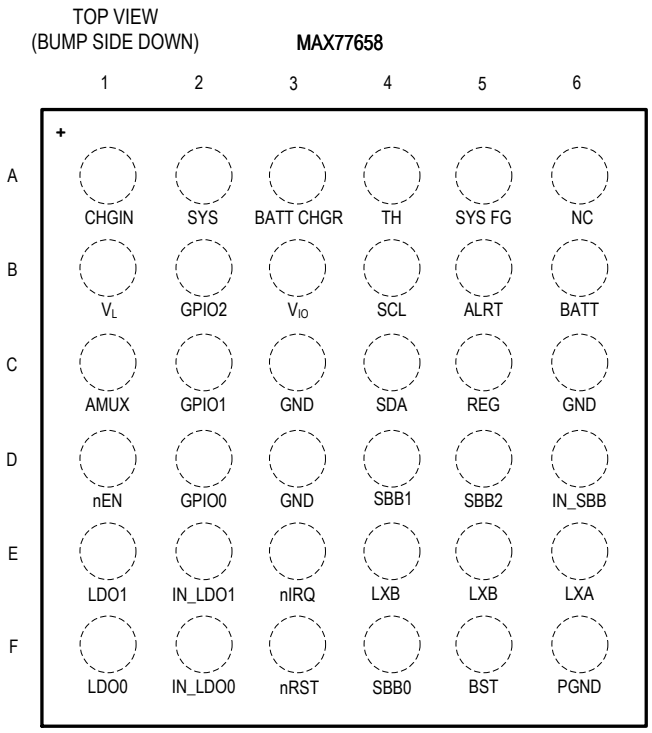
Typical Operating Characteristics

(Typical Applications Circuit. V_{CHGIN} = 0V, V_{SYS} = V_{IN_SBB} = V_{BATT} = 3.7V, V_{IO} = 1.8V, T_A = +25°C, V_{SBB0} = 1.8V, I_{P_SBB0} = 0.5A, SBB0 in Buck mode, V_{SBB1} = 1.1V, I_{P_SBB1} = 0.5A, SBB1 in Buck mode, V_{SBB2} = 3.3V, I_{P_SBB2} = 1A peak, SBB2 in Buck-Boost mode, unless otherwise noted. Inductor = DFE201612E-2R2M, 2.2µH, 116mΩ.)



Pin Configuration

WLP



WLP
(3.228mm x 2.958mm x 0.5mm, 0.5mm PITCH)

PRELIMINARY

Pin Description

PIN	NAME	FUNCTION	TYPE
A6	NC	Not connected.	
TOP LEVEL			
B3	V_{IO}	I^2C Interface and GPIO Driver Power	Power Input
D1	nEN	Active-Low Enable Input. $\overline{EN}$ supports push-button, slide-switch, or logic mode configurations. If not used, connect $\overline{EN}$ to SYS and use the CNFG_SBBx_B.EN_SBBx[2:0] and CNFG_LDOx_B.EN_LDOx[2:0] bitfields to enable channels.	Digital Input
E3	nIRQ	Active-Low, Open-Drain Interrupt Output. Connect a 100kΩ pullup resistor between $\overline{IRQ}$ and a voltage equal to or less than V_{SYS}.	Digital Output
F3	nRST	Active-Low, Open-Drain Reset Output. Connect a 100kΩ pullup resistor between $\overline{RST}$ and a voltage equal to or less than V_{SYS}.	Digital Output
B2	GPIO2	General Purpose Input/Output. The GPIO I/O stage is internally biased with V_{IO}	Digital I/O

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
C2	GPIO1	General Purpose Input/Output. The GPIO I/O stage is internally biased with V_{IO}.	Digital I/O
D2	GPIO0	General Purpose Input/Output. The GPIO I/O stage is internally biased with V_{IO}.	Digital I/O
B4	SCL	I^2C Clock	Digital Input
C4	SDA	I^2C Data	Digital I/O
C1	AMUX	Analog Multiplexer Output. Connect to system ADC to perform conversions on charger power signals.	Analog Output
C3, C6, D3	GND	Quiet Ground. Connect GND to PGND, and the low-impedance ground plane of the PCB.	Ground
CHARGER			
A1	CHGIN	Charger Input. Connect to a DC charging source. Bypass to PGND with a 4.7µF ceramic capacitor.	Power Input
A2	SYS	System Power Output. SYS provides power to the system resources as well as the control logic of the device. Connect to IN_SBB and bypass to GND with a 22µF ceramic capacitor.	Power Output
A3	BATT CHGR	Battery Connection to the Charger. Connect to SYS FG pin if fuel gauge is intended to be used. Otherwise, connect to positive battery terminal. Bypass to GND with a 4.7µF ceramic capacitor.	Power I/O
B1	V_L	Internal charger 3V logic supply powered from CHGIN. Bypass to GND with a 1µF ceramic capacitor. Do not load V_L externally.	Power Output
A4	TH	Thermistor Input. Connect a thermistor from TH to GND. TH also provides battery insertion/removal detection. Connect to BATT if not used.	
SIMO BUCK-BOOST			
D6	IN_SBB	SIMO Power Input. Connect IN_SBB to SYS and bypass to PGND with a minimum of 10µF ceramic capacitor as close as possible to the IN_SBB pin.	Power Input
F4	SBB0	SIMO Buck-Boost Output 0. SBB0 is the power output for channel 0 of the SIMO buck-boost. Bypass SBB0 to PGND with a 22µF ceramic capacitor. If not used, see the *Unused Outputs* section.	Power Output
D4	SBB1	SIMO Buck-Boost Output 1. SBB1 is the power output for channel 1 of the SIMO buck-boost. Bypass SBB1 to PGND with a 22µF ceramic capacitor. If not used, see the *Unused Outputs* section.	Power Output
D5	SBB2	SIMO Buck-Boost Output 2. SBB2 is the power output for channel 2 of the SIMO buck-boost. Bypass SBB2 to PGND with a 22µF ceramic capacitor. If not used, see the *Unused Outputs* section.	Power Output
F5	BST	SIMO Power Input for the High-Side Output NMOS Drivers. Connect a 10nF ceramic capacitor between BST and LXB.	Power Input
E4, E5	LXB	Switching Node B. LXB is driven between PGND and SBBx when SBBx is enabled. LXB is driven to PGND when all SIMO channels are disabled. Connect a 1.5µH inductor between LXA and LXB.	Power Input
E6	LXA	Switching Node A. LXA is driven between PGND and IN_SBB when any SIMO channel is enabled. LXA is driven to PGND when all SIMO channels are disabled. Connect a 1.5µH inductor between LXA and LXB.	Power I/O
F6	PGND	Power ground for the SIMO low-side FETs. Connect PGND to GND, and the low-impedance ground plane of the PCB.	Ground
LDO			
F2	IN_LDO0	Linear Regulator Input. If connected to a SIMO output with a short trace, IN_LDO0 can share the output's capacitor. Otherwise, bypass with a 2.2µF ceramic capacitor to ground. If not used, connect to ground or leave unconnected.	Power Input

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
E2	IN_LDO1	Linear Regulator Input. If connected to a SIMO output with a short trace, IN_LDO1 can share the output's capacitor. Otherwise, bypass with a 2.2µF ceramic capacitor to ground. If not used, connect to ground or leave unconnected.	Power Input
F1	LDO0	Linear Regulator Output 0. Bypass with a 1.0µF ceramic capacitor to GND. If not used, disable LDO0 and connect this pin to ground or leave unconnected.	Power Output
E1	LDO1	Linear Regulator Output 1. Bypass with a 1.0µF ceramic capacitor to GND. If not used, disable LDO1 and connect this pin to ground or leave unconnected.	Power Output
FUEL GAUGE			
B5	ALRT	Alert Output. The ALRT pin is an open-drain active-low output which indicates fuel-gauge alerts. Connect to GND if not used.	
C5	REG	Internal 1.8V Regulator Output. Bypass with an external 0.47µF capacitor to GND. Do not load externally.	
A5	SYS FG	System Power of Fuel Gauge. Connect to BATT CHGR or connect to system load.	
B6	BATT	IC Power Supply and Battery Voltage Sense Input. Connect to the positive terminal of a battery cell. Bypass with a 4.7µF capacitor to GND.	

Detailed Description

The MAX77658 provides a highly-integrated battery charging and power management solution for low-power applications.

The linear charger can charge various Li+ batteries with a wide range of charge current and charger termination voltage options. Temperature monitoring and JEITA compliance settings add additional functionality and safety to the charger.

Five regulators are integrated within this device (see Table 1). A single-inductor, multiple output (SIMO) buck-boost regulator provides three highly-efficient and independently programmable power rails. Two 150mA low-dropout linear regulators (LDOs) provide ripple rejection for audio and other noise sensitive applications.

An ultra-low power fuel gauge which implements the Maxim ModelGauge m5 EZ algorithm is also packed into MAX77658. The ModelGauge m5 algorithm combines the short-term accuracy and linearity of a coulomb-counter with the long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel gauge accuracy. The additional robustness from the ModelGauge m5 EZ algorithm enables simpler implementation for most applications and batteries by avoiding time-consuming battery characterization.

This device includes other features such as an analog multiplexer that switches several internal voltage and current signals to an external node for monitoring with an external ADC. A bidirectional I^2C serial interface allows for configuring and checking the status of the device. An internal on/off controller provides regulator sequencing and supervisory functionality for the device.

Table 1. Regulator Summary

REGULATOR NAME	REGULATOR TOPOLOGY	MAXIMUM I_{OUT} (mA)	V_{IN} RANGE	MAX77658 V_{OUT} RANGE/ RESOLUTION
SBB0	SIMO	Up to 500*	2.7 to 5.5V	0.5 to 5.5V in 25mV steps
SBB1	SIMO	Up to 500*	2.7 to 5.5V	0.5 to 5.5V in 25mV steps
SBB2	SIMO	Up to 750*	2.7 to 5.5V	0.5 to 5.5V in 25mV steps
LDO0/1	PMOS LDOs	150	1.7 to 5.5V	0.5 to 5V in 25mV steps

**Shared capacity with other SBBx channels. See the SIMO Available Output Current section for more information.*

Part Number Decoding

The MAX77658 has different one-time programmable (OTP) options to support a variety of applications. OTP options set default settings such as output voltage or CHGIN current limit. See Figure 1 for how to identify these. Table 2 list all available OTP options. Refer to the *Maxim Integrated naming convention* for more details.

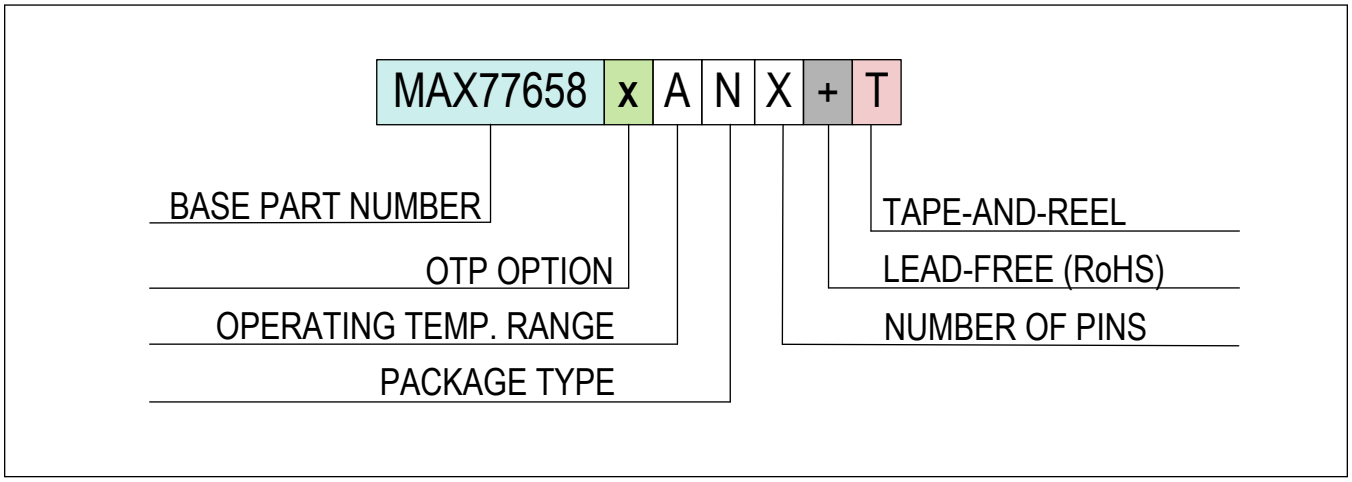


Figure 1. Part Number Decode

Table 2. OTP Options Table

			OTP LETTER AND SETTINGS	
BLOCK	**BIT FIELD NAME**	**SETTING NAME**	**A**	B
Global	SBIA_LPM	Bias Low-Power Mode	NPM	NPM
	DBEN_nEN	nEN Debounce time	500µs	500µs
	nEN_MODE	nEN Mode	Push-Button	Push-Button
	T_MRST	Manual Reset Time	8s	8s
	ALT_GPIO0	GPIO0 Mode	GPIO	GPIO
	ALT_GPIO1	GPIO1 Mode	GPIO	Alt.
	ALT_GPIO2	GPIO2 Mode	GPIO	GPIO
	ADDR	I^2C Address (7-bit)	0x48	0x48
	DIDM	Device ID for Metal Options	0b0	0b0
	CID[4:0]	Chip ID	0x01	0x0B
Watchdog	WDT_LOCK	Watchdog Timer Disable Control	Unlocked	Unlocked
	WDT_EN	Watchdog Timer Enable	Disabled	Disabled
SIMO	SBB_F_SHUTDN	SBB Shutdown from SBB Faults	Disabled	Disabled
	TV_SBB0[7:0]	SBB0 V_{OUT}	3.300V	1.100V
	IP_SBB0[1:0]	SBB0 Inductor Current Peak Limit	1.000A	0.500A
	OP_MODE[1:0] (SBB0)	SBB0 Operating Mode	Automatic	Automatic
	ADE_SBB0	Active-Discharge Resistor Enable	Enabled	Enabled
	EN_SBB0[2:0]	SBB0 Enable Control	FPS Slot 0	Off
	TV_SBB1[7:0]	SBB1 V_{OUT}	1.500V	1.800V
	IP_SBB1[1:0]	SBB1 Inductor Current Peak Limit	1.000A	0.500A
	OP_MODE[1:0] (SBB1)	SBB1 Operating Mode	Automatic	Automatic
	ADE_SBB1	Active-Discharge Resistor Enable	Enabled	Enabled
	EN_SBB1[2:0]	SBB1 Enable Control	FPS Slot 0	On
	TV_SBB2[7:0]	SBB2 V_{OUT}	0.900V	3.300V

Table 2. OTP Options Table (continued)

			OTP LETTER AND SETTINGS	
	IP_SBB2[1:0]	SBB2 Inductor Current Peak Limit	1.0000A	1.000A
	OP_MODE[1:0] (SBB2)	SBB2 Operating Mode	Automatic	Automatic
	ADE_SBB2	Active-Discharge Resistor Enable	Enabled	Enabled
	EN_SBB2[2:0]	SBB2 Enable Control	FPS Slot 0	Off
LDO	TV_OFS_LDO0 and TV_LDO0[6:0]	LDO0 V_{OUT}	1.800V	1.800V
	LDO0_MD	LDO or LSW Mode	LDO	LSW
	ADE_LDO0	Active-Discharge Resistor Enable	Enabled	Enabled
	EN_LDO0[2:0]	LDO0 Enable Control	FPS Slot 0	Off
	TV_OFS_LDO1 and TV_LDO1[6:0]	LDO1 V_{OUT}	1.800V	1.800V
	LDO1_MD	LDO or LSW Mode	LDO	LDO
	ADE_LDO1	Active-Discharge Resistor Enable	Enabled	Enabled
	EN_LDO1[2:0]	LDO1 Enable Control	FPS Slot 0	Off
Charger	CHG_EN	Charger Enable	Disabled	Enabled
	ICHGIN_LIM_DEF	Default Charger Input Current Limit	475mA	475mA

**Future OTP option. Contact Maxim Integrated for availability.*

Support Material

The following support materials are available for this device:

- MAX77658 Programmer's Guide: Basic software implementation advice. *Contact Maxim* for document availability.
- MAX77658 *SIMO Calculator*: Tool to estimate supported maximum current and ripple for specified conditions.
- *ModelGauge m5 EZ User Guide*
  - Documents full fuel gauge register set
  - More details about ModelGauge m5 algorithm
  - Discusses additional applications
- *Model Gauge m5 EZ Software Implementation Guide*
  - Guidelines for software drivers for ModelGauge m5 EZ including example code

Top-Level Interconnect Simplified Diagram

Figure 2 shows the same major blocks as the *Typical Applications Circuit* with an increased emphasis on the routing between each block. This diagram is intended to familiarize the user with the landscape of the device. Many of the details associated with these signals are discussed throughout the data sheet. At this stage of the data sheet, note the addition of the main bias and clock block that are not shown in the *Typical Applications Circuit* section. The main bias and clock block provides voltage, current, and clock references for other blocks as well as many resources for the top-level digital control.

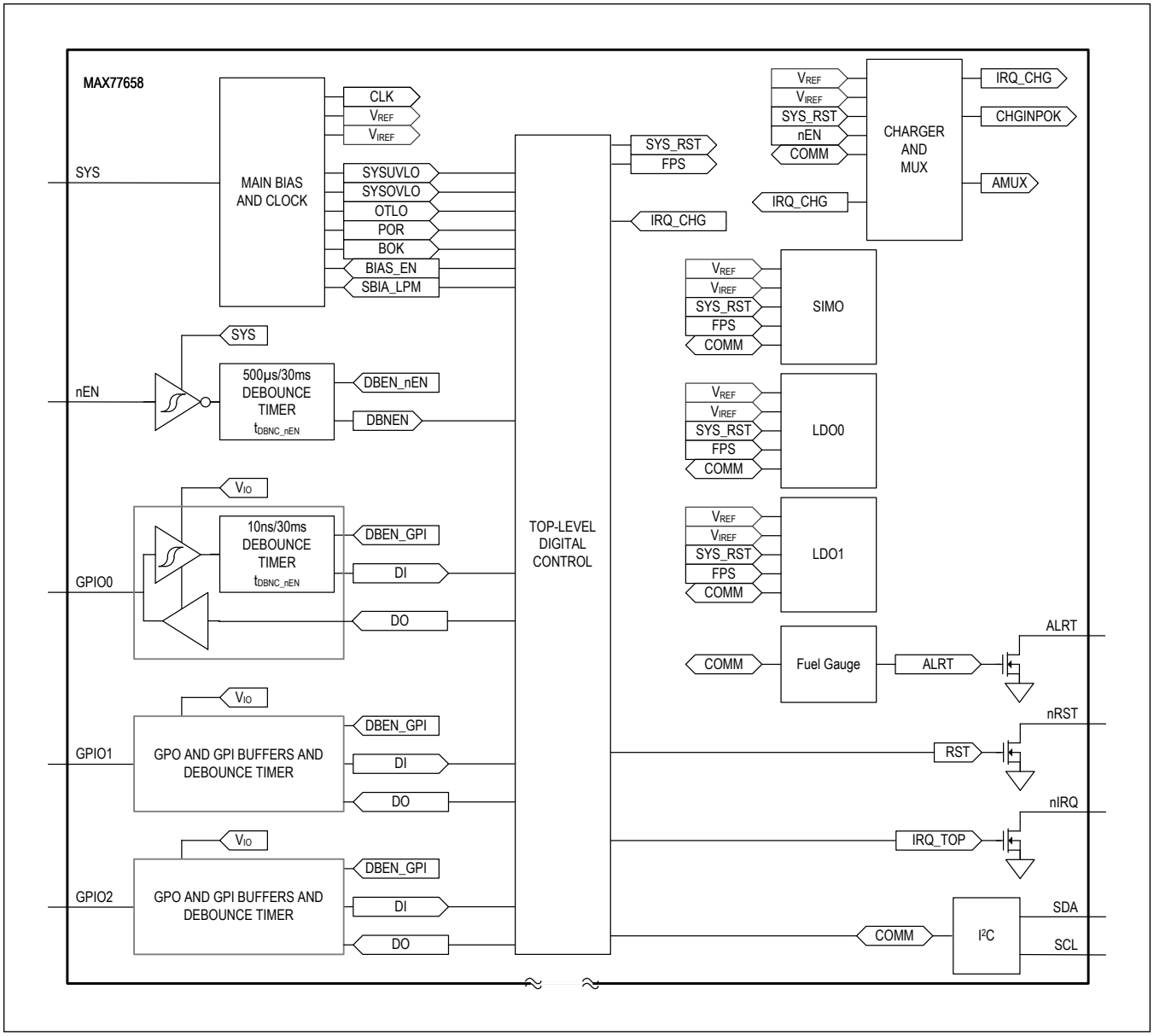


Figure 2. Top-Level Interconnect Simplified Diagram

PRELIMINARY

Detailed Description—Global Resources

The global resources encompass a set of circuits that serve the entire device and ensure safe, consistent, and reliable operation.

Features and Benefits

- Voltage Monitors
  - SYS POR (power-on-reset) comparator generates a reset signal upon power-up.
  - SYS undervoltage ensures repeatable behavior when power is applied to and removed from the device.
  - SYS overvoltage monitor inhibits operation with overvoltage power sources to ensure reliability in faulty environments.
- Thermal Monitors
  - +145°C junction temperature shutdown
- Manual Reset
  - 4s or 8s period
- Wake-up Events
  - Charger insertion (with 120ms debounce)
  - nEN input assertion
- Interrupt Handler
  - Digital interrupt output (nIRQ)
  - All interrupts are maskable
- Push-Button/Slide-Switch/Logic Mode On-key (nEN)
  - Configurable push-button/slide-switch/logic mode functionality
  - 500µs or 30ms debounce timer interfaces directly with mechanical switches
- On/Off Controller
  - Startup/shut-down sequencing
  - Programmable sequencing delay
- GPIO, RST Digital I/Os

Voltage Monitors

The device monitors the system voltage (V_{SYS}) to ensure proper operation using three comparators (POR, UVLO, and OVLO). These comparators include hysteresis to prevent their outputs from toggling between states during noisy system transitions.

SYS POR Comparator

The SYS POR comparator monitors V_{SYS} and generates a power-on reset signal (POR). When V_{SYS} is below V_{POR}, the device is held in reset (SYSRST = 1). When V_{SYS} rises above V_{POR}, internal signals and on-chip memory stabilize and the device is released from reset (SYSRST = 0).

SYS Undervoltage-Lockout Comparator

The SYS undervoltage-lockout (UVLO) comparator monitors V_{SYS} and generates a SYSUVLO signal when the V_{SYS} falls below UVLO threshold. The SYSUVLO signal is provided to the top-level digital controller. See Figure 7 and Table 6 for additional information regarding the UVLO comparator:

- When the device is in the SHUTDOWN state, the UVLO comparator is disabled.
- When transitioning out of the SHUTDOWN state, the UVLO comparator is enabled allowing the device to check for sufficient input voltage. If the device has sufficient input voltage, it can transition to the RESOURCE ON state; if there is insufficient input voltage, the device transitions back to the SHUTDOWN state.

SYS Overvoltage-Lockout Comparator

The device is rated for 5.5V maximum operating voltage (V_{SYS}) with an absolute maximum input voltage of 6.0V. An

overvoltage-lockout monitor increases the robustness of the device by inhibiting operation when the supply voltage is greater than $V_{SYSOVLO}$. See Figure 7 and Table 6 for additional information regarding the OVLO comparator:

- When the device is in the SHUTDOWN state, the OVLO comparator is disabled.

Thermal Monitors

MAX77658 has three global on-chip thermal sensors:

- Junction Temperature Alarm 1 → 80°C
- Junction Temperature Alarm 2 → 100°C
- Junction Temperature Shutdown → 145°C

The Junction Temperature Alarms have maskable rising interrupts as well as status bits (see the *Register Map* section for more information). Unmasking these thermal alarms is recommended for all systems. If the first alarm is triggered, the system software should attempt to lower system power dissipation. If the second alarm is triggered, then attempts to lower the power dissipation were unsuccessful and the system software should turn the device off. Finally, if the junction temperature rises to Junction Temperature Shutdown, then MAX77658 sets the ERCFLAG.TOVLD bit and automatically turns itself off.

After a Junction Temperature Shutdown event, the system can be enabled again. The system software can read the ERCFLAG register during initialization to see ERCFLAG.TOVLD = 1 and log that an extreme thermal event has occurred.

Chip Identification

The MAX77658 offers different one-time-programmable (OTP) options to, for example, set the default output voltages. These options are identified by the chip identification number, which can be read in the CID register.

nEN Enable Input

nEN is an active-low internally debounced digital input that typically comes from the system's on-key. The debounce time is programmable with CNFG_GLBL0.DBEN_nEN[1:0]. The primary purpose of this input is to generate a wake-up signal for the PMIC that turns on the regulators. Maskable rising/falling interrupts are available for nEN (*INT_GLBL0.nEN_R* and *INT_GLBL0.nEN_F*) for alternate functionality.

The nEN input can be configured to work either with a push-button (CNFG_GLBL.nEN_MODE[1:0] = 0b00), a slide-switch (CNFG_GLBL.nEN_MODE[1:0] = 0b01), or Logic Mode (CNFG_GLBL0.nEN_MODE[1:0] = 0b10). See Figure 3 for more information. In both push-button mode and slide-switch mode, the on/off controller looks for a falling edge on the nEN input to initiate a power-up sequence.

nEN Manual Reset

nEN works as a manual reset input when the on/off controller is in the "Resource-On" state. The manual reset function is useful for forcing a power-down in case communication with the processor fails.

When nEN is configured for push-button mode and the input is asserted (nEN = LOW) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to Shutdown mode. When nEN is configured for slide-switch mode and the input is deasserted (nEN = HIGH) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to Shutdown mode.

When nEN is configured as a logic mode, the on/off controller initiates a power-up sequence and goes into Resource ON mode when the input is asserted (nEN = LOW). When the input is deasserted (nEN = HIGH), the on/off controller initiates a power-down sequence and goes into Shutdown mode.

nEN Triple-Functionality: Push-Button vs. Slide-Switch vs. Logic

The nEN digital input can be configured to work with a push-button, a slide-switch, or a logic input. The timing diagram below shows nEN's triple functionality for power-on sequencing and manual reset. The default push-button mode is OTP programmable.

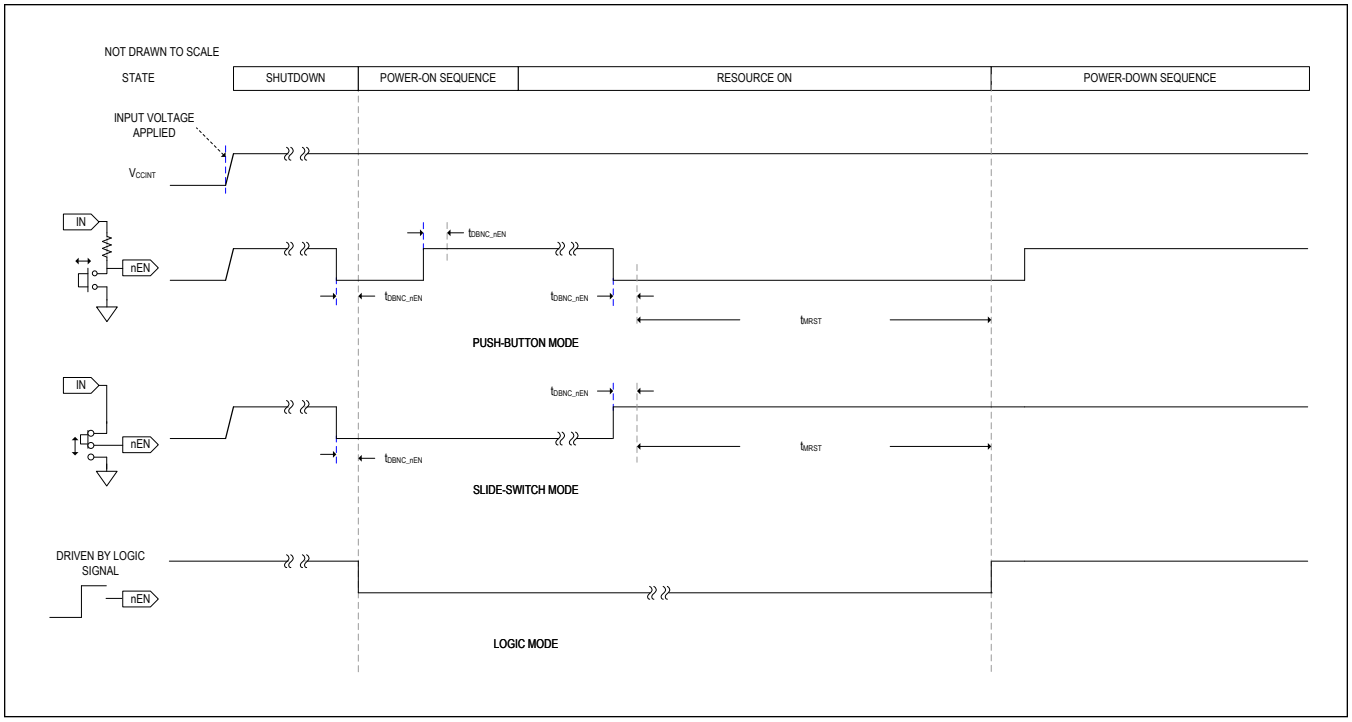


Figure 3. nEN Usage Timing Diagram

nEN Internal Pullup Resistors to V_{CCINT}

The nEN logic thresholds are referenced to V_{CCINT}. There are internal pullup resistors between nEN and V_{CCINT} (R_{nEN_PU}), which can be configured with the CNFG_GLBL.PU_DIS bit. See Figure 4. While CNFG_GLBL.PU_DIS = 0, the pullup value is approximately 200kΩ. While CNFG_GLBL.PU_DIS = 1, the pullup value is 10MΩ.

Applications using a slide-switch on-key or logic mode can reduce quiescent current consumption by changing pullup strength to 10MΩ. Applications using normally-open, momentary, and push-button on-keys (as shown in Figure 4) do not create this leakage path and should use the stronger 200kΩ pullup option.

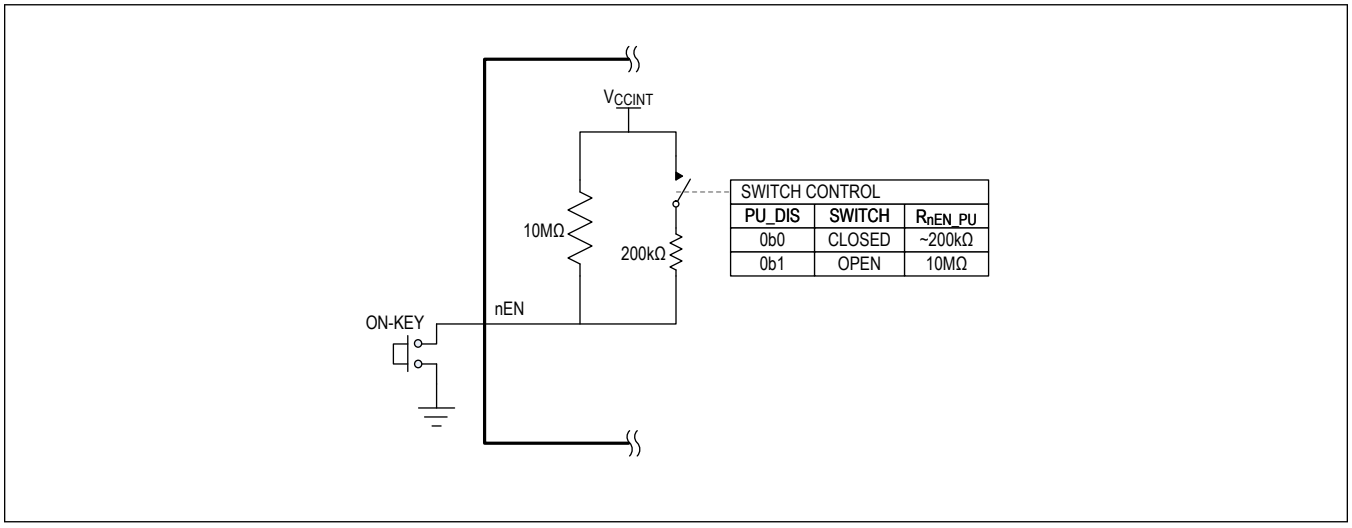


Figure 4. nEN Pullup Resistor Configuration

Debounced Input

The nEN is debounced on both rising and falling edges to reject undesired transitions. The input must be at a stable logic level for the entire debounce period for the output to change its logic state. Figure 5 shows an example timing diagram for the nEN debounce.

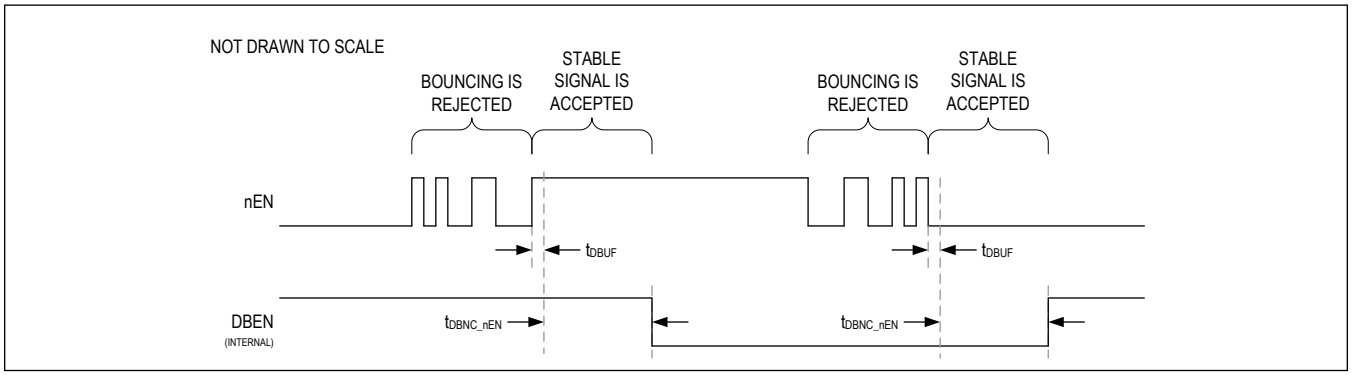


Figure 5. Debounced Input

Interrupts (nIRQ)

nIRQ is an active-low, open-drain output that is typically routed to the host processor's interrupt input to signal an important change in device status. See the *Register Map* section for a comprehensive list of all interrupt bits and status registers.

A pullup resistor to a voltage less than or equal to V_{SYS} is required for this node. nIRQ is the logical *NOR* of all unmasked interrupt bits in the register map.

All interrupts are masked by default. Masked interrupt bits do not cause the nIRQ pin to change. Unmask the interrupt bits to allow nIRQ to assert.

Reset Output (nRST)

nRST is an open-drain, active-low output that is typically used to hold the processor in a reset state when the device is powered down. During a power-up sequence, the nRST deasserts after the last regulator in the power-up chain is enabled (t_{RSTODD}). During a power-down sequence, the nRST output asserts before any regulator is powered down (t_{RSTOAD}). See Figure 11 for nRST timing.

A pullup resistor to a voltage less than or equal to V_{SYS} is required for this node.

General-Purpose Input Output (GPIO)

The MAX77658 provides general-purpose input/output (GPIO) pins increase system flexibility. See Figure 6 for more details.

Clear CNFG_GPIOx.DIR to configure GPIO as a general-purpose output (GPO). The GPO can either be in push-pull mode (CNFG_GPIOx.DRV = 1) or open-drain mode (CNFG_GPIOx.DRV = 0).

- The push-pull output mode is ideal for applications that need fast (~2ns) edges and low power consumption.
- The open-drain mode requires an external pullup resistor (typically 10kΩ–100kΩ). Connect the external pullup resistor to a bias voltage that is less than or equal to V_{IO}.
  - The open-drain mode can be used to communicate to different logic domains. For example, to send a signal from the GPO on a 1.8V logic domain (V_{IO} = 1.8V) to a device on a 1.2V logic domain, connect the external pullup resistor to 1.2V.
  - The open-drain mode can be used to connect several open-drain (or open-collector) devices together on the same bus to create wired logic (wired AND logic is positive-true; wired OR logic is negative-true).
- The general-purpose input (GPI) functions are still available while the pin is configured as a GPO. In other words, the CNFG_GPIOx.DI (input status) bit still functions and does not collide with the state of the CNFG_GPIOx.DIR bit.

Set CNFG_GPIOx.DIR to have the GPIO function as a GPI. The GPI features a 30ms debounce timer (t_{DBNC_GPI}) that can be enabled or disabled with DBEN_GPI.

- Enable the debounce timer (CNFG_GPIOx.DBEN_GPI = 1) if the GPI is connected to a device that can bounce or chatter, like a mechanical switch.
- If the GPI is connected to a circuit with clean logic transitions and no risk of bounce, disable the debounce timer (CNFG_GPIOx.DBEN_GPI = 0) to eliminate logic delays. With no debounce timer, the GPI input logic propagates to nIRQ in 10ns.

A dedicated internal oscillator is used to create the 30ms (t_{DBNC_GPI}) debounce timer. To obtain low V_{IO} supply current, ensure the GPIO voltage is either logic high or logic low. If the GPIO pin is unconnected (either as a GPI or an open-drain GPO) and V_{IO} is powered, the GPIO voltage trends towards the logic level gray area ($0.3 \times V_{IO} < V_{GPIO} < 0.7 \times V_{IO}$). If V_{GPIO} is in the gray area, V_{IO} current can be more than 10µA.

The GPI features edge detectors that feed into the the top-level interrupt system of the chip. This allows software to use interrupts to service events associated with a GPI change instead of polling for these changes.

- If the application wants nIRQ to go low **only on a GPI rising edge**, then it should **clear** the GPI rising edge interrupt mask bit (INTM_GLBL1.GPI_RM = **0**) and **set** the GPI falling edge interrupt mask bit (INTM_GLBL1.GPI_FM = **1**).
- If the application wants nIRQ to go low **only on a GPI falling edge**, then it should **set** the GPI rising edge interrupt mask bit (INTM_GLBL1.GPI_RM = **1**) and **clear** the GPI falling edge interrupt mask bit (INTM_GLBL1.GPI_FM = **0**).
- If the application wants nIRQ to go low **on both GPI falling and rising edges**, then it should **clear** the GPI rising edge interrupt mask bit (INTM_GLBL1.GPI_RM = **0**) and **clear** the GPI falling edge interrupt mask bit (INTM_GLBL1.GPI_FM = **0**).

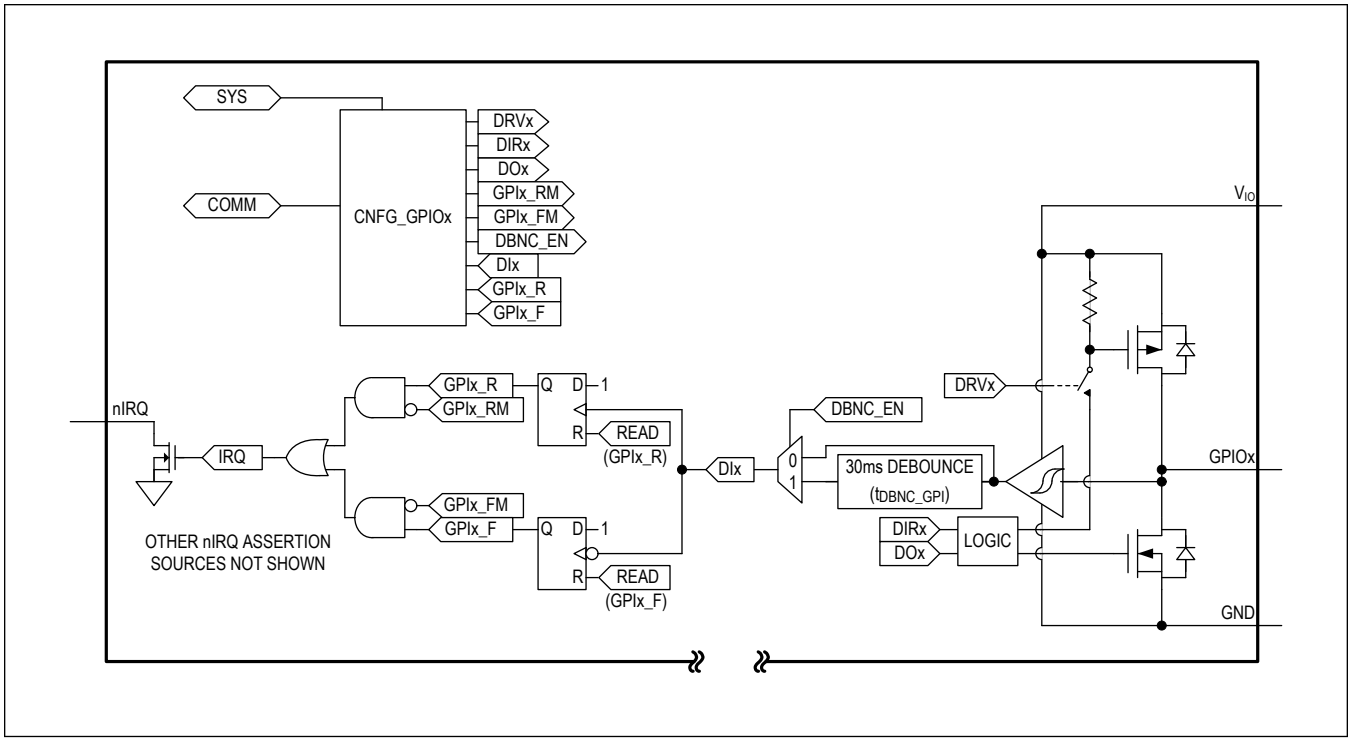


Figure 6. GPIOx Block Diagram

Alternate Mode

Each GPIO in the MAX77658 can be configured to have a different function. Whether a particular GPIO is in GPIO mode or alternate mode can be checked by reading the CNFG_GPIOx.ALT_GPIOx bit. Table 3 summarizes the alternate functions for each GPIO.

Table 3. GPIO Mode

GPIOx	CNFG_GPIOx REGISTER	
	ALT_GPIOx = 0	ALT_GPIOx = 1
GPIO0	Standard GPIO	Active-high input, Force USB Suspend (FUS). FUS is only active if the FUS_M bit is set to 0.
GPIO1	Standard GPIO	Active-high input, controls the DVS feature for SBB0
GPIO2	Standard GPIO	Active-high input, Enable DISQBAT.

Table 4. CHGIN Suspend State Truth Table

CNFG_CHG_G.USBS	CNFG_CHG_G.FUS_M	GPIO0	CHGIN TO SYS FET
0	0	0	ON
0	0	1	OFF
0	1	X	ON
1	X	X	OFF

Table 5. Enabling/Disabling DISQBAT while GPIO2 is in Alternate Mode

GPIO2	CHARGING PATH FROM SYS TO BATT CHGR
0	ON
1	OFF

On/Off Controller

The on/off controller monitors multiple power-up (wake-up) and power-down (shutdown) conditions to enable or disable resources that are necessary for the system and its processor to move between its operating modes.

Many systems have one power management controller and one processor. These systems rely on the on/off controller to be the master controller. In this case, the on/off controller receives wake-up events and enables some or all of the regulators to power-up a processor. That processor then manages the system. To conceptualize this master operation, see Figure 7 and Table 6. A typical path through the on/off controller is:

1. Apply a battery and start in the Shutdown state.
2. Press the system's on-key (nEN = LOW) and follow transition 3 to the Resource-On state. If any resources are on the FPS, transitions 5A and 5B are followed.
3. The device performs its desired functions in the Resource-On state. when it is ready to turn off, a manual reset first drives the transition through transitions 6A and 6B to power down the device. Afterwards, the device automatically follows transition 4 to the Shutdown state.

Some systems have several power management blocks, a main processor, and sub-processors. These systems can use this device as a sub-power management block for a peripheral portion of circuitry as long as there is an I^2C port available from a higher level processor. To conceptualize this operation, see Figure 7 and Table 6. A typical path through the on/off controller used in this way is:

1. Apply a battery to the system and start in the shutdown state.
2. The higher level processor can now control this device's resources with I^2C commands, e.g., turn on/off regulators.
3. When the higher level processor is ready to turn this device off, it turns off everything through I^2C to transition along path 4 to the SHUTDOWN state.

Note that in this style of operation, the CNFG_GLBL_SFT_CTRL[1:0] bits should not be used to turn the device off. The CNFG_GLBL_SFT_CTRL[1:0] bits establish directives to the on/off controller itself that does not make sense in this sub-power management block operation. If the processor uses I^2C commands to enable the device's resources, the processor should also use I^2C commands to disable them.

Top Level On/Off Controller

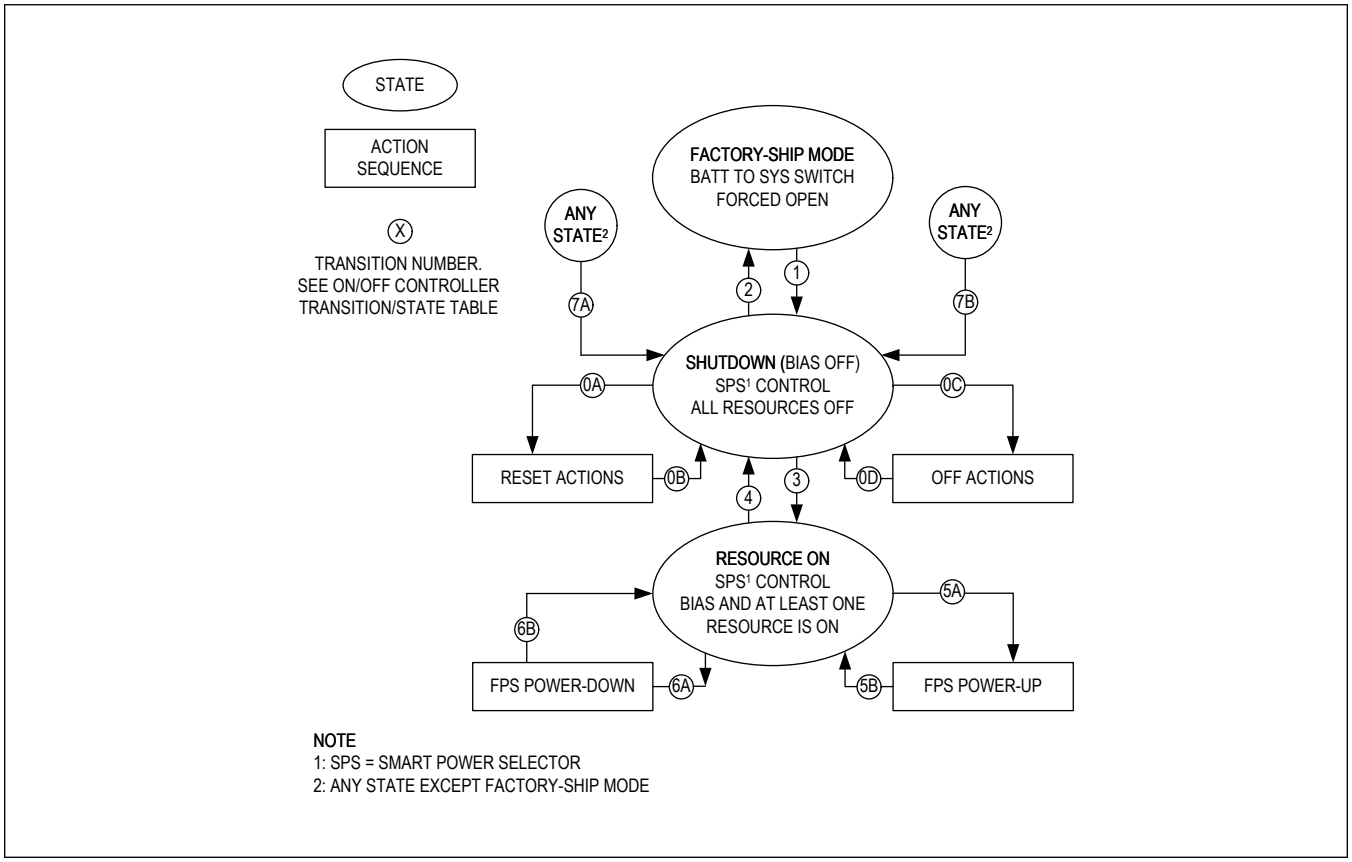


Figure 7. Top Level On/Off Controller State Diagram

On/Off Controller Transition Table

Table 6. On/Off Controller Transition/State

TRANSITION	CONDITION (TRANSITION HAPPENS WHEN...)
0A	Software cold reset (CNFG_GLBL.SFT_CTRL[1:0] = 0b01) **OR** Watchdog timer expired and caused reset (ERCFLAG.WDT_RST = 1, CNFG_WDT.WDT_MODE = 1)
0B	Reset actions completed
0C	Software power-off (CNFG_GLBL.SFT_CTRL[1:0] = 0b10) **OR** Watchdog expired and caused power-off (ERCFLAG.WDT_OFF = 1, CNFG_WDT.WDT_MODE = 0) **OR** Chip over-temperature lockout ($T_J > T_{OTLO}$) **OR** SYS undervoltage lockout ($V_{SYS} < V_{SYSUVLO} + V_{SYSUVLO\_HYS}$) **OR** SYS overvoltage lockout ($V_{SYS} > V_{SYSOVLO}$) **OR** Manual reset occurred (ERCFLAG.MRST = 1)
0D	Off actions completed
1	CHGIN inserted and 120ms debounce valid (STAT_CHG_B.CHGIN_DTLS[1:0] = 0b11) **OR** nEN asserted and debounced (t_{FSM-DB}) **OR** Power to the IC is removed (V_{BATT} < approx. 1.6V) and then reapplied ($V_{BATT} > V_{POR}$)
2	Factory-ship mode requested (CNFG_GLBL.SFT_CTRL[1:0] = 0b11) **AND** nEN not asserted

Table 6. On/Off Controller Transition/State (continued)

TRANSITION	CONDITION (TRANSITION HAPPENS WHEN...)
3	AMUX is being used (CNFG_CHG_I.MUX_SEL[3:0] ≠ 0b0000) OR CHGIN inserted and debounced (STAT_CHG_B.CHGIN_DTLS[1:0] = 0b11) OR Any resources force enabled OR Internal wake-up flags are set (see the *Internal Wake-Up Flags* section)
4	NOT (Transition 3) Factory-ship mode requested (CNFG_GLBL.SFT_CTRL[1:0] = 0b11) OR Software cold reset (CNFG_GLBL.SFT_CTRL[1:0] = 0b01) OR Software power-off (CNFG_GLBL.SFT_CTRL[1:0] = 0b10) OR Watchdog timer expired OR Manual reset occurred (ERCFLAG.MRT = 1)
5A	FPS power-up sequence has not happened yet **AND** Resources are not forced off **AND** Internal wake-up flags are set (see the *Internal Wake-Up Flags* section)
5B	FPS power-up sequence done
6A	FPS power-up sequence completed **AND** All resources are force disabled **OR** Factory-ship mode requested (CNFG_GLBL.SFT_CTRL[1:0] = 0b11) **OR** Software cold reset (CNFG_GLBL.SFT_CTRL[1:0] = 0b01) **OR** Software power-off (CNFG_GLBL.SFT_CTRL[1:0] = 0b10) **OR** Watchdog timer expired **OR** Manual reset occurred (ERCFLAG.MRT = 1)
6B	FPS power-down sequence finished
7A	Chip over-temperature lockout ($T_J > T_{OTLO}$) **OR** SYS undervoltage lockout ($V_{SYS} < V_{SYSUVLO}$) **OR** SYS overvoltage lockout ($V_{SYS} > V_{SYSOVLO}$)
7B	System voltage is below POR threshold ($V_{SYS} < V_{POR}$)

Internal Wake-Up Flags

After transitioning to the shutdown state because of a reset, to allow the device to power-up again, internal wake-up flags are set to remember the wake-up request. In Figure 7 and Table 6, these internal wake-up flags trigger transitions 3 and 5A. The internal wake-up flags are set when any of the following happen:

- nEN is debounced (see the *nEN Enable Input* section)
  - For example, after a push-button is pressed or a slide-switch switched to HIGH.
- CHGIN is debounced and valid (STAT_CHG_B.CHGIN_DTLS[1:0] = 0b11)
- Software cold reset command sent (CNFG_GLBL.SFT_CTRL[1:0] = 0b01)
- Watchdog timer expired and caused reset (ERCFLAG.WDT_RST = 1, CNFG_WDT.WDT_MODE = 1)

Reset and Off Sequences

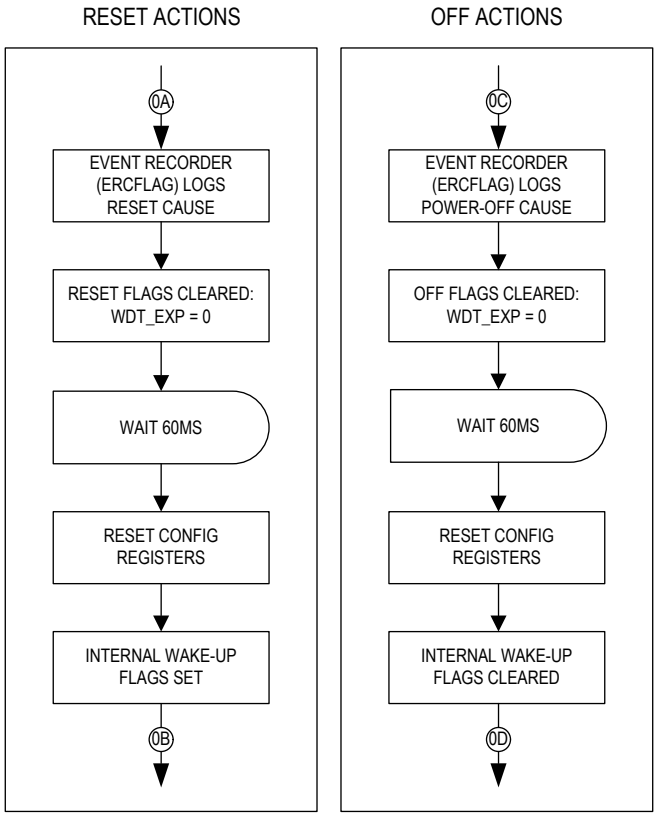


Figure 8. On/Off Controller Reset and Off-Action Sequences

Power-Up/Down Sequence

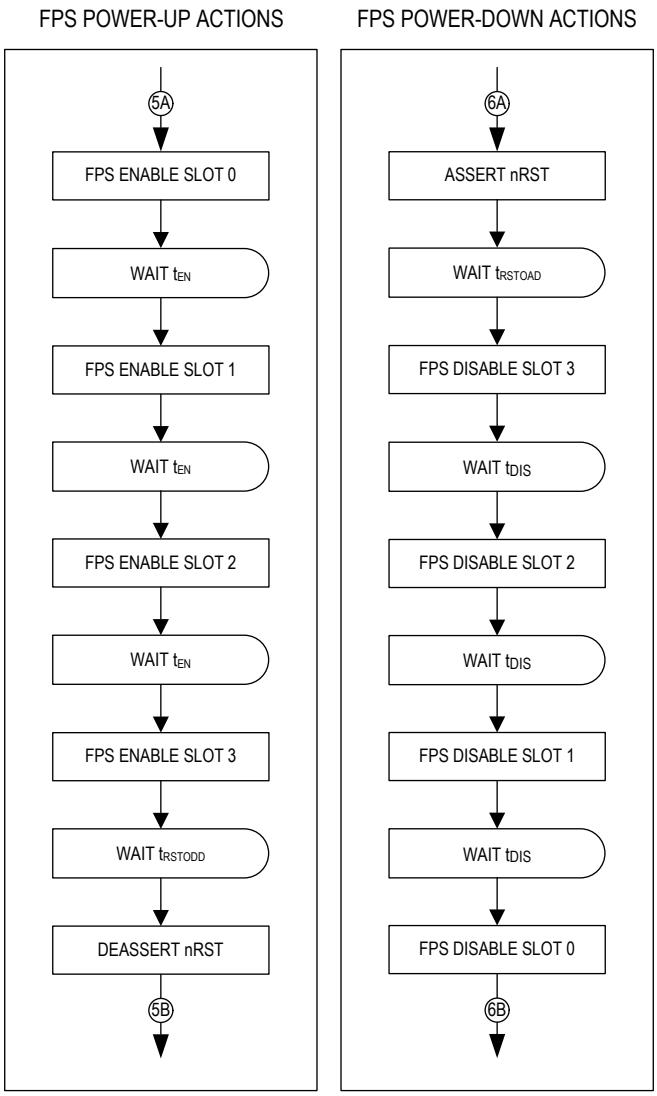


Figure 9. Power-Up/Down Sequence

Flexible Power Sequencer (FPS)

The FPS allows resources to power up under hardware or software control. Additionally, each resource can power up independently or among a group of other regulators with adjustable power-up/down delays (sequencing). Figure 10 shows four resources powering up under the control of the flexible power sequencer.

The flexible sequencing structure consists of one master sequencing timer and four slave resources (SBB0, SBB1, SBB2, LDO0). When the FPS is enabled, a master timer generates four sequencing events for device power-up/down.

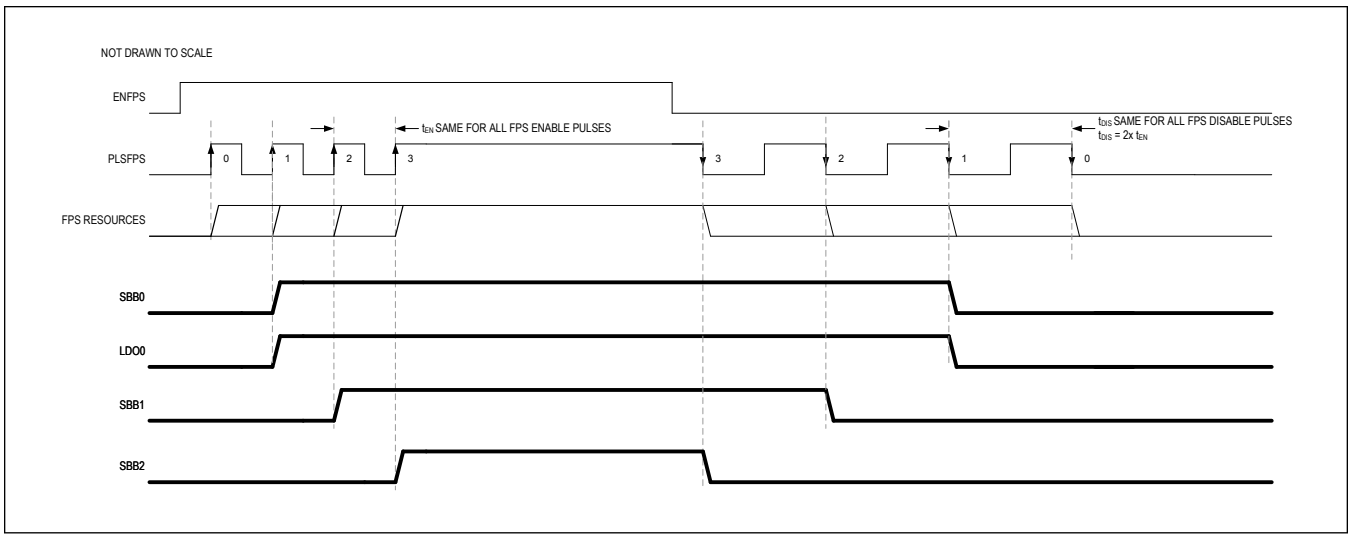


Figure 10. Flexible Power Sequencer Basic Timing Diagram

Startup Timing Diagram Due to nEN

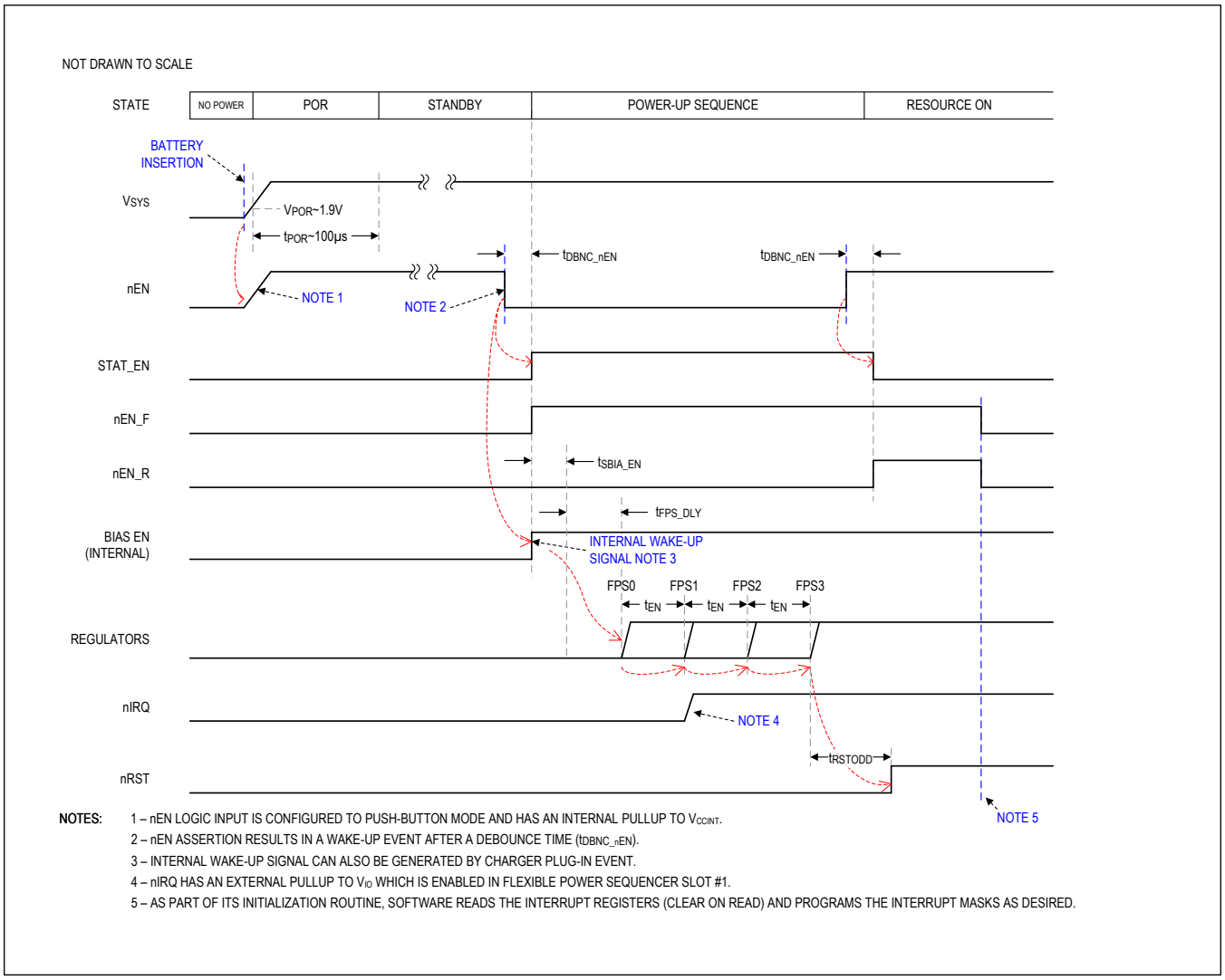


Figure 11. Startup Timing Diagram Due to nEN

Startup Timing Diagram Due to Charge Source Insertion

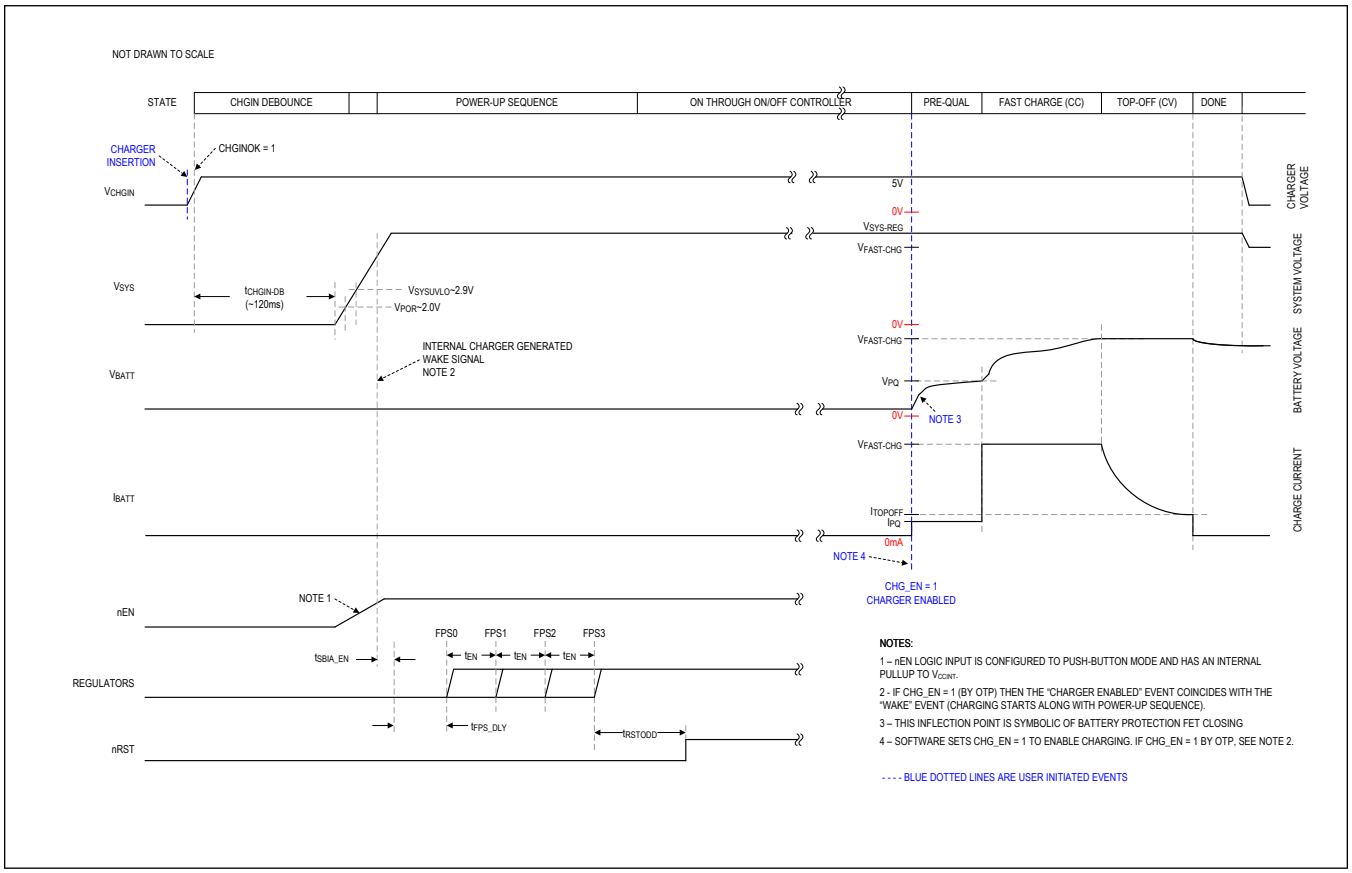


Figure 12. Startup Timing Diagram Due to Charge Source Insertion

Force Enabled/Disabled Channels

Force enable SIMO and LDO output channels by setting CNFG_SBBx_B.EN_SBBx[2:0] (SIMO) or CNFG_LDOx_B.EN_LDOx[2:0] (LDO) = 0x6 or 0x7. Depending on the OTP, output channels may already be force enabled by default. Output channels configured this way are independent of the flexible power sequence and start up as soon as SYS > UVLO rising. The main bias also automatically turns on.

Likewise, output channels can be force disabled by setting EN_SBBx[2:0] or EN_LDOx[2:0] = 0x4 or 0x5.

Factory-Ship Mode (Charger)

Factory-ship mode of the charger internally disconnects the battery (BATT CHGR) from the system (SYS). The battery does not power SYS in this mode. Use this mode to preserve battery life if external circuits on SYS cause the battery to leak.

Write CNFG_GLBL.SFT_CTRL[1:0] = 0b11 using I²C to enter factory-ship mode. The IC responds in two different ways depending on the state of the charger input (CHGIN):

- If CHGIN is valid (STAT_CHG_B.CHGIN_DTLS[1:0] = 0b11) while CNFG_GLBL.SFT_CTRL[1:0] = 0b11, SYS is still powered from CHGIN (regulating to $V_{SYS-REG}$). The factory-ship mode command does not interrupt the charging process if the charger is enabled. Once CHGIN is disconnected, the IC enters factory-ship mode and SYS decays to 0V
- If CHGIN is invalid (STAT_CHG_B.CHG_DTLS[1:0] ≠ 0b11) while CNFG_GLBL.SFT_CTRL[1:0] = 0b11, then the IC enters factory-ship mode and SYS is discharged with the pulldown resistor R_{AD_SYS} to 0V.

Factory-ship mode causes many configuration registers to reset (SYSRST). See the *Register Map* section for details. I²C reads and writes cannot happen in factory-ship mode.

Factory-ship mode exits only after SYS decays below approximately 1.8V. Once this condition is met, there are two ways to exit factory-ship mode:

- Apply a valid DC source at CHGIN for $t_{CHGIN-DB}$ (120ms typical). Factory-ship mode is unlatched (exited) when the charger input becomes valid from a previously invalid state (STAT_CHG_B.CHGIN_DTLS[1:0] = 0b00 → 0b11).
- Assert nEN for $t_{FSM-EXDB}$ (250ms typical) + t_{DBNC_nEN}.

Furthermore, this state is unlatched if power is removed from the IC (BATT voltage falls below approximately 1.6V). In all exit cases, the smart power selector controls the interaction between BATT and SYS until factory-ship mode is entered again (see the *Smart Power Selector* section).

Debounced Inputs (nEN, GPI, CHGIN)

nEN, CHGIN, and GPIO (when operating as an input and CNFG_GPIOx.DBEN_GPI = 1), are debounced on both rising and falling edges to reject undesired transitions. The input must be at a stable logic level for the entire debounce period for the output to change its logic state. Figure 13 shows an example timing diagram for the nEN debounce.

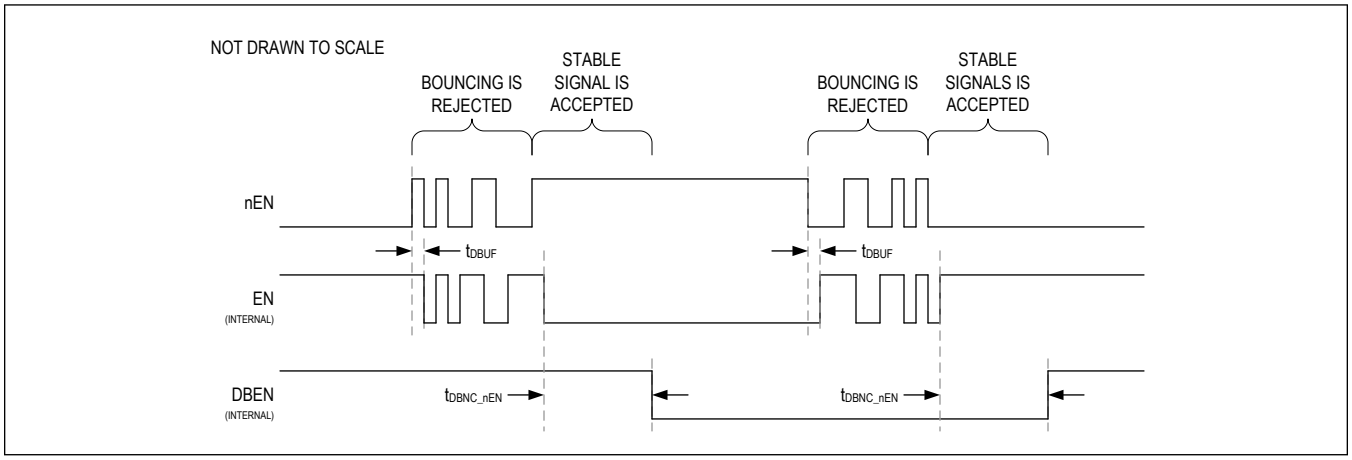


Figure 13. Debounced Inputs (nEN)

PRELIMINARY

Watchdog Timer (WDT)

The IC features a watchdog timer function for operational safety. If this timer expires without being cleared, the on/off controller causes the IC to enter the shutdown state and resets configuration registers. See the *On/Off Controller* and *On/Off Controller Transition Table* sections (transitions 0A and 0C) for more details.

Write CNFG_WDT.WDT_EN = 1 through I²C to enable the timer. The watchdog timer period (t_{WD}) is configurable from 16 to 128 seconds in 4 steps with CNFG_WDT.WDT_PER[1:0]. The default timer period is 128 seconds. While the watchdog timer is enabled, the CNFG_WDT.WDT_CLR bit must be set through I²C periodically (within t_{WD}) to reset the timer and prevent shutdown. See the *Register Map* and Figure 14 for additional details.

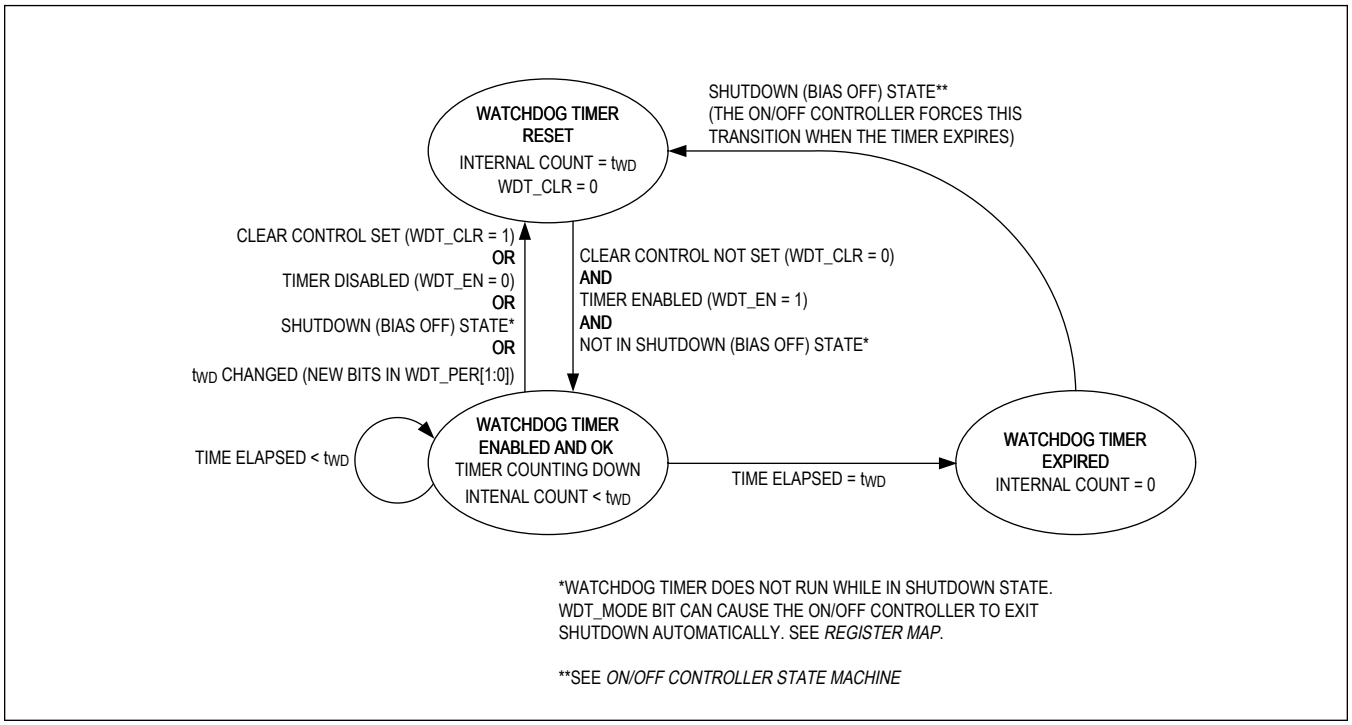


Figure 14. Watchdog Timer State Machine

The timer can be factory-programmed to be enabled by default, disabled by default, or locked from accidental disable. The CNFG_WDT.WDT_LOCK bit is read-only and must be configured at the factory. See Table 7 for a full description.

Table 7. Watchdog Timer Factory-Programmed Safety Options

WDT_LOCK	WDT_EN	FUNCTION
0	0	Watchdog timer is disabled by default. Timer can be enabled or disabled by I²C writes.
0	1	Watchdog timer is enabled by default. Timer can be enabled or disabled by I²C writes.
1	0	Watchdog timer is disabled by default. Timer can be enabled by an I²C write, but only a SYSRST can reset the CNFG_WDT.WDT_EN value back to 0. Timer can not be disabled by direct I²C writes to CNFG_WDT.WDT_EN (write from 1 → 0 is ignored, write from 0 → 1 is accepted).
1	1	Watchdog timer is enabled by default. Nothing can disable the timer.

Detailed Description—Smart Power Selector Charger

Overview

The linear Li+ charger implements power path with Maxim's Smart Power Selector. This allows separate input current limit and battery charge current settings. Batteries are charged faster under the supervision of the Smart Power Selector because charge current is independently regulated and not shared with variable system loads. See the *Smart Power Selector* section for more information.

The programmable constant-current charge rate (7.5mA to 300mA) supports a wide range of battery capacities. The programmable input current limit (95mA to 475mA) supports a range of charge sources, including USB. The charger's programmable battery regulation voltage range (3.6V to 4.6V) supports a wide variety of cell chemistry. The charger accurately terminates charging by detecting battery currents as low as 0.375mA.

Additionally, the robust charger input withstands overvoltage up to 28V. To enhance charger safety, properly configured fuel gauge registers and an externally connected NTC thermistor provide temperature monitoring in accordance with the JEITA recommendations. See the *Temperature Measurement* section for more information.

Charger Symbol Reference Guide

Table 8 lists the names and functions of charger-specific signals and if they can be programmed through I^2C serial communication. See the *Electrical Characteristics* and *Register Map* for more information.

Table 8. Charger Quick Symbol Reference Guide

SYMBOL	NAME	I^2C PROGRAMMABLE?
V_{CHGIN_OVP}	CHGIN overvoltage threshold	No
V_{CHGIN_UVLO}	CHGIN undervoltage-lockout threshold	No
$V_{CHGIN-MIN}$	Minimum CHGIN voltage regulation setpoint	Yes, through CNFG_CHG_B.VCHGIN_MIN[2:0]
$I_{CHGIN-LIM}$	CHGIN input current limit	Yes, through CNFG_CHG_B.ICHGIN_LIM[2:0]
$V_{SYS-REG}$	SYS voltage regulation target	Yes, through CNFG_CHG_D.VSYS_REG[4:0]
$V_{SYS-MIN}$	Minimum SYS voltage regulation setpoint	No, tracks $V_{SYS-REG}$
$V_{FAST-CHG}$	Fast-charge constant-voltage level	Yes, through CNFG_CHG_G.CHG_CV[5:0]
$I_{FAST-CHG}$	Fast-charge constant-current level	Yes, through CNFG_CHG_G_E.CHG_CC[5:0]
I_{PQ}	Prequalification current level	Yes, through CNFG_CHG_B.I_PQ
V_{PQ}	Prequalification voltage threshold	Yes, through CNFG_CHG_C.CHG_PQ[2:0]
I_{TERM}	Termination current level	Yes, through CNFG_CHG_C.I_TERM[1:0]
T_{J-REG}	Die temperature regulation setpoint	Yes, through CNFG_CHG_D.TJ_REG[2:0]
t_{PQ}	Prequalification safety timer	No
t_{FC}	Fast-charge safety timer	Yes, through CNFG_CHG_E.T_FAST_CHG[1:0]
t_{TO}	Top-off timer	Yes, through CNFG_CHG_C.T_TOPOFF[2:0]

Figure 15 indicates the high-level functions of each control circuit within the linear charger.

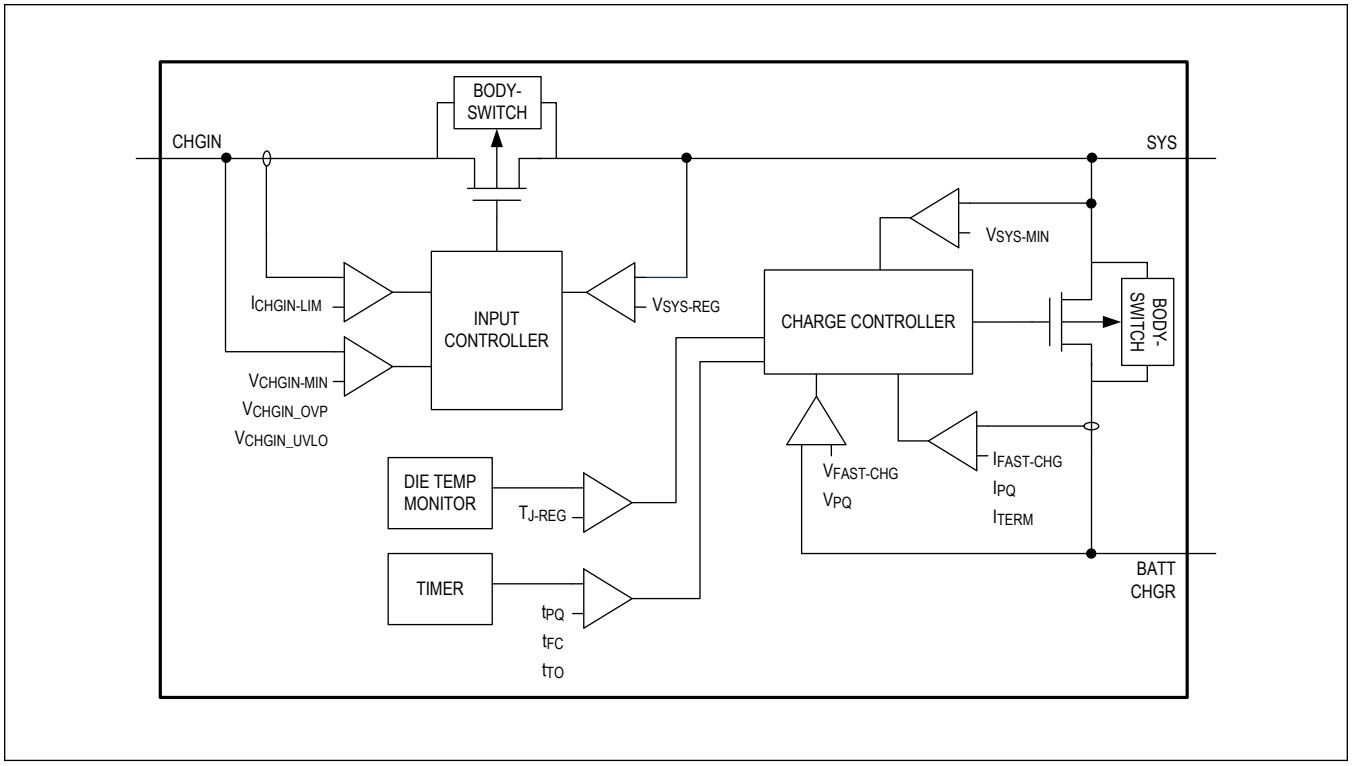


Figure 15. Charger Simplified Control Loops

Smart Power Selector

The Smart Power Selector seamlessly distributes power from the input (CHGIN) to the battery (BATT) and the system (SYS). The Smart Power Selector basic functions are:

- When the system load current is less than the input current limit, the battery is charged with residual power from the input.
- When a valid input source is connected to CHGIN, the system regulates to $V_{SYS-REG}$ to power system loads regardless of the battery's voltage (instant on).
- When the system load current exceeds the input current limit, the battery provides additional current to the system (supplement mode).
- When the battery is finished charging and an input source is present to power the system, the battery remains disconnected from the system.
- When the battery is connected and there is no input power from CHGIN, the system is powered from the battery.

CHGIN Voltage Monitoring

CHGIN is capable of withstanding a maximum of 28V with respect to ground. CHGIN suspends power delivery to the system and battery when V_{CHGIN} exceeds V_{CHGIN_OVP} (7.5V, typ). The input circuit also suspends when V_{CHGIN} falls below V_{CHGIN_UVLO} minus CHGIN UVLO hysteresis (3.5V, typ). While in OVP or UVLO, the charger remains off and the battery provides power to the system.

Power transfer to SYS is delayed by a 120ms debounce timer ($t_{CHGIN-DB}$) after a valid DC source is connected to CHGIN. SYS does not begin regulating to $V_{SYS-REG}$ until after the timer expires.

The STAT_CHG_B.CHGIN_DTLS[1:0] bitfield continuously indicates the state of CHGIN's voltage quality. A maskable interrupt (INT_CHG.CHGIN_I) asserts when STAT_CHG_B.CHGIN_DTLS[1:0] changes.

Minimum Input Voltage Regulation

In the event of a poor-quality charge source, the minimum input voltage regulation loop works to reduce input current if V_{CHGIN} falls below $V_{CHGIN-MIN}$ (programmed by CNFG_CHG_B.VCHGIN_MIN[2:0]). This is important because many commonly used charge adapters feature foldback protection mechanisms where the adapter completely shuts off if its output drops too low. The minimum input voltage regulation loop also prevents V_{CHGIN} from dropping below V_{CHGIN_UVLO} if the cable between the charge source and the charger's input is long or highly resistive.

The input voltage regulation loop improves performance with current limited adapters. If the charger's input current limit is programmed above the current limit of the given adapter, the input voltage loop allows the input to regulate at the current limit of the adapter. The input voltage regulation loop also allows the charger to perform well with adapters that have poor transient load response times.

A maskable interrupt (INT_CHG.CHGIN_CTRL_I) signals when the minimum input voltage regulation loop engages. The state of this loop is reflected by STAT_CHG_A.VCHGIN_MIN_STAT.

Input Current Limiter

The input current limiter limits CHGIN current to not exceed $I_{CHGIN-LIM}$ (programmed by CNFG_CHG_B.ICHGIN_LIM[2:0]). A maskable interrupt (INT_CHG.CHGIN_CTRL_I) signals when the input current limit engages. The STAT_CHG_A.ICHGIN_LIM_STAT bit reflects the state of the current limiter loop.

The default value of $I_{CHGIN-LIM}$ is 475mA.

Table 9. Input Current Limit Factory Options

ICHGIN_LIM[2:0]	475mA FACTORY-DEFAULT	95mA FACTORY-DEFAULT
0b000	475mA	95mA
0b001	380mA	190mA
0b010	285mA	285mA
0b011	190mA	380mA
0b100 to 0b111	95mA	475mA

Minimum System Voltage Regulation

The minimum system voltage regulation loop ensures that the system rail remains close to the programmed SYS regulation voltage ($V_{SYS-REG}$) regardless of system loading. The loop engages when the combined battery charge current and system load current causes the CHGIN input to current limit at $I_{CHGIN-LIM}$. When this happens, the minimum system voltage loop reduces charge current in an attempt to keep the input out of current limit, thereby keeping the system voltage above $V_{SYS-MIN}$ ($V_{SYS-REG}$ - 100mV, typ). If this loop reduces battery current to 0 and the system is in need of more current than the input can provide, then the Smart Power Selector overrides the minimum system voltage regulation loop and allows SYS to collapse to BATT for the battery to provide supplement current to the system. The Smart Power Selector automatically reenables the minimum system voltage loop when the supplement event has ended.

A maskable interrupt (INT_CHG.SYS_CTRL_I) asserts to signal a change in STAT_CHG_A.VSYS_MIN_STAT. This status bit asserts when the minimum system voltage regulation loop is active.

Die Temperature Regulation

If the die temperature exceeds T_{J-REG} (programmed by CNFG_CHG_D.TJ_REG[2:0]) the charger attempts to limit the temperature increase by reducing the battery charge current. The STAT_CHG_A.TJ_REG_STAT bit asserts whenever charge current is reduced due to this loop. The charger's current sourcing capability to SYS remains unaffected when STAT_CHG_A.TJ_REG_STAT is high. A maskable interrupt (INT_CHG.TJ_REG_I) asserts to signal a change in STAT_CHG_A.TJ_REG_STAT. Use the INT_CHG.TJ_REG_I interrupt to signal the system processor to reduce loads on SYS to reduce total system temperature.

Charger State Machine

The battery charger follows a strict state-to-state progression to ensure that a battery is charged safely. The status bitfield STAT_CHG_B.CHG_DTLS[3:0] reflects the charger's current operational state. A maskable interrupt (INT_CHG.CHG_I) is available to signal a change in STAT_CHG_B.CHG_DTLS[3:0].

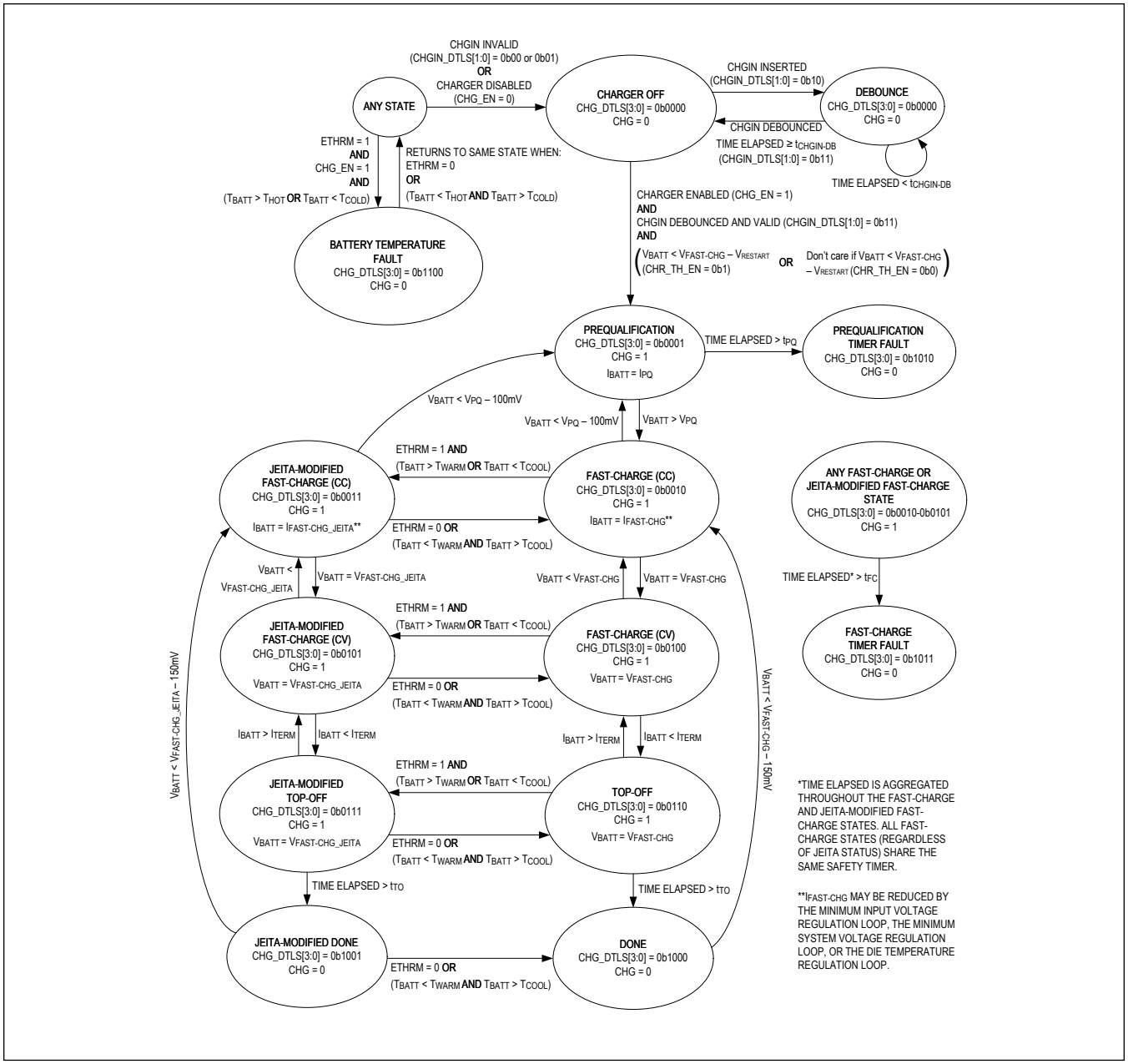


Figure 16. Charger State Machine

Charger-Off State

The charger is off when CHGIN is invalid, the charger is disabled, or the battery is fresh.

CHGIN is invalid when the CHGIN input is invalid (V_{CHGIN} < V_{CHGIN_UVLO} or V_{CHGIN} > V_{CHGIN_OVP}). While CHGIN is invalid, the battery is connected to the system. CHGIN voltage quality can be separately monitored by the STAT_CHG_B.CHGIN_DTLS[1:0] status bitfield. See the *Register Map* section for details.

The charger is disabled when the charger enable bit is 0 (CNFG_CHG_B.CHG_EN = 0). The battery is connected or disconnected to the system depending on the validity of V_{CHGIN} while CNFG_CHG_B.CHG_EN = 0. See the *Smart Power Selector* section.

When the charger restart threshold is enabled (CNFG_CHG_H.CHR_TH_EN = 1, by default), the battery is fresh when the battery is not lower than $V_{FAST-CHG}$ by $V_{RESTART}$ ($V_{BATT} > V_{FAST-CHG} - V_{RESTART}$). The battery is disconnected from the system and not charged while the battery is fresh. The charger state machine exits this state and begins charging when the battery becomes lower than $V_{FAST-CHG} - V_{RESTART}$ ($V_{RESTART}$ = 150mV, typ). This condition is functionally similar to done state. See the *Done State* section.

The charger restart threshold can be disabled with I^2C command by writing CNFG_CHG_H.CHR_TH_EN to 0. When the charger restart threshold is disabled, the battery voltage should be closely monitored by the a micro-controller to avoid unwanted restarted charging event. Note that the charger restart threshold can only be disabled for the transition from Charger-Off State to Prequalification State.

Prequalification State

The prequalification state is intended to assess a low-voltage battery's health by charging at a reduced rate. If the battery voltage is less than the V_{PQ} threshold, the charger is automatically in prequalification. If the cell voltage does not exceed V_{PQ} in 30 minutes (t_{PQ}), the charger faults. The prequalification charge rate is a percentage of $I_{FAST-CHG}$ and is programmable with CNFG_CHG_B.I_PQ. The prequalification voltage threshold (V_{PQ}) is programmable through CNFG_CHG_C.CHG_PQ[2:0].

Fast-Charge States

When the battery voltage is above V_{PQ}, the charger transitions to the fast-charge (CC) state. In this state, the charger delivers a constant current ($I_{FAST-CHG}$) to the cell. The constant current level is programmable from 7.5mA to 300mA by CNFG_CHG_E.CHG_CC[5:0].

When the cell voltage reaches $V_{FAST-CHG}$, the charger state machine transitions to fast-charge (CV). $V_{FAST-CHG}$ is programmable with CNFG_CHG_G.CHG_CV[5:0] from 3.6V to 4.6V. The charger holds the battery's voltage constant at $V_{FAST-CHG}$ while in the fast-charge (CV) state. As the battery approaches full, the current accepted by the battery reduces. When the charger detects that battery charge current has fallen below I_{TERM}, the charger state machine enters the top-off state.

A fast-charge safety timer starts when the state machine enters fast-charge (CC) or JEITA-modified fast-charge (CC) from a non-fast-charge state. The timer continues to run through all fast-charge states regardless of JEITA status. The timer length (t_{FC}) is programmable from 3 hours to 7 hours in 2 hour increments with CNFG_CHG_E.T_FAST_CHG[1:0]. If it is desired to charge without a safety timer, program CNFG_CHG_E.T_FAST_CHG[1:0] with 0b00 to disable the feature. If the timer expires before the fast-charge states are exited, the charger faults. See the *Fast-Charge Timer Fault State* section for more information.

If the charge current falls below 20% of the programmed value during fast-charge (CC), the safety timer pauses. The timer also pauses for the duration of supplement mode and Battery Temperature Fault events. The STAT_CHG_B.TIME_SUS bit indicates the status of the fast-charge safety timer. See the *Register Map* section for more details.

Top-Off State

Top-off state is entered when the battery charge current falls below I_{TERM} during the fast-charge (CV) state. I_{TERM} is a percentage of $I_{FAST-CHG}$ and is programmable through CNFG_CHG_C.I_TERM[1:0]. While in the top-off state, the battery charger continues to hold the battery's voltage at $V_{FAST-CHG}$. A programmable top-off timer starts when the charger state machine enters the top-off state. When the timer expires, the charger enters the done state. The top-off timer value (t_{TO}) is programmable from 0 minutes to 35 minutes with CNFG_CHG_C.T_TOPOFF[2:0]. If it is desired to stop charging as soon as battery current falls below I_{TERM}, program t_{TO} to 0 minutes.

Done State

The charger enters the done state when the top-off timer expires. The battery remains disconnected from the system during done. The charger restarts if the battery voltage falls more than $V_{RESTART}$ (150mV, typ) below the programmed $V_{FAST-CHG}$ value. Status of CNFG_CHG_H.CHR_TH_EN does not affect the threshold to transition from Done state to Fast Charge CC state.

Prequalification Timer Fault State

The prequalification timer fault state is entered when the battery's voltage fails to rise above V_{PQ} in t_{TO} (30 minutes,

typ) from when the prequalification state was first entered. If a battery is too deeply discharged, damaged, or internally shorted, the prequalification timer fault state can occur. During the timer fault state, the charger stops delivering current to the battery and the battery remains disconnected from the system. To exit the prequalification timer fault state, toggle the charger enable (CNFG_CHG_B.CHG_EN) bit or unplug and replug the external voltage source connected to CHGIN.

Fast-Charge Timer Fault State

The charger enters the fast-charge timer fault state if the fast-charge safety timer expires. While in this state, the charger stops delivering current to the battery and the battery remains disconnected from the system. To exit the fast-charge timer fault state, toggle the charger enable bit (CNFG_CHG_B.CHG_EN) or unplug and replug the external voltage source connected to CHGIN.

Battery Temperature Fault State

If the thermistor monitoring circuit of the fuel gauge reports that the battery is either too hot or too cold to charge (as programmed by CNFG_CHG_A.THM_HOT[1:0] and CNFG_CHG_A.THM_COLD[1:0]), the state machine enters the battery temperature fault state. While in this state, the charger stops delivering current to the battery and the battery remains disconnected from the system. This state can only be entered if the thermistor is enabled (Config.ETHRM = 1). Battery temperature fault state has priority over any other fault state, and can be exited when the thermistor is disabled (Config.ETHRM = 0) or when the battery returns to an acceptable temperature. When this fault state is exited, the state machine returns to the last state it was in before battery temperature fault state was entered.

All active charger timers (fast-charge safety timer, prequalification timer, or top-off timer) are paused in this state. When the charger exits this state, the prequalification timer resumes while the fast-charge safety and top-off timers reset.

The STAT_CHG_A.THM_DTLS[2:0] bitfield reports battery temperature status. See the *Adjustable Thermistor Temperature Monitors* and the *Register Map* sections for more information.

JEITA-Modified States

If the thermistor is enabled (Config.ETHRM = 1), then the charger state machine is allowed to enter the JEITA-modified states. These states are entered if the charger's temperature monitors indicate that the battery temperature is either warm (greater than T_{WARM}) or cool (less than T_{COOL}). See the *Adjustable Thermistor Temperature Monitors* section for more information about setting the temperature thresholds.

The charger's current and voltage parameters change from $I_{FAST-CHG}$ and $V_{FAST-CHG}$ to $I_{FAST-CHG\_JEITA}$ and $V_{FAST-CHG\_JEITA}$ while in the JEITA-modified states. The JEITA modified parameters can be independently set to lower voltage and current values so that the battery can charge safely over a wide range of ambient temperatures. If the battery temperature returns to normal, or the thermistor is disabled (Config.ETHRM = 0), the charger exits the JEITA-modified states.

Typical Charge Profile

A typical battery charge profile (and state progression) is illustrated in Figure 17.

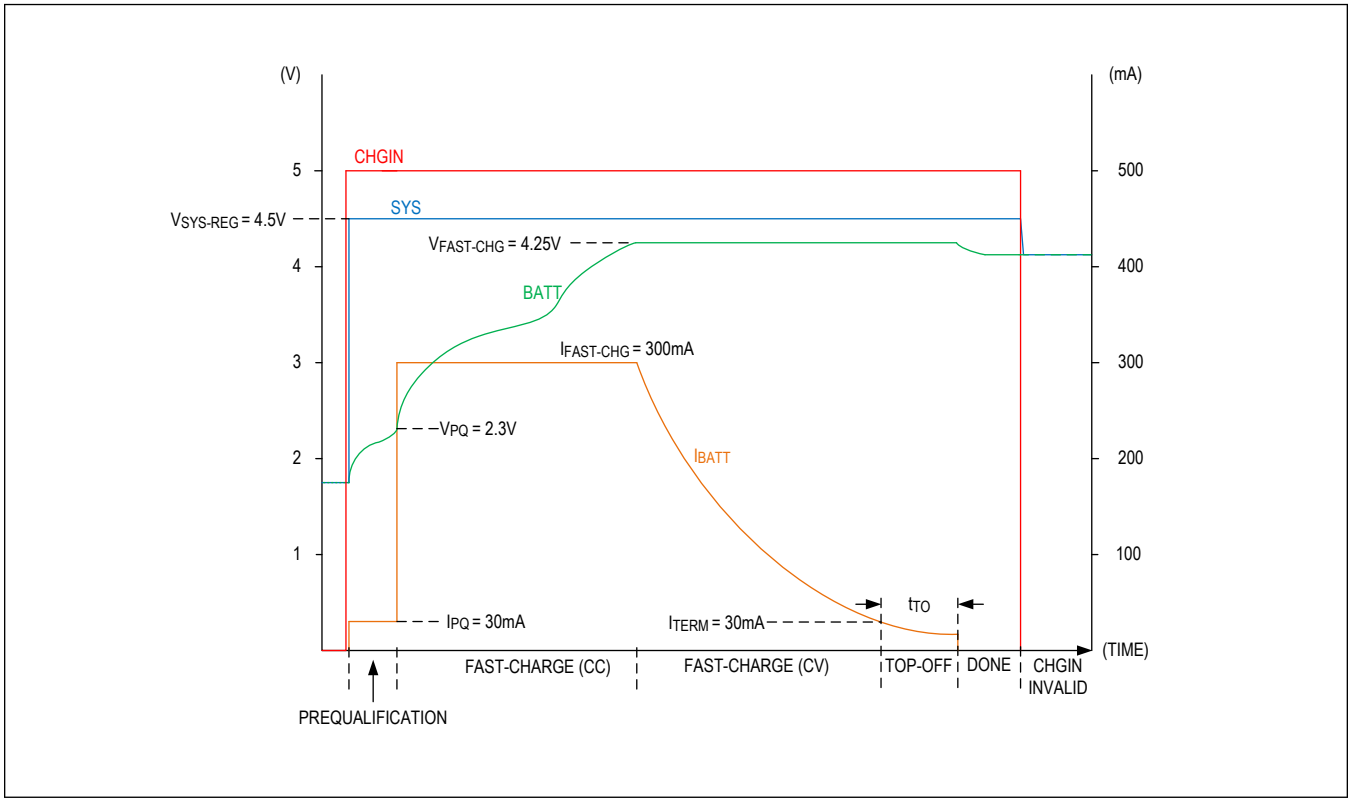


Figure 17. Example Battery Charge Profile

Charger Applications Information

Configuring a Valid System Voltage

The Smart Power Selector begins to regulate SYS to $V_{SYS-REG}$ when CHGIN is connected to a valid source and debounced. To ensure the charger's accuracy specified in the *Electrical Characteristics* table, the system voltage must always be programmed at least 200mV above the charger's constant-voltage level ($V_{FAST-CHG}$). If this condition is not met, then the charger's internal configuration logic forces $V_{FAST-CHG}$ to reduce to satisfy the 200mV requirement by default (CNFG_CHG_H.SYS_BAT_PRT = 1). If this happens, the charger asserts the INT_CHG.SYS_CNFG_I interrupt to alert the user that a configuration error has been made and that the bits in CNFG_CHG_G.CHG_CV[5:0] have changed to reduce $V_{FAST-CHG}$.

The 200mV clamp between $V_{SYS-REG}$ and $V_{FAST-CHG}$ can be disabled by clearing the CNFG_CHG_H.SYS_BAT_PRT bit. If this bit is cleared, the software has to provide the protection to guarantee the overall performance of the charger.

CHGIN/SYS/BATT Capacitor Selection

Bypass CHGIN to GND with a 4.7µF ceramic capacitor to minimize inductive kick caused by long cables between the DC charge source and the product/IC. Larger values increase decoupling for the linear charger, but increase inrush current from the DC charge source when the product/IC is first connected to a source through a cable/plug. If the DC charging source is an upstream USB device, limit the maximum CHGIN input capacitance based on the appropriate USB specification (typically no more than 10µF).

Bypass SYS to GND with a 22µF ceramic capacitor. This capacitor ensures stability of SYS while it is regulated from CHGIN. Larger values of SYS capacitance increase decoupling for all SYS loads. The effective value of the SYS capacitor must be greater than 4µF and no more than 100µF.

Bypass BATT to GND with a 4.7µF ceramic capacitor. This capacitor stabilizes the BATT voltage regulation loop. The effective value of the BATT capacitor must be greater than 1µF.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

Detailed Description—Adjustable Thermistor Temperature Monitors

The optional use of a negative temperature coefficient (NTC) thermistor (thermally coupled to the battery) enables the charger to operate safely over the JEITA temperature range. When the thermistor is enabled (Config.ETHRM = 1), the charger continuously monitors the reading at the Temp register in order to sense the temperature of the battery being charged.

See Figure 18 for a visual example of the following:

- If the battery temperature is higher than T_{COOL} and lower than T_{WARM}, the battery charges normally with the normal values for $V_{FAST-CHG}$ and $I_{FAST-CHG}$. The charger state machine does not enter JEITA-modified states while the battery temperature is normal.
- If the battery temperature is either above T_{WARM} but below T_{HOT}, or, below T_{COOL} but above T_{COLD}, the battery charges with the JEITA-modified voltage and current values. These modified values, $V_{FAST-CHG\_JEITA}$ and $I_{FAST-CHG\_JEITA}$, are programmable through CNFG_CHG_H.CHG_CV_JEITA[5:0] and CNFG_CHG_F.CHG_CC_JEITA[5:0], respectively. These values are independently programmable from the unmodified $V_{FAST-CHG}$ and $I_{FAST-CHG}$ values and can even be programmed to the same values if an automatic response to a warm or cool battery is not desired. The charger state machine enters JEITA-modified states while the battery temperature is outside of normal.
- If the battery temperature is either above T_{HOT} or below T_{COLD}, the charger follows the JEITA recommendation and pauses charging. The charger state machine enters battery temperature fault state while charging is paused due to unacceptably high or low temperatures.

The battery's temperature status is reflected by the STAT_CHG_A.THM_DTLS[2:0] status bitfield. A maskable interrupt (INT_CHG.THM_I) signals a change in status. See the *Register Map* for more information.

To completely disable the charger's automatic response to battery temperature, disable the feature by programming Config.ETHRM = 0.

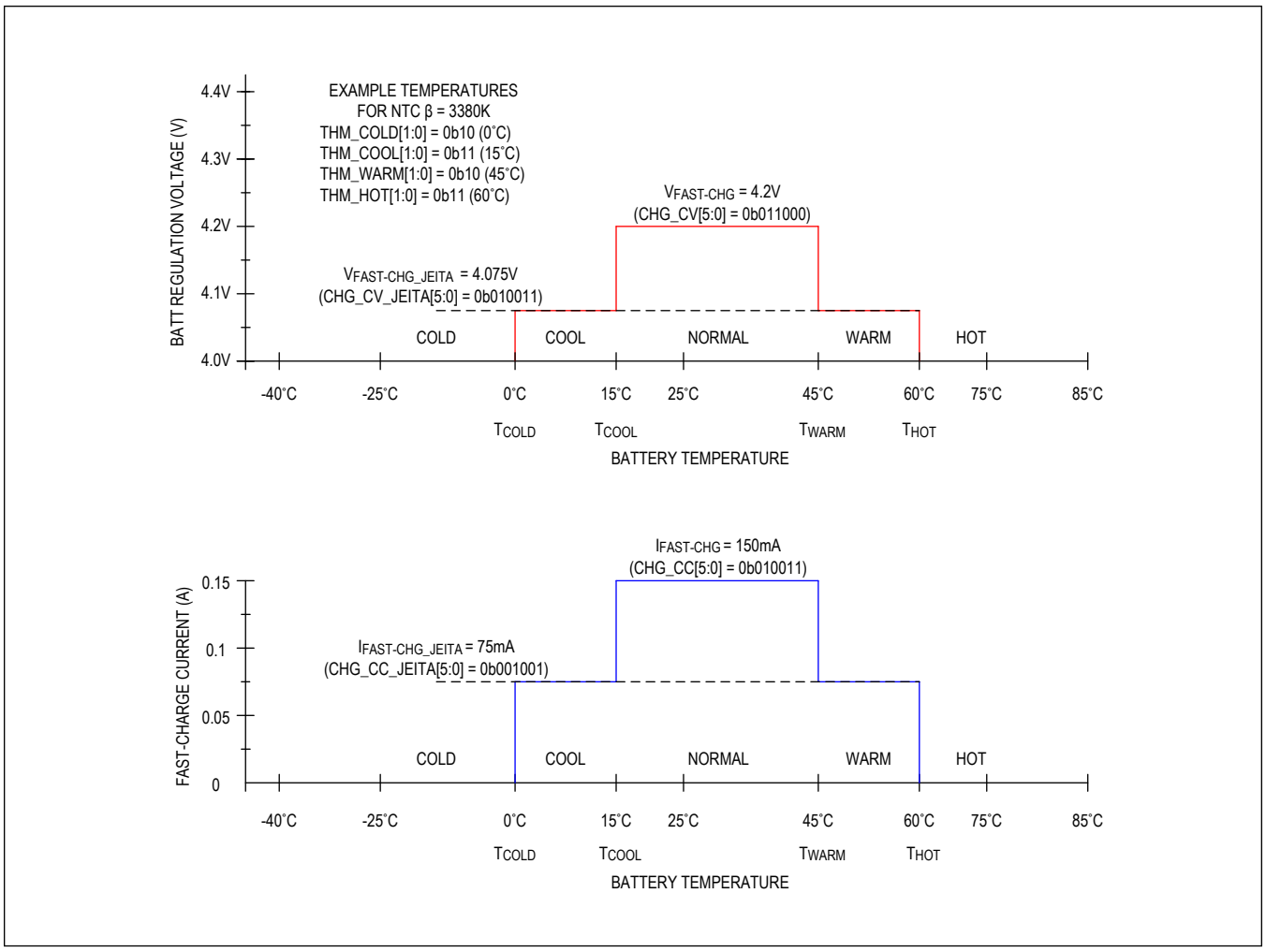


Figure 18. Safe-Charging Profile Example

The JEITA temperature thresholds are independently programmable through CNFG_CHG_A.THM_HOT[1:0], CNFG_CHG_A.THM_WARM[1:0], CNFG_CHG_A.THM_COOL[1:0], and CNFG_CHG_A.THM_COLD[1:0]. Each threshold can be programmed to one of four voltage options spanning 15°C. See the *Register Map* for more information.

Detailed Description—Analog Multiplexer

An external ADC can be used to measure the chip's various signals for general functionality or on-the-fly power monitoring. The CNFG_CHG_I.MUX_SEL[3:0] bitfield controls the internal analog multiplexer responsible for connecting the proper channel to the AMUX pin. Each measurable signal is listed in Table 10 with its appropriate multiplexer channel.

The voltage on the AMUX pin is a buffered output that ranges from 0V to V_{FS} (1.25V, typ). The buffer has 50µA of quiescent current consumption and is only active when a channel is selected (CNFG_CHG_I.MUX_SEL[3:0] ≠ 0b0000). Disable the buffer by programming CNFG_CHG_I.MUX_SEL[3:0] to 0b0000 when not actively converting the voltage on AMUX. The AMUX output is high-impedance while CNFG_CHG_I.MUX_SEL[3:0] is 0b0000.

Table 10 shows how to translate the voltage signal on the AMUX pin to the value of the parameter being measured. See the *Electrical Characteristics* table and the *Register Map* for more details.

Table 10. AMUX Signal Transfer Functions

SIGNAL	MUX_SEL[3:0]	TRANSFER FUNCTION	FULL-SCALE SIGNAL MEANING (V_{AMUX} = 1.25V)	ZERO-SCALE SIGNAL MEANING (V_{AMUX} = 0V)
CHGIN Pin Voltage	0b0001	$V_{CHGIN} = V_{AMUX} / G_{VCHGIN}$	7.5V	0V
CHGIN Pin Current	0b0010	$I_{CHGIN} = V_{AMUX} / G_{ICHGIN}$	0.475A	0A
BATT Pin Voltage	0b0011	$V_{BATT} = V_{AMUX} / G_{VBATT}$	4.6V	0V
BATT Pin Charging Current	0b0100	$I_{BATT(CHG)} = \frac{V_{AMUX}}{V_{FS}} \times I_{FAST-CHG}$	100% of $I_{FAST-CHG}$ (CHG_CC[5:0])	0% of $I_{FAST-CHG}$
BATT Pin Discharge Current	0b0101	$I_{BATT(DISCHG)} = \frac{(V_{AMUX} - V_{NULL})}{(V_{FS} - V_{NULL})} \times I_{DISCHG-SCALE}$	100% of $I_{DISCHG-SCALE}$ (IMON_DISCHG_SCALE[3:0])	0% of $I_{DISCHG-SCALE}$
BATT Pin Discharge Current NULL	0b0110	$V_{NULL} = V_{AMUX}$	1.25V	0V
AGND Pin Voltage*	0b1001	$V_{AGND} = V_{AMUX}$	1.25V	0V
SYS Pin Voltage	0b1010	$V_{SYS} = V_{AMUX} / G_{VSYS}$	4.8V	0V

**AGND pin voltage is accessed through a 100Ω (typ) pulldown resistor.*

Measuring Battery Current

Sampling current in the BATT pin is possible at any time or in any mode with an external ADC. For improved accuracy, the analog circuitry used for monitoring battery discharge current is different from the circuitry monitoring battery charge current. Table 11 outlines how to determine the direction of battery current.

Table 11. Battery Current Direction Decode

MEASUREMENT	CHARGING OR DISCHARGING INDICATORS		
	STAT_CHG_B.CHG	STAT_CHG_B.CHG_DTLS[3:0]	STAT_CHG_B.CHGIN_DTLS[1:0]
Discharging Battery Current (Positive Battery Terminal Sourcing Current)	*Don't care*	*Don't care*	0b00 0b01 0b10
Charging Battery Current (Positive Battery Terminal Sinking Current)	1	0b0001 to 0b0111	0b11

Method for Measuring Discharge Current

1. Program the multiplexer to switch to the discharge NULL measurement by changing CNFG_CHG_I.MUX_SEL[3:0] to 0b0110. A NULL conversion must always be performed first to cancel offsets.
2. Wait the appropriate channel switching time (0.3µs, typ).
3. Convert the voltage on the AMUX pin and store as V_{NULL}.
4. Program the multiplexer to switch to the battery discharge current measurement by changing CNFG_CHG_I.MUX_SEL[3:0] to 0b0101. A nonnulling conversion should be done immediately after a NULL conversion.
5. Wait the appropriate channel switching time (0.3µs, typ).
6. Convert the voltage on the AMUX pin and use the following transfer function to determine the discharge current:

$$I_{BATT(DISCHG)} = \frac{\left(V_{AMUX} - V_{NULL}\right)}{\left(V_{FS} - V_{NULL}\right)} \times I_{DISCHG-SCALE}$$

V_{FS} is 1.25V typical. $I_{DISCHG-SCALE}$ is programmable through CNFG_CHG_I.IMON_DISCHG_SCALE[3:0]. The default value is 300mA. If smaller currents are anticipated, then $I_{DISCHG-SCALE}$ can be reduced for improved measurement accuracy.

Method for Measuring Charge Current

1. Program the multiplexer to switch to the charge current measurement by changing CNFG_CHG_I.MUX_SEL[3:0] to 0b0100.
2. Wait the appropriate channel switching time (0.3µs, typ).
3. Convert the voltage on the AMUX pin and use the following transfer function to determine charging current.

$$I_{BATT(CHG)} = \frac{V_{AMUX}}{V_{FS}} \times I_{FAST-CHG}$$

V_{FS} is 1.25V typical. $I_{FAST-CHG}$ the charger's fast-charge constant-current setting and is programmable through CNFG_CHG_E.CHG_CC[5:0].

Detailed Description—SIMO Buck-Boost

The device has a micropower single-inductor, multiple-output (SIMO) buck-boost DC-to-DC converter designed for applications that emphasize low supply current and small solution size. A single inductor is used to regulate three separate outputs, saving board space while delivering better total system efficiency than equivalent power solutions using one buck and linear regulators.

The buck-boost architecture utilizes the entire battery voltage range due to its ability to create output voltages that are above, below, or equal to the input voltage. Peak inductor current for each output is independently programmable to optimize the balance between efficiency, output ripple, EMI, PCB design, and load capability.

To further boost efficiency, when the output voltage is always lower than the input, individual channel of the SIMO buck-boost converter can be configured to be in buck only mode. Similarly, each SIMO channel can be individually configured to be in boost only mode if the output voltage is constantly higher than the input. The buck only and boost only mode reduce switching losses with less switching operations compared to buck-boost mode, and thus, improves conversion efficiency. MAX77658 also allows each SIMO channel to be configured in automatic mode, which provides automatic decision between buck/boost/buck-boost mode to optimize regulator efficiency based on the V_{IN}/V_{OUT} condition.

SIMO Features and Benefits

- Three Output Channels
- Ideal for Low-Power Designs
  - SBB0/1 Delivers up to 500mA at 1.8V from a 3.7V Input
  - SBB2 Delivers up to 750mA at 1.8V from a 3.7V Input
- Small Solution Size
  - Multiple Outputs from a Single 1.5µH Inductor
  - Small 10µF (0402) Output Capacitors
- Flexible and Easy to Use
  - Glitchless Transitions Between Buck, Boost, and Buck-Boost Modes
  - Programmable Peak Inductor Current
  - Programmable On-Chip Active Discharge
  - Programmable Operating Modes (Buck Only, Boost Only, Buck-Boost Only, Automatic Mode)
  - Automatic Low-Power Mode to Normal-Power Mode Transition
- Long Battery Life
  - > 91% Peak Efficiency at 1.8V Output in Buck-Only Mode
  - > 93% Peak Efficiency at 5.0V Output in Boost-Only Mode
  - Better Total System Efficient than one switching regulator + LDOs
  - Low Quiescent Current, 1µA per Output
  - Low Input Operating Voltage, 2.7V (MIN)
  - Wide Output Voltage Range (0.5V - 5.5V)

SIMO Detailed Block Diagram

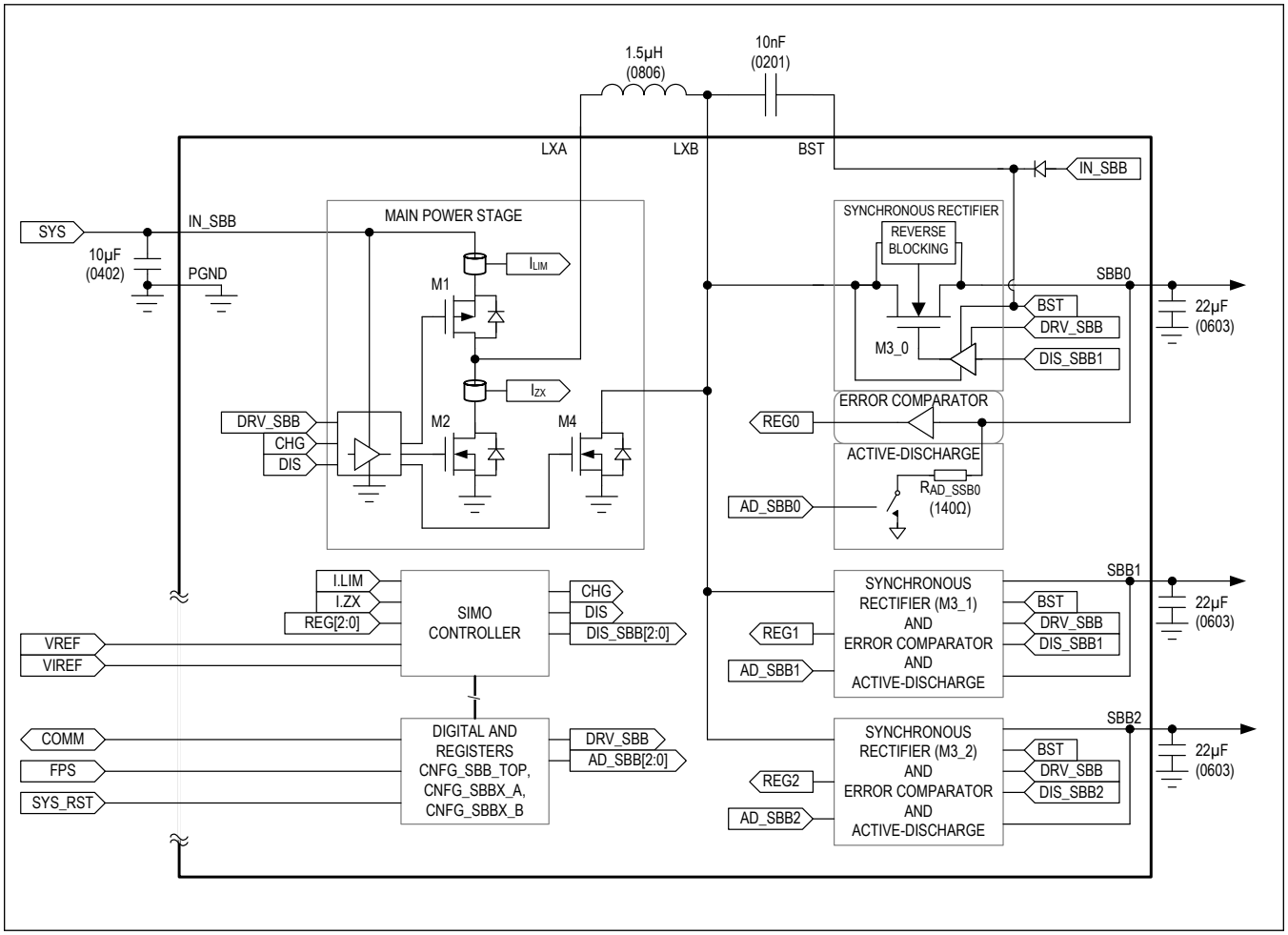


Figure 19. SIMO Detailed Block Diagram

SIMO Control Scheme

The SIMO buck-boost is designed to service multiple outputs simultaneously. A proprietary controller ensures that all outputs get serviced in a timely manner, even while multiple outputs are contending for the energy stored in the inductor. When no regulator needs service, the state machine rests in a low-power rest state.

In buck-boost mode, when the controller determines that a regulator requires service, it charges the inductor (M1 + M4) until the peak current limit is reached (I_{LIM} = CNFG_SBBx_B.IP_SBB[1:0]). The inductor energy then discharges (M2 + M3_x) into the output until the current reaches zero (I_{ZX}). In the event that multiple output channels need servicing at the same time, the controller ensures that no output utilizes all of the switching cycles. Instead, cycles interleave between all the outputs that are demanding service, while outputs that do not need service are skipped.

When the load current for any output is very light, that output automatically switches to an ultra-low-power mode (ULPM) to reduce the quiescent current consumption. Figure 20 shows typical waveform during the ULPM and normal mode. While operating in ULPM, the output voltage is biased 1.7% higher than normal mode by design so that future large load transients can be handled without excessive undershoot.

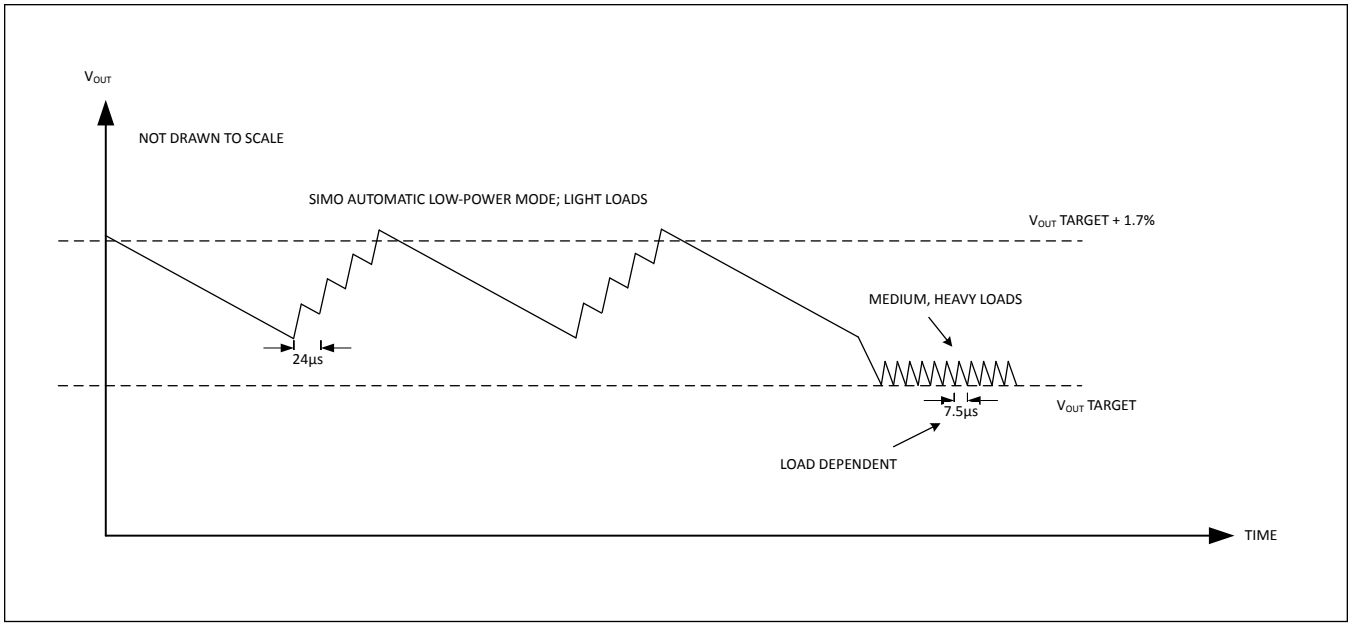


Figure 20. ULPM and Normal Mode Waveforms

Drive Strength

The SIMO regulator's drive strength for its internal power MOSFETs is adjustable using the CNFG_SBB_TOP.DRV_SBB[1:0] bit field. The ideal value is determined experimentally for each application. Faster settings such as DRV_SBB[1:0] = 0b00 result in higher efficiency but generally require stricter PCB layout rules (comparable to the MAX77658 EV kit) or shielding to avoid additional EMI. Slower settings limit EMI in non-ideal settings (e.g., contained layout, antennae adjacent to the device, etc.). Change the drive strength only once during system initialization.

SIMO Output Voltage Configuration

Each of the SIMO outputs are independently configurable. To set the output voltages at SBB0/1/2 for the MAX77658, use the I2C interface to load the configuration registers TV_SBBx[7:0]. This 8-bit configuration is a linear transfer function that starts at 0.5V, ends at 5.5V, with 25mV increments and sets the output voltage as

V_{SBBx} = 0.5V + 25mV x TV_SBBx[7:0] (decimal)

Peak Current Configuration

The peak inductor current limit corresponding to each SIMO output are independently configurable. To set the inductor peak current for the MAX77658, use the I2C interface to load the configuration registers IP_SBBx[1:0].

SIMO Soft-Start

The soft-start feature of the SIMO limits inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup (dV/dt_{SS}).

More output capacitance results in higher input current surges during startup. The following set of equations and example describes the input current surge phenomenon during startup.

In buck-boost mode, the current into the output capacitor (I_{CSBB}) during soft-start is:

$$I_{CSBB} = C_{SBB}\frac{dV}{dt_{SS}} \quad \text{(Equation1)}$$

where:

- C_{SBB} is the capacitance on the output of the regulator
- dV/dt_{SS} is the voltage change rate of the output

The input current (I_{IN}) during soft-start is:

$$I_{IN} = \frac{\left(I_{CSBB} + I_{LOAD}\right)\frac{V_{SBBx}}{V_{IN}}}{\xi} \quad \text{Equation2}$$

where:

- I_{CSBB} is from the calculation above
- I_{LOAD} is current consumed from the external load
- V_{SBBx} is the output voltage
- V_{IN} is the input voltage
- ξ is the efficiency of the regulator

For example, given the following conditions, the peak input current (I_{IN}) during soft-start is ~71mA:

Given:

- V_{IN} is 3.5V
- SBB0 and SBB1 are disabled
- V_{SBB2} is 3.3V
- C_{SBB2} = 10µF
- dV/dt_{SS} = 5mV/µs
- Load2 = 10mA
- ξ is 80%

Calculation:

- I_{CSBB} = 10µF x 5mV/µs (from Equation 1)
- I_{CSBB} = 50mA
- $I_{IN} = \frac{(50mA + 10mA)\frac{3.3V}{3.5V}}{0.80}$ (from Equation1)
- I_{IN} ~ 71mA

SIMO Registers

Each SIMO buck-boost channel has registers to program its target output voltage (CNFG_SBBx_A.TV_SBBx[7:0]) and its peak current limit (CNFG_SBBx_B.IP_SBBx[1:0]). Additional controls are available for enabling/disabling the active-discharge resistors (CNFG_SBBx_B.ADE_SBBx), operatation mode (CNFG_SBBx_B.OP_MODE[1:0]) as well as enabling/disabling the SIMO buck-boost channels (CNFG_SBBx_B.EN_SBBx[2:0]). For a full description of bits, registers, default values, and reset conditions, see the *Register Map*.

SIMO Active Discharge Resistance

Each SIMO buck-boost channel has an active-discharge resistor (R_{AD_SBBx}) that is automatically enabled/disabled based on a CNFG_SBBx_B.ADE_SBBx bit and the status of the SIMO regulator. The active discharge feature may be enabled (CNFG_SBBx_B.ADE_SBBx = 1) or disabled (CNFG_SBBx_B.ADE_SBBx = 0) independently for each SIMO channel. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. If the active-discharge resistor is enabled by default, then the active-discharge resistor is on whenever V_{SYS} is below $V_{SYSUVLO}$ and above V_{POR}.

These resistors discharge the output when CNFG_SBBx_B.ADE_SBBx = 1, and their respective SIMO channel is off. If the regulator is forced on through CNFG_SBBx_B.EN_SBBx[2:0] = 0b110 or 0b111, then the resistors do not discharge the output even if the regulator is disabled by the main-bias.

Note that when V_{SYS} is less than 1.0V, the NMOS transistors that control the active-discharge resistors lose their gate drive and become open.

SIMO Buck Only and Boost Only Mode

If the input voltage at IN_SBB never falls below the target output voltage of one or more SIMO converter channels, the individual channels can be configured to be in buck mode with the bitfield CNFG_SBBx_B.OP_MODE[1:0]. In buck mode, when the buck-mode channel needs service, switch M3_x remains closed and M4 remains open (see Figure 19) when SBBx is being serviced. Only M1 and M2 are toggled as in a traditional buck converter for the switching cycle.

Similarly, if the input voltage at IN_SBB never rises above the target output voltage of one or more SIMO converter channels, individual channels can be configured to be in boost mode with CNFG_SBBx_B.OP_MODE[1:0]. In boost mode, when the boost-mode channel needs service, switch M1 remains closed and M2 remains open (see Figure 19). Only M3x and M4 are toggled as in a traditional boost converter.

Efficiency is boosted in these two modes compared to buck-boost mode due to three major factors:

- Reduced switching loss for each for each switching cycle: buck mode and boost mode toggles only two switches versus the four in buck-boost mode. Therefore, there are less switching events in a switching cycle.
- Lower inductor core losses for each switching cycle: Inductor current changes from 0A to peak current during a switching cycle. The larger the change in current the inductor experiences, the more energy is lost in the inductor core in the form of heat. In buck mode and boost mode, the peak current can be reduced since less average inductor current is needed to support a load. Less inductor current is needed because of direct energy transfer. Direct energy transfer occurs the input (IN_SBB) is connected directly to the output (SBBx) through the inductor. Therefore, the input not only provides energy to charge the inductor, energy is also supplied to the output capacitor and load devices. Thus, less current is needed to charge the inductor to provide sufficient load to the output
- Less frequent switching cycles with the same peak current limit setting: With the same peak current limit, because of direct energy transfer during the converter operation, more energy gets delivered in each switching cycle with buck-only and boost-only mode than that with buck-boost mode.

Maintain a minimum headroom of 0.7V between IN_SBB and SBBx in buck mode because inductor charge time ($dt = L \times I_{P\_SBBx}/(V_{IN\_SBB} - V_{SBBx})$) increases as the difference between the IN_SBB and SBBx voltages shrinks. As the inductor current takes longer to reach the peak current limit, the MAX77658 may trigger a fault flag. Likewise, it is recommended to keep SBBx at least 0.7V higher than IN_SBB to force the rail into boost-only mode so that the inductor current does not take too long to reach zero.

Applications Information

SIMO Available Output Current

The available output current on a given SIMO channel is a function of the input voltage, output voltage, the peak current limit setting, and the output current of the other SIMO channels. Maxim offers the *SIMO Calculator* that outlines the available capacity for specific conditions. Table 12 is an extraction from the calculator.

Table 12. SIMO Available Output Current for Common Applications

PARAMETERS	EXAMPLE 1	EXAMPLE 2	EXAMPLE 3	EXAMPLE 4	EXAMPLE 5
V_{IN_MIN}	2.7V	2.7V	3.2V	3.4V	3.6V
R_{L_DCR}	0.1Ω	0.1Ω	0.1Ω	0.12Ω	0.12Ω
SBB0	1.0V at 100mA	1.0V at 80mA	1.2V at 50mA	1.2V at 20mA	1.2V at 20mA
SBB1	1.2V at 75mA	1.2V at 50mA	2.05V at 100mA	2.05V at 80mA	2.05V at 80mA
SBB2	1.8V at 50mA	1.8V at 40mA	3.3V at 30mA	3.3V at 10mA	2.05V at 5mA
Operating Mode	Buck-Boost	Buck	Buck-Boost	Buck-Boost	Buck

Table 12. SIMO Available Output Current for Common Applications (continued)

I_{P_SBB0}	1A	1A	1A	0.5A	1A
I_{P_SBB1}	1A	1A	0.707A	0.5A	1A
I_{P_SBB2}	1A	1A	1A	0.5A	0.5A
Utilized Capacity	73%	77%	79%	73%	79%

ESR_{C_IN} = ESR_{C_OUT} = 5mΩ, L = 1.5µH

Inductor Selection

Choose an inductance from 1.0µH to 2.2µH; 1.5µH inductors work best for most designs. Larger inductance transfer more energy to the output for each cycle and typically result in lower switching frequency, thus, better efficiency but larger output voltage ripple. See the *Output Capacitor Selection* section for more information on how to size your output capacitor in order to control ripple.

Choose the inductor saturation current to be greater than or equal to the maximum peak current limit setting that is used for all of the SIMO buck-boost channels (I_{P_SBBx}). For example, if SBB0 is set for 0.5A, SBB1 is set for 0.75A, and SBB2 is set for 1.0A, then choose the saturation current to be greater than or equal to 1.0A.

Choose the RMS current rating of the inductor (typically the current at which the temperature rises appreciably) based on the expected load requirement of the system. For systems where the expected load conditions are not well known, be conservative and choose the RMS current to be greater than or equal to half the higher maximum peak current limit setting [$I_{RMS} \geq MAX(I_{P\_SBB0}, I_{P\_SBB1}, I_{P\_SBB2})/2$]. This is a conservative choice because the SIMO buck-boost regulator implements a discontinuous conduction mode (DCM) control scheme, which returns the inductor current to zero at the end of each cycle.

Consider the DC-resistance (DCR), AC-resistance (ACR), and package size of the inductor. Typically, smaller sized inductors have larger DC-resistance and larger AC-resistance that reduces efficiency and the total output power. Note that many inductor manufacturers have inductor families which contain different versions of core material in order to balance trade-offs between DCR, ACR (i.e., core losses), and component cost. For this SIMO regulator, inductors with the lowest ACR in the 1.0MHz to 2.0MHz region tend to provide the best efficiency.

Input Capacitor Selection

Choose the input bypass capacitance (C_{IN_SBB}) to be 22µF. Larger values of C_{IN_SBB} improve the decoupling for the SIMO regulator.

C_{IN_SBB} reduces the current peaks drawn from the battery or input power source during SIMO regulator operation and reduces switching noise in the system. The ESR/ESL of the input capacitor should be very low (i.e., ESR ≤ 5mΩ and ESL ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

To fully utilize the available input voltage range of the SIMO (5.5V, max), use a capacitor with a voltage rating of 6.3V at minimum.

Boost Capacitor Selection

Choose the boost capacitance (C_{BST}) to be 10nF. Smaller values of C_{BST} result in insufficient gate drive for M3. Larger values of C_{BST} have the potential to degrade the startup performance. Ceramic capacitors with 0201 or 0402 case size are recommended.

Output Capacitor Selection

Choose each output bypass capacitance (C_{SBBx}) based on the target output voltage ripple (ΔV_{SBBx}): typical values are 22µF. Larger values of C_{SBBx} improve the output voltage ripple but increase the input surge currents during soft-start and output voltage changes. The output voltage ripple is a function of the inductance (L), the output voltage (V_{SBBx}), and

the peak current limit setting (I_{P_SBBx}). See Equation 3 to estimate required effective capacitance.

$$C_{SBBx} = \frac{I_{P\_SBBx}^2 \times L}{2 \times V_{SBBx} \times \Delta V_{SBBx}} \quad \text{(Equation3)}$$

The *SIMO Calculator* can be used to aid in the selection of the output capacitance. Note that most designs concern themselves with having enough capacitance on the output but there is also a maximum capacitance limitation that is calculated within the SIMO calculator; take care not to exceed the maximum capacitance.

C_{SBBx} is required to keep the output voltage ripple small. The impedance of the output capacitors (ESR, ESL) should be very low (i.e., ESR ≤ 5mΩ and ESL ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

A capacitor's effective capacitance decreases with increased DC bias voltage. This effect is more pronounced as capacitor case sizes decrease. Due to this characteristic, it is possible for an 0603 case size capacitor to perform well, while an 0402 case size capacitor of the same value performs poorly. The SIMO regulator is stable with low output capacitance (1µF) but the output voltage ripple would be large; consider the effective output capacitance value after initial tolerance, bias voltage, aging, and temperature derating.

Example Component Selection

Pick input/output capacitors and the inductor for the given requirements:

- $V_{IN\_SBB,\ typical}$ = 3.7V

Table 13. Design Requirements

	SBB0	SBB1	SBB2
Output Voltage	3.3V	1.8V	1.2V
Maximum Load Current	50mA	60mA	80mA
Maximum Voltage Ripple	50mV	30mV	30mV

Inductor, Peak Current Limit, and Input Capacitor

For the best efficiency, a 1.5µH inductor is chosen. For this example, assume the DFE201610E-1R5M inductor from Murata is used. This particular inductor has 91mΩ of DCR.

Since the load current is low, first choose the inductor current peak to be 0.333A for all outputs. Next, enter these values into Maxim's SIMO calculator as mentioned previously.

Symbol	Value	Unit	Per Channel Symbol		Per Channel Value			Unit
					SBB0	SBB1	SBB2	
Input Section								
V_{IN}	3.7000	V	V_{OUT}		3.300	1.800	1.200	V
L	1.50	µH	I_{OUT}		30.0	60.0	80.0	mA
r_{L_DCR}	91	mΩ	C_{OUT}	Nominal	22.0	22.0	22.0	µF
				Effective	7.8	13.0	17.0	µF
$T_{OPERATING}$	25	°C	Channel Enabled?		Yes	Yes	Yes	
Device Settings Inputs								
Device	MAX77642/643/658		I_{L_Peak}		0.333	0.333	0.333	A
			Operating Mode		Automatic	Automatic	Automatic	
Calculation Results								
Device Characteristics								
			V_{OUT} Range		0.500V - 5.500V	0.500V - 5.500V	0.500V - 5.500V	
			Operating Mode		Buck-Boost	Buck	Buck	
Effective Output Capacitance								
			C_{OUT} Effective		7.8	13.0	17.0	µF
Inductor Utilization								
Total Utilization	120.2%		Utilization		35.3%	36.2%	48.7%	

Figure 21. Component Selection-High Utilization

As shown in [[Component Selection - High Utilization]], the utilization is over 100%, which leads to high output voltage ripple. To lower utilization, increase the inductor peak current limits. For this example, 1A is used for SBB0 and 0.5A for SBB1 and SBB2. [[Component Selection - Final Current Peak Limits]] shows the utilization less than 80%. Using 0.5A for the inductor peak current limit has the added benefit of increased efficiency.

Symbol	Value	Unit	Per Channel Symbol	Per Channel Value			Unit
				SBB0	SBB1	SBB2	
Input Section							
V_{IN}	3.7000	V	V_{OUT}	3.300	1.800	1.200	V
L	1.50	µH	I_{OUT}	30.0	60.0	80.0	mA
r_{L_DCR}	91	mΩ	C_{OUT} Nominal	22.0	22.0	22.0	µF
			C_{OUT} Effective	7.8	13.0	17.0	µF
$T_{OPERATING}$	25	°C	Channel Enabled?	Yes	Yes	Yes	
Device Settings Inputs							
Device	MAX77642/643/658		I_{L_Peak}	0.750	0.500	0.500	A
			Operating Mode	Automatic	Automatic	Automatic	
Calculation Results							
Device Characteristics							
			V_{OUT} Range	0.500V - 5.500V	0.500V - 5.500V	0.500V - 5.500V	
			Operating Mode	Buck-Boost	Buck	Buck	
Effective Output Capacitance							
			C_{OUT} Effective	7.8	13.0	17.0	µF
Inductor Utilization							
Total Utilization	73.0%		Utilization	16.3%	24.1%	32.6%	

Figure 22. Component Selection-Final Current Peak Limits

To support the selected peak currents, choose 22µF for the input capacitor.

Output Capacitors

Using Equation 3 and the selected inductor current peak limits, the minimum output capacitances required are:

$$C_{SBB0\_min} = \frac{I_{P\_SBB0}^2 x L}{2 x V_{SBB0} x \Delta V_{SBB0}} = \frac{1^2 x 2.2 x 10^{-6} A^2 x H}{2 x 3.3 x 0.05 V^2} = 6.67\mu F$$

$$C_{SBB1\_min} = \frac{I_{P\_SBB1}^2 x L}{2 x V_{SBB1} x \Delta V_{SBB1}} = \frac{0.5^2 x 2.2 x 10^{-6} A^2 x H}{2 x 1.8 x 0.03 V^2} = 5.09\mu F$$

$$C_{SBB2\_min} = \frac{I_{P\_SBB2}^2 x L}{2 x V_{SBB2} x \Delta V_{SBB2}} = \frac{0.5^2 x 2.2 x 10^{-6} A^2 x H}{2 x 1.2 x 0.03 V^2} = 7.64\mu F$$

For this example, the 22µF GRM188R61A226ME15 is chosen for all three outputs. The effective capacitance after derating is the following:

C_{SBB0} = 8.113µF

C_{SBB1} = 13.828µF

C_{SBB2} = 16.793µF

Go back to the calculator and enter the capacitance for each channel. Figure 23 shows the expected ripples, which fit the requirements.

Symbol	Value	Unit	Per Channel Symbol		Per Channel Value			Unit
					SBB0	SBB1	SBB2	
Input Section								
V_{IN}	3.7000	V	V_{OUT}		3.300	1.800	1.200	V
L	1.50	µH	I_{OUT}		30.0	60.0	80.0	mA
r_{L_DCR}	91	mΩ	C_{OUT}	Nominal	22.0	22.0	22.0	µF
				Effective	7.8	13.0	17.0	µF
$T_{OPERATING}$	25	°C	Channel Enabled?		Yes	Yes	Yes	
Device Settings Inputs								
Device	MAX77642/643/658		I_{L_Peak}		0.750	0.500	0.500	A
			Operating Mode		Automatic	Automatic	Automatic	
Calculation Results								
Device Characteristics								
			V_{OUT} Range		0.500V - 5.500V	0.500V - 5.500V	0.500V - 5.500V	
			Operating Mode		Buck-Boost	Buck	Buck	
Effective Output Capacitance								
			C_{OUT} Effective		7.8	13.0	17.0	µF
Inductor Utilization								
Total Utilization	73.0%		Utilization		16.3%	24.1%	32.6%	
Current and Power								
			I_{OUT_Max}		0.184	0.249	0.246	A
			P_{OUT_Max}		0.606	0.448	0.295	W
Output Voltage Ripple								
			$V_{OUT\_ripple\_no\_load}$		83.5	57.8	44.9	mV_{pp}
					2.5%	3.2%	3.7%	
			$V_{OUT\_ripple\_w\_load}$		23.9	22.8	19.5	mV_{pp}
					0.7%	1.3%	1.6%	
			f_{OUT_ripple}		253.7	296.0	364.5	kHz
			V_{OUT_peak}		3.313	1.812	1.209	V
			V_{OUT_valley}		3.289	1.789	1.189	V

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Figure 23. Component Selection-Expected Ripple

Summary

- L = 2.2µH
- C_{IN_SBB} = 22µF
- Total Switching Utilization = 79%

Table 14. Summary of Design for Component Selection Example

	SBB0	SBB1	SBB2
I_{P_SBBx}	1A	0.5A	0.5A
C_{SBBx} (nominal)	22µF	22µF	22µF
ΔV_{SBBx}	35.2mV	17.9mV	14.7mV

Real applications should also consider the minimum input voltage since the battery discharges. The following is a

summary using the same components but an input voltage of 3.0V instead. The switching utilization increased to 82.4%, above the recommended 80% but still acceptable.

- L = 2.2µH
- C_{IN_SBB} = 22µF
- Total Switching Utilization = 82.4%

Table 15. Summary of Design with Lower Input Voltage

	SBB0	SBB1	SBB2
I_{P_SBBx}	1A	0.5A	0.5A
C_{SBBx} (nominal)	22µF	22µF	22µF
ΔV_{SBBx}	13.0mV	14.9mV	13.0mV

SIMO Switching Frequency

The SIMO buck-boost regulator uses a pulse frequency modulation (PFM) control scheme. The switching frequency for each output is a function of the operating mode, inductor peak current limit, input voltage, output voltage, load current, and inductance. Output capacitance is a minor factor in SIMO switching frequency. The *SIMO Calculator* can be used to estimate expected switching frequency.

At no load, switching frequencies can be as low as 10Hz. For the 3.7V input to 1.2V output channel from the *Example Component Selection* section, the switching frequency is about 327kHz.

Table 16 lists how different factors increase or decrease switching frequency.

Table 16. Switching Frequency Control

FACTOR	INCREASING FREQUENCY	DECREASING FREQUENCY
Inductor Current Peak Limit	Lower peak limit	Higher peak limit
Operating Mode	Buck-boost mode	Buck mode/ boost mode
Inductor	Decrease inductance	Increase inductance
Input Voltage	Higher voltage	Lower voltage
Output Voltage	Higher voltage	Lower voltage
Load Current	Higher current	Lower current

Unused Outputs

Do not leave unused outputs unconnected. If an output left unconnected is accidentally enabled, the charged inductor experiences an open circuit, and the output voltage soars above the absolute maximum rating, damaging the device. If an output is not used, do one of the following:

1. Disable the output (CNFG_SBBx_B.EN_SBBx[2:0] = 0x4 or 0x5) and connect the output to ground. If an unused output is default enabled or can be accidentally enabled, do one of the following recommendations instead.
2. Bypass the unused output with a 1µF capacitor to ground.
3. Connect the unused output to IN_SBB or a different output channel if the unused output is programmed to a lower voltage. Since the output voltage is higher than the unused output, the regulator does not service the unused output even if it is unintentionally enabled.
    1. Note that some OTP options have the active-discharge resistors enabled by default. Connecting an unused output to IN_SBB is not recommended if the active discharge is enabled by default. If connecting the unused output to a different channel, disable the active-discharge resistor (CNFG_SBBx_B.ADE_SBBx = 0) of the unused channel.

PCB Layout Guide

Figure 24 shows an example layout of the top layer.

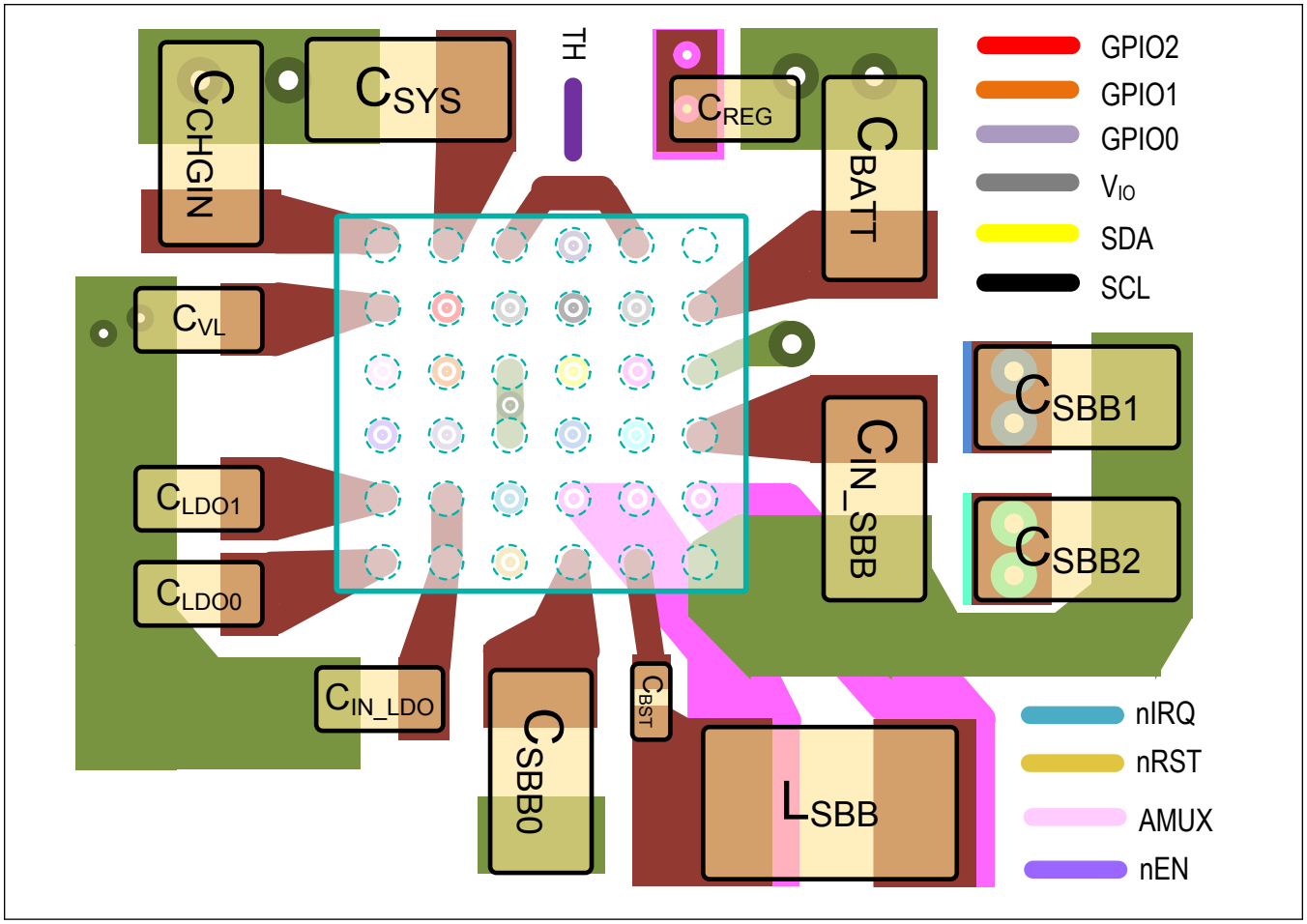

Figure 24. PCB Top-Layer and Component Placement Example

Capacitors

Place decoupling capacitors as close as possible to the IC such that connections from capacitor pads to pin and from capacitor pads to ground pins are short. Keeping the connections short lowers parasitic inductance and resistance, improving performance and shrinking the physical size of hot loops.

If connections to the capacitors are through vias, use multiple vias to minimize parasitics. Also, connect loads to the capacitor pads rather than the device pins.

Most critical are the capacitors for the switching regulator: input capacitor at IN_SBB and output capacitors at SBBx.

Input Capacitor at IN_SBB

Minimize the parasitic inductance from PGND to input capacitor to IN_SBB to reduce ringing on the LXA voltage.

Inductor

Keep the inductor close to the IC to reduce trace resistance; however, prioritize any regulator input/output capacitors over the inductor. Use the appropriate trace width from LXA to inductor to LXB to support the peak inductor current. Likewise, if there are vias in the path, use an appropriate amount of vias to support the peak current.

Ground Connections

As the switching regulator charges and discharges the inductor, current flows from PGND to the input capacitor ground, from output capacitor ground to PGND, or from output capacitor ground to input capacitor ground. Therefore, use a wide,

continuous copper plane to connect PGND to the capacitor grounds.

When connecting the GND and PGND pins together, ensure noise from the power ground does not enter the analog ground (where GND is connected). For example, assuming the ground pins are connected through a solid ground plane on an internal layer, one via connecting GND to the internal ground plane may be sufficient to protect GND from most of the noise in the power-ground plane. Likewise, if there are other higher current or noisy circuitry near this device, avoid connecting the GND pin directly to their grounds.

For more guidelines on proper grounding, visit: *https://www.maximintegrated.com/en/design/partners-and-technology/design-technology/ground-layout-board-designers.html*.

Detailed Description—Low Dropout Linear Regulator (LDO)/Load Switch (LSW)

The device includes two on-chip low-dropout linear regulators (LDO0/1) that can also be configured as load switches. These LDOs are optimized to have low-quiescent current. The input voltage range (V_{IN_LDOx}) allows it to be powered directly from the main energy source such as a Li-Poly battery or from an intermediate regulator. Each linear regulator delivers up to 150mA.

Features and Benefits

- 2x 150mA LDO
- LDO Input Voltage Range: 1.71V to 5.5V
- LSW Input Voltage Range: 1.2V to 5.5V
- Adjustable Output Voltage
- 100mV Maximum Dropout Voltage at ECT Conditions
- Programmable On-Chip Active Discharge

LDO/LSW Simplified Block Diagram

Each LDO/LSW block has one input (IN_LDOx) and one output (LDOx) and several ports that exchange information with the rest of the device (V_{REF}, EN_LDOx, ADE_LDOx). V_{REF} comes from the main bias circuits. CNFG_LDOx_B.EN_LDOx and CNFG_LDOx_B.ADE_LDOx are register bits for controlling the enable and active-discharge feature, respectively. See the *Register Map* for more information.

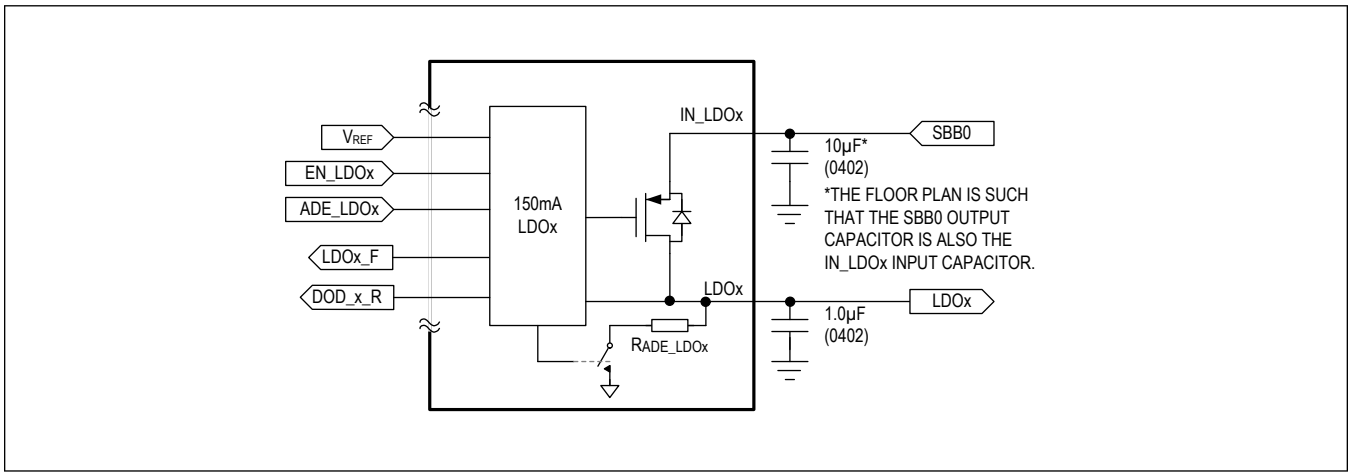

Figure 25. LDO Simplified Block Diagram

LDO/LSW Active-Discharge Resistor

Each LDO/LSW block has an active-discharge resistor (R_{AD_LDOx}) that is enabled if CNFG_LDO_B.ADE_LDOx = 1 and LDOx is disabled. Enabling the active discharge feature helps ensure a complete and timely power down of the resource. During power up, if $V_{SYS} > V_{POR}$ and CNFG_LDO_B.ADE_LDOx = 1, the active-discharge resistor is enabled.

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LDO/LSW Soft-Start

The soft-start feature limits inrush current during startup, and is achieved by limiting the slew rate of the output voltage during startup (dV_{OUT_LDOx}/dt_{SS}).

More output capacitance results in higher input current surges during startup. The equation and example describes the input current surge phenomenon during startup.

The input current (I_{IN_LDOx}) during soft-start is:

$$I_{IN\_LDOx} = C_{LDOx}\frac{dV_{OUT\_LDOx}}{dt_{SS}} + I_{OUT\_LDOx}$$

where:

- C_{LDOx} is the capacitance on the output of the regulator
- dV_{OUT_LDOx}/dt_{SS} is the voltage change rate of the output

For example, given the following conditions, the input current (I_{IN_LDOx}) during soft start is 13.08mA:

Given:

- C_{LDOx} = 2.2µF
- dV_{OUT_LDOx}/dt_{SS} = 1.4mV/µs
- LDOx programmed to 1.85V
- R_{LDOx} = 185Ω (I_{OUT_LDOx} = 1.85V/185Ω = 10mA)

Calculation:

- I_{IN} = 2.2µF x 1.4mV/µs + 10mA
- I_{IN} = 13.08mA

Load Switch Configuration

Both LDO0 and LDO1 can be configured as load switches with the CNFG_LDOx_B.LDOx_MD bit. As shown in Figure 26, the transition from LDO to LSW mode is controlled by a defined slew rate until dropout is detected. Once dropout is detected, the load switch is fully closed and the dropout interrupt flag (INT_GLBL.DODx_R) is set.

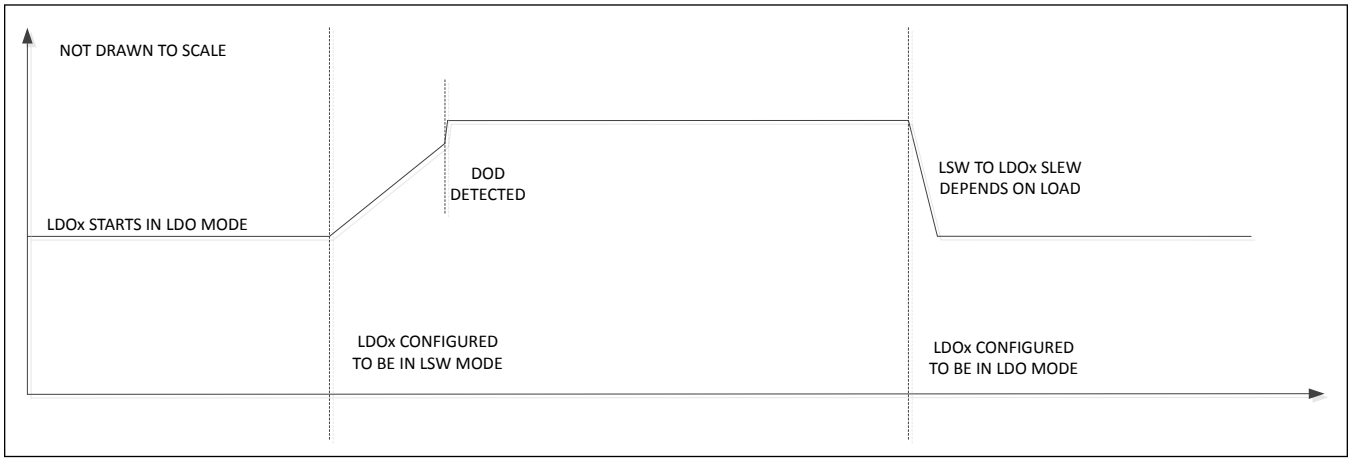


Figure 26. LDO to LSW Transition Waveform

Applications Information

Input Capacitor Selection

Make sure the input bypass capacitance (C_{IN_LDOx}) is at least 2.2µF. Larger values of C_{IN_LDOx} improve the decoupling for LDOx. The floor plan of the device is such that SBB0 is adjacent to IN_LDOx and if the SIMO channel 0 output powers the input of LDOx, then its output capacitor (C_{SBB0}) can also serve as C_{IN_LDOx} such that only one capacitor is required.

C_{IN_LDOx} reduces the current peaks drawn from the battery or input power source during operation. The impedance of the input capacitor (ESR, ESL) should be very low (i.e., ESR ≤ 50mΩ and ESL ≤ 5nH) for frequencies up to 0.5MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

Output Capacitor Selection

For both LDO and LSW modes, choose the output bypass capacitance (C_{LDOx}) to be 1µF.

In LDO mode, larger values of C_{LDOx} improve output PSRR but increase input surge currents during soft-start and output voltage changes. The effective output capacitance should not exceed 2.8µF to maintain stability.

While in LDO mode, C_{LDOx} is required to keep stability. The series inductance of the output capacitor and its series resistance should be low (i.e., ESR ≤ 10mΩ and ESL ≤ 1nH) for frequencies up to 0.5MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

A capacitor's effective capacitance decreases with increased DC bias voltage. This effect is more pronounced with smaller capacitor case sizes. Due to this characteristic, 0603 case size capacitors tend to perform well while 0402 case size capacitors of the same value perform poorly.

Detailed Description—FUEL GAUGE

The MAX77658 is an ultra-low power fuel gauge which implements the Maxim ModelGauge m5 EZ algorithm. The IC measures voltage, current, and temperature accurately to produce fuel gauge results. The ModelGauge m5 EZ robust algorithm provides tolerance against battery diversity. This additional robustness enables simpler implementation for most applications and batteries by avoiding time-consuming battery characterization.

The ModelGauge m5 algorithm combines the short-term accuracy and linearity of a coulomb-counter with the long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel gauge accuracy. The IC automatically compensates for aging, temperature, and discharge rate and provides accurate state of charge (SOC) in percentage (%) and remaining capacity in milliampere-hours (mAhr) over a wide range of operating conditions. Fuel gauge error always converges to 0% as the cell approaches empty.

The IC has a register set that is compatible with Intel's DBPT v2 dynamic power standard. This allows the system designer to safely estimate the maximum allowed CPU turbo-boost power level in complex power conditions. The IC provides accurate estimation of time-to-empty and time-to-full and provides three methods for reporting the age of the battery: reduction in capacity, increase in battery resistance, and cycle odometer.

The IC contains a unique serial number. It can be used for cloud-based authentication. See the *Serial Number Feature* section for more information.

Communication to the host occurs over standard I^2C interface.

ModelGauge m5 EZ Performance

ModelGauge m5 EZ performance provides plug-and-play operation when the IC is connected to most lithium batteries. While the IC can be custom tuned to the application's specific battery through a characterization process for ideal performance, the IC has the ability to provide good performance for most applications with no custom characterization required. Table 17 and Figure 27 show the performance of the ModelGauge m5 algorithm in applications using ModelGauge m5 EZ configuration.

The ModelGauge m5 EZ provides good performance for most cell types. For some chemistries, such as lithium-iron-phosphate ($LiFePO_4$) and Panasonic NCR/NCA series cells, it is suggested that the customer request a custom model from Maxim for best performance.

For even better fuel-gauging accuracy than ModelGauge m5 EZ, contact Maxim for information regarding cell characterization.

Table 17. ModelGauge m5 EZ Performance

DESCRIPTION	AFTER FIRST CYCLE* (%)	AFTER SECOND CYCLE* (%)
Tests with less than 3% error	95	97
Tests with less than 5% error	98.7	99
Tests with less than 10% error	100	100

**Test conditions: +20°C and +40°C, run time of > 3 hours.*

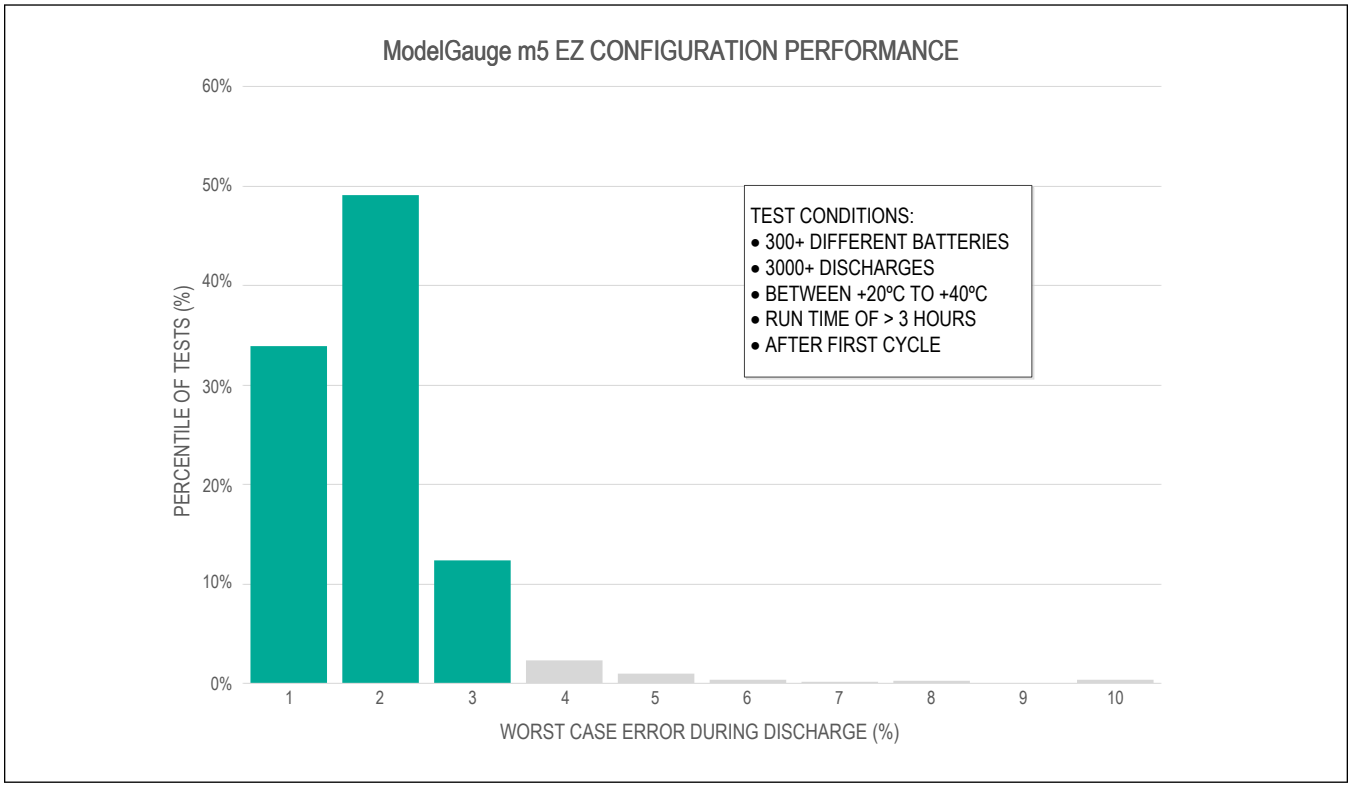


Figure 27. ModelGauge m5 EZ Configuration Performance

Application Notes

This datasheet describes the basic feature sets and the minimal register set needed to support the plug-and-play ModelGauge™ m5 EZ performance. Refer to the following application notes for additional reference material for the fuel

gauge of MAX77658:

- *ModelGauge m5 EZ User Guide*
  - Documents full register set
  - More details about ModelGauge m5 algorithm
  - Discusses additional applications
- *Software Implementation Guide*
  - Guidelines for software drivers including example code

Standard Register Formats

Unless otherwise stated during a given register's description, all the fuel gauge registers of MAX77658 follow the same format depending on the type of register. See Table 18 for the resolution and range of any register described hereafter.

Table 18. ModelGauge m5 Register Standard Resolutions

REGISTER TYPE	LSb SIZE	MINIMUM VALUE	MAXIMUM VALUE	NOTES
Capacity	0.1mAh	0.0mAh	6553.5mAh	
Percentage	1/256%	0.0%	255.9961%	1% LSb when reading only the upper byte.
Voltage	1.25mV/16	0.0V	5.11992V	
Current	31.25µA	-1.024A	1.024A	Signed two's-complement format.
Temperature	1/256°C	-128.0°C	127.996°C	Signed two's-complement format. 1°C LSb when reading only the upper byte.
Resistance	1/4096Ω	0.0Ω	15.99976Ω	
Time	5.625s	0.0s	102.3984h	
Special				Format details are included with the register description.

ModelGauge m5 Algorithm

Classical coulomb-counter-based fuel gauges have excellent linearity and short-term performance. However, they suffer from drift due to the accumulation of the offset error in the current-sense measurement. Although the offset error is often very small, it cannot be eliminated. It causes the reported capacity error to increase over time and requires periodic corrections. Corrections are traditionally performed at full or empty. Some other systems also use the relaxed battery voltage to perform corrections. These systems determine the true state-of-charge (SOC) based on the battery voltage after a long time of no current flow. Both have the same limitation: if the correction condition is not observed over time in the actual application, the error in the system is boundless. The performance of classic coulomb counters is dominated by the accuracy of such corrections. Voltage measurement based SOC estimation has accuracy limitations due to imperfect cell modeling, but does not accumulate offset error over time.

The MAX77658 includes an advanced voltage fuel gauge (VFG) that estimates open-circuit voltage (OCV), even during current flow, and simulates the nonlinear internal dynamics of a Li+ battery to determine the SOC with improved accuracy. The model considers the time effects of a battery caused by the chemical reactions and impedance in the battery to determine SOC. This SOC estimation does not accumulate offset error over time. The IC performs a smart empty compensation algorithm that automatically compensates for the effect of temperature condition and load condition to provide accurate state-of-charge information. The converge-to-empty function eliminates error toward empty state. The IC learns battery capacity over time automatically to improve long-term performance. The age information of the battery is available in the output registers.

The ModelGauge m5 algorithm combines a high-accuracy coulomb counter with a VFG. See Figure 28. The complementary combined result eliminates the weaknesses of both the coulomb counter and the VFG while providing the strengths of both. A mixing algorithm combines the VFG capacity with the coulomb counter and weighs each result so that both are used optimally to determine the battery state. In this way, the VFG capacity result is used to continuously make small adjustments to the battery state, cancelling the coulomb-counter drift.

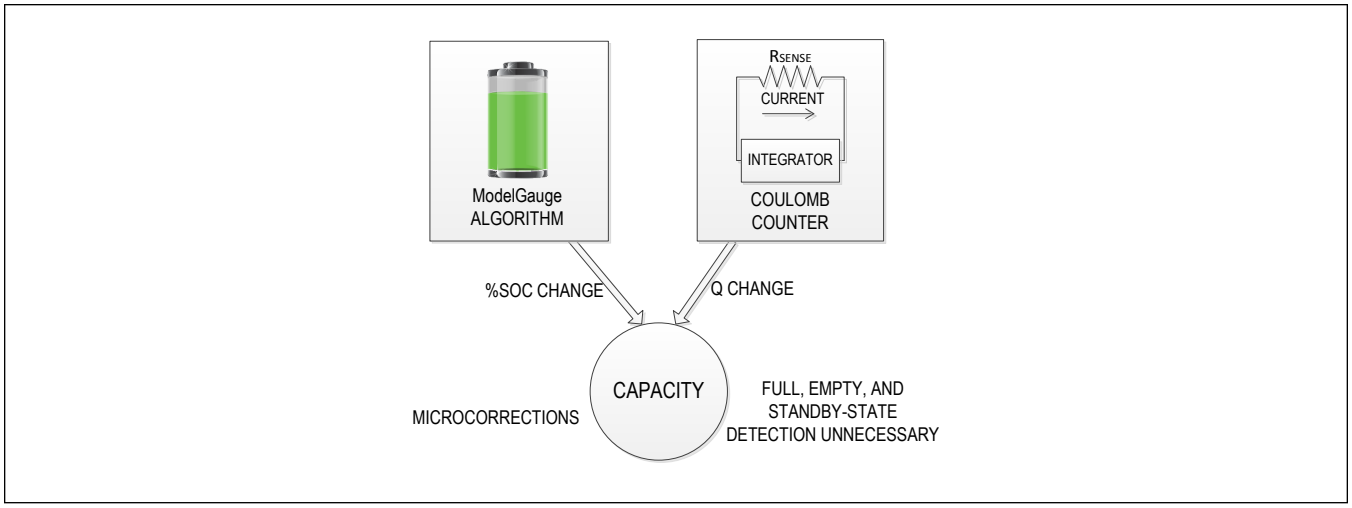


Figure 28. ModelGauge m5 Algorithm

The ModelGauge m5 algorithm uses this battery state information and accounts for temperature, battery current, age, and application parameters to determine the remaining capacity available to the system. As the battery approaches the critical region near empty, the ModelGauge m5 algorithm invokes a special error correction mechanism that eliminates any error.

The ModelGauge m5 algorithm continually adapts to the cell and application through independent learning routines. As the cell ages, its change in capacity is monitored and updated and the voltage-fuel-gauge dynamics adapt based on cell-voltage behavior in the application.

Analog Measurements

The IC monitors voltage, current, and temperature. This information is provided to the fuel-gauge algorithm to predict cell capacity and also made available to the user.

Voltage Measurement

VCell Register (0x09)

Register Type: Voltage

VCell reports the voltage measured between BATT and GND

AvgVCell Register (0x19)

Register Type: Voltage

The AvgVCell register reports an average of the VCell register readings.

MaxMinVolt Register (0x1B)

Register Type: Special

Initial Value: 0x00FF

The MaxMinVolt register maintains the maximum and minimum of VCell register values since the device reset. At power-upo, the maximum voltage value is set to 0x00 (the minimum) and the minimum voltage value is set to 0xFF (the maximum). Therefore, both values are changed to the voltage register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x00FF. The maximum and minimum voltages are each stored as 8-bit values with a 20mV resolution. See the *Register Map* for register format.

Current Measurement

The MAX77658 monitors the current flow through the battery by measuring the voltage across the internal current

sensing element. The IC is precalibrated for current-measurement accuracy in Maxim's factory. Additionally, the IC maintains a record of the minimum and maximum current measured by the IC and an average current.

The maximum current constraints listed in the Absolute Maximum Ratings section should be followed to ensure the 100,000 hours lifetime of the sensing element. In general, the root mean square of current over whole lifetime should below 0.76A, with additional limitation on peak value based on utilization. If the device utilization is 100% (charges or discharges at highest allowable current level without stopping), then the maximum DC current rating is 0.76A. If the device utilization is 10%, then the maximum DC current allowed is 1.07A. For example, it spends 10% of its time charging, and the remaining 90% resting or discharging, then it can be allowed 1.07A charge current, but discharge currents should be below 0.72A. For Pulse current case, if the utilization of the current pulse is 1% of whole lifetime, then the peak pulse current allowed with 250ms pulse width and 10% duty cycle is 1.39A.

Current Register (0x0A)

Register Type: Current

The MAX77658 uses internal current sensing to monitor the current through the SYS FG pin. The measurement value is stored in two's-complement format. Measurement that exceeds maximum and minimum current range is stored as maximum and minimum value. The current register has a LSb value of 31.25µA, a register scale range of ±1.024A, and an allowable measurement range as described in the Absolute Maximum Ratings.

AvgCurrent Register (0x0B)

Register Type: Current

The AvgCurrent register reports an average of Current register readings.

MaxMinCurr Register (0x1C)

Register Type: Special

Initial Value: 0x807F

The MaxMinCurr register maintains the maximum and minimum Current register values since the last IC reset or until cleared by host software. At power-up, the maximum current value is set to (most negative) and the minimum current value is set to 7Fh(most positive). Therefore, both values are changed to the Current register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x807F. The maximum and minimum currents are each stored as two's complement 8-bit values with 160mA resolution. See the *Register Map* for register format.

Temperature Measurement

The IC can be configured to measure its own internal die temperature or an external NTC thermistor.

Set Config.TSEL = 0 (default) to enable die temperature measurement. Set Config.TSEL = 1 to enable thermistor measurement.

Thermistor conversions are initiated by periodically connecting the TH and BATT pins internally. Measurement results of TH pin are compared to the voltage of the BATT pin and converted to a ratiometric value from 0% to 100%. The active pullup is disabled when temperature measurements are complete. This reduces the current consumption.

The ratiometric results are converted to temperature using the temperature gain (TGain), temperature offset (TOff), and temperature curve (Curve) register values. Internal die temperature measurements are factory calibrated and are not affected by TGain, TOff, and Curve register settings. Refer to the *ModelGauge m5 EZ User Guide* for more details. Additionally, the IC maintains a record of the minimum and maximum temperature measured and an average temperature.

Temp Register (0x08)

Register Type: Temperature

The Temp register provides the temperature measured by the thermistor or die temperature based on the Conifg register setting.

MaxMinTemp Register (0x1A)

Register Type: Special

Initial Value: 0x807F

The MaxMinTemp register maintains the maximum and minimum Temp register (0x08) values since the last fuel-gauge reset or until cleared by host software. At power-up, the maximum value is set to 0x80 (most negative) and the minimum value is set to 0x7F(most positive). Therefore, both values are changed the Temp register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x807F. The maximum and minimum temperatures are each stored as two's complement 8-bit values with 1°C resolution. See the *Register Map* for format of the register.

DieTemp Register (0x34)

Register Type: Temperature

The DieTemp register provides the internal die temperature measurement. If Config.TSel = 0, DieTemp and Temp registers have the value of the die temperature.

Power Measurement

Power Register (0xB1)

Instant power calculation from immeidate current and voltage. The LSb is 1.6mW.

AvgPower Register (0xB3)

Filtered average power from the Power register. LSb is 1.6mW.

Alert Function

The Alert Threshold registers allow interrupts to be generated by detecting a high or low voltage, current, temperature, or state-of-charge. Interrupts are generated on the ALRT pin open-drain output driver. An external pullup is required to generate a logic-high signal. Alerts can be triggered by any of the following conditions:

- Battery removal: ($V_{TH} > V_{BATT}$ X V_{DET}) and battery removal detection enabled (Ber = 1).
- Battery insertion: ($V_{TH} < V_{BATT}$ X (V_{DET} - $V_{DET-HYS}$)) and battery insertion detection enabled (Bei = 1).
- Over/undervoltage: VAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/undertemperature: TAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/undercurrent: IAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- Over/under SOC: SAlrtTh register threshold violation (upper or lower) and alerts enabled (Aen = 1).
- 1% SOC change: RepSOC register bit d8 (1% bit) changed (dSOCen = 1).

To prevent false interrupts, the threshold registers should be initialized before setting the *Aen* bit. Alerts generated by battery insertion or removal can only be reset by clearing the corresponding bit in the *Status* (0x00) register. Alerts generated by a threshold-level violation can be configured to be cleared only by software, or cleared automatically when the threshold level is no longer violated. See the *Config* (1Dh) and *Config2* (BBh) register descriptions for details of the alert function configuration.

Serial Number Feature

Each IC provides a unique serial number ID. To read this serial number, clear the AtRateEn and the DPEn bit in the Config2 register. The 128-bit serial information overwrites the Dynamic Power and AtRate output registers. To continue Dynamic Power and AtRate operations after reading the serial number, the host should set Config2.AtRateEn and Config2.DPEn to 1.

Table 19. Serial Number Format

ADDRESS	Config2.AtRateEn = 1 || Config2.DPEn = 1	Config2.AtRateEn = 0 && Config2.DPEn = 0
0xD4	MaxPeakPower	Serial Number Word0

Table 19. Serial Number Format (continued)

0xD5	SusPeakPower	Serial Number Word1
0xD9	MPPCurrent	Serial Number Word2
0xDA	SPPCurrent	Serial Number Word3
0xDC	AtQResidual	Serial Number Word4
0xDD	AtTTE	Serial Number Word5
0xDE	AtAvSoc	Serial Number Word6
0xDF	AtAvCap	Serial Number Word7

ModelGauge m5 Memory Space

Registers that relate to functionality of the ModelGauge m5 fuel gauge are located on pages 0h-4h and are continued on pages Bh and Dh. See the ModelGauge m5 EZ Algorithm section for details of specific register operation. Register locations marked reserved should not be written to.

Table 20. ModelGauge m5 Register Memory Map

PAGE/WORD	00h	10h	20h	30h	40h	B0h	D0h
0h	Status	FullCapRep	TTF	Reserved	Reserved	Status2	RSense / UserMem3
1h	VAlrtTh	TTE	DevName	Reserved	Reserved	Power	ScOcvLim
2h	TAlrtTh	QRTable00	QRTable10	QRTable20	QRTable30	ID / UserMem2	VGain
3h	SAlrtTh	FullSocThr	FullCapNom	Reserved	RGain	AvgPower	SOCHold
4h	AtRate	RCell	Reserved	DieTemp	Reserved	IAlrtTh	MaxPeakPower
5h	RepCap	Reserved	Reserved	FullCap	dQAcc	TTFCfg	SusPeakPower
6h	RepSOC	AvgTA	Reserved	Reserved	dPAcc	CVMixCap	PackResistance
7h	Age	Cycles	AIN	Reserved	Reserved	CVHalfTime	SysResistance
8h	Temp	DesignCap	LearnCfg	RComp0	Reserved	CGTempCo	MinSysVoltage
9h	VCell	AvgVCell	FilterCfg	TempCo	ConvgCfg	Curve	MPPCurrent
Ah	Current	MaxMinTemp	RelaxCfg	VEmpty	VFRemCap	HibCfg	SPPCurrent
Bh	AvgCurrent	MaxMinVolt	MiscCfg	Reserved	Reserved	Config2	ModelCfg
Ch	QResidual	MaxMinCurr	TGain	Reserved	Reserved	VRipple	AtQResidual
Dh	MixSOC	Config	TOff	FStat	QH	RippleCfg	AtTTE
Eh	AvSOC	IChgTerm	CGain	Timer	Reserved	TimerH	AtAvSOC
Fh	MixCap	AvCap	COff	ShdnTimer	Reserved	Reserved	AtAvCap

Detailed Description—I²C Serial Communication

General Description

The IC features a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). This device acts as a slave-only device, relying on the master to generate a clock signal. SCL clock rates from 0Hz to 500kHz are supported.

I²C is an open-drain bus and therefore SDA and SCL require pullups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

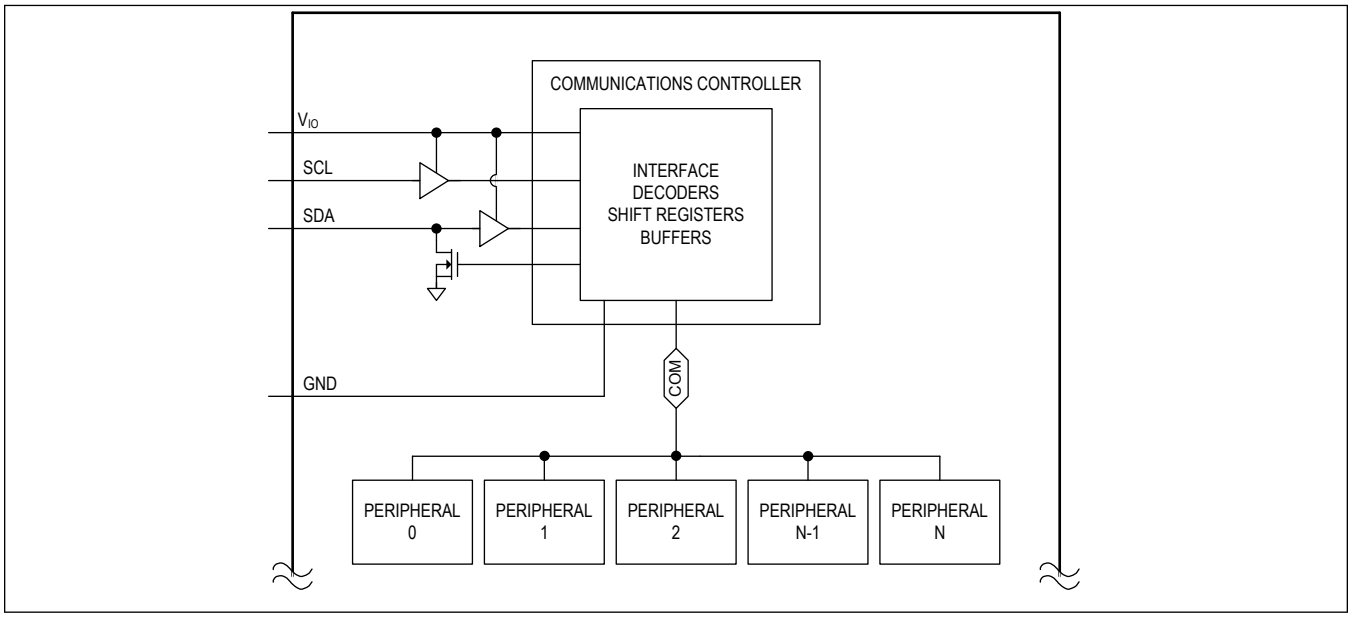
[[I²C Simplified Block Diagram]] shows the functional diagram for the I²C based communications controller. For additional information on I²C, refer to the *I²C Bus Specification and User Manual* which is available for free through the internet.

Features

- I2C Revision 3.0 Compatible Serial Communications Channel
- Compatible with any bus timing up to 400kHz
- Does not utilize I2C Clock Stretching

I2C Simplified Block Diagram

There are three pins (aside from GND) for the I2C-compatible interface. V_{IO} determines the logic level, SCL is the clock line, and SDA is the data line. Note that the interface does **not** have the ability to drive the SCL line.



I2C System Configuration

The I2C-compatible interface is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I2C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. The I2C-compatible interface operates as a slave on the I2C bus with transmit and receive capabilities.

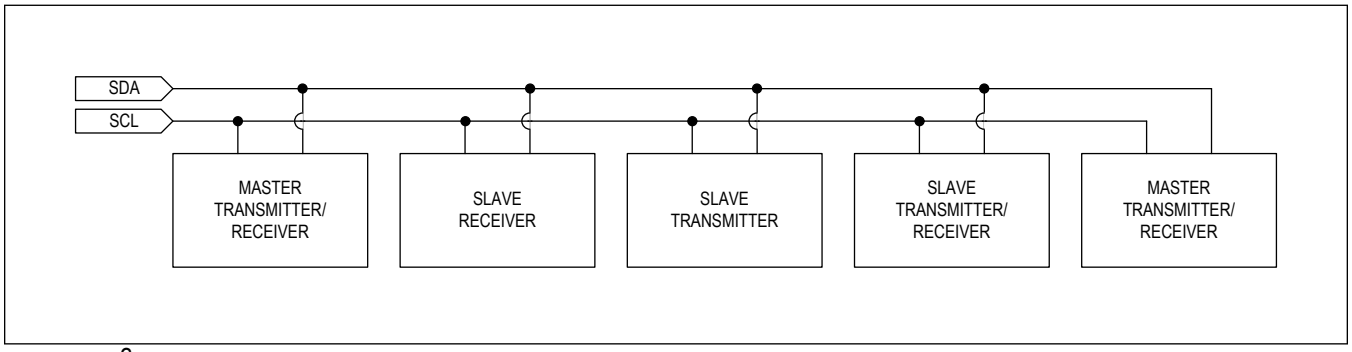


Figure 29. I2C System Configuration

I²C Interface Power

The I²C interface derives its power from V_{IO}. Typically a power input such as V_{IO} would require a local 0.1µF ceramic bypass capacitor to ground. However, in highly integrated power distribution systems, a dedicated capacitor might not be necessary. If the impedance between V_{IO} and the next closest capacitor (≥ 0.1µF) is less than 100mΩ in series with 10nH, then a local capacitor is not needed. Otherwise, bypass V_{IO} to GND with a 0.1µF ceramic capacitor.

V_{IO} accepts voltages from 1.7V to 3.6V (V_{IO}). Cycling V_{IO} does not reset the I²C registers. When V_{IO} is less than V_{IOUVLO} and V_{SYS} is less than $V_{SYSUVLO}$, SDA and SCL are high-impedance

I²C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals. See the *I²C Start and Stop Conditions* section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

I²C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See Figure 30.

A START condition from the master signals the beginning of a transmission to the device. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see the *I²C Acknowledge Bit* section for information on not-acknowledge). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general a repeated start command is functionally equivalent to a regular start command.

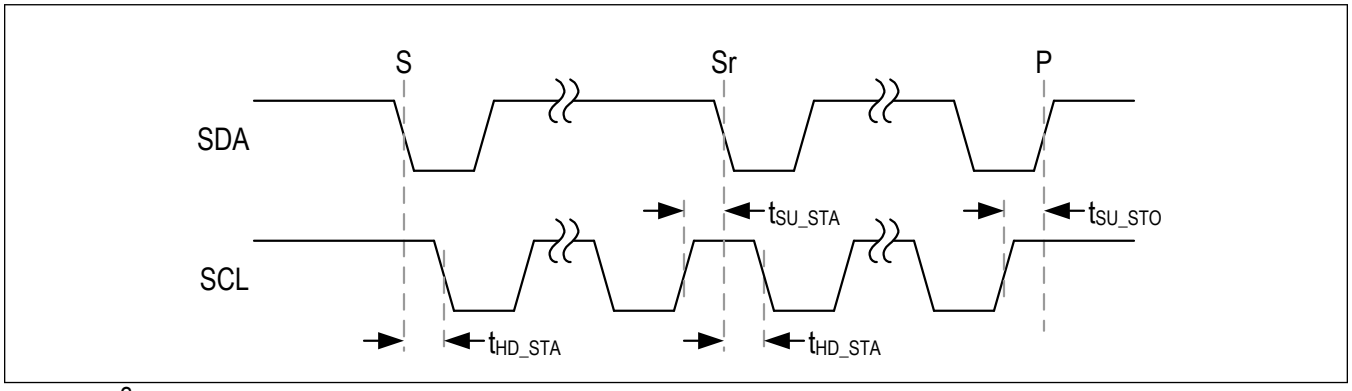


Figure 30. I²C Start and Stop Conditions

I²C Acknowledge Bit

Both the I²C bus master and slave devices generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See Figure 31. To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

This device issues an ACK for all register addresses in the possible address space even if the particular register does not exist.

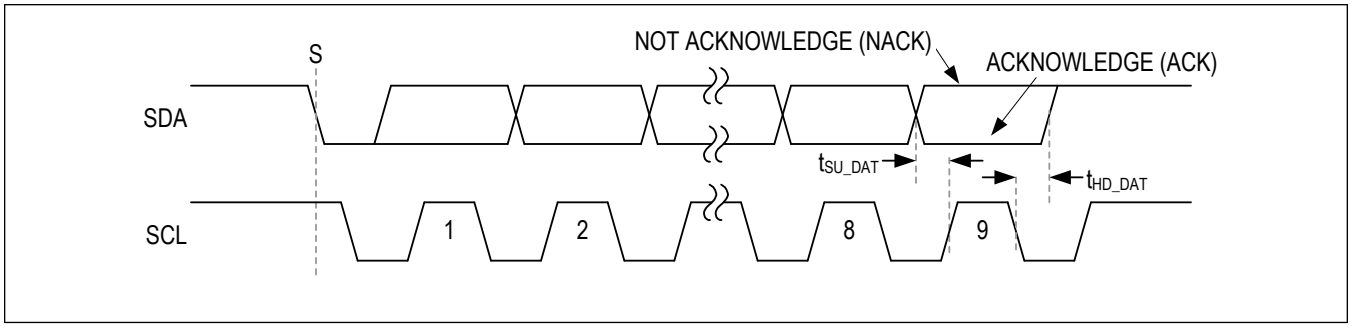


Figure 31. Acknowledge Bit

I²C Slave Address

The I²C controller implements 7-bit slave addressing. The registers of MAX77658 are divided into two blocks with separate slave addresses:

- The main block includes all the registers for the Global Resources, the Smart Selector Charger, the SIMO regulator, and the LDOs. All the registers in the main block are 8-bit registers.
- The fuel gauge block includes all the registers for the fuel gauging. The fuel gauge registers are in 16-bit word.

An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address. See Figure 32. The OTP main address is factory-programmable for one of two options. See Table 21. All slave addresses not mentioned in Table 21 are not acknowledged.

Table 21. I²C Slave Address Options

ADDRESS	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
Main Address (ADDR = 1)*	0x48, 0b 100 1000	0x90, 0b 1001 0000	0x91, 0b 1001 0001
Main Address (ADDR = 0)*	0x40, 0b 100 0000	0x80, 0b 1000 0000	0x81, 0b 1000 0001
Fuel Gauge Address	0x36, 0b 011 0110	0x6C, 0b 0110 1100	0x6D, 0b 0110 1101
Test Mode**	0x49, 0b 100 1001	0x92, 0b 1001 0010	0x93, 0b 1001 0011

*ADDR is a factory one-time programmable (OTP) option, allowing for address changes in the event of a bus conflict.

**When test mode is unlocked, the additional address is acknowledged. Test mode details are confidential. If possible, leave the test mode address unallocated to allow for the rare event that debugging needs to be performed in cooperation with Maxim.

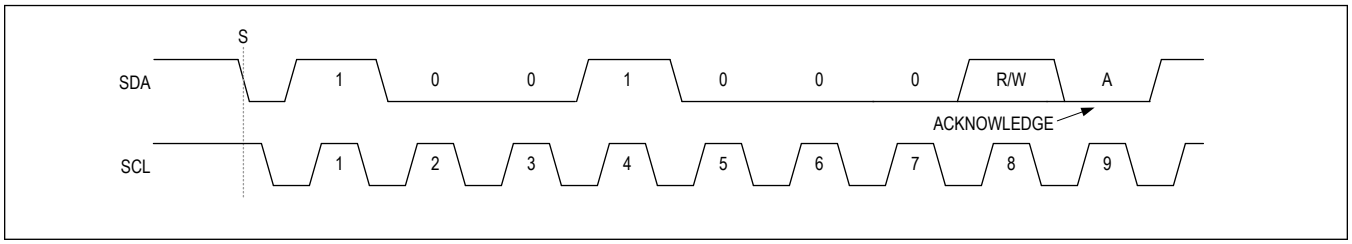


Figure 32. Slave Address Example

I²C Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold

down the clock line.

I²C General Call Address

This device does not implement the I²C specifications general call address and does not acknowledge the general call address (0b0000_0000).

I²C Device ID

This device does not support the I²C Device ID feature.

I²C Communication Speed

This device is compatible with any bus timing up to 400kHz. The main consideration when changing bus speed through this range is the combination of the bus capacitance and pullup resistors. Larger values of bus capacitance and pullup resistance increase the time constant (C x R), slowing bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the I²C bus specification and user manual (available for free on the internet) for detailed guidance on the pullup resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, and a 400kHz bus needs about 1.5kΩ pullup resistors. Remember that, while the open-drain bus is low, the pullup resistor is dissipating power, and lower value pullup resistors dissipate more power (V^2/R). Operating in high-speed mode requires some special considerations. For a full list of considerations, refer to the publicly available I²C bus specification and user manual. Major considerations with respect to this part are:

- The I²C bus master uses current source pullups to shorten the signal rise.
- The I²C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the bus input filters are set for standard mode, fast mode, and fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *I²C Communication Protocols* section.

I²C Communication Protocols

Both writing to and reading from registers are supported as described in the following subsections.

Writing to a Single 8-Bit Register

Figure 33 shows the protocol for the I²C master device to write one byte of data to this device. This protocol is the same as the SMBus specification's write byte protocol.

The write byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave updates with the new data.
8. The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

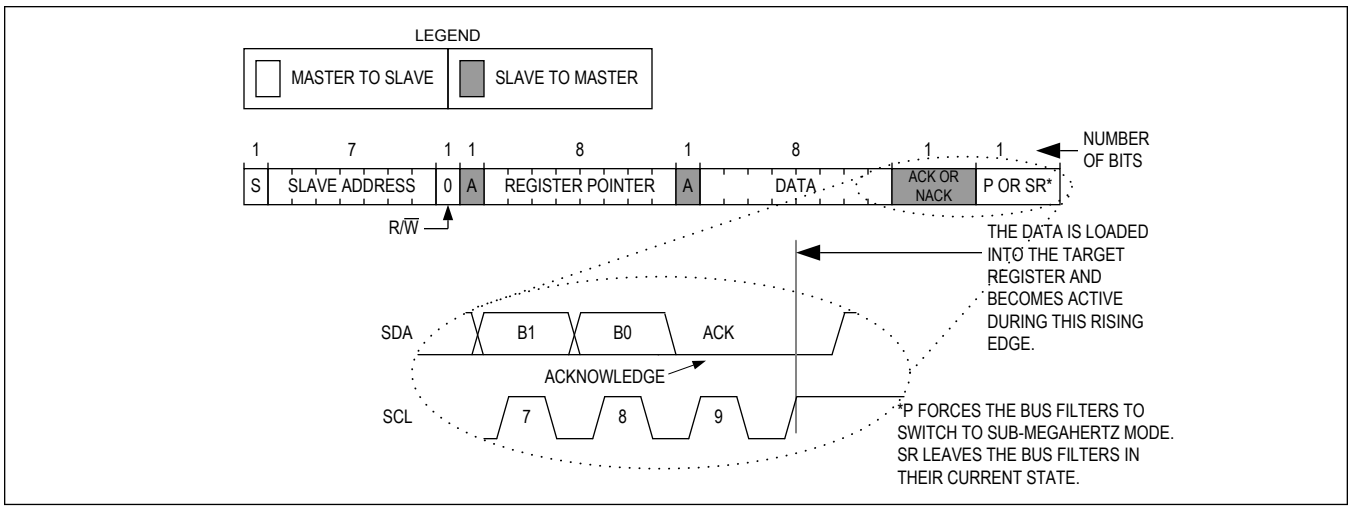


Figure 33. Writing to a Single 8-bit Register with the Write Byte Protocol

Writing Multiple Bytes to Sequential Registers

Figure 34 shows the protocol for writing to sequential registers. This protocol is similar to the write byte protocol above, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a stop or repeated start.

The writing to sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge related clock pulse, the master can issue an acknowledge or a not acknowledge.
10. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

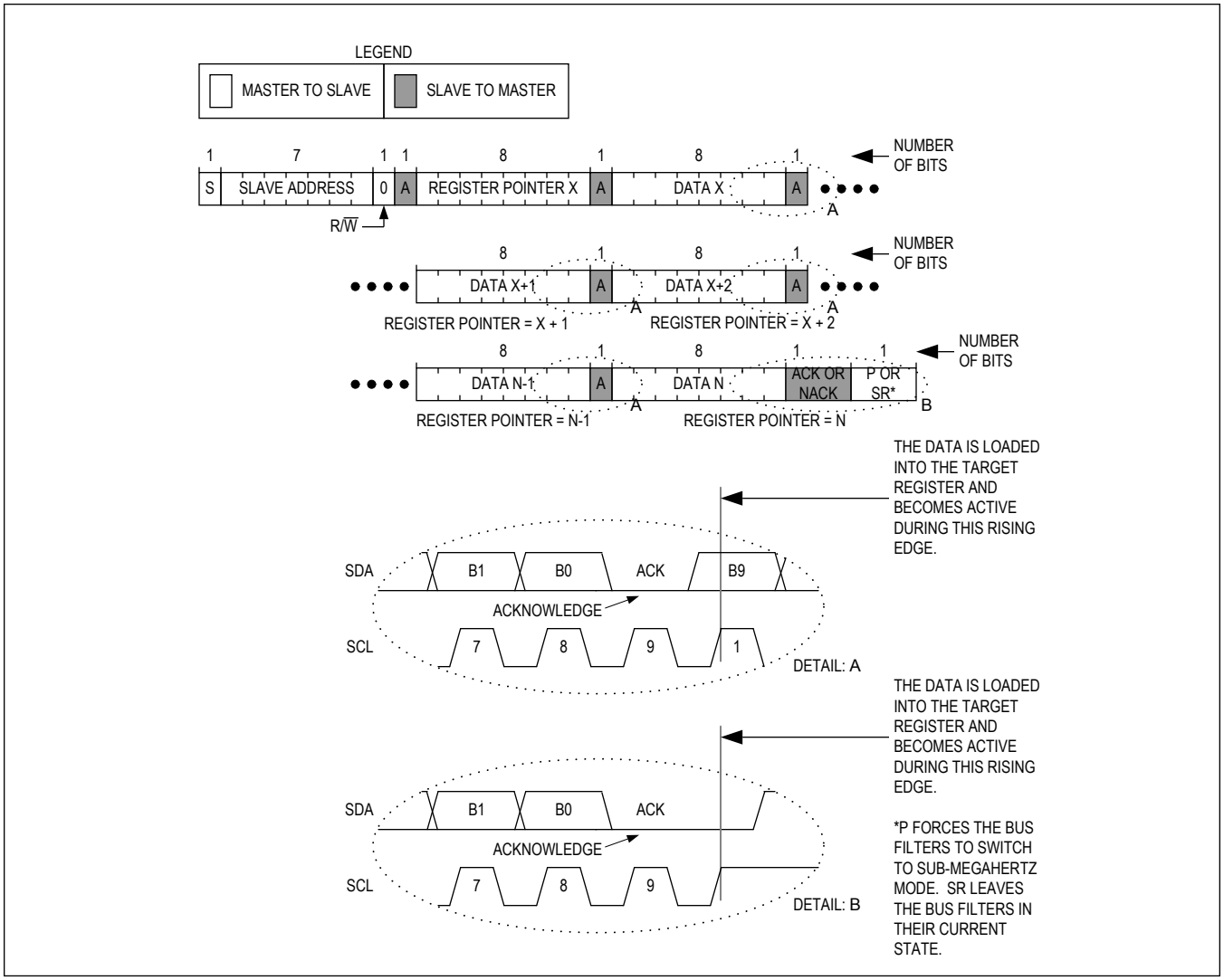


Figure 34. Writing to Sequential Registers X to N

Writing to 16-bit Registers

The Write Data protocol is used to transmit data to the registers of the fuel gauge at memory addresses from 00h to FFh. Addresses 00h to FFh can be written as a block. The memory address is sent by the bus master as a single byte value immediately after the slave address. The LSB of the data to be stored is written immediately after the memory address byte is acknowledged. Because the address is automatically incremented after the last bit of each 16-bit word received by the IC, the LSB of the data at the next memory address can be written immediately after the acknowledgment of the MSB of data at the previous address. The master indicates the end of a write transaction by sending a STOP or Repeated START after receiving the last acknowledge bit. If the bus master continues an auto-incremented write transaction beyond address FFh, the IC ignores the data. Data is also ignored on writes to read-only addresses but not reserved addresses. Do not write to reserved address locations. See [[Example I2C Write 16-bit Data Communication Sequence]] for an example Write Data communication sequence.

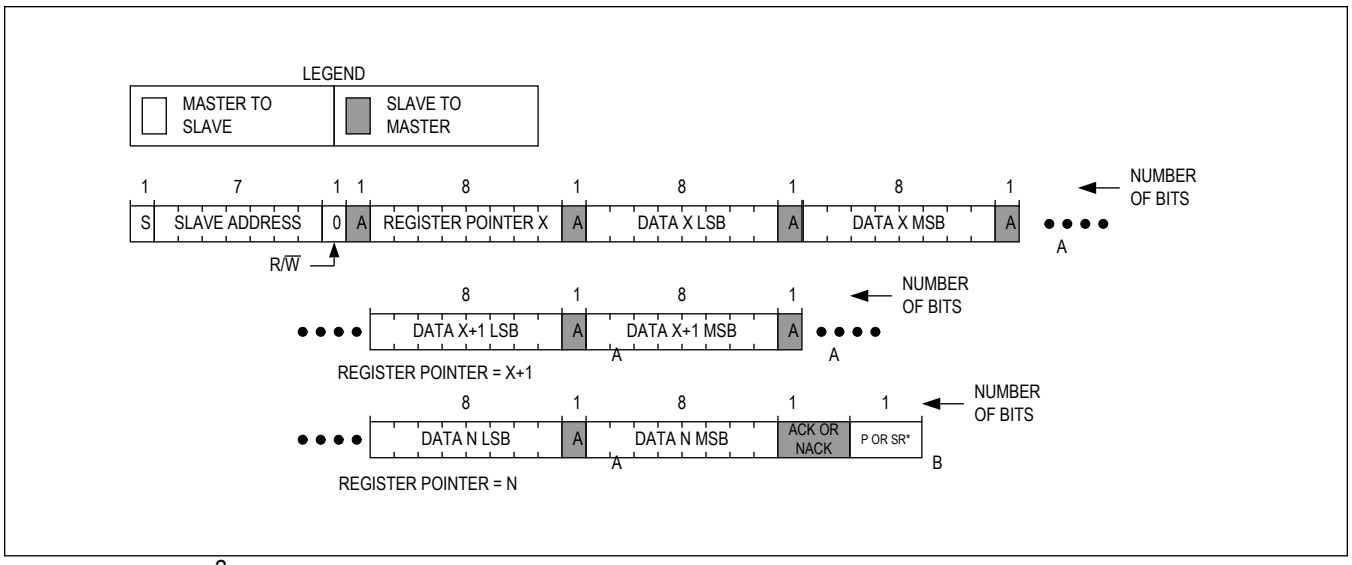


Figure 35. Example I²C Write 16-Bit Data Communication Sequence

Reading from a Single Register

Figure 36 shows the protocol for the I²C master device to read one byte of data. This protocol is the same as the SMBus specification's read byte protocol.

The read byte protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/W = 1).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues a not acknowledge (nA).
11. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop, the register pointer is not modified. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

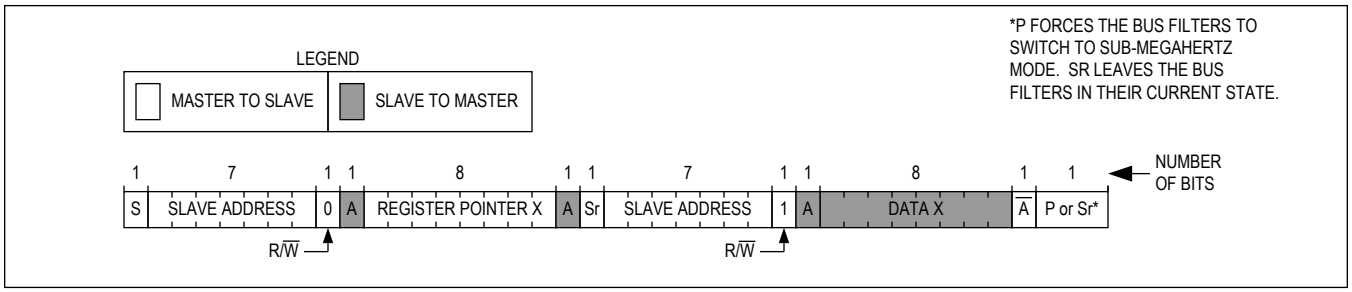


Figure 36. Reading from a Single Register with the Read Byte Protocol

Reading from Sequential Registers

Figure 37 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an acknowledge to signal the slave that it wants more data: when the master has all the data it requires it issues a not acknowledge (nA) and a stop (P) to end the transmission. The continuous read from sequential registers protocol is as follows:

1. The master sends a start command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated start command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/W = 1).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
12. The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop it does not modify its register pointer. Therefore, if the master re-reads the same register, it can immediately send another read command, omitting the command to send a register pointer.

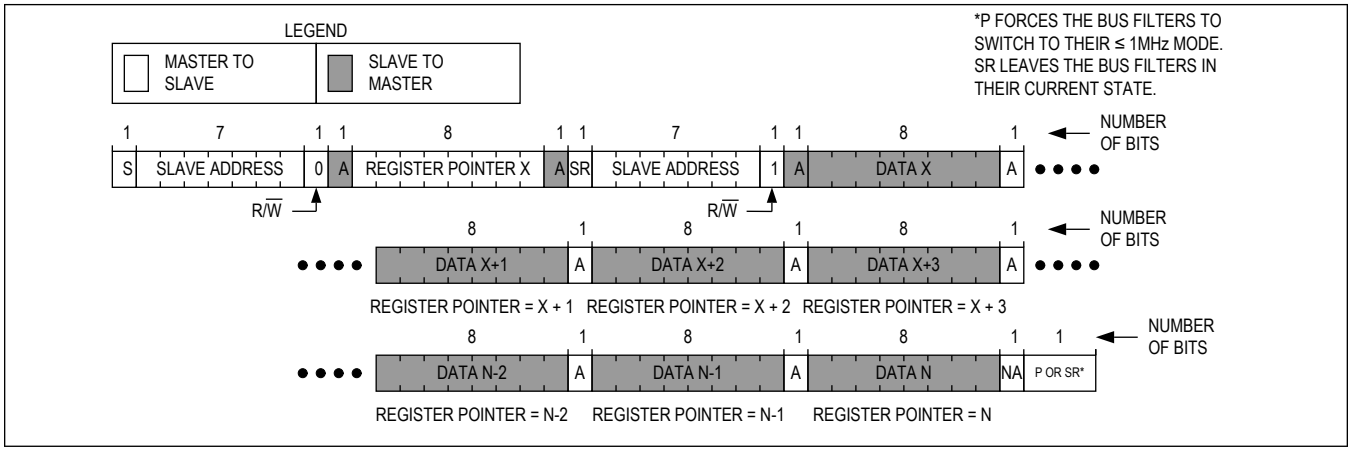


Figure 37. Reading Continuously from Sequential Registers X to N

Reading from 16-Bit Registers

The Read Data protocol is used to transmit data from memory locations of the fuel gauge registers 00h to FFh . The memory address is sent by the bus master as a single byte value immediately after the slave address. Immediately following the memory address, the bus master issues a REPEATED START followed by the slave address. The MAX77658 ACKs the address and begin transmitting data. A word of data is read as two separate bytes that the master must ACK. Because the address is automatically incremented after the final bit of each 16-bit word received by the IC, the LSB of the data at the next memory address can be read immediately after the acknowledgment of the MSB of data at the previous address. The master indicates the end of a read transaction by sending a NACK followed by a STOP. If the bus master continues an auto-incremented read transaction beyond memory address FFh, the IC transmits all 1s until a NACK or STOP is received. Data from reserved address locations is undefined. See [[Example I2C Read 16-bit Data Communication Sequence]] for an example Read Data communication sequence.

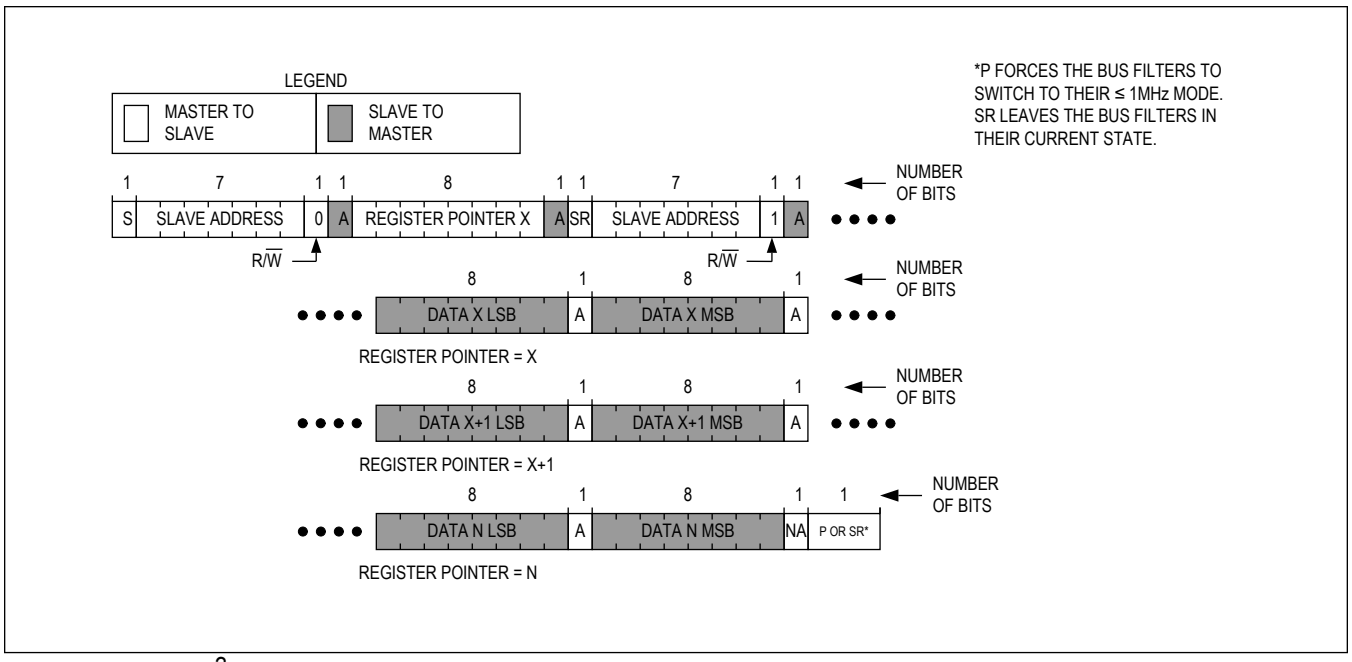


Figure 38. Example I²C Read 16-Bit Data Communication Sequence

Register Map

MAX77658

ADDRESS	NAME	MSB							LSB
Global									
0x00	INT_GLBL0[7:0]	DOD0_R	DOD1_R	TJAL2_R	TJAL1_R	nEN_R	nEN_F	GPI0_R	GPI0_F
0x04	INT_GLBL1[7:0]	RSVD	LDO1_F	LDO0_F	SBB2_F	SBB1_F	SBB0_F	GPI1_R	GPI1_F
0x05	ERCFLAG[7:0]	SBB_FAULT	EVT_WDT_SFT_23OR	SFT_CRST_F	SFT_OFF_F	MRST_F	SYSUVLO	SYSOVLO	TOVLD
0x06	STAT_GLBL[7:0]	DIDM	BOK	DOD0_S	DOD1_S	TJAL2_S	TJAL1_S	STAT_EN	STAT_IRQ
0x08	INTM_GLBL0[7:0]	DOD0_RM	DOD1_RM	TJAL2_RM	TJAL1_RM	nEN_RM	nEN_FM	GPI0_RM	GPI0_FM
0x09	INTM_GLBL1[7:0]	RSVD	LDO1_M	LDO0_M	SBB2_FM	SBB1_FM	SBB0_FM	GPI1_RM	GPI1_FM
0x10	CNFG_GLBL[7:0]	PU_DIS	T_MRST	SBIA_LPM	nEN_MODE[1:0]		DBEN_nEN	SFT_CTRL[1:0]	
0x11	CNFG_GPIO0[7:0]	SBB_F_SHUTDN	–	ALT_GPIO0	DBEN_GPI	DO	DRV	DI	DIR
0x12	CNFG_GPIO1[7:0]	RSVD[1:0]		ALT_GPIO1	DBEN_GPI	DO	DRV	DI	DIR
0x13	CNFG_GPIO2[7:0]	RSVD[1:0]		ALT_GPIO2	DBEN_GPI	DO	DRV	DI	DIR
0x14	CID[7:0]	–	–	–	CID[4:0]				
0x17	CNFG_WDT[7:0]	RSVD[1:0]		WDT_PER[1:0]		WDT_MODE	WDT_CLR	WDT_EN	WDT_LOCK
OVERLAP									
Charger									
0x01	INT_CHG[7:0]	RSVD	SYS_CNFG_I	SYS_CTRL_I	CHGIN_CTRL_I	TJ_REG_I	CHGIN_I	CHG_I	THM_I
0x02	STAT_CHG_A[7:0]	RSVD	VCHGIN_MIN_STAT	ICHGIN_LIM_STAT	VSYS_MIN_STAT	TJ_REG_STAT	THM_DTLS[2:0]		
0x03	STAT_CHG_B[7:0]	CHG_DTLS[3:0]				CHGIN_DTLS[1:0]		CHG	TIME_SUS
0x07	INT_M_CHG[7:0]	DIS_AICL	SYS_CNFG_M	SYS_CTRL_M	CHGIN_CTRL_M	TJ_REG_M	CHGIN_M	CHG_M	THM_M
0x20	CNFG_CHG_A[7:0]	THM_HOT[1:0]		THM_WARM[1:0]		THM_COOL[1:0]		THM_COLD[1:0]	
0x21	CNFG_CHG_B[7:0]	VCHGIN_MIN[2:0]			ICHGIN_LIM[2:0]			I_PQ	CHG_EN
0x22	CNFG_CHG_C[7:0]	CHG_PQ[2:0]			I_TERM[1:0]		T_TOPOFF[2:0]		
0x23	CNFG_CHG_D[7:0]	TJ_REG[2:0]			VSYS_REG[4:0]				
0x24	CNFG_CHG_E[7:0]	CHG_CC[5:0]						T_FAST_CHG[1:0]	
0x25	CNFG_CHG_F[7:0]	CHG_CC_JEITA[5:0]						RSVD	–
0x26	CNFG_CHG_G[7:0]	CHG_CV[5:0]						USBS	FUS_M
0x27	CNFG_CHG_H[7:0]	CHG_CV_JEITA[5:0]						SYS_BAT_PRT	CHR_TH_EN

ADDRESS	NAME	MSB							LSB
0x28	CNFG_CHG_I[7:0]	IMON_DISCHG_SCALE[3:0]				MUX_SEL[3:0]			
SBB									
0x38	CNFG_SBB_TOP[7:0]	DIS_LPM	IPK_1P5A	–	–	–	–	DRV_SBB[1:0]	
0x39	CNFG_SBB0_A[7:0]	TV_SBB0[7:0]							
0x3A	CNFG_SBB0_B[7:0]	OP_MODE[1:0]		IP_SBB0[1:0]		ADE_SBB0	EN_SBB0[2:0]		
0x3B	CNFG_SBB1_A[7:0]	TV_SBB1[7:0]							
0x3C	CNFG_SBB1_B[7:0]	OP_MODE[1:0]		IP_SBB1[1:0]		ADE_SBB1	EN_SBB1[2:0]		
0x3D	CNFG_SBB2_A[7:0]	TV_SBB2[7:0]							
0x3E	CNFG_SBB2_B[7:0]	OP_MODE[1:0]		IP_SBB2[1:0]		ADE_SBB2	EN_SBB2[2:0]		
0x3F	CNFG_DVS_SBB0_A[7:0]	TV_SBB0_DVS[7:0]							
LDO									
0x48	CNFG_LDO0_A[7:0]	TV_OFS_LDO0	TV_LDO0[6:0]						
0x49	CNFG_LDO0_B[7:0]	–	–	–	LDO0_MD	ADE_LDO0	EN_LDO0[2:0]		
0x4A	CNFG_LDO1_A[7:0]	TV_OFS_LDO1	TV_LDO1[6:0]						
0x4B	CNFG_LDO1_B[7:0]	–	–	–	LDO1_MD	ADE_LDO1	EN_LDO1[2:0]		

Register Details

INT_GLBL0 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	DOD0_R	DOD1_R	TJAL2_R	TJAL1_R	nEN_R	nEN_F	GPI0_R	GPI0_F
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
DOD0_R	7	LDO Dropout Detector Rising Interrupt	0 = The LDO has not detected dropout since the last time this bit was read. 1 = The LDO has detected dropout since the last time this bit was read.
DOD1_R	6	LDO Dropout Detector Rising Interrupt	0 = The LDO has not detected dropout since the last time this bit was read. 1 = The LDO has detected dropout since the last time this bit was read.
TJAL2_R	5	Thermal Alarm 2 Rising Interrupt	0 = The junction temperature has not risen above TJAL2 since the last time this bit was read. 1 = The junction temperature has risen above TJAL2 since the last time this bit was read.

BITFIELD	BITS	DESCRIPTION	DECODE
TJAL1_R	4	Thermal Alarm 1 Rising Interrupt	0 = The junction temperature has not risen above TJAL1 since the last time this bit was read. 1 = The junction temperature has risen above TJAL1 since the last time this bit was read.
nEN_R	3	nEN Rising Interrupt	0 = No nEN rising edges have occurred since the last time this bit was read. 1 = A nEN rising edge has occurred since the last time this bit was read.
nEN_F	2	nEN Falling Interrupt	0 = No nEN falling edges have occurred since the last time this bit was read. 1 = A nEN falling edge occurred since the last time this bit was read.
GPI0_R	1	GPI Rising Interrupt Note that "GPI" refers to the GPIO programmed to be an input.	0 = No GPI rising edges have occurred since the last time this bit was read. 1 = A GPI rising edge has occurred since the last time this bit was read.
GPI0_F	0	GPI Falling Interrupt Note that the GPI is the GPIO programmed to be an input.	0 = No GPI falling edges have occurred since the last time this bit was read. 1 = A GPI falling edge has occurred since the last time this bit was read.

INT_GLBL1 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	LDO1_F	LDO0_F	SBB2_F	SBB1_F	SBB0_F	GPI1_R	GPI1_F
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.	
LDO1_F	6	LDO1 Fault Interrupt	0 = No fault has occurred on LDO1 since the last time this bit was read. 1 = LDO1 has fallen out of regulation since the last time this bit was read.
LDO0_F	5	LDO0 Fault Interrupt	0 = No fault has occurred on LDO0 since the last time this bit was read. 1 = LDO0 has fallen out of regulation since the last time this bit was read.
SBB2_F	4	SBB2 Fault Indicator	0b0 = No fault has occurred on SBB2 since the last time this bit was read. 0b1 = SBB2 has fallen out of regulation since the last time this bit was read.
SBB1_F	3	SBB1 Fault Indicator	0b0 = No fault has occurred on SBB1 since the last time this bit was read. 0b1 = SBB1 has fallen out of regulation since the last time this bit was read.
SBB0_F	2	SBB0 Fault Indicator	0b0 = No fault has occurred on SBB0 since the last time this bit was read. 0b1 = SBB0 has fallen out of regulation since the last time this bit was read.

BITFIELD	BITS	DESCRIPTION	DECODE
GPI1_R	1	GPI Rising Interrupt Note that "GPI" refers to the GPIO programmed to be an input.	0 = No GPI rising edges have occurred since the last time this bit was read. 1 = A GPI rising edge has occurred since the last time this bit was read.
GPI1_F	0	GPI Falling Interrupt Note that the GPI is the GPIO programmed to be an input.	0 = No GPI falling edges have occurred since the last time this bit was read. 1 = A GPI falling edge has occurred since the last time this bit was read.

ERCFLAG (0x05)

BIT	7	6	5	4	3	2	1	0
Field	SBB_FAULT	EVT_WDT_SFT_23OR	SFT_CRST_F	SFT_OFF_F	MRST_F	SYSUVLO	SYSOVLO	TOVLD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
SBB_FAULT	7	SBB Fault Shutdownflag	0 = No shutdown event has occurred from SBB fault since the last time this bit was read. 1 = A shutdown event has occurred from SBB fault since the last time this bit was read.
EVT_WDT_SFT_23OR	6	Watchdog Timer Expired Flag. This bit sets when the watchdog timer expires and causes a power-off (WDT_MODE = 0) or a power-reset (WDT_MODE = 1).	0 = Watchdog timer has not expired since the last time this bit was read. 1 = Watchdog timer has expired since the last time this bit was read.
SFT_CRST_F	5	Software Cold Reset Flag	0 = The software cold reset has not occurred since the last read of this register. 1 = The software cold reset has occurred since the last read of this register. This indicates that software has set SFT_CTRL[1:0] = 0b01.
SFT_OFF_F	4	Software OFF Flag	0 = The SFT_OFF function has not occurred since the last read of this register. 1 = The SFT_OFF function has occurred since the last read of this register. This indicates that software has set SFT_CTRL[1:0] = 0b10.
MRST_F	3	Manual Reset Timer	0 = A manual reset has not occurred since the last read of this register. 1 = A manual reset has occurred since the last read of this register.
SYSUVLO	2	SYS Domain Undervoltage Lockout	0 = The SYS domain undervoltage lockout has not occurred since the last read of this register. 1 = The SYS domain undervoltage lockout has occurred since the last read of this register. This indicates that the SYS domain voltage fell below $V_{SYSUVLO}$ (~2.6V)
SYSOVLO	1	SYS Domain Overvoltage Lockout	0 = The SYS domain overvoltage lockout has not occurred since the last read of this register. 1 = The SYS domain overvoltage lockout has occurred since the last read of this register. This indicates that the SYS domain voltage rose below $V_{SYSOVLO}$ (~5.85V)

BITFIELD	BITS	DESCRIPTION	DECODE
TOVLD	0	Thermal Overload	0 = Thermal overload has not occurred since the last read of this register. 1 = Thermal overload has occurred since the last read of this register. This indicates that the junction temperature has exceeded 145ºC.

STAT_GLBL (0x06)

BIT	7	6	5	4	3	2	1	0
Field	DIDM	BOK	DOD0_S	DOD1_S	TJAL2_S	TJAL1_S	STAT_EN	STAT_IRQ
Reset	OTP	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
DIDM	7	Device Identification Bits for Metal Options	0 = MAX77658 1 = Reserved
BOK	6	BOK Interrupt Status	0 = Main bias is not ready. 1 = Main bias enabled and ready.
DOD0_S	5	LDO0 Dropout Detector Rising Status	0 = LDO0 is not in dropout. 1 = LDO0 is in dropout.
DOD1_S	4	LDO1 Dropout Detector Rising Status	0 = LDO1 is not in dropout. 1 = LDO1 is in dropout.
TJAL2_S	3	Thermal Alarm 2 Status	0 = The junction temperature is less than TJA2. 1 = The junction temperature is greater than TJAL2.
TJAL1_S	2	Thermal Alarm 1 Status	0 = The junction temperature is less than TJAL1. 1 = The junction temperature is greater than TJAL1.
STAT_EN	1	Debounced Status for the nEN Input	0 = nEN is not active (logic-high). 1 = nEN is active (logic-low).
STAT_IRQ	0	Software Version of the nIRQ MOSFET Gate Drive	0 = Unmasked gate drive is logic-low. 1 = Unmasked gate drive is logic-high.

INTM_GLBL0 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	DOD0_RM	DOD1_RM	TJAL2_RM	TJAL1_RM	nEN_RM	nEN_FM	GPI0_RM	GPI0_FM
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DOD0_RM	7	LDO Dropout Detector Rising Interrupt Mask	0 = Unmasked. If DOD0_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to DOD0_R.

BITFIELD	BITS	DESCRIPTION	DECODE
DOD1_RM	6	LDO Dropout Detector Rising Interrupt Mask	0 = Unmasked. If DOD1_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to DOD1_R.
TJAL2_RM	5	Thermal Alarm 2 Rising Interrupt Mask	0 = Unmasked. If TJAL2_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to TJAL2_R.
TJAL1_RM	4	Thermal Alarm 1 Rising Interrupt Mask	0 = Unmasked. If TJAL1_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to TJAL1_R.
nEN_RM	3	nEN Rising Interrupt Mask	0 = Unmasked. If nEN_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to nEN_R.
nEN_FM	2	nEN Falling Interrupt Mask	0 = Unmasked. If nEN_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to nEN_F.
GPI0_RM	1	GPI Rising Interrupt Mask	0 = Unmasked. If GPI_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to GPI_R.
GPI0_FM	0	GPI Falling Interrupt Mask	0 = Unmasked. If GPI_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to GPI_F.

INTM_GLBL1 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	LDO1_M	LDO0_M	SBB2_FM	SBB1_FM	SBB0_FM	GPI1_RM	GPI1_FM
Reset	0b0	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.	
LDO1_M	6	LDO1 Fault Interrupt Mask	0 = Unmasked. If LDO1_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to LDO1_F.
LDO0_M	5	LDO0 Fault Interrupt Mask	0 = Unmasked. If LDO0_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to LDO0_F.

BITFIELD	BITS	DESCRIPTION	DECODE
SBB2_FM	4	SBB2 Fault Interrupt Mask	0b0 = Unmasked. If SBB2_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to SBB2_F.
SBB1_FM	3	SBB1 Fault Interrupt Mask	0b0= Unmasked. If SBB1_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to SBB1_F.
SBB0_FM	2	SBB0 Fault Interrupt Mask	0b0 = Unmasked. If SBB0_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 0b1 = Masked. nIRQ does not go low due to SBB0_F.
GPI1_RM	1	GPI Rising Interrupt Mask	0 = Unmasked. If GPI_R goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to GPI_R.
GPI1_FM	0	GPI Falling Interrupt Mask	0 = Unmasked. If GPI_F goes from 0 to 1, then nIRQ goes low. nIRQ goes high when all interrupt bits are cleared. 1 = Masked. nIRQ does not go low due to GPI_F.

CNFG_GLBL (0x10)

BIT	7	6	5	4	3	2	1	0
Field	PU_DIS	T_MRST	SBIA_LPM	nEN_MODE[1:0]		DBEN_nEN	SFT_CTRL[1:0]	
Reset	0b0	OTP	OTP	OTP		OTP	0b00	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
PU_DIS	7	nEN Internal Pullup Resistor	0 = Strong internal nEN pullup (200kΩ) 1 = Weak internal nEN pullup (10MΩ)
T_MRST	6	Sets the Manual Reset Time (t_{MRST})	0 = 8s 1 = 4s
SBIA_LPM	5	Main Bias Low-Power Mode Software Request	0 = Main bias requested to be in normal-power mode by software. 1 = Main bias request to be in low-power mode by software.
nEN_MODE	4:3	nEN Input (ON-KEY) Default Configuration Mode	0b00 = Push-button mode 0b01 = Slide-switch mode 0b10 = Logic mode 0b11 = Reserved
DBEN_nEN	2	Debounce Timer Enable for the nEN Pin	0 = 500µs Debounce 1 = 30ms Debounce

BITFIELD	BITS	DESCRIPTION	DECODE
SFT_CTRL	1:0	Software Reset Functions Note that the SFT_CRST and SFT_OFF commands initiate the power-down sequence flow as described in the data sheet. This power-down sequence flow has delay elements that add up to 205.24ms (60ms delay + 10.24ms nRST assert delay + 4x2.56ms power-down slot delays + 125ms output discharge delay). If issuing the SFT_CRST and/or SFT_OFF functions in software, wait for more than 300ms before trying to issue any additional commands through I2C.	0b00 = No action 0b01 = Software cold reset (SFT_CRST). The device powers down, resets, and then powers up again. 0b10 = Software off (SFT_OFF). The device powers down, resets, and then remains off and waiting for a wake-up event. 0b11 = Factory-ship mode enter (FSM). The IC powers down, configuration registers reset, and the internal BATT to SYS switch opens. The device remains this way until a factory-ship mode exit event occurs.

CNFG_GPIO0 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	SBB_F_SHUTDN	–	ALT_GPIO0	DBEN_GPI	DO	DRV	DI	DIR
Reset	OTP	–	OTP	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SBB_F_SHUTDN	7	SBB Shutdown from SBB Fault	0b0 = The SBB regulator does not shut off when an SBB fault occurs 0b1 = The SBB regulator powers down sequentially when an SBB fault occurs
ALT_GPIO0	5	Alternate Mode Enable for GPIO0	0 = Standard GPIO. 1 = Active-high input, Force USB Suspend (FUS). FUS is only active if the FUS_M bit is set to 0.
DBEN_GPI	4	General Purpose Input Debounce Timer Enable for GPI0	0 = No debounce 1 = 30ms Debounce
DO	3	General Purpose Output Data Output for GPO0	This bit is a don't care when DIR = 1 (configured as input). When set for GPO (DIR = 0): 0 = GPIO is output logic low. 1 = GPIO is output logic high when set as push-pull output (DRV = 1). GPIO is high-impedance when set as an open-drain output (DRV = 0).
DRV	2	General Purpose Output Driver Type for GPO0	This bit is a don't care when DIR = 1 (configured as input). When set for GPO (DIR = 0): 0 = Open-drain 1 = Push-pull
DI	1	GPIO Digital Input Value for GPI0. Irrespective of whether the GPIO is set for GPI (DIR = 1) or GPO (DIR = 0), DI reflects the state of the GPIO.	0 = Input logic-low 1 = Input logic-high
DIR	0	GPIO Direction for GPIO0	0 = General purpose output (GPO) 1 = General purpose input (GPI)

CNFG_GPIO1 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		ALT_GPIO1	DBEN_GPI	DO	DRV	DI	DIR
Reset	0b00		OTP	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	Reserved. Unutilized bit. Write to 0. Reads are don't care.	
ALT_GPIO1	5	Alternate Mode Enable for GPIO1	Alternate Mode Enable for GPIO1 0b0 = SBB0 is set by TV_SBB0 1b0 = SBB0 is set by TV_SBB0_DVS
DBEN_GPI	4	General Purpose Input Debounce Timer Enable for GPI1	0 = No debounce 1 = 30ms Debounce
DO	3	General Purpose Output Data Output for GPO1	This bit is a don't care when DIR = 1 (configured as input). When set for GPO (DIR = 0): 0 = GPIO is output logic low. 1 = GPIO is output logic high when set as push-pull output (DRV = 1). GPIO is high-impedance when set as an open-drain output (DRV = 0).
DRV	2	General Purpose Output Driver Type for GPO1	This bit is a don't care when DIR = 1 (configured as input). When set for GPO (DIR = 0): 0 = Open-drain 1 = Push-pull
DI	1	GPIO Digital Input Value for GPI1. Irrespective of whether the GPIO is set for GPI (DIR = 1) or GPO (DIR = 0), DI reflects the state of the GPIO.	0 = Input logic-low 1 = Input logic-high
DIR	0	GPIO Direction for GPIO1	0 = General purpose output (GPO) 1 = General purpose input (GPI)

CNFG_GPIO2 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		ALT_GPIO2	DBEN_GPI	DO	DRV	DI	DIR
Reset	0b00		OTP	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Read Only	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	Reserved. Unutilized bit. Write to 0. Reads are don't care.	
ALT_GPIO2	5	Alternate Mode Enable for GPIO2.	0 = Standard GPIO 1 = Active-high input, Enable DISQBAT.
DBEN_GPI	4	General Purpose Input Debounce Timer Enable for GPI2	0 = No debounce 1 = 30ms Debounce

BITFIELD	BITS	DESCRIPTION	DECODE
DO	3	General Purpose Output Data Output for GPO2	This bit is a don't care when DIR = 1 (configured as input). When set for GPO (DIR = 0): 0 = GPIO is output logic low. 1 = GPIO is output logic high when set as push-pull output (DRV = 1). GPIO is high-impedance when set as an open-drain output (DRV = 0).
DRV	2	General Purpose Output Driver Type for GPO2	This bit is a don't care when DIR = 1 (configured as input). When set for GPO (DIR = 0): 0 = Open-drain 1 = Push-pull
DI	1	GPIO Digital Input Value for GPI2. Irrespective of whether the GPIO is set for GPI (DIR = 1) or GPO (DIR = 0), DI reflects the state of the GPIO.	0 = Input logic-low 1 = Input logic-high
DIR	0	GPIO Direction for GPIO2	0 = General purpose output (GPO) 1 = General purpose input (GPI)

CID (0x14)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	CID[4:0]				
Reset	–	–	–	OTP				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
CID	4:0	Chip Identification Code The chip identification code refers to a set of reset values in the register map, or the "OTP configuration."

CNFG_WDT (0x17)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[1:0]		WDT_PER[1:0]		WDT_MODE	WDT_CLR	WDT_EN	WDT_LOCK
Reset	0b00		0b11		0b0	0b0	OTP	OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7:6	Reserved. Unutilized bit. Write to 0. Reads are don't care.	
WDT_PER	5:4	Watchdog Timer Period. Sets t_{WD}. Watchdog timer is reset to the programmed value as soon as this bitfield is changed.	0b00 = 16 seconds 0b01 = 32 seconds 0b10 = 64 seconds 0b11 = 128 seconds

BITFIELD	BITS	DESCRIPTION	DECODE
WDT_MODE	3	Watchdog Timer Expired Action. Determines what the IC does after the watchdog timer expires.	0 = Watchdog timer expire causes power-off. 1 = Watchdog timer expire causes power-reset.
WDT_CLR	2	Watchdog Timer Clear Control. Set this bit to feed (reset) the watchdog timer.	0 = Watchdog timer period is not reset. 1 = Watchdog timer is reset back to t_{WD}.
WDT_EN	1	Watchdog Timer Enable. Write protected depending on WDT_LOCK.	0 = Watchdog timer is not enabled. 1 = Watchdog timer is enabled. The timer expires if not reset by setting WDT_CLR.
WDT_LOCK	0	Factory-Set Safety Bit for the Watchdog Timer. Determines if the timer can be disabled through WDT_EN or not.	0 = Watchdog timer can be enabled and disabled with WDT_EN. 1 = Watchdog timer can not be disabled with WDT_EN. However, WDT_EN can still be used to enable the watchdog timer.

INT_CHG (0x01)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	SYS_CNFG_I	SYS_CTRL_I	CHGIN_CTRL_I	TJ_REG_I	CHGIN_I	CHG_I	THM_I
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.	
SYS_CNFG_I	6	System Voltage Configuration Error Interrupt	0 = The bit combination in CHG_CV has not been forced to change since the last time this bit was read. 1 = The bit combination in CHG_CV has been forced to change to ensure $V_{SYS-REG} = V_{FAST-CHG}$ + 200mV since the last time this bit was read.
SYS_CTRL_I	5	Minimum System Voltage Regulation-Loop Related Interrupt. This interrupt signals a change in the status bit VSYS_MIN_STAT.	0 = The minimum system voltage regulation loop has not engaged since the last time this bit was read. 1 = The minimum system voltage regulation loop has engaged since the last time this bit was read.
CHGIN_CTRL_I	4	CHGIN Control-Loop Related Interrupt. This bit asserts when the input reaches current limit ($I_{CHGIN-LIM}$) or V_{CHGIN} falls below V_{CHGIN_MIN}.	0 = Neither the VCHGIN_MIN_STAT nor the ICHGIN_LIM_STAT bits have changed since the last time this bit was read. 1 = The VCHGIN_MIN_STAT or ICHGIN_LIM_STAT bits have changed since the last time this bit was read.
TJ_REG_I	3	Die Junction Temperature Regulation Interrupt. This bit asserts when the die temperature (T_J) exceeds T_{J-REG}. This interrupt signals a change in the status bit TJ_REG_STAT.	0 = The die temperature has not exceeded T_{J-REG} since the last time this bit was read. 1 = The die temperature has exceeded T_{J-REG} since the last time this bit was read.
CHGIN_I	2	CHGIN Related Interrupt	0 = The bits in CHGIN_DTLS[1:0] have not changed since the last time this bit was read. 1 = The bits in CHGIN_DTLS[1:0] have changed since the last time this bit was read.

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_I	1	Charger Related Interrupt	0 = The bits in CHG_DTLS[3:0] have not changed since the last time this bit was read. 1 = The bits in CHG_DTLS[3:0] have changed since the last time this bit was read.
THM_I	0	Thermistor Related Interrupt	0 = The bits in THM_DTLS[2:0] have not changed since the last time this bit was read. 1 = The bits in THM_DTLS[2:0] have changed since the last time this bit was read.

STAT_CHG_A (0x02)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	VCHGIN_MIN_STAT	ICHGIN_LIM_STAT	VSYS_MIN_STAT	TJ_REG_STAT	THM_DTLS[2:0]		
Reset	0b0	0b0	0b0	0b0	0b0	0b000		
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.	
VCHGIN_MIN_STAT	6	Minimum Input Voltage Regulation Loop Status	0 = The minimum CHGIN voltage regulation loop is not engaged. 1 = The minimum CHGIN voltage regulation loop has engaged to regulate $V_{CHGIN} \geq V_{CHGIN-MIN}$.
ICHGIN_LIM_STAT	5	Input Current Limit Loop Status	0 = The CHGIN current limit loop is not engaged. 1 = The CHGIN current limit loop has engaged to regulate $I_{CHGIN} \leq I_{CHGIN-LIM}$.
VSYS_MIN_STAT	4	Minimum System Voltage Regulation Loop Status	0 = The minimum system voltage regulation loop is not enganged. 1 = The minimum system voltage regulation loop is engaged to regulate $V_{SYS} \geq V_{SYS-MIN}$.
TJ_REG_STAT	3	Maximum Junction Temperature Regulation Loop Status	0 = The maximum junction temperature regulation loop is not engaged. 1 = The maximum junction temperature regulation loop has engaged to regulate the junction temperature to less than T_{J-REG}.
THM_DTLS	2:0	Battery Temperature Details. Valid only when CHGIN_DTLS[1:0] = 0b11.	0b000 = Thermistor is disabled (Config.TSel = 0). 0b001 = Battery is cold as programmed by THM_COLD[1:0]. If thermistor and charger are enabled while the battery is cold, a battery temperature fault occurs. 0b010 = Battery is cool as programmed by THM_COOL[1:0]. 0b011 = Battery is warm as programmed by THM_WARM[1:0]. 0b100 = Battery is hot as programmed by THM_HOT[1:0]. If thermistor and charger are enabled while the battery is hot, a battery temperature fault occurs. 0b101 = Battery is in the normal temperature region. 0b110 to 0b111 = Reserved.

STAT_CHG_B (0x03)

BIT	7	6	5	4	3	2	1	0
Field	CHG_DTLS[3:0]				CHGIN_DTLS[1:0]		CHG	TIME_SUS
Reset	0x0				0b00		0b0	0b0
Access Type	Read Only				Read Only		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_DTLS	7:4	Charger Details	0b0000 = Off 0b0001 = Prequalification mode. 0b0010 = Fast-charge constant-current (CC) mode. 0b0011 = JEITA modified fast-charge constant-current mode. 0b0100 = Fast-charge constant-voltage (CV) mode. 0b0101 = JEITA modified fast-charge constant-voltage mode. 0b0110 = Top-off mode. 0b0111 = JEITA modified top-off mode. 0b1000 = Done 0b1001 = JEITA modified done (done was entered through the JEITA-modified fast-charge states). 0b1010 = Prequalification timer fault. 0b1011 = Fast-charge timer fault. 0b1100 = Battery temperature fault. 0b1101 to 0b1111 = Reserved.
CHGIN_DTLS	3:2	CHGIN Status Detail	0b00 = The CHGIN input voltage is below the UVLO threshold ($V_{CHGIN} < V_{UVLO}$). 0b01 = The CHGIN input voltage is above the OVP threshold ($V_{CHGIN} > V_{OVP}$). 0b10 = The CHGIN input is being debounced (no power accepted from CHGIN during debounce). 0b11 = The CHGIN input is okay and debounced.
CHG	1	Quick Charger Status	0 = Charging is not happening. 1 = Charging is happening.
TIME_SUS	0	Time Suspend Indicator	0 = The charger's timers are either not active, or not suspended. 1 = The charger's active timer is suspended due to one of three reasons: charge current dropped below 20% of $I_{FAST-CHG}$ while the charger state machine is in FAST CHARGE CC mode, the charger is in SUPPLEMENT mode, or the charger state machine is in BATTERY TEMPERATURE FAULT mode.

INT_M_CHG (0x07)

BIT	7	6	5	4	3	2	1	0
Field	DIS_AICL	SYS_CNFG_M	SYS_CTRL_M	CHGIN_CTRL_M	TJ_REG_M	CHGIN_M	CHG_M	THM_M
Reset	0b0	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_AICL	7	Active input current loop disable	0 = Active Input Current Loop Active 1 = Active Input Current Loop Disabled
SYS_CNFG_M	6	Setting this bit prevents the SYS_CNFG_I bit from causing hardware IRQs.	0 = SYS_CNFG_I is not masked. 1 = SYS_CNFG_I is masked.
SYS_CTRL_M	5	Setting this bit prevents the SYS_CTRL_I bit from causing hardware IRQs.	0 = SYS_CTRL_I is not masked. 1 = SYS_CTRL_I is masked.
CHGIN_CTRL_M	4	Setting this bit prevents the CHGIN_CTRL_I bit from causing hardware IRQs.	0 = CHGIN_CTRL_I is not masked. 1 = CHGIN_CTRL_I is masked.
TJ_REG_M	3	Setting this bit prevents the TJREG_I bit from causing hardware IRQs.	0 = TJREG_I is not masked. 1 = TJREG_I is masked.
CHGIN_M	2	Setting this bit prevents the CHGIN_I bit from causing hardware IRQs.	0 = CHGIN_I is not masked. 1 = CHGIN_I is masked.
CHG_M	1	Setting this bit prevents the CHG_I bit from causing hardware IRQs.	0 = CHG_I is not masked. 1 = CHG_I is masked.
THM_M	0	Setting this bit prevents the THM_I bit from causing hardware IRQs.	0 = THM_I is not masked. 1 = THM_I is masked.

CNFG_CHG_A (0x20)

BIT	7	6	5	4	3	2	1	0
Field	THM_HOT[1:0]		THM_WARM[1:0]		THM_COOL[1:0]		THM_COLD[1:0]	
Reset	0b00		0b00		0b11		0b11	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
THM_HOT	7:6	Sets the T_{HOT} JEITA Temperature Threshold	0b00 = T_{HOT} = 45ºC 0b01 = T_{HOT} = 50ºC 0b10 = T_{HOT} = 55ºC 0b11 = T_{HOT} = 60ºC
THM_WARM	5:4	Sets the T_{WARM} JEITA Temperature Threshold	0b00 = T_{WARM} = 35ºC 0b01 = T_{WARM} = 40ºC 0b10 = T_{WARM} = 45ºC 0b11 = T_{WARM} = 50ºC
THM_COOL	3:2	Sets the T_{COOL} JEITA Temperature Threshold	0b00 = T_{COOL} = 0ºC 0b01 = T_{COOL} = 5ºC 0b10 = T_{COOL} = 10ºC 0b11 = T_{COOL} = 15ºC
THM_COLD	1:0	Sets the T_{COLD} JEITA Temperature Threshold	0b00 = T_{COLD} = -10ºC 0b01 = T_{COLD} = -5ºC 0b10 = T_{COLD} = 0ºC 0b11 = T_{COLD} = 5ºC

CNFG_CHG_B (0x21)

BIT	7	6	5	4	3	2	1	0
Field	VCHGIN_MIN[2:0]			ICHGIN_LIM[2:0]			I_PQ	CHG_EN
Reset	0b000			0b000			0b0	OTP
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VCHGIN_MIN	7:5	Minimum CHGIN Regulation Voltage ($V_{CHGIN-MIN}$)	0b000 = 4.0V 0b001 = 4.1V 0b010 = 4.2V 0b011 = 4.3V 0b100 = 4.4V 0b101 = 4.5V 0b110 = 4.6V 0b111 = 4.7V
ICHGIN_LIM	4:2	CHGIN Input Current Limit ($I_{CHGIN-LIM}$)	0b000 = 475mA 0b001 = 380mA 0b010 = 285mA 0b011 = 190mA 0b100 = 95mA 0b101 to 0b111 = Reserved. Defaults to 0b100.
I_PQ	1	Sets the prequalification charge current (I_{PQ}) as a percentage of $I_{FAST-CHG}$.	0 = 10% 1 = 20%
CHG_EN	0	Charger Enable	Default value defined by OTP bit CHG_EN_DFT: 0 = The battery charger is disabled. 1 = The battery charger is enabled.

CNFG_CHG_C (0x22)

BIT	7	6	5	4	3	2	1	0
Field	CHG_PQ[2:0]			I_TERM[1:0]		T_TOPOFF[2:0]		
Reset	0b111			0b11		0b000		
Access Type	Write, Read			Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_PQ	7:5	Battery Prequalification Voltage Threshold (V_{PQ})	0b000 = 2.3V 0b001 = 2.4V 0b010 = 2.5V 0b011 = 2.6V 0b100 = 2.7V 0b101 = 2.8V 0b110 = 2.9V 0b111 = 3.0V
I_TERM	4:3	Charger Termination Current (I_{TERM}). I_TERM[1:0] sets the charger termination current as a percentage of the fast-charge current $I_{FAST-CHG}$.	00 = 5% 01 = 7.5% 10 = 10% 11 = 15%
T_TOPOFF	2:0	Top-Off Timer Value (t_{TO})	0b000 = 0 minutes 0b001 = 5 minutes 0b010 = 10 minutes 0b011 = 15 minutes 0b100 = 20 minutes 0b101 = 25 minutes 0b110 = 30 minutes 0b111 = 35 minutes

CNFG_CHG_D (0x23)

BIT	7	6	5	4	3	2	1	0
Field	TJ_REG[2:0]			VSYS_REG[4:0]				
Reset	0b000			0b10110				
Access Type	Write, Read			Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
TJ_REG	7:5	Sets the die junction temperature regulation point, T_{J-REG}.	0b000 = 60ºC 0b001 = 70ºC 0b010 = 80ºC 0b011 = 90ºC 0b100 to 0b111 = 100ºC
VSYS_REG	4:0	System Voltage Regulation ($V_{SYS-REG}$) This 5-bit configuration is a linear transfer function that starts at 3.4V and ends at 4.8V, with 50mV increments. Program V_{SYS_REG} to at least 200mV above the higher of $V_{FAST-CHG}$ and $V_{FAST-CHG-JEITA}$.	0x0 = 3.400V 0x1 = 3.450V 0x2 = 3.500V ... 0x1B = 4.750V 0x1C - 0x1F = 4.800V

CNFG_CHG_E (0x24)

BIT	7	6	5	4	3	2	1	0
Field	CHG_CC[5:0]						T_FAST_CHG[1:0]	
Reset	0b000001						0b01	
Access Type	Write, Read						Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_CC	7:2	Sets the fast-charge constant current value, $I_{FAST-CHG}$. This 6-bit configuration is a transfer function with 7.5mA increments starts at 7.5mA and ends at 300mA, with 7.5mA increments.	0x0 = 7.5mA 0x1 = 15.0mA 0x2 = 22.5mA ... 0x26 = 292.5mA 0x27 to 0x3F = 300.0mA
T_FAST_CHG	1:0	Sets the fast-charge safety timer, t_{FC}.	0b00 = Timer disabled 0b01 = 3 hours 0b10 = 5 hours 0b11 = 7 hours

CNFG_CHG_F (0x25)

BIT	7	6	5	4	3	2	1	0
Field	CHG_CC_JEITA[5:0]						RSVD	–
Reset	0b000001							–
Access Type	Write, Read						Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_CC_JEITA	7:2	Sets $I_{FAST-CHG-JEITA}$ for when the battery is either cool or warm as defined by the V_{COOL} and V_{WARM} temperature thresholds. This register is a don't care if the battery temperature is normal. This 6-bit configuration is a transfer function with 7.5mA increments starts at 7.5mA and ends at 300mA, with 7.5mA increments.	0x0 = 7.5mA 0x1 = 15.0mA 0x2 = 22.5mA ... 0x26 = 292.5mA 0x27 to 0x3F = 300mA
RSVD	1	Reserved. Unutilized bit. Write to 0. Reads are don't care.	

CNFG_CHG_G (0x26)

BIT	7	6	5	4	3	2	1	0
Field	CHG_CV[5:0]						USBS	FUS_M
Reset	0b000000						0b0	0b1
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_CV	7:2	Sets fast-charge battery regulation voltage, $V_{FAST-CHG}$. This 6-bit configuration is a linear transfer function that starts at 3.6V and ends at 4.6V, with 25mV increments. Program V_{SYS_REG} to at least 200mV above the higher of $V_{FAST-CHG}$ and $V_{FAST-CHG-JEITA}$.	0x0 = 3.600V 0x1 = 3.625V 0x2 = 3.650V ... 0x27 = 4.575V 0x28 to 0x3F = 4.600V
USBS	1	Setting this bit places CHGIN in USB suspend mode.	0 = CHGIN is not suspended and may draw current from an adapter source. 1 = CHGIN is suspended and may not draw current from an adapter source. **Note:** USBS = 1 results in CHGIN_I interrupt AND CHGIN_DTLS[1:0] = 0b00.
FUS_M	0	Forced USB Suspend Mask	FUS (ALT mode of GPIO0) is only active if the FUS_M bit is set to 0. See the *GPIO Alternate Mode* section for more details.

CNFG_CHG_H (0x27)

BIT	7	6	5	4	3	2	1	0
Field	CHG_CV_JEITA[5:0]						SYS_BAT_PRT	CHR_TH_EN
Reset	0b000000						0b1	0b1
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_CV_JEITA	7:2	Sets the modified $V_{FAST-CHG-JEITA}$ for when the battery is either cool or warm as defined by the V_{COOL} and V_{WARM} temperature thresholds. This register is a don't care if the battery temperature is normal. This 6-bit configuration is a linear transfer function that starts at 3.6V and ends at 4.6V, with 25mV increments. Program V_{SYS_REG} to at least 200mV above the higher of $V_{FAST-CHG}$ and $V_{FAST-CHG-JEITA}$.	0x0 = 3.600V 0x1 = 3.625V 0x2 = 3.650V ... 0x27 = 4.575V 0x28 to 0x3F = 4.600V
SYS_BAT_PRT	1	VSYS_REG - CHG_CV clamp By default, the V_{SYS_REG} has to be at least 200mV higher than the programmed CHG_CV. If this bit is set (hardware protection is turned off), the software has to provide the protection (the SYS voltage has to be 200mV higher than the BATT voltage). If the V_{SYS_REG} is lower than CHG_CV+200mV, the charger reduces CHG_CV to satisfy the 200mV requirement.	
CHR_TH_EN	0	Charger restart threshold enable	

CNFG_CHG_I (0x28)

BIT	7	6	5	4	3	2	1	0
Field	IMON_DISCHG_SCALE[3:0]				MUX_SEL[3:0]			
Reset	0xF				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
IMON_DISCHG_SCALE	7:4	Selects the battery discharge current full-scale current value.	0x0 = 8.2mA 0x1 = 40.5mA 0x2 = 72.3mA 0x3 = 103.4mA 0x4 = 134.1mA 0x5 = 164.1mA 0x6 = 193.7mA 0x7 = 222.7mA 0x8 = 251.2mA 0x9 = 279.3mA 0xA to 0xF = 300.0mA

BITFIELD	BITS	DESCRIPTION	DECODE
MUX_SEL	3:0	Selects the analog channel to connect to AMUX: Note that the multiplexer consumes current unless it is in the 0b0000 state. When measurements are not needed, make sure to configure MUX_SEL[3:0] = 0b0000. Also note that for AMUX to operate, the on/off controller must be in the "Resource On" state.	0b0000 = Multiplexer is disabled and AMUX is high-impedance. 0b0001 = CHGIN voltage monitor. 0b0010 = CHGIN current monitor. 0b0011 = BATT voltage monitor. 0b0100 = BATT charge current monitor. Valid only while battery charging is happening (CHG = 1). 0b0101 = BATT discharge current monitor normal measurement. 0b0110 = BATT discharge current monitor nulling measurement. 0b0111 = Reserved. 0b1000 = Reserved. 0b1001 = AGND voltage monitor (through 100Ω pulldown resistor). 0b1010 to 0b1111 = SYS voltage monitor.

CNFG_SBB_TOP (0x38)

BIT	7	6	5	4	3	2	1	0
Field	DIS_LPM	IPK_1P5A	–	–	–	–	DRV_SBB[1:0]	
Reset	0b0	0b0	–	–	–	–	0b00	
Access Type	Write, Read	Write, Read	–	–	–	–	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
DIS_LPM	7	Disables the automatic Low-Power Mode for Each SIMO Channel.	0b0 = Automatic Low Power Mode for each SIMO channel 0b1 = Disable LPM feature for each SIMO channel
IPK_1P5A	6	SBB2 Inductor Current Limit Offset	0b0 = SBB2 inductor current limit is 1.0A for the 1.0A setting. 0b1 = SBB2 inductor current limit is 1.5A for the 1.0A setting.
DRV_SBB	1:0	SIMO Buck-Boost (all channels) Drive Strength Trim. See the *Drive Strength* section for more details.	0b00 = Fastest transition time 0b01 = A little slower than 0b00 0b10 = A little slower than 0b01 0b11 = A little slower than 0b10

CNFG_SBB0_A (0x39)

BIT	7	6	5	4	3	2	1	0
Field	TV_SBB0[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TV_SBB0	7:0	SIMO Buck-Boost Channel 0 Target Output Voltage This 8-bit configuration is a linear transfer function that starts at 0.5V, ends at 5.5V, with 25mV increments.	0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V … 0xC5 = 5.425V 0xC6 = 5.450V 0xC7 = 5.475V 0xC8 to 0xFF = 5.500V

CNFG_SBB0_B (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	OP_MODE[1:0]		IP_SBB0[1:0]		ADE_SBB0	EN_SBB0[2:0]		
Reset	OTP		OTP		OTP	OTP		
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
OP_MODE	7:6	Operation Mode of SBB0	0b00 = Automatic 0b01 = Buck mode 0b10 = Boost mode 0b11 = Buck-boost mode
IP_SBB0	5:4	SIMO Buck-Boost Channel 0 Peak Current Limit	0b00 = 1.000A 0b01 = 0.750A 0b10 = 0.500A 0b11 = 0.333A
ADE_SBB0	3	SIMO Buck-Boost Channel 0 Active-Discharge Enable	0b0 = The active discharge function is disabled. When SBB0 is disabled, its discharge rate is a function of the output capacitance and the external load. 0b1 = The active discharge function is enabled. When SBB0 is disabled, an internal resistor (R_{AD_SBB0}) is activated from SBB0 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB0} load.
EN_SBB0	2:0	Enable Control for SIMO Buck-Boost Channel 0, selecting either an FPS slot the channel powers-up and powers-down in or whether the channel is forced on or off.	0b000 = FPS slot 0 0b001 = FPS slot 1 0b010 = FPS slot 2 0b011 = FPS slot 3 0b100 = Off irrespective of FPS 0b101 = Same as 0b100 0b110 = On irrespective of FPS 0b111 = Same as 0b110

CNFG_SBB1_A (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	TV_SBB1[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TV_SBB1	7:0	SIMO Buck-Boost Channel 1 Target Output Voltage This 8-bit configuration is a linear transfer function that starts at 0.5V, ends at 5.5V, with 25mV increments.	0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V ... 0xC5 = 5.425V 0xC6 = 5.450V 0xC7 = 5.475V 0xC8 to 0xFF = 5.500V

CNFG_SBB1_B (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	OP_MODE[1:0]		IP_SBB1[1:0]		ADE_SBB1	EN_SBB1[2:0]		
Reset	OTP		OTP		OTP	OTP		
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
OP_MODE	7:6	Operation Mode of SBB1	0b00 = Automatic 0b01 = Buck mode 0b10 = Boost mode 0b11 = Buck-boost mode
IP_SBB1	5:4	SIMO Buck-Boost Channel 1 Peak Current Limit	0b00 = 1.000A 0b01 = 0.750A 0b10 = 0.500A 0b11 = 0.333A
ADE_SBB1	3	SIMO Buck-Boost Channel 1 Active-Discharge Enable	0b0 = The active discharge function is disabled. When SBB1 is disabled, its discharge rate is a function of the output capacitance and the external load. 0b1 = The active discharge function is enabled. When SBB1 is disabled, an internal resistor (R_{AD_SBB1}) is activated from SBB1 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB1} load.

BITFIELD	BITS	DESCRIPTION	DECODE
EN_SBB1	2:0	Enable control for SIMO buck-boost channel 1, selecting either an FPS slot the channel powers-up and powers-down in or whether the channel is forced on or off.	0b000 = FPS slot 0 0b001 = FPS slot 1 0b010 = FPS slot 2 0b011 = FPS slot 3 0b100 = Off irrespective of FPS 0b101 = Same as 0b100 0b110 = On irrespective of FPS 0b111 = Same as 0b110

CNFG_SBB2_A (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	TV_SBB2[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TV_SBB2	7:0	SIMO Buck-Boost Channel 2 Target Output Voltage This 8-bit configuration is a linear transfer function that starts at 0.5V, ends at 5.5V, with 25mV increments.	0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V ... 0xC5 = 5.425V 0xC6 = 5.450V 0xC7 = 5.475V 0xC8 to 0xFF = 5.500V

CNFG_SBB2_B (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	OP_MODE[1:0]		IP_SBB2[1:0]		ADE_SBB2	EN_SBB2[2:0]		
Reset	OTP		OTP		OTP	OTP		
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
OP_MODE	7:6	Operation Mode of SBB2	0b00 = Automatic 0b01 = Buck mode 0b10 = Boost mode 0b11 = Buck-boost mode
IP_SBB2	5:4	SIMO Buck-Boost Channel 2 Peak Current Limit	0b00 = 1.000A 0b01 = 0.750A 0b10 = 0.500A 0b11 = 0.333A

BITFIELD	BITS	DESCRIPTION	DECODE
ADE_SBB2	3	SIMO Buck-Boost Channel 2 Active-Discharge Enable	0b0 = The active discharge function is disabled. When SBB2 is disabled, its discharge rate is a function of the output capacitance and the external load. 0b1 = The active discharge function is enabled. When SBB2 is disabled, an internal resistor (R_{AD_SBB2}) is activated from SBB2 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB2} load.
EN_SBB2	2:0	Enable control for SIMO buck-boost channel 2, selecting either an FPS slot the channel powers-up and powers-down in or whether the channel is forced on or off.	0b000 = FPS slot 0 0b001 = FPS slot 1 0b010 = FPS slot 2 0b011 = FPS slot 3 0b100 = Off irrespective of FPS 0b101 = Same as 0b100 0b110 = On irrespective of FPS 0b111 = Same as 0b110

CNFG_DVS_SBB0_A (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	TV_SBB0_DVS[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TV_SBB0_DVS	7:0	SIMO Buck-Boost Channel 0 Target Output Voltage This 7-bit configuration is a linear transfer function that starts at 0.5V, ends at 5.5V, with 25mV increments.	0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V ... 0xC5 = 5.425V 0xC6 = 5.450V 0xC7 = 5.475V 0xC8 to 0xFF = 5.500V

CNFG_LDO0_A (0x48)

BIT	7	6	5	4	3	2	1	0
Field	TV_OFS_LDO0	TV_LDO0[6:0]						
Reset	OTP	OTP						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TV_OFS_LDO0	7	LDO0 Output Voltage Offset. This bit applies a 1.325V offset to the output voltage of the LDO0.	0b0 = No Offset 0b1 = 1.325V Offset
TV_LDO0	6:0	LDO0 Target Output Voltage The tareget output voltage of the LDO would be TV_OFS_LDO0 + TV_LDO0. This 7-bit configuration is a linear transfer function that starts at 0.5V, ends at 3.675V, with 25mV increments.	0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V ... 0x7E = 3.650V 0x7F = 3.675V When TV_LDO[7] = 0, TV_LDO[6:0] sets the LDO's output voltage range from 0.5V to 3.675V. When TV_LDO[7] = 1, TV_LDO[6:0] sets the LDO's output voltage from 1.825V to 5V.

CNFG_LDO0_B (0x49)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDO0_MD	ADE_LDO0	EN_LDO0[2:0]		
Reset	–	–	–	OTP	OTP	OTP		
Access Type	–	–	–	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LDO0_MD	4	Operation Mode of LDO0	0b0 = Low dropout linear regulator (LDO) mode 0b1 = Load switch (LSW) mode
ADE_LDO0	3	LDO0 Active-Discharge Enable	0b0 = The active discharge function is disabled. When LDO0 is disabled, its discharge rate is a function of the output capacitance and the external load. 0b1 = The active discharge function is enabled. When LDO is disabled, an internal resistor (R_{AD_LDO}) is activated from LDO to GND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_LDO} load.
EN_LDO0	2:0	Enable Control for LDO0, selecting either an FPS slot the channel powers-up and powers-down in or whether the channel is forced on or off.	0b000 = FPS slot 0 0b001 = FPS slot 1 0b010 = FPS slot 2 0b011 = FPS slot 3 0b100 = Off irrespective of FPS 0b101 = Same as 0b100 0b110 = On irrespective of FPS 0b111 = Same as 0b110

CNFG_LDO1_A (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	TV_OFS_LDO1	TV_LDO1[6:0]						
Reset	OTP	OTP						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
TV_OFS_LDO1	7	LDO1 Output Voltage Offset. This bit applies a 1.325V offset to the output voltage of the LDO1.	0b0 = No offset 0b1 = 1.325V offset
TV_LDO1	6:0	LDO1 Target Output Voltage The tareget output voltage of the LDO would be TV_OFS_LDO1 + TV_LDO1. This 7-bit configuration is a linear transfer function that starts at 0.5V, ends at 3.675V, with 25mV increments.	0x00 = 0.500V 0x01 = 0.525V 0x02 = 0.550V 0x03 = 0.575V 0x04 = 0.600V 0x05 = 0.625V 0x06 = 0.650V 0x07 = 0.675V 0x08 = 0.700V ... 0x7E = 3.650V 0x7F = 3.675V When TV_LDO[7] = 0, TV_LDO[6:0] sets the LDO's output voltage range from 0.5V to 3.675V. When TV_LDO[7] = 1, TV_LDO[6:0] sets the LDO's output voltage from 1.825V to 5V.

CNFG_LDO1_B (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	LDO1_MD	ADE_LDO1	EN_LDO1[2:0]		
Reset	–	–	–	OTP	OTP	OTP		
Access Type	–	–	–	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
LDO1_MD	4	Operation Mode of LDO	0b0 = Low dropout linear regulator (LDO) mode 0b1 = Load switch (LSW) mode
ADE_LDO1	3	LDO1 Active-Discharge Enable	0b0 = The active discharge function is disabled. When LDO0 is disabled, its discharge rate is a function of the output capacitance and the external load. 0b1 = The active discharge function is enabled. When LDO is disabled, an internal resistor (R_{AD_LDO}) is activated from LDO to GND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_LDO} load.

BITFIELD	BITS	DESCRIPTION	DECODE
EN_LDO1	2:0	Enable Control for LDO1, selecting either an FPS slot the channel powers-up and powers-down in or whether the channel is forced on or off.	0b000 = FPS slot 0 0b001 = FPS slot 1 0b010 = FPS slot 2 0b011 = FPS slot 3 0b100 = Off irrespective of FPS 0b101 = Same as 0b100 0b110 = On irrespective of FPS 0b111 = Same as 0b110

Fuel Gauge

ADDRESS	NAME	MSB							LSB
Status and Configuration Registers									
0x00	Status[15:8]	Br	Smx	Tmx	Vmx	Bi	Smn	Tmn	Vmn
	Status[7:0]	dSOCi	Imx	X	X	Bst	Imn	POR	X
0x01	VAlrtTh[15:8]	VMAX[7:0]							
	VAlrtTh[7:0]	VMIN[7:0]							
0x02	TAlrtTh[15:8]	TMAX[7:0]							
	TAlrtTh[7:0]	TMIN[7:0]							
0x03	SAlrtTh[15:8]	SMAX[7:0]							
	SAlrtTh[7:0]	SMIN[7:0]							
0x13	FullSOCThr[15:8]	FullSOCThr[15:8]							
	FullSOCThr[7:0]	FullSOCThr[7:0]							
0x18	DesignCap[15:8]	DesignCap[15:8]							
	DesignCap[7:0]	DesignCap[7:0]							
0x1D	Config[15:8]	TSel	SS	TS	VS	IS	THSH	Ten	Tex
	Config[7:0]	SHDN	COMMSH	0	ETHRM	FTHRM	Aen	Bei	Ber
0x1E	IChgTerm[15:8]	ICHGTerm[15:8]							
	IChgTerm[7:0]	ICHGTerm[7:0]							
0x21	DevName[15:8]	–	–	–	–	–	–	–	–
	DevName[7:0]	–	–	–	–	–	–	–	–
0x28	LearnCfg[15:8]	0	1	0	0	0	1	0	0
	LearnCfg[7:0]	1	LS[2:0]			0	1	1	0
0x29	FilterCfg[15:8]	1	1	–	–	–	MIX[3:1]		
	FilterCfg[7:0]	MIX[0]	VOLT[2:0]			NCURR[3:0]			
0x3A	VEmpty[15:8]	VE[8:1]							
	VEmpty[7:0]	VE[0]	VR[6:0]						
0xB1	Power[15:8]	–	–	–	–	–	–	–	–
	Power[7:0]	–	–	–	–	–	–	–	–
0xB3	AvgPower[15:8]	AvgPower[15:8]							
	AvgPower[7:0]	AvgPower[7:0]							
0xB4	IAlrtTh[15:8]	IMAX[7:0]							
	IAlrtTh[7:0]	IMIN[7:0]							
0xBB	Config2[15:8]	0	0	AtRateEN	DPEN	POWR[3:0]			

ADDRESS	NAME	MSB							LSB
	Config2[7:0]	dSOCen	TAlrtEn	LDMdl	–	DRCfg[1:0]		CPMode	–
OVERLAP									
Measurement Registers									
0x08	Temp[15:8]	TEMP[15:8]							
	Temp[7:0]	TEMP[7:0]							
0x09	Vcell[15:8]	VCELL[15:8]							
	Vcell[7:0]	VCELL[7:0]							
0x0A	Current[15:8]	Current[15:8]							
	Current[7:0]	Current[7:0]							
0x0B	AvgCurrent[15:8]	AvgCurrent[15:8]							
	AvgCurrent[7:0]	AvgCurrent[7:0]							
0x16	AvgTA[15:8]	AvgTA[15:8]							
	AvgTA[7:0]	AvgTA[7:0]							
0x19	AvgVCell[15:8]	AvgVCELL[15:8]							
	AvgVCell[7:0]	AvgVCELL[7:0]							
0x1A	MaxMinTemp[15:8]	MaxTemperature[7:0]							
	MaxMinTemp[7:0]	MinTemperature[7:0]							
0x1B	MaxMinVolt[15:8]	MaxVoltage[7:0]							
	MaxMinVolt[7:0]	MinVoltage[7:0]							
0x1C	MaxMinCurr[15:8]	MaxChargeCurrent[7:0]							
	MaxMinCurr[7:0]	MaxDisCurrent[7:0]							
0x27	AIN0[15:8]	AIN0[15:8]							
	AIN0[7:0]	AIN0[7:0]							
0x3E	Timer[15:8]	TIMER[15:8]							
	Timer[7:0]	TIMER[7:0]							
0xBE	TimerH[15:8]	TIMERH[15:8]							
	TimerH[7:0]	TIMERH[7:0]							
OVERLAP									
ModelGauge m5 Output Registers									
0x05	RepCap[15:8]	RepCap[15:8]							
	RepCap[7:0]	RepCap[7:0]							
0x06	RepSOC[15:8]	RepSOC[15:8]							
	RepSOC[7:0]	RepSOC[7:0]							
0x0E	AvSOC[15:8]	AvSOC[15:8]							
	AvSOC[7:0]	AvSOC[7:0]							
0x10	FullCapRep[15:8]	FullCapRep[15:8]							
	FullCapRep[7:0]	FullCapRep[7:0]							
0x11	TTE[15:8]	TTE[15:8]							
	TTE[7:0]	TTE[7:0]							
0x14	RCell[15:8]	RCell[15:8]							
	RCell[7:0]	RCell[7:0]							
0x17	Cycles[15:8]	Cycles[15:8]							

ADDRESS	NAME	MSB							LSB
	Cycles[7:0]	Cycles[7:0]							
0x1F	AvCap[15:8]	AvCap[15:8]							
	AvCap[7:0]	AvCap[7:0]							
0x20	TTF[15:8]	TTF[15:8]							
	TTF[7:0]	TTF[7:0]							

Register Details

Status (0x00)

Interrupt status register for the FG block.

BIT	15	14	13	12	11	10	9	8
Field	Br	Smx	Tmx	Vmx	Bi	Smn	Tmn	Vmn
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BIT	7	6	5	4	3	2	1	0
Field	dSOCi	Imx	X	X	Bst	Imn	POR	X
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b1	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
Br	15	Battery Removal	This bit is set to 1 when the device detects that a battery has been removed from the system. This bit must be cleared by system software to detect the next removal event. Br is set to 1 at power-up.
Smx	14	Maximum SOCALRT Threshold Exceeded	This bit is set to 1 whenever SOC rises above the maximum SAlrtTh value. This bit may or may not need to be cleared by system software to detect the next event. See the Config.SS description. The bit is cleared to 0 at power-up.
Tmx	13	Maximum TALRT Threshold Exceeded	This bit is set to 1 whenever reading at Temperature register rises above the maximum TAlrtTh value. This bit may or may not need to be cleared by system software to detect the next event. See the Config.TS description. The bit is cleared to 0 at power-up.
Vmx	12	Maximum VALRT Threshold Exceeded	This bit is set to 1 whenever a VCell register reading is above the maximum VAlrtTh value. This bit may or may not need to be cleared by system software to detect the next event. See the Config.VS description. This bit is set to 0 at power-up.
Bi	11	Battery Insertion	This bit is set to 1 when the device detects that a battery has been inserted into the system by monitoring the AIN pin. This bit must be cleared by system software to detect the next insertion event. Bi is set to 0 at power-up.

BITFIELD	BITS	DESCRIPTION	DECODE
Smn	10	Minimum SOCALRT Threshold Exceeded.	This bit is set to 1 whenever SOC rises above the minimum SAlrtTh value. This bit may or may not need to be cleared by system software to detect the next event. See the Config.SS description. The bit is cleared to 0 at power-up.
Tmn	9	Minimum TALRT Threshold Exceeded.	This bit is set to 1 whenever reading at Temperature register rises above the minimum TAlrtTh value. This bit may or may not need to be cleared by system software to detect the next event. See the Config.TS description. The bit is cleared to 0 at power-up.
Vmn	8	Minimum VALRT Threshold Exceeded.	This bit is set to 1 whenever a VCell register reading is above the minimum VAlrtTh value. This bit may or may not need to be cleared by system software to detect the next event. See the Config.VS description. This bit is set to 0 at power-up.
dSOCi	7	1% SOC Change Alert	This bit is set to 1 whenever the RepSOC register crosses an interger percentage boundary such as 50.0%, 51.0%, etc. Must be cleared by host software. dSOCi is set to 1 at power-up.
Imx	6	Maximum Current-Alert Threhold Exceeded	This bit is set to 1 whenever a Current register reading is above the IAlrtTh.IMAX threhold. This bit may or may not need to be cleared by system software to detect the next event. See the Config.IS description. The bit is cleared to 0 at power-up.
X	5	Don't Care	This bit is undefined and can be logic 0 or 1
X	4	Don't Care	This bit is undefined and can be logic 0 or 1
Bst	3	Battery Status	Useful when the IC is used in a host-side application. This bit is set to 0 when a battery is present in the system, and set to 1 when the battery is absent. Bst is set to 0 at power-up.
Imn	2	Minimum Current-Alert Threshold Exceeded	This bit is set to 1 whenever a Current register reading is below the IAlrtTH.IMIN threshold. This bit may or may not need to be cleared by system software to detect the next event. See the Config.IS description. The bit is cleared to 0 at power-up.
POR	1	Power-On Reset.	This bit is set to 1 when the device detects that a software or hardware POR event has occurred. This bit must be cleared by system software to detect the next POR event. POR is set to 1 at power-up.
X	0	Don't Care	This bit is undefined and can be logic 0 or 1.

VAlrtTh (0x01)

The VAlrtTh register sets upper and lower limits that generate an alert if exceeded by the VCell register value.

BIT	15	14	13	12	11	10	9	8
Field	VMAX[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	VMIN[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VMAX	15:8	Maximum voltage reading. An alert is generated if the VCell register reading exceeds this value.	Register type: special Set Max = 0xFF to disable. Selectable with 20mV resolution over the full operating range of the VCell register.
VMIN	7:0	Minimum voltage reading. An alert is generated if the VCell register reading falls below this value.	Register type: special Set Min = 0x00 to disable. Selectable with 20mV resolution over the full operating range of the VCell register.

TAlrtTh (0x02)

The TAlrtTh register sets upper and lower limits that generate an alert if exceeded by the Temp register value.

BIT	15	14	13	12	11	10	9	8
Field	TMAX[7:0]							
Reset	0x7F							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	TMIN[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TMAX	15:8	Sets an alert threshold for maximum temperature.	Register type: special Set Max = 0x7F to disable. Stored in two's complement format with 1˚C resolution over the full operating range of the Temp register.
TMIN	7:0	Sets an alert threshold for minimum temperature.	Register type: special Set Min = 0x80 to disable. Stored in two's complement format with 1˚C resolution over the full operating range of the Temp register.

SAlrtTh (0x03)

The SAlrtTh register sets upper and lower limits that generate an alert if exceeded by RepSOC.

BIT	15	14	13	12	11	10	9	8
Field	SMAX[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	SMIN[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SMAX	15:8	Sets an alert for maximum SOC.	Register type: special This may be used for charge termination, or for power-management near full. Set to 0xFF to disable. The threshold is configurable with 1% resolution over the full operating range of the RepSOC register.
SMIN	7:0	Sets an alert for minimum SOC.	Register type: special This may be used for discharge termination, or for power-management near empty. Set to 0x00 to disable. The threshold is configurable with 1% resolution over the full operating range of the RepSOC register.

FullSOCThr (0x13)

The FullSOCThr register gates detection of end-of-charge. VFSOC must be larger than the FullSOCThr value before IChgTerm is compared to the AvgCurrent register value. The recommended FullSOCThr register setting for most custom characterized applications is 95% (default, 0x5F05). For EZ Performance applications, the recommendation is 80% (0x5005). See the *IChgTerm* register description and refer to the *ModelGauge m5 EZ User Guide* for details.

BIT	15	14	13	12	11	10	9	8
Field	FullSOCThr[15:8]							
Reset	0x5000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	FullSOCThr[7:0]							
Reset	0x5000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FullSOCThr	15:0	Default value: 95%.	Register type: percentage

DesignCap (0x18)

The DesignCap register holds the nominal capacity of the cell. This value is used to determine the age of the cell by comparing against the measured present cell capacity.

BIT	15	14	13	12	11	10	9	8
Field	DesignCap[15:8]							
Reset	0x0BB8							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	DesignCap[7:0]							
Reset	0x0BB8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DesignCap	15:0	Expected cell capacity.	Register type: capacity

Config (0x1D)

The Config registers hold all shutdown enable, alert enable, and temperature enable control bits. Writing a bit location enables the corresponding function within one task period.

BIT	15	14	13	12	11	10	9	8
Field	TSel	SS	TS	VS	IS	THSH	Ten	Tex
Reset	0b0	0b0	0b1	0b0	0b0	0b0	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	SHDN	COMMSH	0	ETHRM	FTHRM	Aen	Bei	Ber
Reset	0b0	0b0	0b0	0b1	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TSel	15	Temperature Sensor Select	Temperature sensor select. Set to 0 to use internal die temperature. Set to 1 to use temperature information from thermistor. ETHRM bit must be set to 1 when TSel is 1.
SS	14	SOC ALRT Sticky	SOC ALRT Sticky. When SS = 1, SOC alerts can only be cleared through software. When SS = 0, SOC alerts are cleared automatically when the threshold is no longer exceeded.
TS	13	Temperature ALRT Sticky	When TS = 1, temperature alerts can only be cleared through software. When TS = 0, temperature alerts are cleared automatically when the threshold is no longer exceeded.
VS	12	Voltage ALRT Sticky	When VS = 1, voltage alerts can only be cleared through software. When VS = 0, voltage alerts are cleared automatically when the threshold is no longer exceeded. VS is set to 0 at power-up.
IS	11	Current ALRT Sticky	When IS = 1, current alerts can only be cleared through software. When IS = 0, current alerts are cleared automatically when the threshold is no longer exceeded.

BITFIELD	BITS	DESCRIPTION	DECODE
THSH	10	TH Pin Shutdown	TH Pin Shutdown. Set to 1 to enable device shutdown when the IC is mounted host-side and the battery is removed. The IC enters shutdown if the TH pin remains high ($V_{TH} > V_{BATT} - V_{DET}$) for longer than the timeout of the ShdnTimer register. This also configures the device to wake up when TH is pulled low with a thermistor on-cell insertion. Note that if COMMSH and AINSH are both set to 0, the device wakes up on any edge of SDA.
Ten	9	Enable Temperature Channel	Set to 1 and set ETHRM or FTHRM to 1 to enable temperature measurements
Tex	8	Temperature External	When set to 1, the fuel gauge requires external temperature measurements to be written from the host. When set to 0, the ICs own measurements are used instead.
SHDN	7	Shutdown	Write this bit to logic 1 to force a shutdown of the device after timeout of the SHDNTIMER register (default 45s delay). SHDN is reset to 0 at power-up and upon exiting shutdown mode. In order to command shutdown within 45 seconds, first write HibCFG = 0x0000 to enter active mode.
COMMSH	6	Communication Shutdown	Communication Shutdown. Set to logic 1 to force the device to enter shutdown mode if both SDA and SCL are held low for more than timeout of the ShdnTimer register. This also configures the device to wake up on a rising edge of any communication. Note that if COMMSH and THSH are both set to 0, the device wakes up on any edge of SDA. Refer to the *User Guide* for details.
0	5	Bit must be written 0.	Do not write 1
ETHRM	4	Enable Thermistor	Enable Thermistor. Set to logic 1 to enable the TH pin measurement.
FTHRM	3	Force Thermistor Bias Switch	Force Thermistor Bias Switch. This allows the host to control the bias of the thermistor switch or enable fast detection of battery removal. Set FTHRM = 1 to always enable the thermistor bias switch. With a standard 10kΩ thermistor, this adds an additional ~200µA to the current drain of the circuit.
Aen	2	Enable alert on fuel-gauge outputs.	Enable alert on fuel-gauge outputs. When Aen = 1, any violation of the alert threshold register values by temperature, voltage, current, or SOC triggers an alert. This bit affects the ALRT pin operation only. The Smx, Smn, Tmx, Tmn, Vmx, Vmn, Imx, and Imn bits of the Status register (0x000) are not disabled.
Bei	1	Enable alert on battery insertion when the IC is mounted host-side.	When Bei = 1, a battery-insertion condition, as detected by the TH pin voltage, triggers an alert.
Ber	0	Enable alert on battery removal when the IC is mounted host-side.	When Ber = 1, a battery-removal condition, as detected by the TH pin voltage, triggers an alert.

IChgTerm (0x1E)

The IChgTerm register allow the device to detect when charge termination has occurred.

BIT	15	14	13	12	11	10	9	8
Field	ICHGTerm[15:8]							
Reset	0x0640							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	ICHGTerm[7:0]							
Reset	0x0640							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
ICHGTerm	15:0	Program IChgTerm to the exact charge termination current used in the application	Register type: current

DevName (0x21)

The DevName register holds revision information. This allows host software to easily identify the type of IC being communicated to.

LearnCfg (0x28)

The LearnCFG register controls all functions relating to adaptation during operation. The LearnCFG register default values should not be changed unless specifically required by the application.

BIT	15	14	13	12	11	10	9	8
Field	0	1	0	0	0	1	0	0
Reset	0b0	0b1	0b0	0b0	0x0	0b001	0x0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Field	1	LS[2:0]			0	1	1	0
Reset	0b1	0b000			0b0	0b1	0b1	0b0
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
0	15	Bit must be written 0.	Do not write 1
1	14	Bit must be written 1.	Do not write 0
0	13	Bit must be written 0.	Do not write 1
0	12	Bit must be written 0.	Do not write 1
0	11	Bit must be written 0.	Do not write 1
1	10	Bit must be written 1.	Do not write 0
0	9	Bit must be written 0.	Do not write 1
0	8	Bit must be written 0.	Do not write 1
1	7	Bit must be written 1.	Do not write 0

BITFIELD	BITS	DESCRIPTION	DECODE
LS	6:4	Learn Stage. The Learn Stage value controls the influence of the voltage fuel gauge on the mixing algorithm.	Learn Stage defaults 0x0, making the voltage fuel gauge dominate. Learn Stage then advances to 0x7 over the course of two full cell cycles to make the coulomb counter dominate. Host software can write the Learn Stage value to 0x7 to advance to the final stage at any time. Values between 0x1 and 0x6 are ignored.
0	3	Bit must be written 0.	Do not write 1
1	2	Bit must be written 1.	Do not write 0
1	1	Bit must be written 1.	Do not write 0
0	0	Bit must be written 0.	Do not write 1

FilterCfg (0x29)

The FilterCfg register sets the average time period for all A/D readings, for mixing OCV results and coulomb-count results. It is recommended that these values are not changed unless absolutely required by the application.

BIT	15	14	13	12	11	10	9	8
Field	1	1	–	–	–	MIX[3:1]		
Reset		0b11	–	–	–	0xD		
Access Type	Write, Read	Write, Read	–	–	–	Write, Read		

BIT	7	6	5	4	3	2	1	0
Field	MIX[0]	VOLT[2:0]			NCURR[3:0]			
Reset	0xD	0b010			0x4			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
1	15	Bit must be written 1.	Do not write 0
1	14	Bit must be written 1.	Do not write 0
MIX	10:7	Sets the time constant for the mixing algorithm. The default POR value of 0xD gives a time constant of 12.8 hours.	The equation setting the period is: Mixing Period = 45s x $2^{(MIX-3)}$
VOLT	6:4	Sets the time constant for the AvgVCell register. The default POR value of 0x4 gives a time constant of 45s.	The equation setting the period is: AvgVCell time constant = 45s x $2^{(VOLT-2)}$
NCURR	3:0	Sets the time constant for the AverageCurrent register. The default POR value of 4h gives a time constant of 11.25 seconds.	The equation setting the period is:AverageCurrent time constant = 175.8ms × 2^(2+NCURR)

VEmpty (0x3A)

The VEmpty register sets thresholds related to empty detection during operation.

BIT	15	14	13	12	11	10	9	8
Field	VE[8:1]							
Reset	0b101001010							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	VE[0]	VR[6:0]						
Reset	0b101001010	0b1100001						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
VE	15:7	Empty voltage target during load. The fuel gauge provides capacity and percentage relative to the empty voltage target, eventually declaring 0% at VE	A 10mV resolution gives a 0V to 5.11V range. This value defaults to 3.3V after reset.
VR	6:0	Recovery Voltage. Sets the voltage level for clearing empty detection. Once the cell voltage rises above this point, empty voltage detection is reenabled	A 40mV resolution gives a 0V to 5.08V range. This value defaults to 3.88V, which is recommended for most applications.

AvgPower (0xB3)

BIT	15	14	13	12	11	10	9	8
Field	AvgPower[15:8]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AvgPower[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvgPower	15:0	Filtered average power from the Power register	LSB is 0.171mW.

IAlrtTh (0xB4)

The IAlrtTh register sets upper and lower limits that generate an alert if exceeded by the Current register value. Interrupt threshold limits are selectable with 8.567mA resolution over the full operating range of the Current register.

BIT	15	14	13	12	11	10	9	8
Field	IMAX[7:0]							
Reset	0x7F							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	IMIN[7:0]							
Reset	0x80							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
IMAX	15:8	The upper 8 bits set the maimum value	Register type: special An alert is generated if the current register reading exceeds this value.
IMIN	7:0	The lower 8 bits set the minimum value	An alert is generated if the current register reading falls below this value.

Config2 (0xBB)

The Config registers hold all shutdown enable, alert enable, and temperature enable control bits. Writing a bit location enables the corresponding function within one task period.

BIT	15	14	13	12	11	10	9	8
Field	0	0	AtRateEN	DPEN	POWR[3:0]			
Reset			0b1	0b1	0b0100			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	dSOCen	TAlrtEn	LDMdl	–	DRCfg[1:0]		CPMode	–
Reset	0b0	0b1	0b0	–	0b10			–
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read		Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
0	15	Bit must be written 0.	Do not write 1.
0	14	Bit must be written 0.	Do not write 1.
AtRateEN	13	AtRate Enable	When this bit is set to 0, AtRate calculations are disabled and registers AtQResidual/AtTTE/ AtAvSOC/AtAvCap can be used as general purpose memory.
DPEN	12	Dynamic Power Enable	When this bit is set to 0, Dynamic Power calculations are disabled and registers MaxPeakPower/SusPeakPower/MPPCurrent/ SPPCurrent can be used as general purpose memory.
POWR	11:8	Sets the time constant for the AvgPower register	The default POR value of 0100b gives a time constant of 11.25s. The equation setting the period is: AvgPower time constant = 45s x $2^{(POWR-6)}$
dSOCen	7	SOC Change Alert Enable	Set this bit to 1 to enable alert output with the Status.dSOCi bit function. Write this bit to 0 to disable alert output with the Status.dSOCi bit. This bit is set to 0 at power-up.
TAlrtEn	6	Temperature Alert Enable	Set this bit to 1 to enable temperature based alerts. Write this bit to 0 to disable temperature alerts. This bit is set to 1 at power-up.
LDMdl	5	Load New Model	Host sets this bit to 1 in order to initiate firmware to finish processing a newly loaded model. Firmware clears this bit to zero to indicate that model loading is finished.
DRCfg	3:2	Deep Relax Time Configuration	00 for 0.8 to 1.6 hours, 01 for 1.6 to 3.2 hours, 10 for 3.2 to 6.4 hours and 11 for 6.4 to 12.8 hours.

BITFIELD	BITS	DESCRIPTION	DECODE
CPMode	1	Constant-Power Mode	Set to 1 to enable constant-power mode. If it is set to 0, AtRate/AvgCurrent is used for (At)TTE/(At)QResidual/(At)AvSOC/(At)AvCap. If it is set to 1, AtRate/AvgCurrent x AvgVCell / (AvgVCell + VEmpty) / 2 is used for those calculations

Temp (0x8)

The Temp register provides the temperature measured by the thermistor or die temperature.

BIT	15	14	13	12	11	10	9	8
Field	TEMP[15:8]							
Reset	0x1600							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	TEMP[7:0]							
Reset	0x1600							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TEMP	15:0	This is the most recent trimmed temperature measurement. Temperature is measured every 1.4 seconds	Register type: temperature When using AIN for temperature (Tex = 0), configure TGain and TOff to adjust the AIN measurement to provide units degrees in the high-byte of Temp. When TGain and TOff are configured properly for the selected thermistor, the LSB is 0.0039˚C and the upper Byte has units 1°C. Temp is a signed register. To configure the BT07 to receive temperature information from the I^2C, set Tex = 1 and periodically write the Temp register with the appropriate temperature.

Vcell (0x9)

VCell reports the voltage measured between BATT and CSP.

BIT	15	14	13	12	11	10	9	8
Field	VCELL[15:8]							
Reset	0xB400							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	VCELL[7:0]							
Reset	0xB400							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VCELL	15:0	This is the most recent trimmed cell voltage result. It represents an FIR average of raw results. The VOLT_Raw is sampled every 175.8ms and gain and offset trim are applied to calculate VCELL.	Register type: voltage

Current (0xA)

The MAX77658 uses internal current sensing to monitor the current through the SYS FG pin. The measurement value is stored in two's-complement format. Measurement that exceeds maximum and minimum current range is stored as maximum and minimum value. The current register has a LSB value of 33.487µA, a register scale of 1.097A, and an allowable measurement range as described in the Absolute Maximum Ratings

BIT	15	14	13	12	11	10	9	8
Field	Current[15:8]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	Current[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
Current	15:0		Register type: current

AvgCurrent (0x0B)

The AvgCurrent register reports an average of Current register readings.

BIT	15	14	13	12	11	10	9	8
Field	AvgCurrent[15:8]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AvgCurrent[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvgCurrent	15:0	This is the 0.7s to 6.4hr (configurable) IIR average of the current. This register represents the upper 16 bits of the 32-bit shift register that filters current. The average should be set equal to Current upon startup.	Register type: current

AvgTA (0x16)

The AvgTA register reports an average of the readings from the Temp register.

BIT	15	14	13	12	11	10	9	8
Field	AvgTA[15:8]							
Reset	0x1600							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AvgTA[7:0]							
Reset	0x1600							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvgTA	15:0	This is the 6min to 12hr (configurable) IIR average of the Temperature.The average is set equal to Temp upon startup.	Register type: temperature

AvgVCell (0x19)

The AvgVCell register reports an average of the VCell register readings.

BIT	15	14	13	12	11	10	9	8
Field	AvgVCELL[15:8]							
Reset	0xB400							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AvgVCELL[7:0]							
Reset	0xB400							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvgVCELL	15:0	This reports the 12s to 24min (configurable) IIR average of VCELL.The average is set equal to VCELL at startup.	Register type: voltage

MaxMinTemp (0x1A)

The MaxMinTemp register maintains the maximum and minimum Temp register values since the last fuel-gauge reset or until cleared by host software. At power-up, the maximum value is set to 0x80 (most negative) and the minimum value is set to 0x7F (most positive). Therefore, both values are changed to the Temp register reading after the first update. Host software can rest this register by writing it to its power-up value of 0x807F. The maximum and minimum temperatures are each stored as two's complemetn 8-bit values with 1°C resolution.

BIT	15	14	13	12	11	10	9	8
Field	MaxTemperature[7:0]							
Reset	0x80							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	MinTemperature[7:0]							
Reset	0x7F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MaxTemperature	15:8	Records the maximum Temperature	Register type: special Two's complement 8-bit value with 1°C resolution
MinTemperature	7:0	Records the minimum Temperature.	Register type: special Two's complement 8-bit value with 1°C resolution

MaxMinVolt (0x1B)

The MAXMINVolt register maintains the maximum and minimum of VCell register values since device reset. At power-up, the maximum vaoltage is set to 00h (the minimum) and the minimum voltage value is set to FFh (the maximum). Therefore, both values are changed to the voltage register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x00FF. The maximum and minimum voltasges are each stored as 8-bit values with a 20mV resolution.

BIT	15	14	13	12	11	10	9	8
Field	MaxVoltage[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	MinVoltage[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MaxVoltage	15:8	Records the VCELL maximum voltage.	Register type: special The maximum and minimum voltages are each stored as 8-bit values with a 20mV resolution.
MinVoltage	7:0	Records the VCELL minimum voltage.	Register type: special The maximum and minimum voltages are each stored as 8-bit values with a 20mV resolution.

MaxMinCurr (0x1C)

The MaxMinCurr register maintains the maximum and minimum Current register values since the last IC reset or until cleared by host software. At power-up, the maximum current value is set to 80h (most negative) and the minimum current value is set to 7Fh (most positive). Therefore, both values are changed to the Current register reading after the first update. Host software can reset this register by writing it to its power-up value of 0x807F. The maximum and minimum currents are each stored as two's complent 8-bit values with 8mA resolution.

BIT	15	14	13	12	11	10	9	8
Field	MaxChargeCurrent[7:0]							
Reset	0x80							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	MaxDisCurrent[7:0]							
Reset	0x7F							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
MaxChargeCurrent	15:8	Records the maximum charge current.	Register type: special Two's complement 8-bit values with 8.57mA resolution.
MaxDisCurrent	7:0	Records the maximum discharge current.	Register type: special Two's complement 8-bit values with 8.57mA resolution.

AIN0 (0x27)

The external temperature measurement on the TH pin is compared to the BATT pin voltage.

BIT	15	14	13	12	11	10	9	8
Field	AIN0[15:8]							
Reset	0x88D0							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AIN0[7:0]							
Reset	0x88D0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AIN0	15:0	The TGain, TOff, and Curve register values are then applied to this ratio-metric reading to convert the result to temperature.	Register type: special The MAX77658 stores the result as a ratio-metric value from 0% to 100% in the AIN register with an LSB of 0.0122%.

Timer (0x3E)

TimerH and Timer provide a long-duration time count since last POR.

BIT	15	14	13	12	11	10	9	8
Field	TIMER[15:8]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	TIMER[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TIMER	15:0	Timer increments once every task period. With default TaskPeriod, timer has units 0.1758 seconds.The timer manages the following tasks: 1) Thermistor measurements occur once every 8 tasks. 2) Debouncing repeats for 8 TIMER ticks. 3) dV is measured based on dTthr TIMER ticks.	Register type: special The Timer register LSb is 175.8ms, giving a full-scale range of 0 to 3.2 hours.

TimerH (0xBE)

TimerH and Timer provide a long-duration time count since last POR.

BIT	15	14	13	12	11	10	9	8
Field	TIMERH[15:8]							
Reset	0x0000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	TIMERH[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TIMERH	15:0	TIMERH is a 16-bit high-word extension to the TIMER register. This extension allows time counting up to 24 years. This register can be enabled in the save and restore registers	Register type: special A 3.2-hour LSb gives a full-scale range for the register of up to 23.94 years.

RepCap (0x05)

RepCap is the reported remaining capacity in mAh.

BIT	15	14	13	12	11	10	9	8
Field	RepCap[15:8]							
Reset	0x05DC							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	RepCap[7:0]							
Reset	0x05DC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RepCap	15:0	RepCap or reported capacity is a filtered version of the AvCap register that prevents large jumps in the reported value caused by changes in the application such as abrupt changes in tempreature or load current	Register type: capacity

RepSOC (0x06)

RepSOC is the reported state-of-charge percenttage output for use by the application GUI

BIT	15	14	13	12	11	10	9	8
Field	RepSOC[15:8]							
Reset	0x3200							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	RepSOC[7:0]							
Reset	0x3200							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RepSOC	15:0	RepSOC is the complete calculation for State of Charge. This includes all processing, including: ModelGauge Mixing, Empty Compensation	Register type: percentage

AvSOC (0xE)

The AvSOC registers hold the calculated available percentage of the battery based on all inputs from the ModelGauge m5 algorithm, including empty compensation. This register provides unfiltered results. Jumps in the reported values can be caused by abrupt changes in load current or temperature. Refer to the *ModelGauge m5 EZ User Guide* for details.

BIT	15	14	13	12	11	10	9	8
Field	AvSOC[15:8]							
Reset	0x3200							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AvSOC[7:0]							
Reset	0x3200							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvSOC	15:0	This register provides unfiltered results. Jumps in the reported values can be caused by abrupt changes in load current or temperature. Refer to the *ModelGauge m5 EZ User Guide* for more details. This includes all processing, including: ModelGauge Mixing, Empty Compensation	Register type: percentage

FullCapRep (0x10)

This register reports the full capacity that goes with RepCap, generally used for reporting to the GUI.

BIT	15	14	13	12	11	10	9	8
Field	FullCapRep[15:8]							
Reset	0x0BB8							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	FullCapRep[7:0]							
Reset	0x0BB8							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
FullCapRep	15:0	Most applications should only monitor FullCapRep, instead of FullCap or FullCapNom. A new full-capacity value is calculated at the end of every charge cycle in the application.	Register type: capacity

TTE (0x11)

The TTE register holds the estimated time to empty for the application under present temperature and load conditions.

BIT	15	14	13	12	11	10	9	8
Field	TTE[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	TTE[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TTE	15:0	The TTE value is determined by relating AvCap with AvgCurrent. The corresponding AvgCurrent filtering gives a delay in TTE but provides more stable results.	Register type: time

RCell (0x14)

BIT	15	14	13	12	11	10	9	8
Field	RCell[15:8]							
Reset	0x0290							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	RCell[7:0]							
Reset	0x0290							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
RCell	15:0	This register provides the calculated internal resistance of the cell. RCell is determined by comparing open-circuit voltage (VFOCV) against measured voltage (VCell) over a long time period while under load or charge current.	Register type: resistance

Cycles (0x17)

BIT	15	14	13	12	11	10	9	8
Field	Cycles[15:8]							
Reset	0x0000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	Cycles[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
Cycles	15:0	Odometer style accumulation of battery cycles.	Register type: special The LSB indicates 1% of a battery cycle (1% charge + 1% discharge). One cycle (Cycles = 100%) indicates 100% charge and discharge.

AvCap (0x1F)

The AvCAP registers hold the calculated available capacity of the battery based on all inputs from the ModelGauge m5 algorithm, including empty compensation. This register provides unfiltered results. Jumps in the reported values can be caused by abrupt changes in load current or temperature. Refer to the *ModelGauge m5 EZ User Guide* for details.

BIT	15	14	13	12	11	10	9	8
Field	AvCap[15:8]							
Reset	0x05DC							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	AvCap[7:0]							
Reset	0x05DC							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
AvCap	15:0	This is the remaining capacity with coulomb-counter + Voltage-Fuel-Gauge mixing, after accounting for capacity that is unavailable due to the discharge rate.	Register type: capacity

TTF (0x20)

The TTF register holds the estimated time to full for the application under present conditions.

BIT	15	14	13	12	11	10	9	8
Field	TTF[15:8]							
Reset								
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	TTF[7:0]							
Reset								
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TTF	15:0	The TTF value is determined by learning the constant current and constant voltage portions of the charge cycle based on experience of prior charge cycles. Time-to-full is then estimated by comparing the present charge current to the charge termination current. Operation of the TTF register assumes all charge profiles are consistent in the application. The TTF register is only valid when the current register is positive.	Register type: time

Typical Application Circuits

Typical Applications Circuit

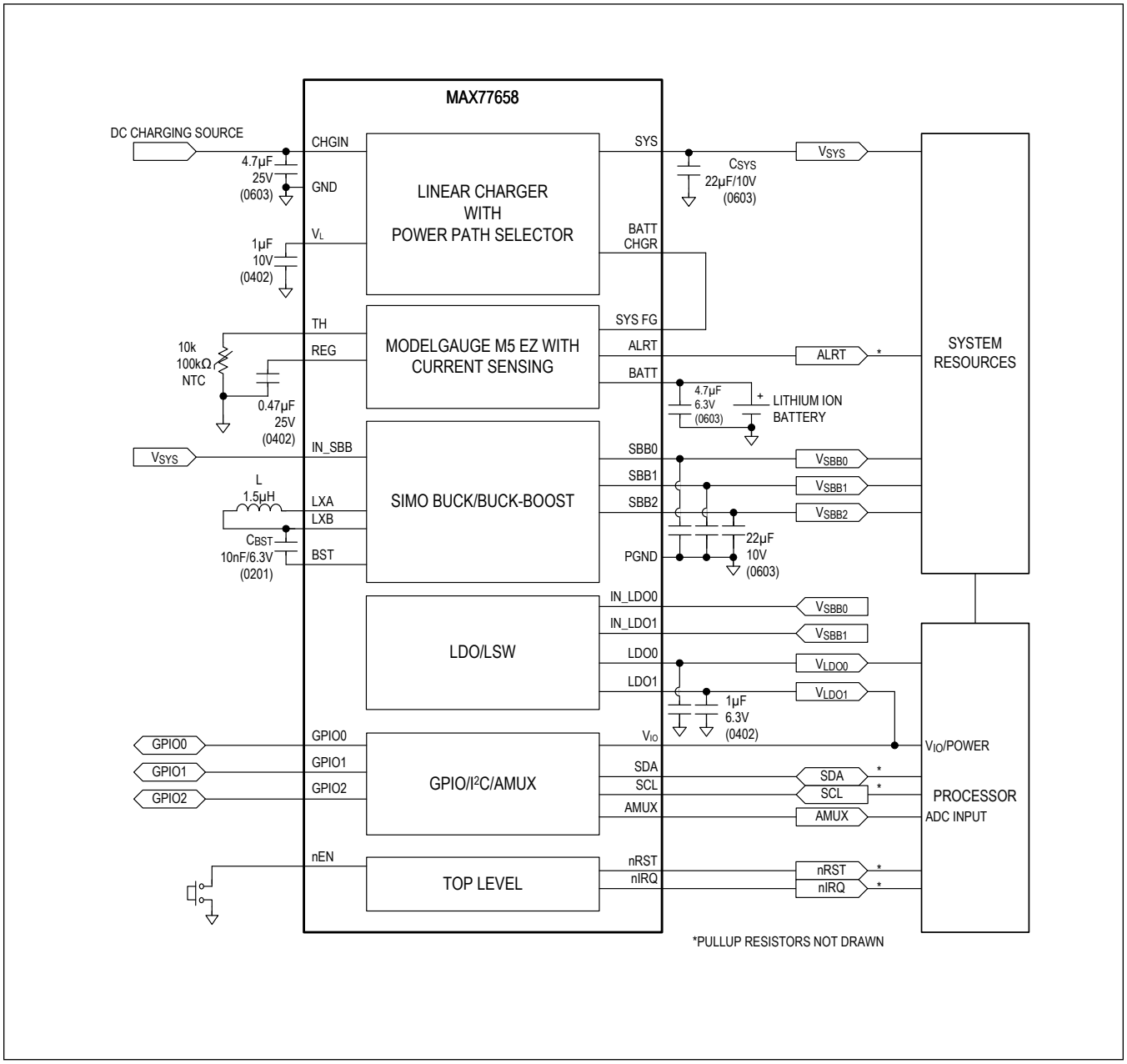


Figure 39. Typical Application Circuit

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	OPTIONS
MAX77658ANX+*	-40°C to +125°C	36 WLP	
MAX77658AANX+T	-40°C to +125°C	36 WLP	Table 2
MAX77658BANX+T**	-40°C to +125°C	36 WLP	Table 2

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Custom samples only. Not for production or stock. Contact factory for more information.*

***Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/21	Initial release	—