AW7698N Datasheet

Version: 1.8

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Document Revision History

Revision	Date	Description
1.0	4 Mar. 2019	Initial draft
1.1	5 Aug. 2019	Revise BT pinmux table
1.2	5 Sep. 2019	Update Wi-Fi power performance and BLE current consumption
1.3	22 Oct. 2019	Updated operating condition
1.4	4 Nov. 2019	Added 3 rows for mode selection
1.5	20 Nov. 2019	Removed flash in the diagram
1.6	2 Dec. 2019	Removed 40MHz
1.7	9 Dec. 2019	Fixed table 11.1-1
1.8	13 Dec. 2019	Fixed table 11.2-2

Features

Wi-Fi

- IEEE 802.11 b/g/n (2.4GHz, 1x1)
- Supports 20MHz, 40MHz bandwidth in 2.4GHz band
- Wi-Fi security WEP/WPA2/WPS
- SoftAP, sniffer
- Dynamically switching between STA and SoftAP modes at runtime
- Airoha Smart Connection
- Multi-cloud connectivity
- RX antenna diversity
- Integrated balun, PA/LNA
- Optional external LNA and PA support
- Support Wi-Fi/BLE coexistence

Microcontroller subsystem of Wi-Fi

- 192MHz ARM® Cortex®-M4 with FPU
- 16 DMA channels
- An RTC timer, one 64-bit and five 32-bit general purpose timers
- Hardware DFS from 3MHz to 192MHz
- Development support: SWD, JTAG
- Crypto engine
    - AES 128, 192, 256 bits
    - DES, 3DES
    - MD5, SHA-1, 224, 256, 384, 512
- True random number generator
- JTAG password protection

Memory of Wi-Fi

- Up to 384KB SRAM, with zero-wait state, max frequency 96MHz
    - Up to 32KB L1 cache, with high hit rate, zero-wait state, maximum frequency at 192MHz

Communication interfaces of Wi-Fi

- An SDIO 2.0 master or SDIO 2.0 slave
- Two I2C (3.4Mbps) interfaces
- Two UART interfaces (3Mbps)
- An SPI master or SPI slave with up to 48MHz SCK, quad mode
- One I2S interfaces
    - 16/24-bit, master/slave mode;
    - TX/RX channels with 16, 24, 48, 96, 192, 11.025, 22.05 and 44.1kHz frequencies
- Six PWM channels
- 16 GPIOs (fast IOs, 5V-tolerant)
- Four channels of 12-bit AUXADC

Power management of Wi-Fi

- Integrated DC-DC
- Power input
    - V_{RTC}: from 1.62V to 3.63V
    - V_{PMU} / V_{RF}: 3.3V (+/-10%)
    - V_{IO*}: 1.8V, 2.8V, 3.3V (+/-10%)
- Off mode: <0.5μA
- Retention mode (with RTC)
    - <2.7μA (RTC only)
    - ~4.7μA with 8KB RAM sleep mode
- Deep sleep mode (with external 32kHz clock, SDIO off)
    - 90μA with 0KB RAM sleep mode
    - 118μA with 384KB RAM sleep mode
- G-band RX power: 42mA
- G-band TX power
    - FPA: 248mA 19dBm CCK

  - FPA: 220mA 16.5dBm OFDM

- DTIM interval with 32kHz external clock source and 384KB SRAM
  - DTIM=1: 0.95mA
  - DTIM=3: 0.30mA

- Ambient temperature from -40°C to 105°C

Bluetooth subsystem

- Integrated 1.8V switching regulator & 1.8V LDO regulator
- Support BLE (Bluetooth low energy) 5.0 including BLE 1M/2M/long range and BLE extended advertising features
- Support 8 data link connection
- Support 128bit AES

Clock source

- 26MHz crystal oscillator
- 32Mhz crystal oscillator
- 32kHz crystal oscillator or internal 32kHz RC for RTC

Package type

- 7.1-mm x 7.1-mm x 1.05-mm 122 balls TFBGA with 0.5-mm ball pitch

Note:
The power consumption data is measured at 25°C.

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Lists of Tables and Figures

1. Overview of Wi-Fi System

AW7698N is a highly integrated chipset featuring an application processor, a low-power 1x1 11n single-band Wi-Fi sub-system, a low-power Bluetooth sub-system and a power management unit (PMU).

The Wi-Fi subsystem of AW7698N is based on ARM® Cortex®-M4 with floating point microcontroller unit (MCU). The Wi-Fi subsystem contains 802.11b/g/n radio, baseband and MAC designed to meet both low-power and high throughput application requirements. It also contains a 32-bit RISC CPU to fully offload the application processor.

The Bluetooth subsystem integrates baseband, radio for mesh controllers, mobile payments, and wearable device applications. It meets the Bluetooth version 5.0 specification.

AW7698N also supports interfaces including UART, I2C, SPI, I2S, PWM, SDIO and ADC.

1.1. Platform features

1.1.1. Micro-controller subsystem

- ARM® Cortex®-M4 with FPU as application processor with maximum frequency at 192MHz
- 32KB L1 cache with high hit rate and zero wait state, with maximum frequency at 192MHz
- 384KB SYSRAM with zero wait state, with max frequency at 96MHz
- Crypto engine that supports AES, DES/3DES, MD5, SHA1/SHA2
- True random number generator
- Single RTC timer, one 64-bit and five 32-bit general purpose timers (GPTs)
- 16 DMA channels
- Up to 16 GPIO interfaces with 5V-tolerant fast IOs; Each IO can be configured as an external interrupt source
- 23 GPO interfaces.

1.1.2. Interfaces

Up to two PWM channels are multiplexed with GPO. In addition, the following interfaces are multiplexed with GPIO.

- One SPI master interface, 1, 2 or 4-bit mode, up to 48MHz or SPI slave interface, 1, 2 or 4-bit mode, up to 48MHz
- One SDIO host interface (v2.0) or SDIO device interface (v2.0)
- One I2S interface supporting 16 or 24-bit, master or slave mode
  (supports 16, 24, 48, 96, 192, 11.025, 22.05 and 44.1kHz sample rates, transmit or receive, two channels)
- Up to two UART interfaces with hardware flow control (~3Mbps)
- Up to two I2C master interfaces (3.4Mbps)
- Up to four channels of 12-bit ADC

- Up to six PWM channels

1.2. Wi-Fi subsystem features

1.2.1. Wi-Fi MAC

- Supports all data rates of 802.11g including 6, 9, 12, 18, 24, 36, 48 and 54Mbps
- Supports short GI and all data rates of 802.11n including MCS0 to MCS7
- Wi-Fi security WEP, WPA2 and WPS
- Supports SoftAP and sniffer modes
- Supports Airoha Smart Connection
- Supports multi-cloud connectivity
- Supports Wi-Fi/BLE coexistence

1.2.2. WLAN baseband

- 20 and 40MHz channels
- MCS0-7 (BPSK, r=1/2 through 64QAM, r=5/6)
- Supports greenfield, mixed mode and legacy modes
- Short guard interval
- Supports digital pre-distortion to enhance PA performance
- Supports RX antenna diversity

1.2.3. WLAN RF

- Integrated 2.4GHz PA and LNA and T/R switch
- Supports frequency band from 2402 to 2494MHz
- Single-ended RFIO with integrated balun
- Supports an optional external LNA and PA

1.2.4. Core processor

- Dedicated high-performance 32-bit RISC CPU N9 up to 160MHz clock speed
- Feasibility Wi-Fi host subsystem in Cortex-M4 MCU to support custom applications

1.3. System block diagram

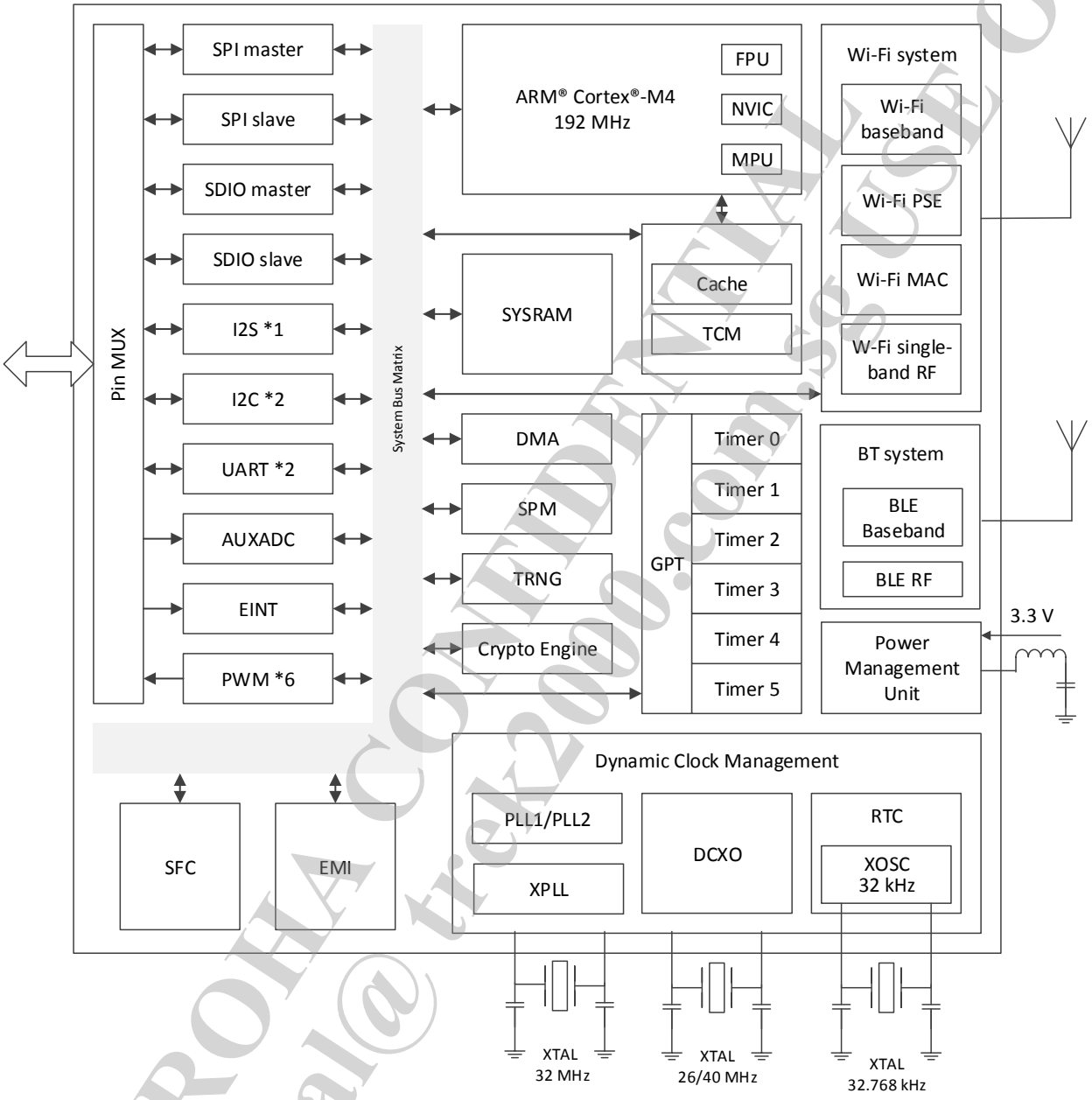


Figure 1.3-1. AW7698N system block diagram

2. Functional Overview of Wi-Fi

2.1. Host processor subsystem

2.1.1. ARM® Cortex®-M4 with FPU

The Cortex-M4 with FPU is a low-power processor with 3-stage pipeline Harvard architecture. It has reduced pin count and low-power consumption and delivers very high performance efficiency and low interrupt latency, making it ideal for embedded microcontroller products.

The processor incorporates:

- IEEE754-compliant single-precision floating-point computation unit (FPU).
- A Nested Vectored Interrupt Controller (NVIC) to achieve low latency interrupt processing.
- Enhanced system debugging with extensive breakpoint.
- An optional Memory Protection Unit (MPU) to ensure platform security robustness.

The Cortex-M4 executes the Thumb®-2 instruction set with 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers. The instruction set is fully backward compatible with Cortex-M3/M0+.

AW7698N has further enhanced the Cortex-M4 with FPU to reduce the power by another 11% (in Dhrystone) compared to the original Cortex-M4. Low-power consumption is a significant feature for IoT and Wearables application development.

2.1.2. Cache controller

A configurable 32KB cache is implemented to improve the code fetch performance when the CPU accesses a non-zero wait-state memory such as EMI, external flash or boot ROM through the on-chip bus.

The core cache is a small block of memory containing a copy of a small portion of cacheable data in the external memory. If the CPU reads a cacheable datum, the datum will be copied to the core cache. When the CPU requests the same datum again, it can be obtained directly from the core cache (called cache hit) to achieve zero wait-state latency, instead of fetching it again from the external memory.

The cache can be disabled and this block of memory can be turned into tightly coupled memory (TCM), a high-speed memory for normal data storage. The sizes of TCM and cache can be set to one of the following four configurations:

- 32KB cache, 64KB TCM
- 16KB cache, 80KB TCM
- 8KB cache, 88KB TCM
- 0KB cache, 96KB TCM

2.1.3. Memory management

One types of memories are implemented for use:

1) On-die memories (SRAMs) with up to 96KB at CPU clock speed with zero wait state.

The SRAMs are composed of TCMs and L1 caches. The L1 cache (up to 32KB) is implemented to improve processor access performance of the long latency memories (external flash).

TCMs are designed for high speed, low latency and low-power demanding applications. Each TCM has its own power state; active, retention or power-down. TCM must be in an active state for normal read and write access. Retention state saves the SRAM content and consumes the minimum leakage current with no access. Power-down loses the content and consumes almost zero power.

The TCMs can also be accessed by other internal AHB masters like DMA or multimedia subsystem for low-power applications. These applications can run on TCM without powering on flash to save more power.

Boot ROM is also implemented for processor boot–up and its content is unchangeable.

2.1.4. Memory protection unit (MPU)

The MPU is an optional component to manage the CPU access to memory. The MPU provides full support for:

- Protection regions (up to 8 regions and can be further divided up into 8 sub-regions).
- Overlapping protection regions, with region priority.
- Access permissions.
- Exporting memory attributes to the system.
- The MPU is useful for applications where a critical code must be protected against the misbehavior of other tasks. It can be used to define access rules, enforce privilege rules and separate processes.

2.1.5. Nested vectored interrupt controller (NVIC)

The NVIC supports up to 32 maskable interrupts and 16 interrupt lines of Cortex-M4 with 32 priority levels. The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked or nested interrupts to enable tail-chaining of interrupts. The processor supports both level and pulse interrupts with programmable active-high or low control.

2.1.6. External interrupt controller

The external interrupt controller consists of up to 32 edge detectors for generating event/interrupt requests. Each input line can be independently configured to select the type (interrupt or event) and the corresponding trigger event (rising edge or falling edge or both or level). Each line can also be masked independently. A pending register maintains the status line of the interrupt requests. Up to 18 GPIOs can be connected to 18 external interrupt lines.

2.1.7. Bus architecture

To better support various IoT applications, AW7698N adopts 32-bit multi-AHB matrix to provide low-power, fast and flexible data operation. Table 2.1-1 shows the interconnections between bus masters and slaves.

- The bus masters include Cortex-M4, SPM, SPI master, SPI slave, SDIO master, SDIO slave, Crypto engine, Wi-Fi connectivity system and DMA.
- The bus slaves include the Always On (AO) domain APB peripherals, Power Down (PD) domain APB peripherals, TCM, SFC, EMI, SYSRAM, RTC SRAM and Wi-Fi connectivity system.

Table 2.1-1. AW7698N bus connection

Master / Slave	ARM Cortex-M4	PD DMA	SPM	SPI Master	SPI Slave	SDIO Master	SDIO Slave	Crypto Engine	CONNSYS Master
AO APB Peripherals	●	●	●					●	
PD APB Peripherals	●	●	●					●	
TCM	●	●	●					●	
EMI	●	●	●	●	●	●	●	●	●
SFC	●	●	●					●	
SYSRAM	●	●	●	●	●	●	●	●	●
RTC SRAM	●	●	●	●	●	●	●	●	●
CONNSYS	●	●	●					●	

2.1.8. Direct memory access (DMA) controller

The AW7698N chipset features three DMA controllers, containing 16 channels in power down domain. They manage data transfer between the peripheral devices and memory.

There are three types of DMA channels in the DMA controller – full-size DMA channel, half-size DMA channel, and virtual FIFO DMA for different peripheral devices. DMA controllers support ring-buffer and double-buffer memory data transactions.

To improve the bus efficiency, the DMA controllers provide an unaligned-word access function. When this function is enabled, it can automatically convert the address format from the unaligned type to aligned type, ensuring compliance with the AHB/APB protocol.

Each peripheral device is connected to a dedicated DMA channel that can configure transfer data sizes, source address and destination address by software. The DMA controllers can be used with the following peripherals:

- Two I2C interfaces
- A single HIF
- One I2S interfaces
- Two UART interfaces

2.2. Boot source

There are three boot source options:

- External serial flash

- SPI slave (to load binary from host)
- SDIO slave (to load binary from host)

The host may transmit a binary through SPI slave or SDIO slave to internal SRAM. The MCU (Cortex-M4) can execute on internal SRAM after transmission is complete. The boot source in boot ROM is determined according to the flowchart shown in Figure 2.2-1. HIF_EN and HIF_SEL can be configured at power up using GPIO_4 and GPIO_13, respectively.

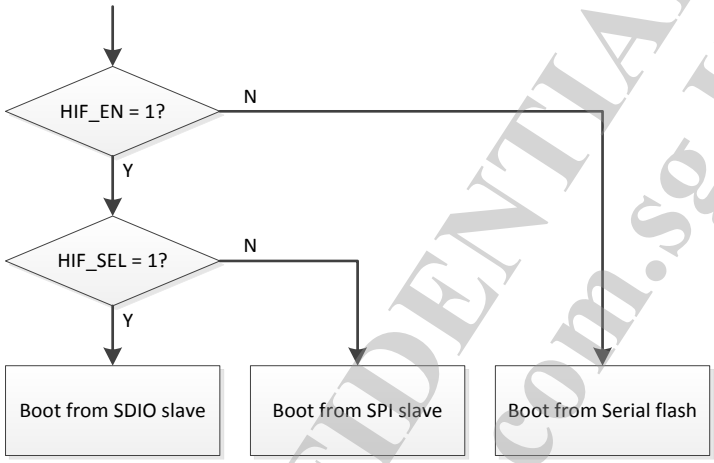


Figure 2.2-1. Boot source flow

2.3. Clock architecture

The clock controller (see below Figure 2.3-1) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler –** To get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching –** The clock sources can be changed safely at runtime through a configuration register.
- **Clock management –** To reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals, or memory. The AHB and APB clock supports Dynamic Clock Management (DCM) with a dynamic clock slow down or gating when the bus fabric is idle.
- **System clock source –** Two different clock sources can be used to drive the master clock (F_{CPU} and F_{BUS}):
  - 26MHz Crystal Oscillator (XO), that can supply reference clock for PLLs.
  - 32Mhz Crystal Oscillator (XO) is for the Bluetooth subsystem
  - 32Mhz quartz crystal resonator (XTAL) is for the Bluetooth subsystem
  - Baseband PLL1 (BBPLL1) with XO as a reference clock and a maximum frequency at 1040MHz.
  - Baseband PLL2 (BBPLL2) with XO as a reference clock or divided from BBPLL1 and a fixed frequency at 960MHz.
- **Auxiliary clock source –** Three ultra-low-power clock sources that can be used to drive the real-time clock F_FRTC_CK.

- Embedded EOSC32K is the default F_FRTC_CK clock source:
  - 32 kHz low-speed internal RC (EOSC32K) with ±5% variation
- The fifth bit (nm_trap_slow_src_sel) of SYSTEM_INFO is 1, users can switch to low-speed internal clock divided from Crystal Oscillator (XO) (XO_DIV_32K_CK) to get more accurate clock source:
  - XO_DIV_32K_CK is 32.745 kHz (0.07%).
- The fifth bit (nm_trap_slow_src_sel) of SYSTEM_INFO is 0, users can switch to XOSC32K:
  - 32.768 kHz low-speed external crystal (XOSC32K)

- **Peripheral clock sources –** Three types of peripheral clock source options are used. Each peripheral has its own gating register:
  - Several peripherals (SDIOMST (MSDC), SPIMST and SFC) have their own clock independent from the system clock. BBPLL1 and BBPLL2, each having independent outputs allowing the highest flexibility, can generate independent clocks for the SDIOMST (MSDC), SPIMST and SFC.
  - Clock of several peripherals including three I2Cs, crypto engine, DMA and more is the same as fast AHB/APB bus clock (FBUS).
  - Clock of several low speed peripherals (SEJ, AUXADC, EFUSE and more) is from F_FXO_CK (26MHz or 20MHz). The clock frequency of GPTIMER is from either F_FXO_D2_CK (13MHz or 10MHz) or F_RTC_CK (32kHz).
- **Clock-out**
  - Default output from CLKOUT pin (CLKO0~CLKO4) is the F_FRTC_CK clock. It also can output F_FXO_CK clock (26MHz or 20MHz) or XPLL clock (26MHz, 24.576MHz or 22.5792MHz) by setting GPIO_CLKO_CTRL_A and GPIO_CLKO_CTRL_B.

26MHz XO is selected on reset as the default CPU clock. This clock source is input to a set of cascaded PLL (BBPLL1 and BBPLL2) that enables the CPU frequency (F_{CPU}) to increase up to 192MHz when VCORE is 1.15V. Several prescalers allow the configuration of the fast bus clock, the maximum frequency of the AHB and APB bus (F_{BUS}) is 96MHz, while the maximum frequency of low-speed bus domains is 26MHz. The frequency ratio of F_{CPU} and F_{BUS} needs to be 2:1. The devices with an embedded low jitter XPLL achieve better I2S performance. The XPLL can output either 24.576MHz for 48kHz base I2S sample rate or 22.5792MHz for 44.1kHz base I2S sample rate.

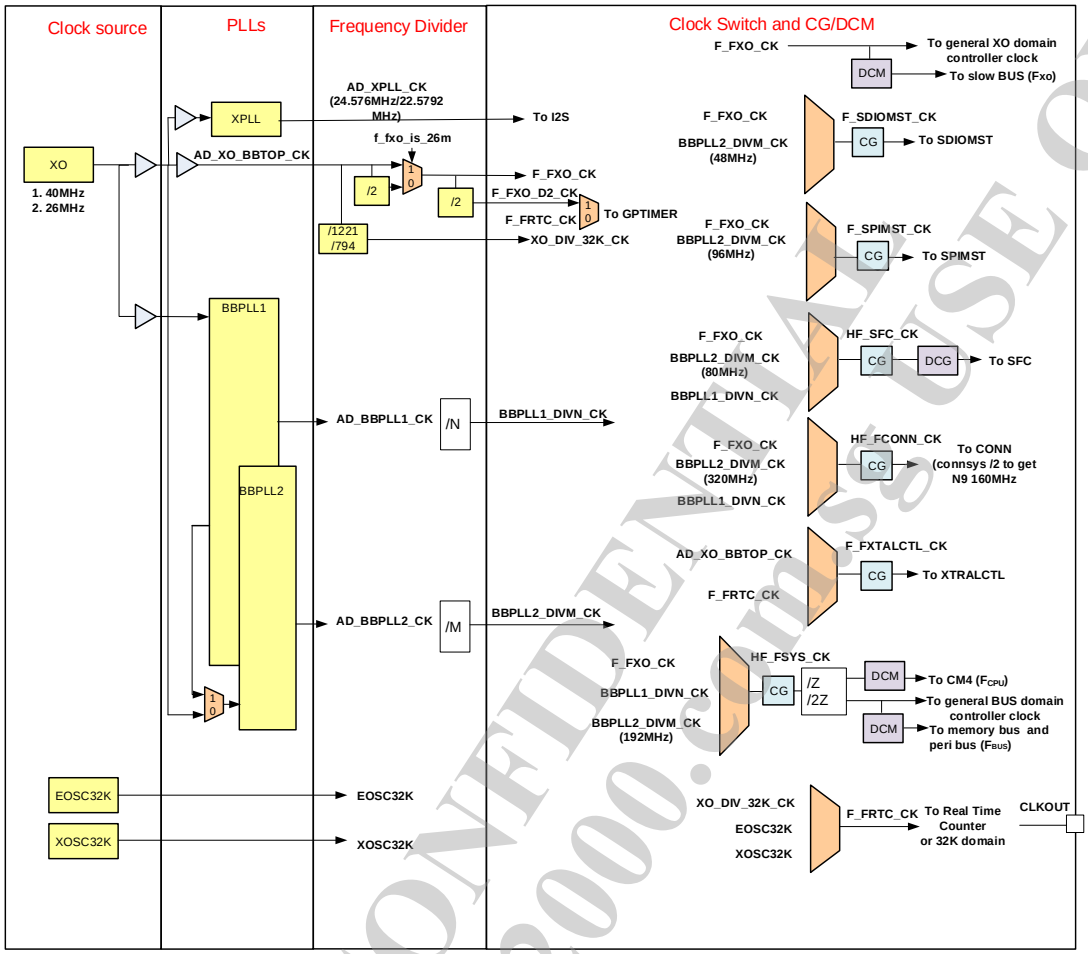


Figure 2.3-1. AW7698N clock source architecture

2.4. Analog baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are dedicated interfaces for data transfer. The dedicated data interface of each analog block is implemented in the corresponding digital block. Analog circuits include the following analog functions for data conversion and clocking purposes:

1) Auxiliary ADC — provides an ADC for the battery and other auxiliary analog functions monitoring.
2) Clock generation — a PLL providing clock signals to the audio interface unit.
3) XOSC32 — a 32kHz crystal oscillator circuit for RTC applications on analog blocks.

2.4.1. Auxiliary ADC

2.4.1.1. Block description

The auxiliary ADC includes the following functional blocks:

1) Analog multiplexer — selects a signal from one of the seven auxiliary input pins. Real-time signals, such as temperature are transferred and monitored in the voltage domain.
2) 12-bit A/D converter — converts the multiplexed input signal to 12-bit digital data.

Table 2.4-1. Auxiliary ADC input channel

Channel	Application	Input range [V]
0	AGPIO	0V to Min{AVDD25, VDDIO}
Others	No other channel used	N/A

2.4.1.2. Functional specifications

The functional specifications of the auxiliary ADC are listed in Table 2.4-2.

Table 2.4-2. Auxiliary ADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate			4	MHz
FS	Sampling rate at N-Bit		FC/(N+4)		MSPS
	Input swing	0		AVDD25	V
CIN	• Input capacitance ○ Unselected channel ○ Selected channel		 100 6.4		 fF pF
RIN	• Input resistance ○ Unselected channel ○ Selected channel	 400 0.2			 MΩ MΩ
	Clock latency		N+4		1/FC
DNL	Differential nonlinearity		± 1		LSB
INL	Integral nonlinearity		± 2		LSB
OE	Offset error (AVDD25 variation is not included, which is dependent on BG accuracy)		± 10		mV
FSE	Full swing error (AVDD25 variation is not included, which is dependent on BG accuracy)		± 10		mV
SINAD	Signal to noise and distortion ratio (1kHz full swing input and 4MHz clock rate)		65		dB
DVDD	Digital power supply		1.2		V
AVDD25	2.5V analog power supply for auxiliary ADC (regulated from AVDD33)	2.4	2.5	2.6	V
AVDD33	3.3V analog power supply for 2.5V LDO and 2.5V reference generator	3	3.3	3.6	V
T	Operating temperature	-40		105	°C
	Auxiliary ADC current consumption (from AVDD25)		280		µA
	• Selected channel AVDD33 current consumption (includes 2.5V LDO and 2.5V reference generator) ○ Power-up ○ Power-down		 750 1		 µA µA

2.4.2. Audio phase-locked loop (XPLL)

2.4.2.1. Overview

A low-cost fractional-N XPLL for general-purpose clocking is introduced in this section. The PLL is programmable to generate clocks ranging from 0.5GHz to 1.5GHz with a 7-bit integer and 24-bit fractional divisor. Low-to-high level shifters, self-bias circuit, and internal regulators are built-in to enhance portability and performance.

The XPLL design specifications are summarized in Table 2.4-3. Detailed setting instructions and restrictions are illustrated in following sections.

Table 2.4-3. XPLL design specifications

Mode		Support	Unit	Notes
	Input clock frequency (Fin)	0.1 to 120	MHz	After pre-divider
	Output clock frequency (Fout)	VDD=3.3±10% 500 to 1500	MHz	64 bands; need K-band
		VDD=2.5±10% 500 to 1000	MHz	64 bands; need K-band
SPEC	Feedback divide ratio (**integer-N**)	1 to 128		
	Output clock long-term jitter (delay 1us)	50ps RMS	ps	
	Output clock period jitter	50ps P-P	ps	
	Output clock phase jitter	100ps RMS	ps	
	Digital power supply (DVDD)	1.08 to 1.26	V	
	Analog power supply (AVDD)	2.25 to 3.63	V	
	Current consumption	< 3	mA	
	Power down current	< 1	µA	
	Operating temperature	-40 to 105	˚C	

2.4.2.2. Configuration and block diagram

The XPLL top block diagram with a fractional-N PLL and a bandgap bias circuit is shown in Figure 2.4-1. The bandgap bias circuit generates a temperature-independent bias current of 25µA for fractional-N XPLL usage.

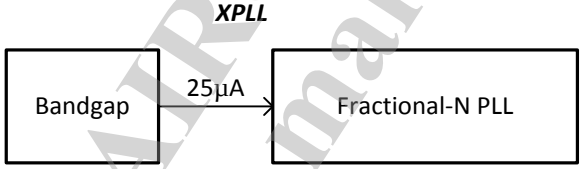


Figure 2.4-1. XPLL block diagram

Figure 2.4-2 shows the fractional-N PLL block diagram with typical PLL components such as phase frequency detector (PFD), charge pump (CHP), low pass filter (LPF), voltage-controlled oscillator (VCO) and several frequency dividers. The internal low dropout regulator (LDO) is used for improving the PSRR of sensitive blocks such as PFD, CHP, and VCO.

The PLL feedback divider is implemented by a 7-bit multi-module divider (MMD) which can operate at very high speed with wide divisor range. The MMD divisor is controlled by the DDS for fractional-N frequency multiplication.

The period-controlled word (PCW) of the DDS is a 31-bit binary number which consists of a 7-bit integer part and 24-bit fractional part. The pre-divider and post-divider are both simple binary dividers added to facilitate PLL frequency configuration.

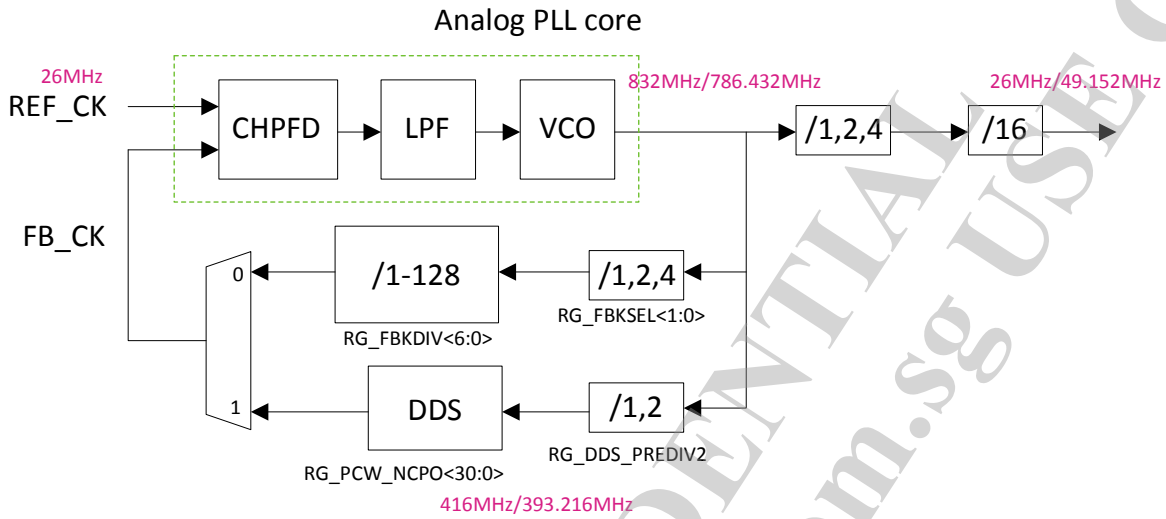


Figure 2.4-2. Fractional-N XPLL block diagram

2.4.3. External clock source

2.4.3.1. Digitally controlled crystal oscillator (DCXO)

The Digitally Controlled Crystal Oscillator (DCXO) uses a two-pin 26MHz crystal resonator. Crystals with a 1612 and a 3225 footprint are both supported. Please refer to Table 2.4-4 for the supported crystal resonator capacitance load and tuning sensitivity range. The on-chip programmable capacitor array is used for frequency-tuning, whereby the tuning range is ±50ppm. This DCXO supports 32kHz crystal-less operation.

Table 2.4-4. DCXO Characteristics (TA = 250C, VDD = 1.8V unless otherwise stated) (1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating frequency	Fref			26		MHz
Crystal C load	CL		6	7.5		pF
Crystal tuning sensitivity	TS		12.5	33		ppm/pF
Static range	SR	CDAC from 0 to 511		± 50		Ppm
Start-up time	TDCXO	Frequency error < 10ppm Amplitude > 90 %		0.6	2.5	Ms
Pushing figure				0.2		ppm/V
Fref buffer output level	VFref	Max. loading = 10pF		1.1		V_{p-p}
Fref buffer output phase noise		10kHz offset Jitter noise		-138		dBc/Hz

(1) Guaranteed by design, not tested in production.

2.4.3.2. 32kHz crystal oscillator (XOSC32)

The low-power 32kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. It is designed to be a clock source of RTC for lower-power platforms. Please refer to The minimum VRTC value means the minimum VRTC for the clock to stay alive is 1.4V when the crystal oscillator successfully starts.

The crystal parameters determine the oscillation allowance. Table 2.4-6 shows the recommend crystal parameters to be used with XOSC32.

Table 2.4-5 for more information about the key performance.

The minimum VRTC value means the minimum VRTC for the clock to stay alive is 1.4V when the crystal oscillator successfully starts.

The crystal parameters determine the oscillation allowance. Table 2.4-6 shows the recommend crystal parameters to be used with XOSC32.

Table 2.4-5. Functional specifications of XOSC32

Symbol	Parameter	Min.	Typical	Max.	Unit
VRTC	RTC module power		3.3		V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	30	50		%
	Current consumption		3		µA
T	Operating temperature	-40		105	°C

Table 2.4-6. Recommended parameters for 32kHz crystal

Symbol	Parameter	Min.	Typical	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level			1.5	µW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance		50	70	kΩ
C0	Static capacitance		0.9	2	pF
CL1	Load capacitance	6		12.5	pF

The –R is more than 3 times bigger with this CL range and crystal. If a larger CL is selected, the frequency accuracy decreases and the –R degrades.

2.5. Serial interfaces

2.5.1. Universal asynchronous receiver transmitter (UART)

The AW7698N chipset houses two UART interfaces that provide full duplex serial communication between the baseband chipset and external devices.

- The universal asynchronous receiver transmitter (UART) provides full duplex serial communication channels between the baseband chipset and external devices.

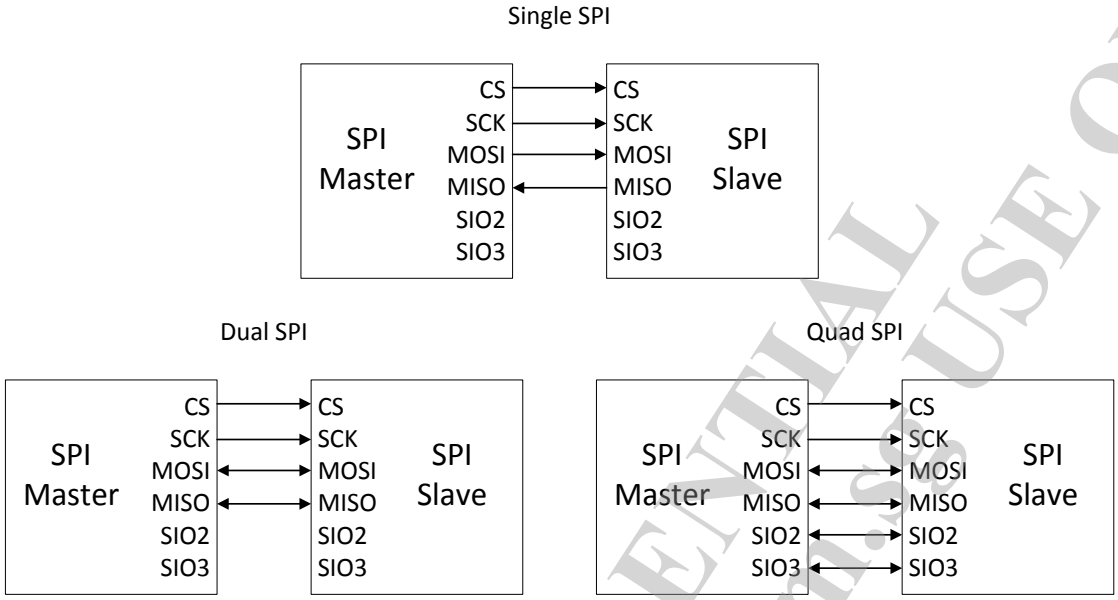
- The UART has both M16C450 and M16550A modes of operation that are compatible with a range of standard software drivers. The extensions are designed to be broadly software compatible with M16550A variants, but certain areas offer no consensus.
- The UART supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits and is fully programmable by an 8-bit CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included together with separate transmit and receive FIFOs. Two modem control lines and a diagnostic loop-back mode are provided. The UART also includes two DMA handshake lines, indicating when the FIFOs are ready to transfer data to the CPU.
- Note, that the UART is designed so that all internal operation is synchronized by the clock signal. This synchronization results in minor timing differences between the UART and industry standard M16550A device, which means that the core is not clocked for clock identical to the original device.
- After hardware reset, the UART will be in M16C450 mode. Its FIFOs can then be enabled and the UART can enter M16550A mode. The UART also has further additional functions beyond the M16550A mode. Each of the extended functions can be selected individually under software control.
- There are three UART channels supporting software flow control. Two of them support hardware flow control. Each UART has an individual interrupt source.
- For transmission, the UART supports word lengths from 5 to 8 bits with an optional parity bit and 1 or 2 stop bits.
- The UART supports standard baud rates of 110bps, 300bps, 1200bps, 2400bps, 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps, 921600bps and non-standard baud rates from 110bps to 3Mbps.
- There are dedicated DMA channels for both transmit (TX) and receive (RX) for each UART.

The UART supports automatic baud rate detection in RX mode. The recommended baud rate range is from 300bps to 115,200bps.

2.5.2. Serial peripheral interface (SPI)

The AW7698N chipset features one SPI master controller or one SPI slave controller to receive/transmit device data using single, dual and quad SPI protocols.

- The Serial Peripheral Interface (SPI) is a serial transmission protocol, which supports single mode (four-pin), dual mode (four-pin) and quad mode (six-pin) for increased data throughput. The maximum serial clock (SCK) frequency is 48MHz. Note that single mode can support full duplex, but dual and quad mode only support half duplex. Figure 2.5-1 is an example of the connection between the SPI master and SPI slave. Table 2.5-1 shows the characteristic of each pin.



- *Figure 2.5-1. Pin connection between SPI master and SPI slave*

Table 2.5-1. SPI master controller interface

Signal name	Type	Default value	Description
CS	O	1 (output)	Active low chip selection signal
SCK	O	0 (output)	The (bit) serial clock. Maximum SCK clock rate is 48MHz.
MOSI	I/O	1 (output)	Data signal 0
MISO	I/O	Pull down (input)	Data signal 1
SIO2	I/O	1 (output)	Data signal 2
SIO3	I/O	1 (output)	Data signal 3

-

2.5.2.1. SPI master controller

- The SPI master controller supports single mode, dual mode and quad mode. The controller can automatically switch port direction for data input/output according to registers SPIM_TYPE and SPIM_RW_MODE.
- The SCK frequency can be configured as 96/N MHz when core power is 1.1V or 1.3V, and 26/N MHz when core power is 0.9V, where N ranges from 2 to 2^{17}, with CPOL and CPHA features for different applications. CPOL defines the SCK polarity. CPHA defines the legal timing to sample data. The CS signal setup time, hold time and idle time can be configured, too. The detailed timing diagram of the SCK and CS is shown in Figure 2.5-2.

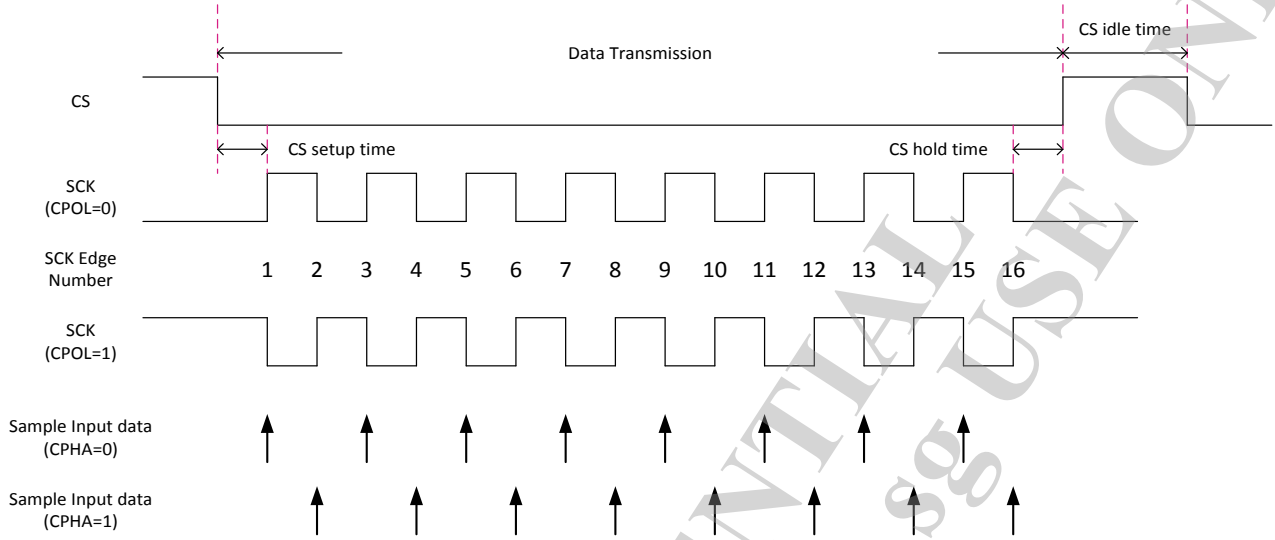


Figure 2.5-2. SPI transmission formats

- There are two modes for data read/write in SPI master controller:
  - Direct mode. The CPU directly write data to or read data from the SPI master controller FIFO.
  - DMA (Direct Memory Access) mode. The SPI master controller includes DMA design, which can automatically and continuously write data from memory to the SPI master controller or read data from the SPI master controller to memory. In DMA mode, the endian order of memory data is adjustable.
- Unlimited length transmission can be achieved by enabling pause mode. In pause mode, the CS signal stays active after one transfer. During this period, the SPI master controller is in **PAUSE_IDLE** state and waits for the resume command to start the next transfer. Figure 2.5-3 shows the state transition diagram.

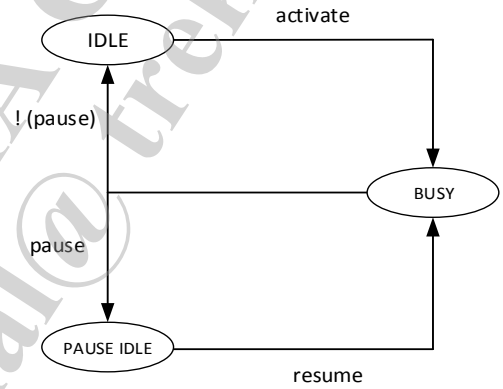


Figure 2.5-3. Operation flow with and without PAUSE mode

- A configurable option to control CS de-assertion between byte transfers is available. The SPI master controller supports a special transmission format called CS de-assert mode. Figure 2.5-4 illustrates the waveform in this transmission format.

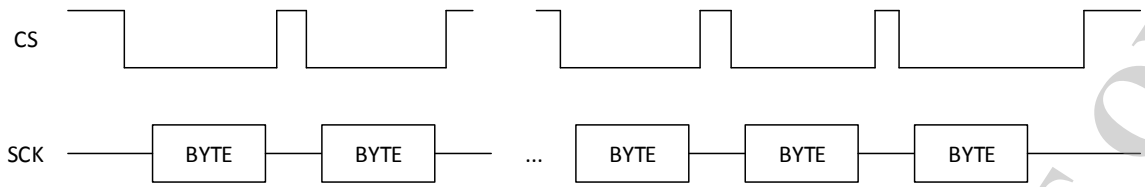


Figure 2.5-4. CS de-assert mode

- When the SPI master controller operates in dual or quad mode, the transmission package includes three parts: command phase, dummy phase and data phase.
  - Command phase always operates at single mode.
  - Dummy phase cannot transmit or receive data.
  - Data phase operation depends on **SPIM_TYPE** and **SPIM_RW_MODE** settings. The command phase and dummy phase are useful for special applications, such as read or write serial flash data.
- The sample clock, SCK and data delay is adjustable to solve the timing skew issue.
  - If the critical path latency between master and slave is larger than half of SCK cycle, the SPI master controller may samples the wrong data. The critical path of SPI transmission includes two parts:
    - Master transmits SCK to slave
    - Slave feeds back data to master

The sampling clock delay (register **SPIM_GET_DELAY**) and sampling edge (register **SAMPLE_SEL**) can be adjusted to solve this issue. Each interval of **SPIM_GET_DLY** is 10.42 ns. The detailed description is shown in Figure 2.5-5.

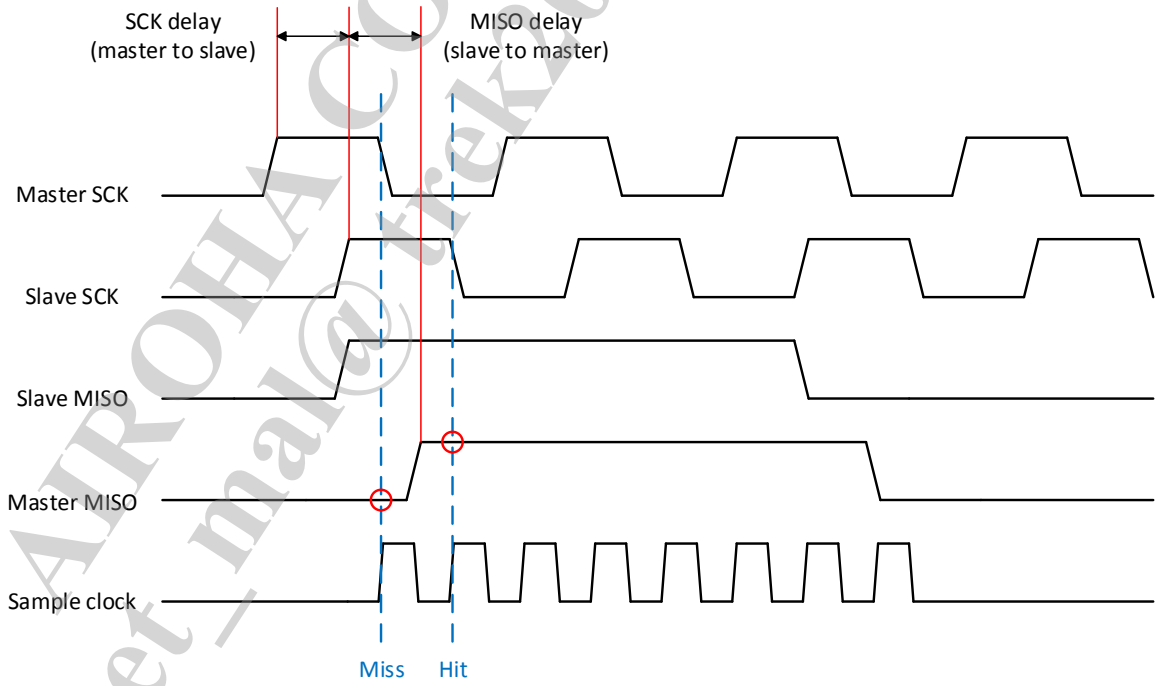


Figure 2.5-5. SPI master controller critical path sampling

- If the timing skew between SCK and data is too big, the received data on slave can be corrupted. This issue can be solved by adjusting the delay on SCK and data path (registers **SPIM_SEL_ADDR** and **SPIM_SEL_WDATA**), as shown in Figure 2.5-6.

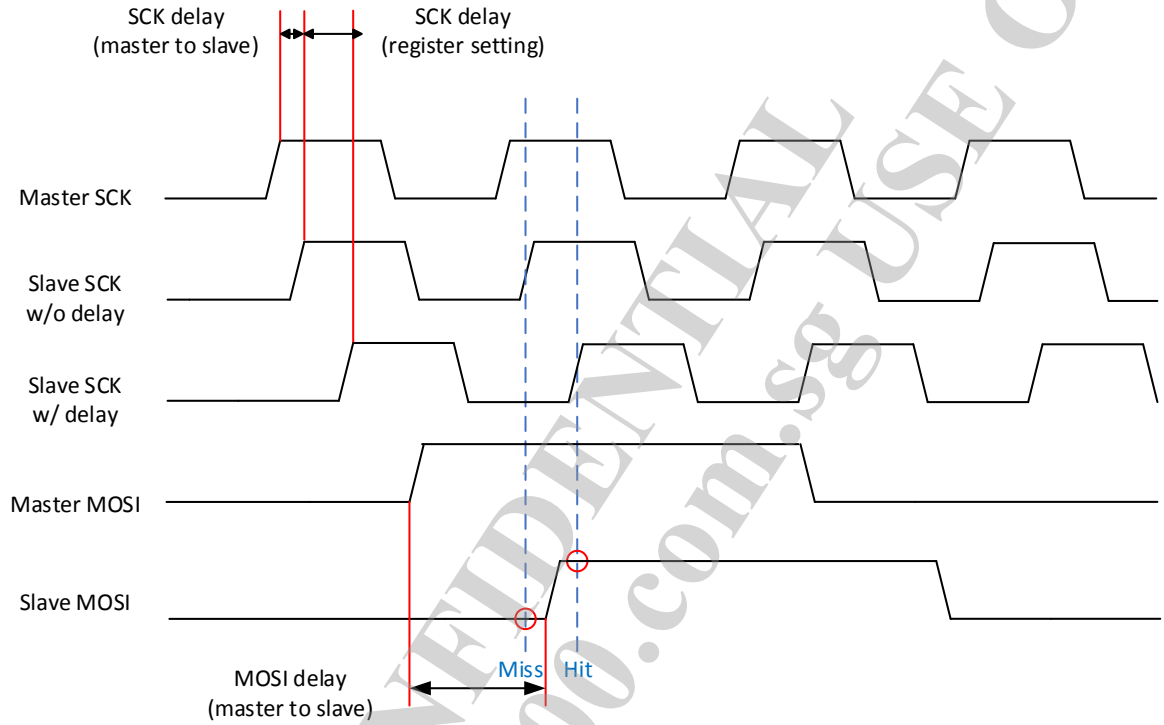


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Figure 2.5-6. SPI master controller SCK and data delay

2.5.2.2 SPI slave controller

- The SPI slave controller supports single mode, dual mode and quad mode. The controller can automatically switch port direction for data input/output according to register SPIS_TYPE.
- There are two methods to determine the memory address for SPI slave to write/read data
  - When **SPIS_DEC_ADDR_EN** is 0, the address is determined by SPISLV_BUFFER_BASE_ADDR and CW/CR command from the master. The address and length from master CW/CR command is stored in SPIS_TRANS_ADDR and SPIS_TRANS_LENGTH. The start address of the transfer is "SPISLV_BUFFER_BASE_ADDR + SPIS_TRANS_ADDR", and the end address is "SPISLV_BUFFER_BASE_ADDR + SPIS_TRANS_ADDR + SPIS_TRANS_LENGTH". The CW/CR command can only succeed if the end address does not exceed the maximum available memory address, which is "SPISLV_BUFFER_BASE_ADDR + SPISLV_BUFFER_SIZE".
  - When **SPIS_DEC_ADDR_EN** is 1, the address is directly determined by **SPISLV_BUFFER_BASE_ADDR**.
- The maximum SCK frequency supported is 48 MHz with CPOL and CPHA features. CPOL defines the SCK polarity. CPHA defines the legal timing to sample data. The detailed timing diagram of the SCK and CS is shown in Figure 2.5-7.

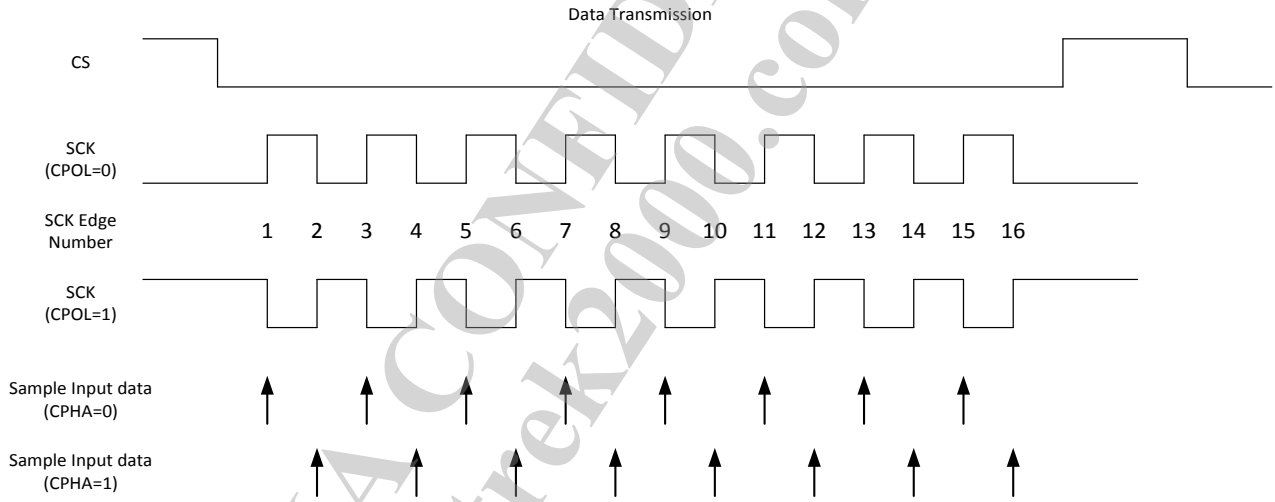


Figure 2.5-7. SPI transmission formats

- The SPI slave controller support early transmission feature to solve data path latency issue. The timing diagram is shown in
- Figure 2.5-8.

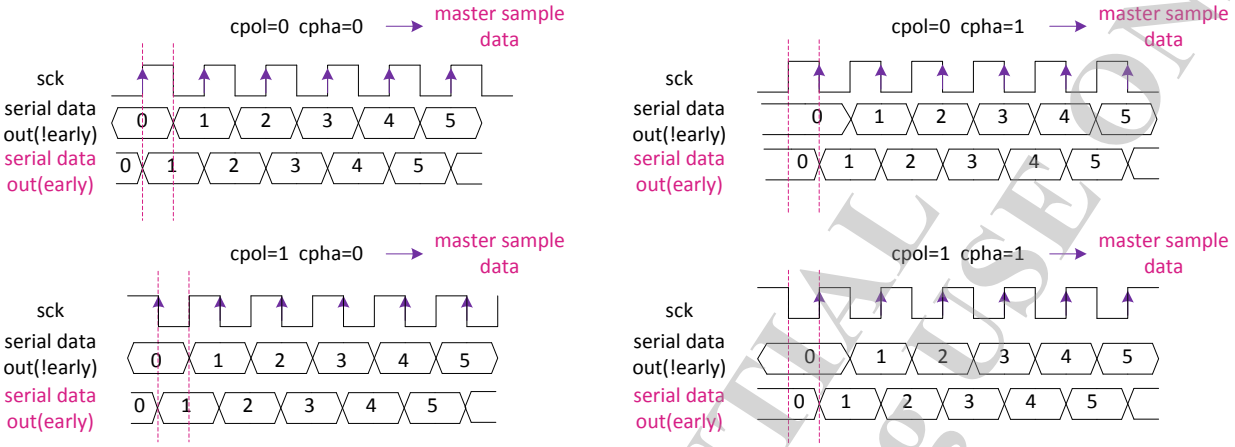


Figure 2.5-8. SPI slave controller early transmission

Inter-IC sound interface (I2S)

The AW7698N chipset provides one Inter-IC Sound Interface (I2S) controllers. The controllers can be selected as master or slave. There are two types of transfer protocols in the I2S controllers: one is the I2S protocol, supporting 24-bit/16-bit addressing and mono/stereo transaction; the other one is the TDM protocol, supporting 16-bit addressing and TDM32/TDM64/TDM128 transaction. I2S controllers can be served by the DMA controller and the sample rate can support either 16/24/48/96/192kHz or 11.025/22.05/44.1kHz when sharing only one internal PLL. Detailed specifications of the I2S and TDM are shown in Table 2.5-2 and Table 2.5-3.

Table 2.5-2. I2S protocol specifications

I2S Protocol	Bit Width	Input/output Sample
Master Mode	I2S0: 16b I2S1: 16b/24b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, mono/stereo XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4 kHz, mono/stereo XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192 kHz, mono/stereo
Slave Mode	I2S0: 16b I2S1: 16b/24b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, mono/stereo XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4 kHz, mono/stereo XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192 kHz, mono/stereo

Table 2.5-3. TDM protocol specifications

TDM Protocol	Bit Width	Input/output Sample
Master Mode	I2S0: 16b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, TDM32/TDM64 XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4 kHz, TDM32/TDM64 XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192 kHz, TDM32/TDM64
Slave Mode	I2S0: 16b	XO or XPLL 26MHz: 8, 12, 16, 24, 32, 48 kHz, TDM32/TDM64/TDM128 (up to 4 channels for TDM128) XPLL 22.5792MHz (either of the following): • 11.025, 22.05, 44.1, 88.2 kHz, TDM32/TDM64/TDM128 (up to 4 channels for TDM128) • 176.4 kHz, TDM32/TDM64 XPLL 24.576MHz (either of the following): • 8, 12, 16, 24, 32, 48, 96 kHz, TDM32/TDM64/TDM128 (up to 4 channels for TDM128) • 192 kHz, TDM32/TDM64

2.5.4. SD memory card controller

AW7698N supports SD memory card bus protocol, as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0.

Furthermore, the controller also partially supports the SDIO card specification version 2.0. However, the controller can only be configured as the host of the SD memory card.

Main features of the controller:

- 32-bit access for control registers
- 8, 16, or 32-bit access for FIFO in PIO mode
- Built-in CRC circuit
- Supports PIO mode, basic DMA mode and descriptor DMA mode for SD controller.
- Interrupt capabilities
- Data rate of up to 48Mbps in 1-bit mode, 48x4 Mbps in 4-bit mode. The module is targeted at 48MHz operating clock
- Programmable serial clock rate on SD bus (256 gears)
- Card detection capabilities (AW7698N uses the EINT controller for card detection)
- Does not support SPI mode for SD memory card
- Does not support suspend/resume for SD memory card.

2.6. Peripherals

2.6.1. Pulse-width modulation (PWM)

There are six PWM controllers to generate pulse signals. The duty cycle, high time and low time of pulse signals can be programmed. The PWM controllers can be configured to use 13MHz or 32kHz clock source to support a wide range of output pulse frequencies.

2.6.2. General purpose input/output (GPIO)

Each of the General Purpose Input/Output (GPIO) pins are software configurable as an output (push-pull or open-drain) or as an input (with or without pull-up or pull-down) that supports input floating with buffer gating to reduce power consumption. Most of the GPIOs are multiplexed with peripheral functions and have selectable output driving strength. The maximum toggling speeds of a single GPIO are listed in Table 2.6-1.

If the MCU handles more than one GPIO at a time or receives an interrupt, a rapid performance degradation may occur.

Dedicated IOs operate at higher speeds depending on the peripheral or interface usage. For example, PWM IOs can output 20 MHz when VCORE is 1.15V.

OD_GPIO includes OD_GPIO0_B/1_B/2_B. All of them are an open drain type output with a ground domain ESD, and can be used as LED drivers.

Table 2.6-1. GPIO speeds when the Cortex-M4 cache is enabled

VCORE	Cortex-M4 speed	Maximum toggling speed of single GPIO pins

VCORE	Cortex-M4 speed	Maximum toggling speed of single GPIO pins
1.15V	192MHz	1MHz
1.15V	96MHz	500kHz
0.85V	N/A	N/A (Cortex-M4 is in deep sleep mode)

2.6.3. General purpose timer (GPT)

The GPT includes five 32-bit timers and one 64-bit timer. Each timer has four operation modes and can operate on one of the two clock sources; RTC clock (32.768kHz) and system clock (13MHz).

2.6.4. Real time clock (RTC)

The RTC module provides time and data information, as well as 32.768kHz clock source. The clock is selected between three clock sources — one from an external (XOSC32) and two from an internal (XO, EOSC32). The RTC block has an independent power supply. When the AW7698N platform is at retention mode, a dedicated regulator will supply power to the RTC block. In addition to providing timing data, an alarm interrupt will be generated and can be used to power up the baseband core. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches the maximum value. The year span is supported until up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

2.6.5. True random number generator (TRNG)

The TRNG is a device in power-down domain that generates random numbers from the ring oscillator (RO) outputs. Various types of ROs are adopted, including Hybrid Fibonacci Ring Oscillator (H-FIRO), Hybrid Ring Oscillator (H-RO) and Hybrid Galois Ring Oscillator (H-GARO). Interrupt request (IRQ) will be issued once the random data is successfully generated.

3. RF Subsystem of Wi-Fi

3.1. Wi-Fi radio characteristics

3.1.1. Wi-Fi RF block diagram

Front-end loss with an external balun (2.4GHz band with band insertion loss of 1dB).

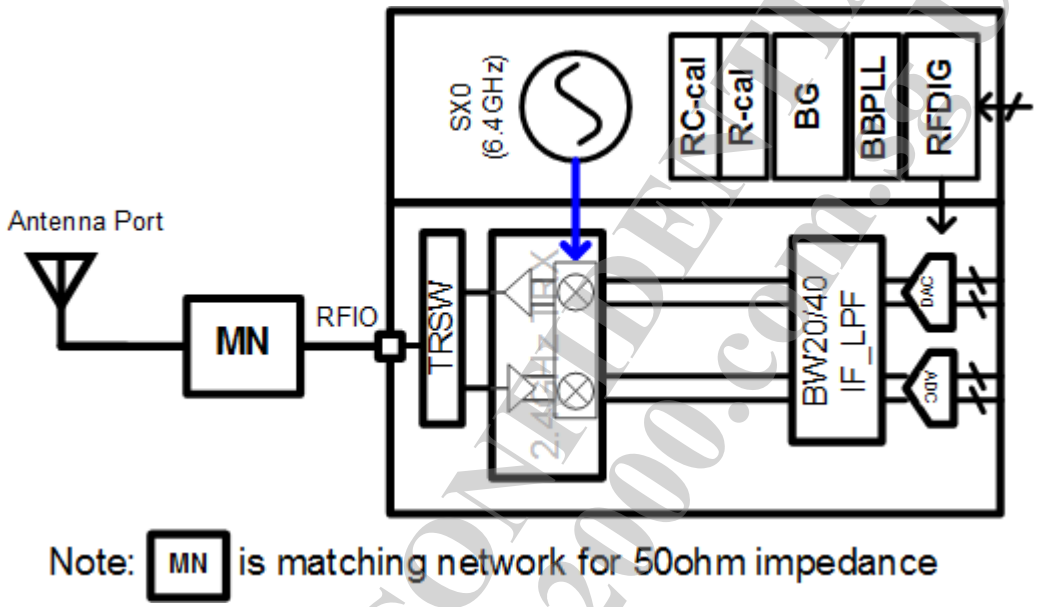


Figure 3.1-1. 2.4GHz RF Block Diagram

3.1.2. Wi-Fi 2.4GHz band RF receiver specifications

The specifications listed in Table 3.1-1 are measured at the antenna port, which includes the front-end loss.

Table 3.1-1. 2.4GHz RF receiver specifications

Parameter	Description	Performance			
		Minimum	Typical	Maximum	Unit
Frequency range	Center channel frequency	2412		2484	MHz
RX sensitivity	1 Mbps CCK	-	-97.5	-	dBm
	2 Mbps CCK	-	-94.5	-	dBm
	5.5 Mbps CCK	-	-92.5	-	dBm
	11 Mbps CCK	-	-89.5	-	dBm
RX sensitivity	BPSK rate 1/2, 6 Mbps OFDM	-	-94.5	-	dBm
	BPSK rate 3/4, 9 Mbps OFDM	-	-93.3	-	dBm
	QPSK rate 1/2, 12 Mbps OFDM	-	-91.5	-	dBm
	QPSK rate 3/4, 18 Mbps OFDM	-	-89.1	-	dBm
	16QAM rate 1/2, 24 Mbps OFDM	-	-85.8	-	dBm
	16QAM rate 3/4, 36 Mbps OFDM	-	-82.4	-	dBm
	64QAM rate 1/2, 48 Mbps OFDM	-	-78.2	-	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-	-77.0	-	dBm
RX sensitivity	MCS 0, BPSK rate 1/2	-	-93.9	-	dBm

Parameter	Description	Performance			
20MHz bandwidth Mixed mode 800ns guard interval Non-STBC	MCS 1, QPSK rate 1/2	-	-90.7	-	dBm
	MCS 2, QPSK rate 3/4	-	-88.3	-	dBm
	MCS 3, 16QAM rate 1/2	-	-85.3	-	dBm
	MCS 4, 16QAM rate 3/4	-	-81.8	-	dBm
	MCS 5, 64QAM rate 2/3	-	-77.4	-	dBm
	MCS 6, 64QAM rate 3/4	-	-76	-	dBm
	MCS 7, 64QAM rate 5/6	-	-74.8	-	dBm
RX sensitivity 40MHz bandwidth Mixed mode 800ns guard interval Non-STBC	MCS 0, BPSK rate 1/2	-	-90.5	-	dBm
	MCS 1, QPSK rate 1/2	-	-87.7	-	dBm
	MCS 2, QPSK rate 3/4	-	-85.2	-	dBm
	MCS 3, 16QAM rate 1/2	-	-81.7	-	dBm
	MCS 4, 16QAM rate 3/4	-	-78.6	-	dBm
	MCS 5, 64QAM rate 2/3	-	-74.0	-	dBm
	MCS 6, 64QAM rate 3/4	-	-72.7	-	dBm
	MCS 7, 64QAM rate 5/6	-	-71.5	-	dBm
Maximum receive level	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-20	-	dBm
Receive adjacent Channel rejection	1 Mbps CCK	-	40	-	dBm
	11 Mbps CCK	-	40	-	dBm
	BPSK rate 1/2, 6 Mbps OFDM	-	34	-	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-	22	-	dBm
	HT20, MCS 0, BPSK rate 1/2	-	33	-	dBm
	HT20, MCS 7, 64QAM rate 5/6	-	15	-	dBm
	HT40, MCS 0, BPSK rate 1/2	-	29	-	dBm
	HT40, MCS 7, 64QAM rate 5/6	-	9	-	dBm

3.1.3. Wi-Fi 2.4GHz band RF transmitter specifications

The specifications listed in Table 3.1-2 are measured at the antenna port, which includes the front-end loss.

Table 3.1-2. 2.4GHz RF transmitter specifications

Parameter	Description	Performance			
		Minimum	Typical	Maximum	Unit
Frequency range		2412	-	2484	MHz
Output power with spectral mask and EVM compliance	1 Mbps CCK	-	19	-	dBm
	11 Mbps CCK	-	19	-	dBm
	6 Mbps OFDM	-	18.5	-	dBm
	54 Mbps OFDM	-	16.5	-	dBm
	HT20, MCS 0	-	17.5	-	dBm
	HT20, MCS 7	-	15.5	-	dBm
	HT40, MCS 0	-	16.5	-	dBm
	HT40, MCS 7	-	14.5	-	dBm
TX EVM	6 Mbps OFDM	-	-	-5	dB
	54 Mbps OFDM	-	-	-25	dB
	HT20, MCS 0	-	-	-5	dB
	HT20, MCS 7	-	-	-28	dB
	HT40, MCS 0	-	-	-5	dB

Parameter	Description	Performance			
	HT40, MCS 7	-	-	-28	dB
Output power variation[1]	TSSI closed-loop control across all temperature ranges and channels and VSWR ≦ 1.5:1.	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic output power	Second harmonic	-	-45	-43	dBm/MHz
	Third harmonic	-	-45	-43	dBm/MHz

3.2. Radio MCU subsystem

3.2.1. CPU

AW7698N features the 32-bit N9 CPU, with the following features:

- 5-stage pipeline with extensive clock-gating
- Dynamic branch prediction with BTB
- 16/32-bit mixed instruction format
- Multiply-accumulate and multiply-subtract instructions
- Instructions optimized for audio applications
- Instruction and data local memory
- Programmable data endian control
- JTAG based debug interface

3.2.2. RAM/ROM

The radio MCU subsystem features instruction local memory (ILM), data local memory (DLM), and SYSRAM. The ROM code is in the ILM.

3.2.3. Memory map

Table 3.2-1 describes how peripherals are mapped to the memory space in the radio MCU subsystem. When the MCU performs a read transaction to an undefined address, the bus returns 0. When the MCU performs a write transaction to an undefined address, the bus regards it as an invalid transaction and does nothing.

Table 3.2-1. N9 memory map

Start address	End address	Function	Description
0x0000_0000	0x0000_FFFF	ILM ROM	Instruction local memory ROM for N9
0x0001_0000	0x0002_3FFF	ILM RAM	Instruction local memory RAM for N9
0x0010_0000	0x0010_7FFF	SYSRAM N9	System RAM for N9

[1] No SYSRAM data is retained in these scenarios.

Start address	End address	Function	Description
0x0200_0000	0x0200_021C	Patch & CR	N9 ROM patch engine
0x0209_0000	0x0209_7FFF	DLM RAM	Data local memory for N9
0x5000_0000	0x501F_FFFF	HIF_device	Host interface device controller
0x6000_0000	0x6FFF_FFFF	WIFISYS	Wi-Fi subsystem
0x7000_0000	0x70FF_FFFF	PDA DMA port	Patch decryption accelerator DMA slave
0x7800_0000	0x7800_0000	VFF access port0	Virtual FIFO access port 0 of N9 DMA
0x7800_0100	0x7800_0100	VFF access port1	Virtual FIFO access port 1 of N9 DMA
0x7900_0000	0x7900_FFFF	VFF_CM4 access port	Virtual FIFO access ports of Cortex-M4 DMA
0x8000_0000	0x800C_FFFF	APB0	APB bridge 0 (synchronous to N9)
0x8000_0000	0x8000_FFFF	CONFG	N9 subsystem configuration
0x8001_0000	0x8001_FFFF	DMA	Generic DMA engine for N9
0x8002_0000	0x8002_FFFF	TOP_CFG_OFF	TOP_OFF (N9) power domain chip level configuration (GPIO, PinMux, RF, PLL, clock control)
0x8008_0000	0x8008_FFFF	AHB_MON	AHB bus monitor
0x800A_0000	0x800A_FFFF	UART_DSN	UART for N9 debug
0x800B_0000	0x800B_FFFF	SEC	Secure boot configuration
0x800C_0000	0x800C_FFFF	HIF	Host interface configuration
0x8100_0000	0x810C_FFFF	APB1	APB bridge 1 (synchronous to N9)
0x8102_0000	0x8102_FFFF	TOP_CFG_AON	TOP_AON power domain chip level configuration (RGU, PinMux, PMU, XTAL, clock control)
0x8103_0000	0x8103_FFFF	DBG_CIRQ	Debug interrupt controller for N9
0x8104_0000	0x8104_FFFF	CIRQ	Interrupt controller for N9
0x8105_8000	0x8105_FFFF	GPT	General purpose timer for N9
0x8106_0000	0x8106_FFFF	PTA	Packet traffic arbitrator for Wi-Fi coexistence
0x8108_0000	0x8108_FFFF	WDT	Watchdog timer for N9
0x8109_0000	0x8109_FFFF	PDA	Patch decryption accelerator
0x810A_0000	0x810A_FFFF	RDD	Wi-Fi debug
0x810C_0000	0x810C_FFFF	RBIST	RF BIST configuration

Start address	End address	Function	Description
0x8300_0000	0x810C_FFFF	APB2	APB bridge 1 (synchronous to Cortex-M4)
0xA000_0000	0xAFFF_FFFF	PSE	Packet switch engine memory

3.2.4. N9 bus fabric

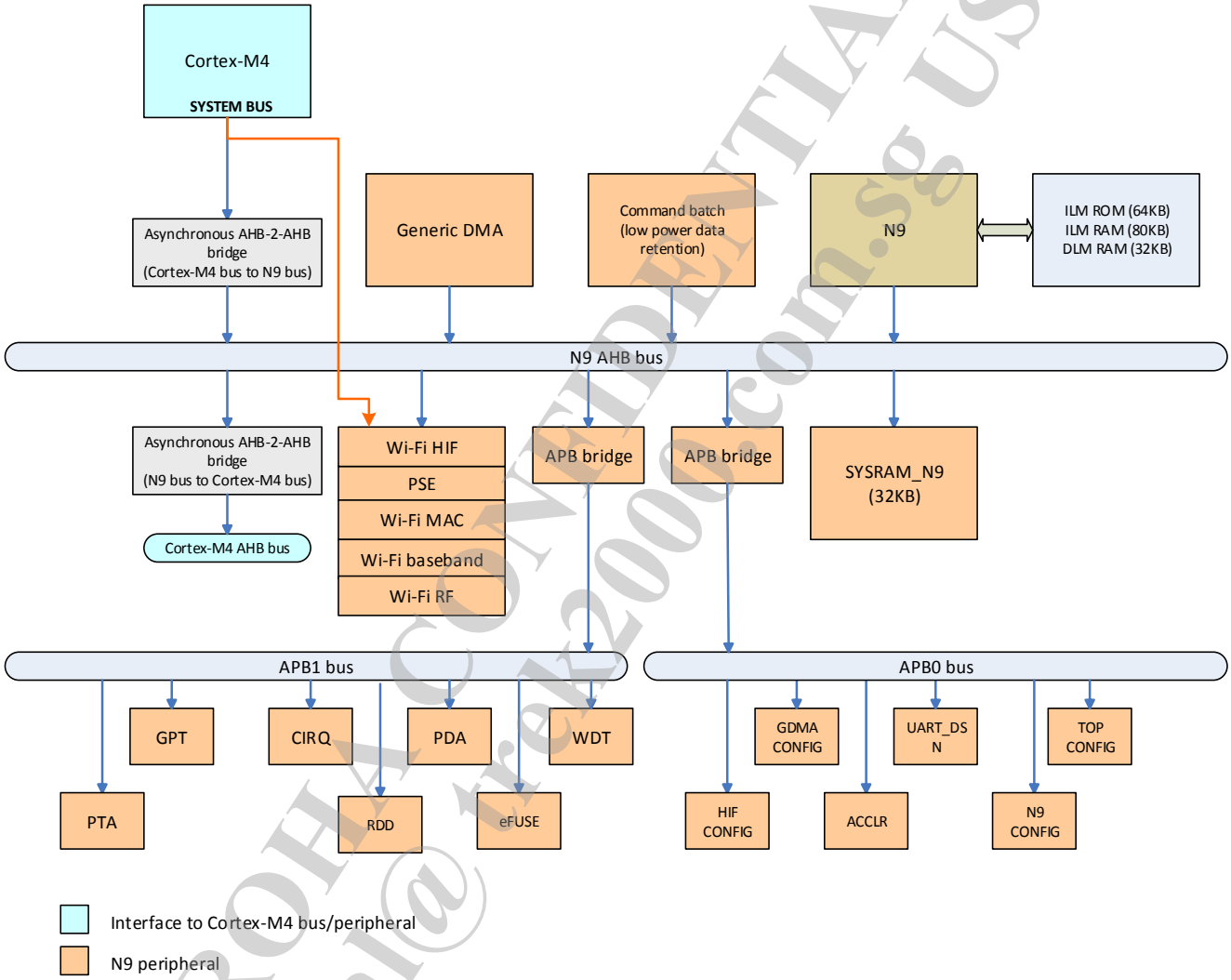


Figure 3.2-1. N9 bus fabric

N9 bus fabric functional description:

- Command batch: Used to save and restore critical CR and memory data when entering and leaving low-power mode.
- Wi-Fi HIF: The host control and data interface from N9 to Wi-Fi subsystem.
- Wi-Fi PSE: The packet switch engine used to transfer packets from N9 to Wi-Fi MAC/radio or from Cortex-M4 to Wi-Fi MAC/radio, and vice versa.
- PDA: Packet decryption agent, used to download firmware and decipher the encrypted firmware.

- PTA: Packet traffic arbitration, used to execute Wi-Fi traffic arbitration when the two radios are transmitting and receiving at the same time.
- RDD: The Wi-Fi debug function.
- eFUSE: The eFUSE macro used for Wi-Fi MAC and radio configuration.

3.2.5. CIRQ

N9 subsystem uses an interrupt controller CIRQ to control internal interrupt source selection, mask, edge/level sensitivity and software enabling, as well as external interrupt mask and edge/level sensitivity. CIRQ also integrates the de-bounce circuit for external interrupts.

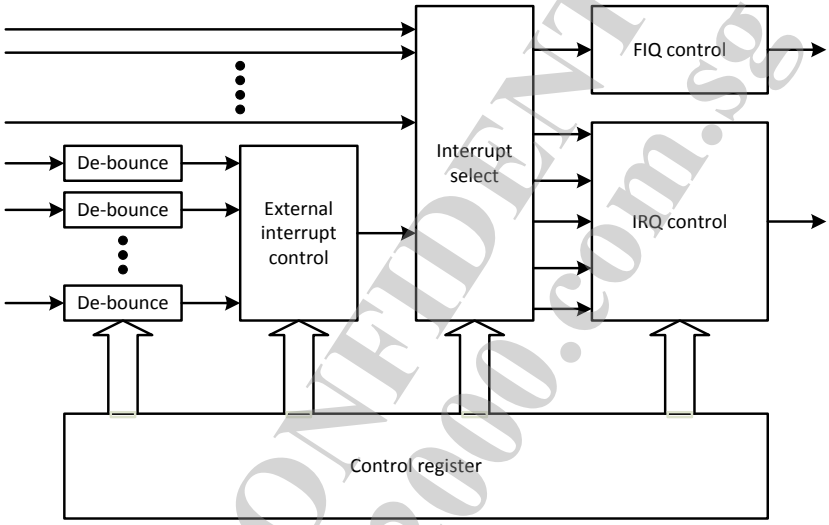


Figure 3.2-2. N9 interrupt controller

There are a total of 23 interrupts and 14 external interrupts. The power domain/subsystem lists the power domain and subsystem from which the interrupt is generated. Table 3.2-2 lists the interrupt sources of internal and external interrupts.

Table 3.2-2. N9 interrupt source

IRQ number	Interrupt source	Power domain /subsystem	External interrupt	Wake-up capability (1)	De-bounce	Description
INT0	(Reserved)					
INT1	DMA	CONN_OFF/MCUSYS				Generic DMA in N9 subsystem
INT2	HIFSYS	CONN_AON/HIF				WIFI_HIF(SDIO)
INT3	(Reserved)					
INT4	THERM	CONN_OFF				Thermometer
INT5	(Reserved)					
INT6	WIFI	CONN_OFF/MAC				Wi-Fi subsystem
INT7	ICAP	CONN_OFF/MCUSYS				Internal capture in RBIST module
INT8	EINT	CONN_AON/MCUSYS				External interrupt
INT9	(Reserved)					
INT10	WDT_N9	CONN_AON/MCUSYS				Watch dog timer in N9 subsystem

IRQ number	Interrupt source	Power domain /subsystem	External interrupt	Wake-up capability (1)	De-bounce	Description
INT11	AHB_MONITOR	CONN_OFF/MCUSYS				AHB monitor
INT12	(Reserved)					
INT13	PLC_ACCLR	CONN_OFF/MCUSYS				Packet Loss Concealment accelerator
INT14	(Reserved)					
INT15	PSE	CONN_OFF/PSE				Packet switch engine
INT16	(Reserved)					
INT17	HIFSYS	CONN_OFF/HIFSYS				HIF subsystem
INT18	(Reserved)					
INT19	PTA	CONN_OFF/MCUSYS				PTA module
INT20	CMBT	CONN_OFF				Command batch module
INT21	GPT3	CONN_AON/MCUSYS				General purpose timer module
INT22	N9_PM	CONN_OFF/MCUSYS				N9 performance monitor
EINT0	(Reserved)		V	V	Available	
EINT1	CM4_TO_N9_SW		V	V	Available	Cortex-M4 software interrupt N9
EINT2	HIFSYS	CONN_AON/HIF	V	V	Available	WIFI_HIF (SDIO)
EINT3	(Reserved)		V	V	Available	
EINT4	(Reserved)		V	V	Available	
EINT5	(Reserved)		V	V	Available	
EINT6	GPT	CONN_AON/MCUSYS	V	V	Available	General purpose timer module (GPT0 timer and GPT1 timer)
EINT7	(Reserved)		V	V	Available	
EINT8	(Reserved)		V	V	Available	
EINT9	DSLP_IRQ	CONN_AON	V	V	Available	Deep sleep control
EINT10	(Reserved)		V	V	Available	
EINT11	(Reserved)		V	V	Available	

Note 1: Capable to wake up N9 firmware when ''s in sleep mode.

4. Power Management Unit of Wi-Fi

4.1. Overview

The power management unit (PMU) manages the power supply of the entire chip, including baseband, processor, memory, camera, vibrator and more. There are two power input sources for AW7698N:

1) AVDD33_RTC for RTC timer control.

This is operated by wider input voltage range from 1.62V to 3.63V, and supports real time clock control and alarm logic. Because of the ultra-low input voltage and lower current consumption, it can efficiently enhance battery lifetime by alkaline or other portable batteries.

2) AVDD33_BUCK for PMU control.

A single regulated 3.3V power supply is required for AW7698N. It could be from an external DC-DC converter to convert a higher voltage supply to 3.3V or boost from a lower voltage supply to 3.3V. The PMU contains Under-Voltage Lockout (UVLO) circuit, several Low Drop-out Regulators (LDOs), a high efficiency buck converter and a reference band-gap circuit. The circuits are optimized for low quiescent current, low drop-out voltage, efficient line/load regulation, high ripple rejection and low output noise.

4.2. Low-power operating mode

The AW7698N power state diagram is shown in Figure 4.2-1.

In **ACTIVE** mode, the Cortex-M4 and N9 power states operate independently, and both have Idle, Active and Sleep modes. When both are in sleep mode, the chipset enters **SLEEP** mode.

In **SLEEP** mode, the PMU can be changed to low-power mode to further lower current consumption.

RETENTION mode provides a lower current consumption than **SLEEP** mode. It is suitable for applications that remain idle for a long period. To enter **RETENTION** mode is software configurable and to exit, use RTC timer or EINT.

OFF mode is controlled by the CHIP_EN signal and in this state, only always-on PMU logics are alive to maintain the lowest current consumption.

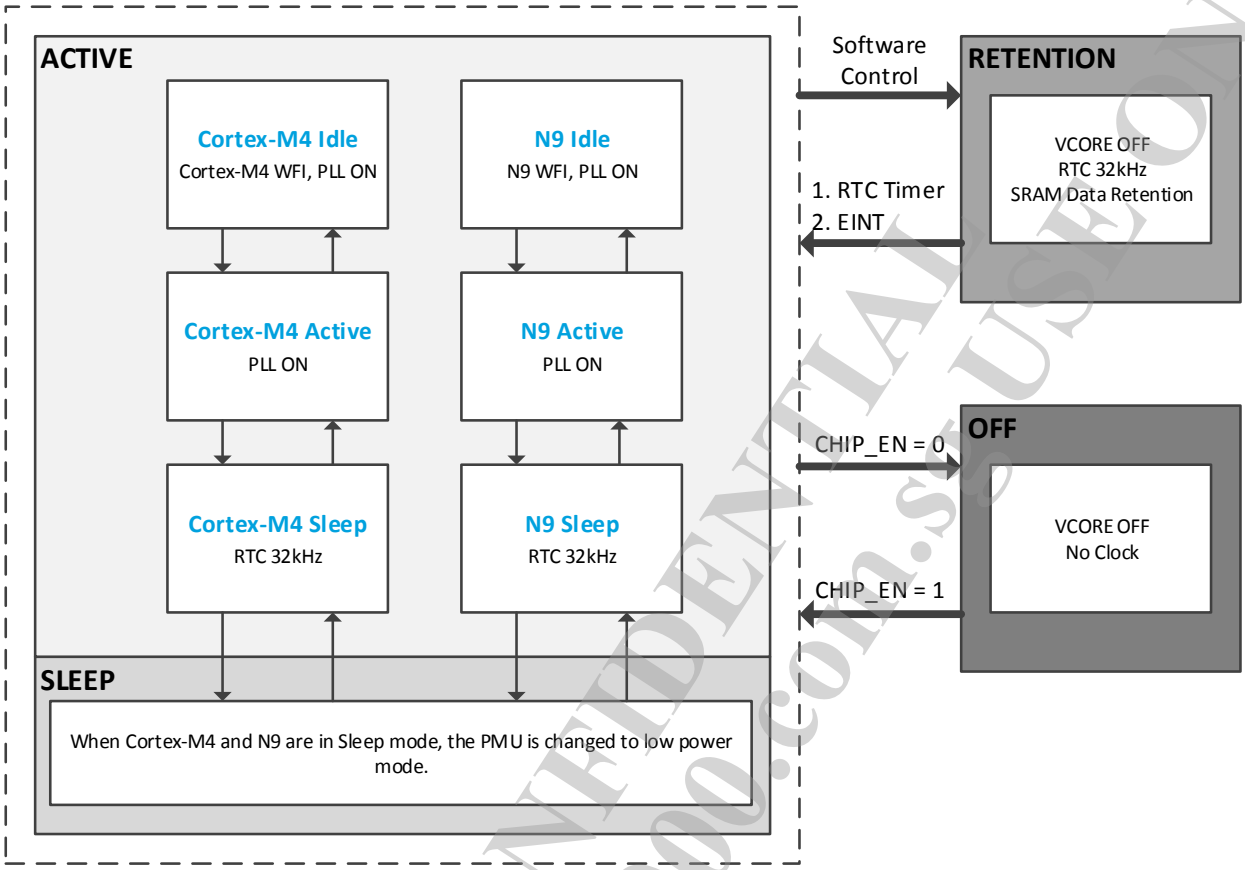


Figure 4.2-1. AW7698N Cortex-M4 and N9 power state and power mode

4.3. PMU architecture

The 3.3V power source is directly supplied to the switching regulator, digital IOs and RF-related circuit. It is converted to 1.45V by the buck converter for low voltage circuits. The built-in digital LDOs and RF LDOs convert 1.45V to 1.15V for digital, RF and BBPLL core circuits. The three LDOs are CLDO, SLDO-H and MLDO. SLDO-H stands for sleep mode LDO, CLDO stands for digital core LDO, and MLDO stands for internal or external memory LDO.

In **ACTIVE** mode, the buck converter converts 1.45V output to other subsystems in AW7698N. It can operate in either PFM mode or PWM mode. With an external on-board LC filter (2.2µH inductor and 10µF cap), it outputs a low ripple 1.45V to Wi-Fi RF system and CLDO input power. In **ACTIVE** mode, CLDO is under BUCK domain, and then it outputs 1.15V for whole chip digital logics.

In **SLEEP** mode, BUCK output voltage will be kept by SLDO-H. The SLDO-H also generates 1.45V output voltage to Wi-Fi RF system and CLDO input power. While AW7698N is in **SLEEP** mode, CLDO will reduce its output level from 1.15V to 0.85V for whole chip digital logics used to reduce power consumption.

In **RETENTION** mode, BUCK, CLDO, SLDO-H and MLDO will be shut down. During this mode, only always-on PMU logics, RTC timer controller and retention SRAM are alive to keep lower current consumption.

Once AW7698N goes into **OFF** mode (controlled by CHIP_EN), BUCK, CLDO, SLDO-H, MLDO and RTC controller will be shut down. During this mode, only some PMU AO domain blocks are alive to keep lowest current consumption.

4.4. Power performance

Table 4.4-1 lists example current consumptions in VBAT domain.

Table 4.4-1. Current consumption in different power modes

Operation Mode		Test Conditions	Current Consumptions [1]	Unit
Power Mode	Scenario			
OFF	OFF	• CHIP_EN keeps low	< 0.5	µA
RETENTION	RETENTION	• RTC Timer • 0KB SRAM data retention	2.7	µA
		• RTC Timer • 8KB SRAM data retention	4.7	µA
SLEEP	SLEEP_ext_32Khz	• Cortex-M4 in sleep state • TCM 96KB SRAM is retained • SYSRAM 384KB SRAM is retained • XTAL 32kHz	120	µA
	SLEEP_int_32Khz	• Cortex-M4 in sleep state • TCM 96KB SRAM is retained • SYSRAM 384KB SRAM is retained • Internal 32kHz	390	µA
ACTIVE	Wi-Fi TX	• CCK 19dBm • N9 in idle state • Cortex-M4 in active state • TCM 96KB SRAM is retained • XTAL 32kHz	260	mA
		• OFDM 16.5dBm • N9 in idle state • Cortex-M4 in active state • TCM 96KB SRAM is retained • XTAL 32kHz	220	mA
	Wi-Fi RX	• HT20_MCS7 • N9 in active state • Cortex-M4 in active state • XTAL 32kHz	40	mA
		• HT20_MCS7 • N9 in idle state • Cortex-M4 in sleep state • XTAL 32kHz	30	mA
ACTIVE & SLEEP	DTIM = 1	• Cortex-M4 in sleep state • TCM 96KB SRAM is retained • XTAL 32kHz	950	µA

[1] Conditions: VBAT and VDDIO at 3.3V, temperature at 25°C, typical corner IC, XTAL at 26MHz

4.5. Power-on sequence

The AW7698N power-on sequence is shown in Figure *4.5-1*.

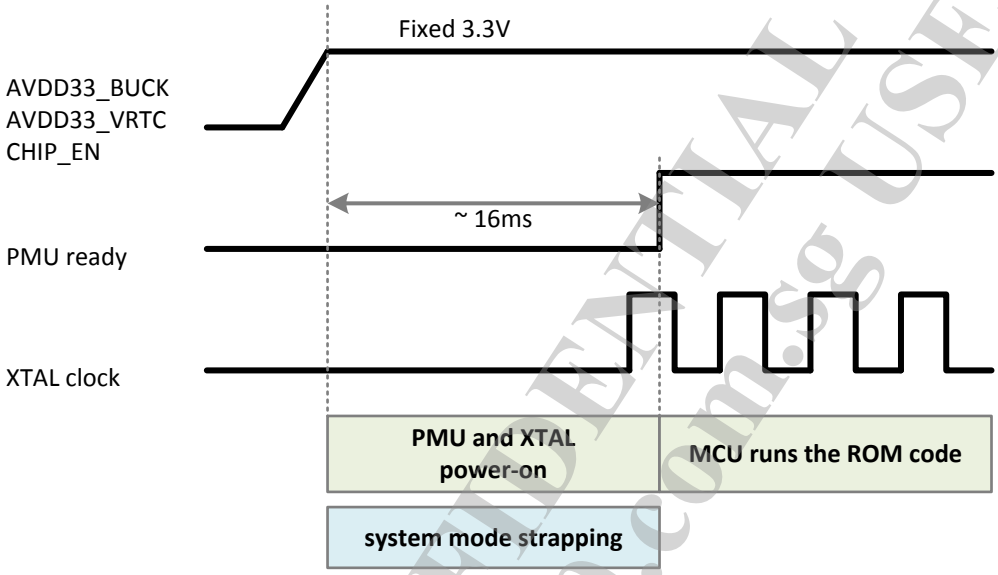


Figure 4.5-1***. Power-on sequence***

5. Electrical Characteristics of Wi-Fi

5.1. Absolute maximum ratings

Table 5.1-1. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
AVDD33_MISC	Power input	-0.3	3.63	V
AVDD33_VRTC	RTC domain power supply (V_{RTC})	-0.3	3.63	V
AVDD18_MLDO	MLDO power output for Serial Flash	-0.3	3.63	V
AVDD15_CLDO	CLDO power input from BUCK	-0.3	1.595	V
AVDD33_BUCK	Buck power input (V_{BAT})	-0.3	3.63	V
AVDD12_CLDO	CLDO power output for core power	-0.3	1.265	V

Table 5.1-2. Absolute maximum ratings for I/O power supply

Symbol or pin name	Description	Min.	Typ.1	Typ.2	Max.	Unit
DVDD_IO_0	Power supply for GPIO group 0	1.62	1.8	3.3	3.63	V
DVDD_IO_1	Power supply for GPIO group 1	1.62	1.8	3.3	3.63	V
DVDD_MLDO	Power supply for SF/EMI IO 1.8V group	1.62	1.8	-	1.98	V

Table 5.1-3. Absolute maximum ratings for voltage input

Symbol or pin name	Description	Min.	Max.	Unit
VIN0	Digital input voltage for IO Type 0	-0.3	3.63	V
VIN1	Digital input voltage for IO Type 1	-0.3	5.5	V
VIN2	Digital input voltage for IO Type 2	-0.3	5.5	V
VIN3	Digital input voltage for IO Type 3	-0.3	5.5	V

Table 5.1-4. Absolute maximum ratings for storage temperature

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	°C

5.2. Operating conditions

5.2.1. General operating conditions

Table 5.2-1. General operating conditions

Item	Description	Condition	Min.	Typ.	Max.	Unit
F_{CPU}	Internal Cortex-M4 & TCM & Cache clock	VCORE = 1.15V	0	-	192	MHz

Item	Description	Condition	Min.	Typ.	Max.	Unit
F_{MEMS}	Internal memory (SFC and EMI) related AHB and APB clock. Synchronous with F_{CPU}.	VCORE = 1.15V	0	-	96	MHz

Table 5.2-2. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD33_MISC	Power input	2.97	3.3	3.63	V
AVDD33_VRTC	RTC domain power supply (V_{RTC})	1.62	3.3	3.63	V
AVDD18_MLDO	MLDO power output for Serial Flash	1.62	1.8	1.98	V
AVDD15_CLDO	CLDO power input from BUCK	1.305	1.45	1.595	V
AVDD33_BUCK	Buck power input (V_{BAT})	2.97	3.3	3.63	V
AVDD12_CLDO	CLDO power output for core power	1.035	1.15	1.265	V

Table 5.2-3. Recommended operating conditions for voltage input

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN0	Digital input voltage for IO Type 0	-0.3	-	DVDIO+0.3	V
VIN1	Digital input voltage for IO Type 1	-0.3	-	DVDIO+0.3	V
VIN2	Digital input voltage for IO Type 2	-0.3	-	DVDIO+0.3	V
VIN3	Digital input voltage for IO Type 3	-0.3	-	DVDIO+0.3	V

Table 5.2-4. Recommended operating conditions for operating temperature

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
Tc	Operating temperature	-30	-	105	°C

5.2.2. Input or output port characteristics

Table 5.2-5. Electrical characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH0	Digital high input current for IO Type 0	• PU/PD disabled • DVDIO = 3.3/2.8/1.8V, • DVDIO*0.65 < VIN0 < DVDIO+0.3V	-5	-	5	µA
		• PU enabled • DVDIO = 3.3/2.8/1.8V • DVDIO*0.75 < VIN0 < DVDIO	-35	-	5	µA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		• PD enabled • DVDIO = 3.3/2.8/1.8V • DVDIO*0.75 < VIN0 < DVDIO	7	-	70	µA
DIIL0	Digital low input current for IO Type 0	• PU/PD disabled • DVDIO = 3.3/2.8/1.8V, • -0.3V < VIN0 < DVDIO*0.35	-5	-	5	µA
		• PU enabled, • DVDIO = 3.3/2.8/1.8V • 0 < VIN0 < DVDIO*0.25	-60	-	-6	µA
		• PD enabled, • DVDIO = 3.3/2.8/1.8V • 0 < VIN0 < DVDIO*0.25	-5	-	40	µA
DIOH0	Digital high output current for IO Type 0	• DVOH = 2.805V • DVDIO = 3.3V • Max. driving mode	24	-	-	mA
		• DVOH = 2.38V • DVDIO = 2.8V • Max. driving mode	20	-	-	mA
		• DVOH = 1.53V • DVDIO = 1.8V • Max. driving mode	8	-	-	mA
DIOL0	Digital low output current for IO Type 0	• DVOL = 0.495V • DVDIO = 3.3V • Max. driving mode	24	-	-	mA
		• DVOL = 0.442V • DVDIO = 2.8V • Max. driving mode	20	-	-	mA
		• DVOL = 0.27V • DVDIO = 1.8V • Max. driving mode	8	-	-	mA
DRPU0	Digital I/O pull-up resistance for IO Type 0	• DVDIO = 3.3V • VIN = 0V	40	85	190	kΩ
		• DVDIO = 2.8V	40	85	190	kΩ

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		• VIN = 0				
		• DVDIO = 1.8V • VIN = 0V	80	160	320	kΩ
DRPD0	Digital I/O pull-down resistance for IO Type 0	• DVDIO = 3.3V • VIN = 3.3V	40	85	190	kΩ
		• DVDIO = 2.8V • VIN = 2.8V	40	85	190	kΩ
		• DVDIO = 1.8V • VIN = 1.8V	80	160	320	kΩ
DVOH0	Digital output high voltage for IO Type 0	• DVDIO = 3.3V	2.4	-	-	V
		• DVDIO = 2.8V	1.89	-	-	V
		• DVDIO = 1.8V	1.215	-	-	V
DVOL0	Digital output low voltage for IO Type 0	• DVDIO = 3.3V	-	-	0.495	V
		• DVDIO = 2.8V	-	-	0.42	V
		• DVDIO = 1.8V	-	-	0.27	V
DVIH0	Digital input high voltage for IO Type 0	• DVDIO = 3.3V	2.0	-	DVDIO	V
		• DVDIO = 2.8V	0.65* DVDIO	-	DVDIO	V
		• DVDIO = 1.8V	0.65* DVDIO	-	DVDIO	V
DVIL0	Digital input low voltage for IO Type 0	• DVDIO = 3.3V	0	-	0.8	V
		• DVDIO = 2.8V	0	-	0.35* DVDIO	V
		• DVDIO = 1.8V	0	-	0.35* DVDIO	V
DIIH1	Digital high input current for IO Type 1	• PU/PD disabled • DVDIO = 3.3/2.8/1.8V, • DVDIO*0.65 < VIN1 < DVDIO+0.3V	-5	-	5	µA
		• DVDIO = 3.3V • 4.5V < VIN1 < 5.5V	-5	-	5	µA
		• PU enabled • DVDIO = 3.3/2.8/1.8V • DVDIO*0.75 < VIN1 < DVDIO	-35		5	µA
		• PD enabled • DVDIO =	7		70	µA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		3.3/2.8/1.8V • DVDIO*0.75 < VIN1 < DVDIO				
DIIL1	Digital low input current for IO Type 1	• PU/PD disabled • DVDIO = 3.3/2.8/1.8V, • -0.3V < VIN1 < DVDIO*0.35	-5	-	5	µA
		• PU enabled • DVDIO = 3.3/2.8/1.8V • 0 < VIN1 < DVDIO*0.25	-60	-	-6	µA
		• PD enabled • DVDIO = 3.3/2.8/1.8V • 0 < VIN1 < DVDIO*0.25	-5	-	40	µA
DIOH1	Digital high output current for IO Type 1	• DVOH = 2.805V • DVDIO = 3.3V • Max. driving mode	24	-	-	mA
		• DVOH = 2.38V • DVDIO = 2.8V • Max. driving mode	20	-	-	mA
		• DVOH = 1.53V • DVDIO = 1.8V • Max. driving mode	8	-	-	mA
DIOL1	Digital low output current for IO Type 1	• DVOL = 0.495V • DVDIO = 3.3V • Max. driving mode	24	-	-	mA
		• DVOL = 0.442V • DVDIO = 2.8V • Max. driving mode	20	-	-	mA
		• DVOL = 0.27V • DVDIO = 1.8V • Max. driving mode	8	-	-	mA
DRPU1	Digital I/O pull-up resistance for IO Type 1	• DVDIO = 3.3V • VIN = 0V	40	85	190	kΩ
		• DVDIO = 2.8V • VIN = 0V	40	85	190	kΩ
		• DVDIO = 1.8V	80	160	320	kΩ

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		• VIN = 0V				
DRPD1	Digital I/O pull-down resistance for IO Type 1	• DVDIO = 3.3V • VIN = 3.3V	40	85	190	kΩ
		• DVDIO = 2.8V • VIN = 2.8V	40	85	190	kΩ
		• DVDIO = 1.8V • VIN = 1.8V	80	160	320	kΩ
DVOH1	Digital output high voltage for IO Type 1	• DVDIO = 3.3V	2.4	-	-	V
		• DVDIO = 2.8V	1.89	-	-	V
		• DVDIO = 1.8V	1.215	-	-	V
DVOL1	Digital output low voltage for IO Type 1	• DVDIO = 3.3V	-	-	0.495	V
		• DVDIO = 2.8V	-	-	0.42	V
		• DVDIO = 1.8V	-	-	0.27	V
DVIH1	Digital input high voltage for IO Type 1	• DVDIO = 3.3V	2.0	-	5	V
		• DVDIO = 2.8V	0.65* DVDIO	-	5	V
		• DVDIO = 1.8V	0.65* DVDIO	-	5	V
DVIL1	Digital input low voltage for IO Type 1	• DVDIO = 3.3V	0	-	0.8	V
		• DVDIO = 2.8V	0	-	0.35* DVDIO	V
		• DVDIO = 1.8V	0	-	0.35* DVDIO	V
DIIH2	Digital high input current for IO Type 2	• PU/PD disabled • DVDIO = 3.3/2.8/1.8V, • DVDIO*0.65 < VIN2 < DVDIO+0.3V	-5	-	5	µA
		• DVDIO = 3.3V • 4.5V < VIN2 < 5.5V	-5	-	5	µA
		• PU enabled, RSEL1 • DVDIO = 3.3/2.8/1.8V • DVDIO*0.75 < VIN2 < DVDIO	-60	-	5	µA
		• PU enabled, RSEL2 • DVDIO = 3.3/2.8/1.8V • DVDIO*0.75 < VIN2 < DVDIO	-120	-	5	µA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		• PD enabled, RSEL1 • DVDIO = 3.3/2.8/1.8V • DVDIO*0.75 < VIN2 < DVDIO	10	-	110	µA
		• PD enabled, RSEL2 • DVDIO = 3.3/2.8/1.8V • DVDIO*0.75 < VIN2 < DVDIO	20	-	220	µA
DIIL2	Digital low input current for IO Type 2	• PU/PD disabled, • DVDIO = 3.3/2.8/1.8V, • -0.3V < VIN2 < DVDIO*0.35	-5	-	5	µA
		• PU enabled, RSEL1 • DVDIO = 3.3/2.8/1.8V • 0 < VIN2 < DVDIO*0.25	-100	-	-10	µA
		• PU enabled, RSEL2 • DVDIO = 3.3/2.8/1.8V • 0 < VIN2 < DVDIO*0.25	-200	-	-20	µA
		• PD enabled, RSEL1 • DVDIO = 3.3/2.8/1.8V • 0 < VIN2 < DVDIO*0.25	-5	-	60	µA
		• PD enabled, RSEL2 • DVDIO = 3.3/2.8/1.8V • 0 < VIN2 < DVDIO*0.25	-5	-	120	µA
DIOH2	Digital high output current for IO Type 2	• DVOH = 2.805V • DVDIO = 3.3V • Max. driving mode	24	-	-	mA
		• DVOH = 2.38V • DVDIO = 2.8V • Max. driving mode	20	-	-	mA
		• DVOH = 1.53V	8	-	-	mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		• DVDIO = 1.8V • Max. driving mode				
DIOL2	Digital low output current for IO Type 2	• DVOL = 0.495V • DVDIO = 3.3V • Max. driving mode	24	-	-	mA
		• DVOL = 0.42V • DVDIO = 2.8V • Max. driving mode	20	-	-	mA
		• DVOL = 0.27V • DVDIO = 1.8V • Max. driving mode	8	-	-	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	• DVDIO = 3.3V • VIN = 0V, RSEL1	25	45	100	kΩ
		• DVDIO = 3.3V • VIN = 0V, RSEL2	10	23	50	kΩ
		• DVDIO = 2.8V • VIN = 0V, RSEL1	25	45	100	kΩ
		• DVDIO = 2.8V • VIN = 0V, RSEL2	10	23	50	kΩ
		• DVDIO = 1.8V • VIN = 0V, RSEL1	50	100	200	kΩ
		• DVDIO = 1.8V • VIN = 0V, RSEL2	25	50	100	kΩ
DRPD2	Digital I/O pull-down resistance for IO Type 2	• DVDIO = 3.3V • VIN = 3.3V, RSEL1	25	45	100	kΩ
		• DVDIO = 3.3V • VIN = 3.3V, RSEL2	10	23	50	kΩ
		• DVDIO = 2.8V • VIN = 2.8V, RSEL1	25	45	100	kΩ
		• DVDIO = 2.8V • VIN = 2.8V, RSEL2	10	23	50	kΩ
		• DVDIO = 1.8V • VIN = 1.8V, RSEL1	50	100	200	kΩ
		• DVDIO = 1.8V • VIN = 1.8V, RSEL2	25	50	100	kΩ
DVOH2	Digital output high voltage for IO Type 2	• DVDIO = 3.3V	2.805	-	-	V
		• DVDIO = 2.8V	2.38	-	-	V
		• DVDIO = 1.8V	1.53	-	-	V

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DVOL2	Digital output low voltage for IO Type 2	• DVDIO = 3.3V	-	-	0.495	V
		• DVDIO = 2.8V	-	-	0.42	V
		• DVDIO = 1.8V	-	-	0.27	V
DVIH2	Digital input high voltage for IO Type 2	• DVDIO = 3.3V	2.0	-	5	V
		• DVDIO = 2.8V	0.65* DVDIO	-	5	V
		• DVDIO = 1.8V	0.65* DVDIO	-	5	V
DVIL2	Digital input low voltage for IO Type 2	• DVDIO = 3.3V	0	-	0.8	V
		• DVDIO = 2.8V	0	-	0.35* DVDIO	V
		• DVDIO = 1.8V	0	-	0.35* DVDIO	V
DIIH3	Digital high input current for IO Type 3	• PU/PD disabled • DVDIO = 3.3/2.8/1.8V • DVDIO*0.65 < VIN3 < DVDIO+0.3V	-5	-	5	µA
		• DVDIO =3.3V • 4.5V < VIN3 < 5.5V	-5	-	5	µA
		• PU enabled • DVDIO = 3.3/2.8/1.8V • DVDIO*0.75 < VIN3 < DVDIO	-35	-	5	µA
		• PD enabled • DVDIO = 3.3/2.8/1.8V • DVDIO*0.75 < VIN3 < DVDIO	7	-	70	µA
DIIL3	Digital low input current for IO Type 3	• PU/PD disabled • DVDIO = 3.3/2.8/1.8V • -0.3V < VIN3 < DVDIO*0.35	-5	-	5	µA
		• PU enabled • DVDIO = 3.3/2.8/1.8V • 0 < VIN3 < DVDIO*0.25	-60	-	-6	µA
		• PD enabled	-5	-	40	µA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		• DVDIO = 3.3/2.8/1.8V • 0 < VIN3 < DVDIO*0.25				
DIOH3	Digital high output current for IO Type 3	• DVOH = 2.805V • DVDIO = 3.3V • Max. driving mode	24	-	-	mA
		• DVOH = 2.38V • DVDIO = 2.8V • Max. driving mode	20	-	-	mA
		• DVOH = 1.53V • DVDIO = 1.8V • Max. driving mode	8	-	-	mA
DIOL3	Digital low output current for IO Type 3	• DVOL = 0.495V • DVDIO = 3.3V • Max. driving mode	24	-	-	mA
		• DVOL = 0.42V • DVDIO = 2.8V • Max. driving mode	20	-	-	mA
		• DVOL = 0.27V • DVDIO = 1.8V • Max. driving mode	8	-	-	mA
DRPU3	Digital I/O pull-up resistance for IO Type 3	• DVDIO = 3.3V • VIN = 0V, RSEL1	25	45	100	kΩ
		• DVDIO = 3.3V • VIN = 0V, RSEL2	10	23	50	kΩ
		• DVDIO = 2.8V • VIN = 0V, RSEL1	25	45	100	kΩ
		• DVDIO = 2.8V • VIN = 0V, RSEL2	10	23	50	kΩ
		• DVDIO = 1.8V • VIN = 0V, RSEL1	50	100	200	kΩ
		• DVDIO = 1.8V • VIN = 0V, RSEL2	25	50	100	kΩ
DRPD3	Digital I/O pull-down resistance for IO Type 3	• DVDIO = 3.3V • VIN = 3.3V, RSEL1	25	45	100	kΩ
		• DVDIO = 3.3V • VIN = 3.3V, RSEL2	10	23	50	kΩ
		• DVDIO = 2.8V	25	45	100	kΩ

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		• VIN = 2.8V, RSEL1				
		• DVDIO = 2.8V • VIN = 2.8V, RSEL2	10	23	50	kΩ
		• DVDIO = 1.8V • VIN = 1.8V, RSEL1	50	100	200	kΩ
		• DVDIO = 1.8V • VIN = 1.8V, RSEL2	25	50	100	kΩ
DVOH3	Digital output high voltage for IO Type 3	• DVDIO = 3.3V	2.805	-	-	V
		• DVDIO = 2.8V	2.38	-	-	V
		• DVDIO = 1.8V	1.53	-	-	V
DVOL3	Digital output low voltage for IO Type 3	• DVDIO = 3.3V	-	-	0.495	V
		• DVDIO = 2.8V	-	-	0.42	V
		• DVDIO = 1.8V	-	-	0.27	V
DVIH3	Digital input high voltage for IO Type 3	• DVDIO = 3.3V	2.0	-	5	V
		• DVDIO = 2.8V	0.65* DVDIO	-	5	V
		• DVDIO = 1.8V	0.65* DVDIO	-	5	V
DVIL3	Digital input low voltage for IO Type 3	• DVDIO = 3.3V	0	-	0.8	V
		• DVDIO = 2.8V	0	-	0.35* DVDIO	V
		• DVDIO = 1.8V	0	-	0.35* DVDIO	V

5.2.3. ESD electrical sensitivity

Table 5.2-6. ESD electrical characteristics of the AW7698N series

ESD mode	Description	Pin name	Min.	Max.	Unit
HBM	All pins exclude RF pins	JESD22-A114-F	-2000	2000	V
	RF pins	JESD22-A114-F	-1000	1000	V
CDM	All pins exclude RF pins	JESD22-C101-D	-500	500	V
	RF pins	JESD22-C101-D	-250	250	V

6. System Configuration of Wi-Fi

6.1. Mode selection

Strapping pin definition and condition are listed as Table 6.1-1. Core reset refers to the condition chip changes from either OFF or RETENTION mode to ACTIVE mode.

Table 6.1-1. Mode selection table

Mode Selection	Pin name	Description	Trapping condition
XO source frequency select	GPIO_17	GND : XO input is 26MHz (default)	Core reset
32kHz clock source select	GPIO_14	GND : External 32kHz source DVDD_IO_0 : Internal 32kHz source (divided from 26MHz clock) (default)	Core reset
Boot with host interface (HIF_EN)	GPIO_4	GND : Boot with host interface disabled DVDD_IO_1 : Boot with host interface enabled (default)	Core reset
Host interface select (active if HIF_EN is enabled)	GPIO_13	(Active if HIF_EN = 1) GND : Host interface via SPI slave DVDD_IO_0 : Host interface via SDIO slave (default)	Core reset
Boot ROM bypass select	GPIO_16	GND : Boot up bypass boot ROM (directly jump to flash) DVDD_IO_0 : Boot up with boot ROM (default)	Core reset
JTAG pins fixed for use	GPIO_15	GND : JTAG pins fixed for JTAG use DVDD_IO_0 : JTAG pins as GPIO (configurable after boot up) (default)	Core reset
UART download	GPIO_12	GND : Enter UART download mode in Boot ROM DVDD_IO_0 : Skip UART download in Boot ROM (default)	Core reset or watchdog reset
UART mode select	GPIO0_B	GND : SPI mode DVDD_IO_0 : UART mode (default)	Core reset
Normal mode	OD_GPIO0_B	Pull-high	Core reset
Normal mode	OD_GPIO1_B	Pull-high	Core reset
Normal mode	OD_GPIO2_B	Pull-high	Core reset

Note 1: Strapping resistors for default option are implemented as internal pull-down or internal pull-up.

Note 2: If non-default option is used, it is recommended to use pull-down or pull-up 10kΩ as external strapping resistors.

Note 3: SDIO master and slave interfaces are limited to 1-bit mode if the 32kHz source is external.

7. Overview of the Bluetooth subsystem

7.1. General description

The Bluetooth subsystem integrates baseband, radio for mesh controllers, mobile payments, and wearable device applications. It meets the Bluetooth Version 5.0 specification including BLE 1M/2M/long range and BLE extended advertising features

7.2. Features

- Integrate 1.8V switching regulator and 1.8V LDO regulator
- Ultra-low power consumption for battery enabled applications
- Support BLE 1M, 2M and long range
- Support BLE extended advertising
- 128bit AES
- Four PWM channels

8. Electrical Characteristics of the Bluetooth subsystem

8.1. Absolute maximum ratings

Any stress in excess of the absolute maximum ratings listed below could cause damage to the Bluetooth subsystem.

Table 8.1-1 Absolute maximum rating

Item	Min.	Max.	UNIT
I/O supply voltage (VCCIO)	**-0.3**	**3.6**	**V**
Analog/RF supply voltage (VCCANA, VCCRF)	**-0.3**	**2.0**	**V**
Operating temperature	**-40**	**+105**	**°C**
Storage temperature	**-65**	**+150**	**°C**

8.2. Recommended operating conditions

Table 8.2-1 Recommended operating conditions

Item	Min.	Typ.	Max.	Unit
Core supply voltage (VCCANA, VCCRF)	1.65		1.75	V
I/O supply voltage (VCCIO)	1.7		3.6	V
VBAT for Bluetooth	2.97	3.3	3.63	V

8.3. Digital terminals

Table 8.3-1 Digital terminals

Item	Min.	Typ.	Max.	Unit
Input Voltage Levels				
Input logic level low (V_{IL})	0		0.3*VCCIO	V
Input logic level high (V_{IH})	0.7*VCCIO		VCCIO+0.4	V
Output Voltage Levels (1.7V≦VCCIO≦3.6)				
Output logic level low (V_{OL}), I_O=4.0mA			0.2	V
Output logic level high (V_{OH}), I_O=-4.0mA	VCCIO-0.2			V

8.4. Reference clock

Table 8.4-1 Reference clock

Item	Min.	Typ.	Max.	Unit
Crystal Requirement				
Nominal Frequency		32		MHz
Load Capacitance		9		pF

Item	Min.	Typ.	Max.	Unit
Frequency Stability over Temperature		±20		ppm

8.5. Radio characteristics

8.5.1. Transmitter

Low Energy

Table 8.5-1 Transmitter low energy

Item		Min.	Typ.	Max.	Unit
Maximum RF transmit power*1			9.5		dBm
Peak power – Average power				3	dB
In-band emissions	≥ +3MHz			-30	dBm
	+2MHz			-20	dBm
	-2MHz			-20	dBm
	≤ -3MHz			-30	dBm
Modulation characteristics	Δf1avg	225		275	KHz
	Percent of Δf2max > 185kHz	99.9		100	%
	Δf2avg/Δf1avg		1		
Center freq. deviation, Fn (n = 0,1,2,….k)		-150		+150	KHz
Freq. drift, |F0 - Fn| (n = 2,3,4,…k)		-50		+50	KHz
Initial freq. drift, |F1 - F0|		-20		+20	KHz
Max. freq. drift rate, |Fn - Fn-5| (n = 6,7,8,…k)		-20		+20	KHz/50us
Harmonics (cable mode)			-45		dBm

8.5.2. Receiver

Low Energy

Table 8.5-2 Receiver low energy

Item		Min.	Typ.	Max.	Unit
Sensitivity			-94		dBm
Maximum input level		-10			dBm
Co-Channel interference, C/I				21	dB
Adjacent channel interference, C/I	F = F0+1MHz			15	dB
	F = F0-1MHz			15	dB
	F = F0+2MHz			-17	dB
	F = F0-2MHz (image)			-15	dB
	F = F0+3MHz			-27	dB
	F = F0-3MHz (image-1)			-9	dB
Intermodulation		-50			dBm
Blocking	30-2000 MHz	-30			dBm

Item		Min.	Typ.	Max.	Unit
	2003-2399 MHz	-35			dBm
	2484-2997 MHz	-35			dBm
	3000-12750 MHz	-30			dBm
PER report integrity			50		%

8.6. Power

8.6.1. Switching regulator

External inductor = 10uH, external capacitor = 4.7uF

Table 8.6-1 Switching regulator

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		1.9	3	3.6	V
Output Voltage		1.5	1.7	2	V
Rated Output Current (Iout)	Normal mode		50		mA
	Retention mode			2	mA

8.6.2. 1.8V LDO

External capacitor = 4.7uF

Table 8.6-2 1.8V LDO

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		1.9	3	3.6	V
Output Voltage		1.5	1.7	2	V
Rated Output Current (Iout)	Normal mode		50		mA
	Retention mode			2	mA

8.6.3. 1.5V LDO

External capacitor = 1uF

Table 8.6-3 1.5V LDO

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		1.4	1.7	3.6	V
Output Voltage		1.1		1.6	V
Rated Output Current (Iout)	Normal mode		20		mA
	Retention mode			1	mA

8.6.4. Power fail monitor

Table 8.6-4 Power fail monitor

Item	Condition	Min.	Typ.	Max.	Unit
Programmable threshold		1.8		3.3	V
Threshold voltage tolerance		-5		+5	%
Threshold voltage hysteresis			200		mV
Current consumption			0.6		uA

8.7. Typical current consumption

Table 8.7-1 Typical current consumption

Parameter	Current (avg.)	Units	Notes
Tx current @9.5dBm	25.9	mA	
Rx current @1Mbps (9.5dBm)	10.6	mA	
Sleep	31	uA	
Deepsleep	0.5	uA	

Note: The current consumption values were recorded under the following conditions:
1. Buck mode, VCCIO=VBAT pin=3V, Tx=9.5dBm
2. LEDs disconnected.

9. Function Description of the Bluetooth subsystem

9.1. Radio transceiver

The RF transceiver is a 2.4GHz-band transceiver for Bluetooth data applications. There are three primary functions – transmitter, receiver, and synthesizer. The Baseband Processing Unit supplies the control signals for these functions.

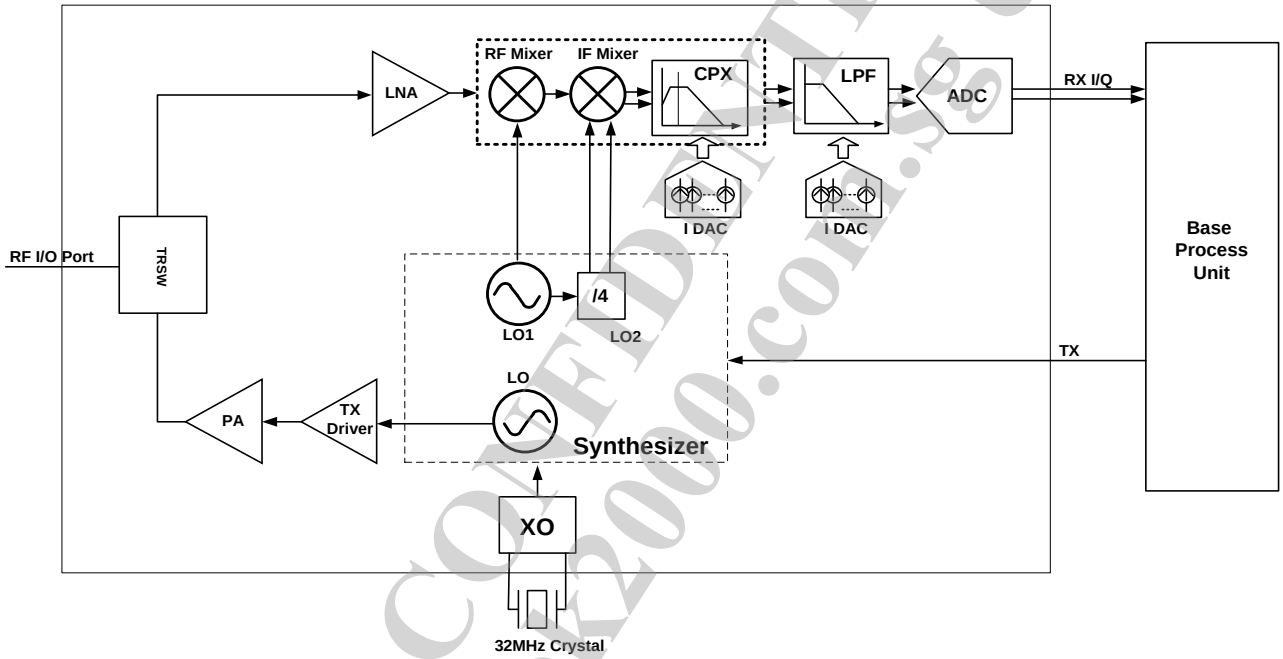


Figure 9.1-1 Radio transceiver

9.1.1. RF front end

The RX input ports and TX output ports use the same RF terminals so that no external T/R switch is required. Only a few related components are put outside of the RF terminals.

9.1.2. Receiver

The RF receiver contains two parts: An RF front-end and an IF part. The RF front-end contains an LNA and an RF mixer, and an IF Mixer. The IF part contains a complex filter (CPX) and a low-pass filter (LPF) for out-band filtering.

The LNA input uses the same RF ports as the TX output. The RX front-end gain can be adjusted, and thus reduces the probability of bit errors caused by a poor signal-to-noise ratio. The LNA is followed by an RF mixer and an IF Mixer mixer that down-converts the RF signal to the IF band.

During the IF process, the down-converted signal is filtered by CPX and LPF and is then sent to the ADC for demodulation. The 3dB bandwidth of the LPF can be adjusted via the RF registers. The RX front end provides more than 80dB gain control range.

9.1.3. Transmitter

The RF transmitter contains a synthesizer, a TX driver, and a TXPA stage. The TX baseband signals are fed from the digital baseband and the synthesizer is used to synthesize the channel frequency and directly convert the baseband signal to an RF modulation signal. The TX driver and TX PA amplify the output power to the necessary level.

9.1.4. Synthesizer

The features a fractional-N synthesizer with an embedded VCO and loop filter without the need for external components. It also integrates an internal crystal oscillator. Only an external 16MHz crystal is necessary.

9.2. Baseband processing unit

The baseband processing unit contains a Link Manager and a Modem to manage the Bluetooth protocol and the data transmission and reception via the RF channels.

9.2.1. Link manager

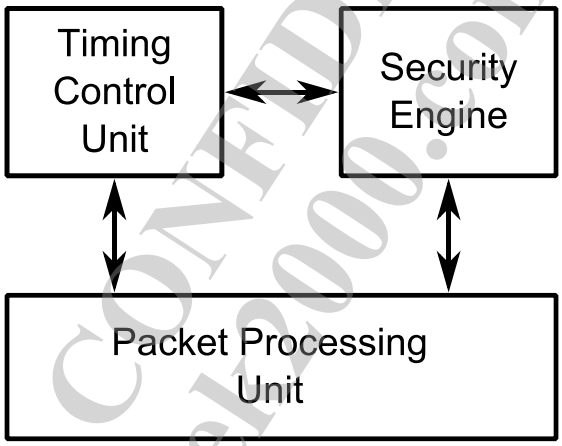


Figure 9.2-1 Link manager

The Link Manager contains a Timing Control Unit, a Security Engine, and a Packet Processing Unit. The Timing Control Unit generates and keeps the timing information for all Bluetooth links. The Packet Processing Unit assembles and disassembles Bluetooth packets and has dedicated hardware for processing data whitening and a cyclic redundancy check (CRC). The Security Engine encrypts and decrypts the data if the encryption option is turned on. Both AES and P256 are supported.

9.2.2. Modem

The Modem only supports Bluetooth Low Energy (BLE) mode. It satisfies the requirements of the Bluetooth version 5.0 Low Energy specification including BLE 1M/2M and BLE long range.

9.2.3. UART

The UART interface supports flexible configurations as shown below. There are local FIFOs and DMA which provide high throughput serial communication. The UART also supports the hardware flow control. When it is enabled, two additional signals, UART_RTS and UART_CTS, are required. To provide the maximum flexibility, both UART_RTS and UART_CTS can be configured via any available GPIOs.

Table 9.2-1 UART configuration parameters

Configuration Parameters	Supported Values
Data Length	8 bits
Flow control	Hardware RTS/CTS None
Parity	Even Odd None
Number of stop bits	1 or 2
Baud rate	1200 2400 4800 9600 19200 38400 57600 76800 115200 230400 460800 921600 1228800 2000000

Table 9.2-2 Baud rate accuracy per bit

Baud Rate	Percent Error for 12MHz clk_sys	Percent Error for 16MHz clk_sys
1200	0	0.00
2400	0	0.00
4800	0	0.01
9600	0	-0.02
19200	0	0.04
38400	0.16	-0.08
57600	0.16	-0.08
76800	0.16	0.16
115200	0.16	-0.08
230400	0.16	0.64
460800	0.16	-0.79
921600	0.16	2.12
1228800	-2.34	0.16
2000000	0	0

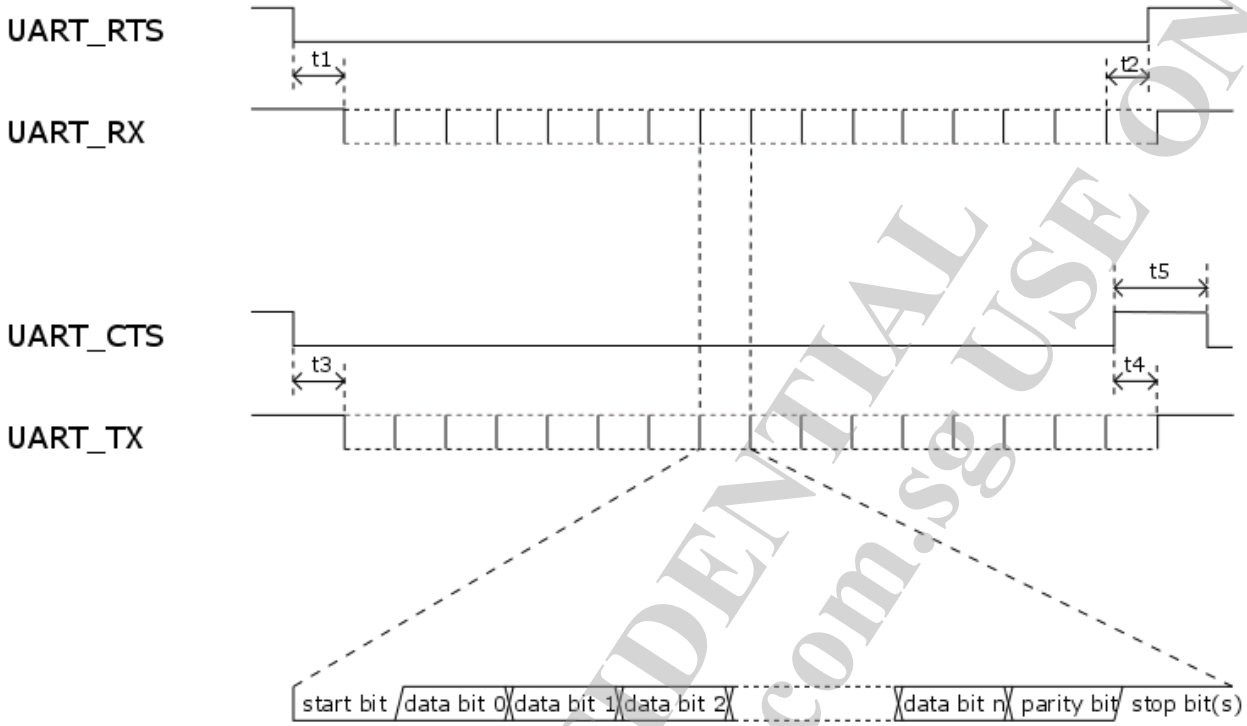


Figure 9.2-2 UART timing diagram

Table 9.2-3 Description of the symbols in Figure 9.2-2

symbol	description	min	max	unit
t1	RTS low to start receiving	0	-	us
t2	Last 2 byte received to RTS high	-	1	byte
t3	CTS low to start transmitting	0.5	1.5	bit
t4	CTS high to stop transmitting	-	1	byte
t5	CTS-high pulse width	1	-	bit

9.3. Power management / regulation of BT

The Bluetooth subsystem integrates a Power Management Unit (PMU), Bulk regulator and LDO regulator.

9.3.1. Buck/LDO regulator

The Buck Regulators are embedded to convert VBAT to 1.8V voltage to supply the Bluetooth subsystem. The block shows the buck circuit with LC component (L+C1). The LDO Regulators are embedded to convert VBAT to 1.8V voltage to supply the Bluetooth subsystem (C2). Both Buck and LDO support retention mode with lower quiescent current for low power operation.

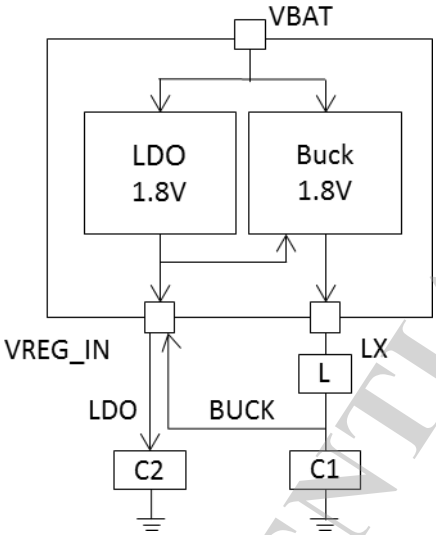


Figure 9.3-1 Buck_LDO regulator circuit

9.3.2. Power management unit of BT

The Power Management Unit (PMU) is designed in AW7698N for the BT power management tasks. The PMU controls the Buck and LDO Regulator power in sequence. During general operations, MCU may go into sleep mode for power saving. During power saving, the PMU monitors the keys and wakes up the MCU if one of the keys is pressed. PMU also monitors the battery voltage and reports to MCU.

9.4. Power control of BT

The Bluetooth subsystem supports various power control features for power saving purpose. There are three special power modes:

- Active mode
- Sleep mode
- Deep-sleep mode

In different power mode, power management unit (PMU) controls Buck/LDO/clocks to reduce power consumption automatically, as shown in Table 9.4-1 Operating power mode.

Table 9.4-1 Operating power mode

Power mode	Buck/LDO	System clock	32KHz clock	Wake-up pins
Active	ON	ON	ON	-
Sleep	Retention	OFF	ON	All input pins
Deep-sleep	Retention	OFF	ON/OFF	All input pins

In active mode, MCU clock rate may also can be controlled by changing clock sources, bypassing PLL, or altering clock divider value. Sleep mode and deep-sleep mode are two types of low power modes supported by AW7698N. In low power mode, system clock is stopped and Buck/LDO enter retention mode to reduce leakage current. All

input pins serve as external wake-up pins to PMU to wake up chip from low power mode. For further power reduction, most of digital circuit is shut off and 32KHz clock is also selectable to be turned off in deep-sleep mode.

10. Software for the Bluetooth subsystem

10.1. Protocol stack

AW7698N includes the complete BLE stack/profiles. The BLE stack includes ATT, GATT, Security Manager and standard based services/profiles. In summary, AW7698N enables customers to support BT 5.0 data communication in their products very easily. Figure 10.1-1 shows the AW7698N software architecture.

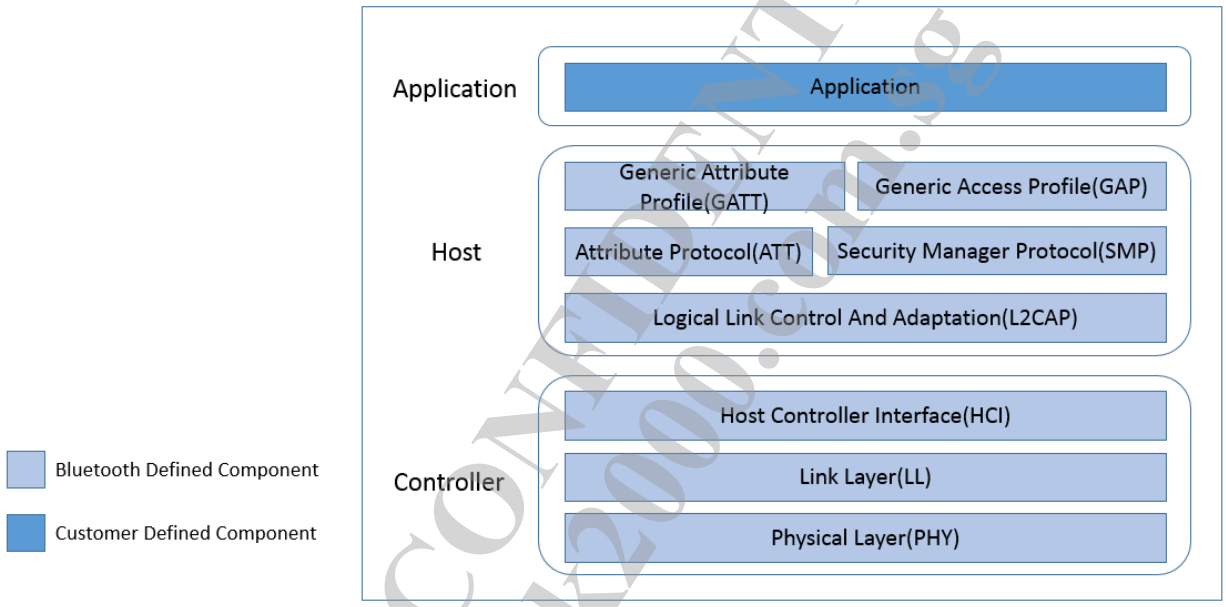


Figure 10.1-1 AW7698N Software Stack for Bluetooth

11. Pin Description

11.1. AW7698N pin list

For AW7698N, a 7.1-mm x 7.1-mm x 1.05-mm 122 balls TFBGA with 0.5-mm ball pitch package is offered. Pin-outs and the top view for this package are shown in Figure 11.1-1.

122	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	GPIO4_B	AVDD15_XO	AVSS15_WF0_LF	XO	DVDD_CORE		VSSLNA		VSSLNA	GPIO8		GPIO10	NC	A
B	GPIO2_B	GPIO1_B			AVSS15_WF0_LF			VSSLNA	BTRF	VSSLNA	GPIO6	GPIO7	GPIO9	SFSIN	B
C	AVDD15_WF0_TRX	GPIO6_B			GPIO0	GPIO2	GPIO4					DVDD_IO_1	SFSHOLD	SFSCK	C
D	AVDD33_WF0_G_TX				GPIO1	GPIO3		VSSLNA		GPIO5			SFSCS0		D
E	AVSS_WFRF	AVSS_WFRF			GPIO3_B	GPIO0_B				VSSANA	VCCANA	GND	SFSOUT	SFSWP	E
F	WF0_G_RFIO	AVSS_WFRF					GND	GND	VCCRF				DVDD18_MLDO		F
G	AVSS_WFRF			GPIO20			GND	GND	VSSANA	VSSANA	XTAL_IN_XO32M	XTAL_OUT_XO32M	AVDD15_V2P5NA	GPIO21_B	G
H	AVDD33_WF0_G_PA	OD_GPIO2_B	GPIO19	BT_UART_TX	GPIO18	BT_UART_RX					BTRST_N	GPIO18_B	GPIO19_B	GPIO20_B	H
J		OD_GPIO1_B							EXT_PWR_EN	TESTMODE	BTREGEN	BTVBAT			J
K	GPIO17	OD_GPIO0_B				GPIO8_B			VREG_OUT15	DEVICE_MODE			AVSS33_BUCK	AVDD33_BUCK	K
L	GPIO11	GPIO13	GPIO12	GPIO22	GPIO21	GPIO7_B			CHIP_EN		AVSS33_MISC			LXBK	L
M		GPIO16		GPIO11_B		GPIO5_B			RTC_EINT		VREG_IN	VSSBUCK		AVDD15_CLDO	M
N	GPIO14	GPIO15	GPIO12_B	GPIO10_B	GPIO9_B	GND	XIN	XOUT	VCCDIG	AVDD18_MLDO	AVDD33_MISC	AVSS33_MISC	VSSBUCK	AVDD12_CLDO	N
P	NC	DVDD_IO_0	DVDD_CORE		GPIO13_B	GPIO14_B		GND	VCCIO		AVDD33_VRTC		LX	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 11.1-1. AW7698N pin diagram and top view

11.1.1. AW7698N pin coordination

Table 11.1-1. AW7698N pin coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	NC	A2	GPIO4_B	A3	AVDD15_XO
A4	AVSS15_WF0_LF	A5	XO	A6	DVDD_CORE
A8	VSSLNA	A10	VSSLNA	A11	GPIO8
A13	GPIO10	A14	NC	B1	GPIO2_B
B2	GPIO1_B	B5	AVSS15_WF0_LF	B8	VSSLNA
B9	BTRF	B10	VSSLNA	B11	GPIO6
B12	GPIO7	B13	GPIO9	B14	SFSOUT
C1	AVDD15_WF0_TRX	C2	GPIO6_B	C5	GPIO0
C6	GPIO2	C7	GPIO4	C12	DVDD_IO_1
C13	SFSHOLD	C14	SFSCK	D1	AVDD33_WF0_G_TX

Pin#	Net name	Pin#	Net name	Pin#	Net name
D5	GPIO1	D6	GPIO3	D8	VSSLNA
D10	GPIO5	D13	SFSCS0	E1	AVSS_WFRF
E2	AVSS_WFRF	E5	GPIO3_B	E6	GPIO0_B
E10	VSSLNA	E11	VCCANA	E12	GND
E13	SFSIN	E14	SFSWP	F1	WF0_G_RFIO
F2	AVSS_WFRF	F7	GND	F8	GND
F9	VCCRF	F13	DVDD18_MLDO	G1	AVSS_WFRF
G4	GPIO20	G7	GND	G8	GND
G9	VSSANA	G10	VSSANA	G11	XTAL_IN_XO32M
G12	XTAL_OUT_XO32M	G13	AVDD15_V2P5NA	G14	GPIO21_B
H1	AVDD33_WF0_G_PA	H2	OD_GPIO2_B	H3	GPIO19
H4	BT_UART_TX	H5	GPIO18	H6	BT_UART_RX
H11	BTRST_N	H12	GPIO18_B	H13	GPIO19_B
H14	GPIO20_B	J2	OD_GPIO1_B	J9	EXT_PWR_EN
J10	TESTMODE	J11	BTREGEN	J12	BTVBAT
K1	GPIO17	K2	OD_GPIO0_B	K6	GPIO8_B
K9	VREG_OUT15	K10	DEVICE_MODE	K13	AVSS33_BUCK
K14	AVDD33_BUCK	L1	GPIO11	L2	GPIO13
L3	GPIO12	L4	GPIO22	L5	GPIO21
L6	GPIO7_B	L9	CHIP_EN	L11	AVSS33_MISC
L14	LXBK	M2	GPIO16	M4	GPIO11_B
M6	GPIO15_B	M9	RTC_EINT	M11	VREG_IN
M12	VSSBUCK	M14	AVDD15_CLDO	N1	GPIO14
N2	GPIO15	N3	GPIO12_B	N4	GPIO10_B
N5	GPIO9_B	N6	GND	N7	XIN
N8	XOUT	N9	VCCDIG	N10	AVDD18_MLDO
N11	AVDD33_MISC	N12	AVSS33_MISC	N13	VSSBUCK
N14	AVDD12_CLDO	P1	NC	P2	DVDD_IO_0
P3	DVDD_CORE	P5	GPIO13_B	P6	GPIO14_B
P8	GND	P9	VCCIO	P11	AVDD33_VRTC
P13	LX	P14	NC		

11.2. AW7698N pins

Table 11.2-1. Acronym for pin types and I/O structure

Name	Abbreviation	Description
Pin Type	AI	Analog input
	AO	Analog output

Name	Abbreviation	Description
	AIO	Analog bi-direction
	DI	Digital input
	DO	Digital output
	DIO	Digital bi-direction
	P	Power
	G	Ground
I/O Structure	TYPE0	Pull-up/down 3.63V tolerance
	TYPE1	Pull-up/down 5V tolerance
	TYPE2	Pull-up/down 5V tolerance SDIO characteristic support
	TYPE3	Pull-up/down 5V tolerance Analog input/output
	TYPE4	Pull-up/down VCCIO tolerance

Table 11.2-2. AW7698N series pin function description and power domain

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
Real-time clock						
M9	RTC_EINT	DIO	TYPE0	Dedicate EINT input in RTC	-	AVDD33_VRTC
N8	XOUT	AIO	-	Input pin for 32K crystal	-	AVDD33_VRTC
N7	XIN	AIO	-	Input pin for 32K crystal	-	AVDD33_VRTC
Wi-Fi radio interface						
A5	XO	AI	-	Crystal input or external clock input (26/40 MHz)	-	AVDD15_XO
C1	AVDD15_WF0_TRX	P	-	Wi-Fi TRX 1.5V power input	-	-
D1	AVDD33_WF0_G_TX	P	-	Wi-Fi TX 3.3V power input	-	-
H1	AVDD33_WF0_G_PA	P	-	Wi-Fi PA 3.3V power input (VRF)	-	-
F1	WF0_G_RFIO	AIO	-	Wi-Fi RF IO	-	AVDD33_WF0_G_PA (AO)/ AVDD15_WF0_TRX (AI)
A3	AVDD15_XO	P	-	XO 1.5V power input	-	-
Power management unit						

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
L9	CHIP_EN	AI	-	Chip enable	-	AVDD33_VRTC
J9	EXT_PWR_EN	AO	-	PMU enable	-	AVDD33_VRTC
N11	AVDD33_MISC	P	-	Power input	-	-
P11	AVDD33_VRTC	P	-	RTC domain power supply (VRTC)	-	-
N10	AVDD18_MLDO	P	-	MLDO power output for Serial Flash	-	-
M14	AVDD15_CLDO	P	-	CLDO power input from BUCK	-	-
L14	LXBK	P	-	SW node for BUCK	-	-
K13	AVSS33_BUCK	G	-	GND of AVDD33_BUCK	-	-
G13	AVDD15_V2P5NA	P	-	Internal power of BUCK	-	-
K14	AVDD33_BUCK	P	-	Buck power input (VBAT)	-	-
N14	AVDD12_CLDO	P	-	CLDO power output for core power	-	-
Serial Flash I/O						
B14	SFSOUT	DIO		serial flash data output		DVDD_MLDO
C13	SFSHOLD	DIO		serial flash data hold		DVDD_MLDO
C14	SFSCK	DIO		serial flash clock		DVDD_MLDO
D13	SFSCS0	DIO		serial flash chip select		DVDD_MLDO
E13	SFSIN	DIO		serial flash data input		DVDD_MLDO
General purpose I/O						
C5	GPIO0	DIO	TYPE3	General purpose input/output, Pin 0 Default pull-up	UART (1) I2C (1) I2S Master/Slave Cortex-M4 JTAG External front-end support BT_PRI1 PWM (0)	DVDD_IO_1
D5	GPIO1	DIO	TYPE3	General purpose input/output, Pin 1 Default pull-up	UART (1) I2C (1) I2S Master/Slave Cortex-M4 JTAG External front-end support BT_PRI3 PWM (1)	DVDD_IO_1

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
C6	GPIO2	DIO	TYPE3	General purpose input/output, Pin 2 Default pull-up	UART (0) PWM (0) I2S Master/Slave Cortex-M4 JTAG CLKO0 BT_PRI0 External front-end support	DVDD_IO_1
D6	GPIO3	DIO	TYPE3	General purpose input/output, Pin 3 Default pull-down	UART (0) PWM (1) I2S Master/Slave Cortex-M4 JTAG External front-end support	DVDD_IO_1
C7	GPIO4	DIO	TYPE1	General purpose input/output, Pin 4 Default no pull	SPI Slave (0) SPI Master (0) Cortex-M4 JTAG External front-end support	DVDD_IO_1
D10	GPIO5	DIO	TYPE1	General purpose input/output, Pin 5 Default pull-down	SPI Slave (0) SPI Master (0) UART (1) External front-end support I2S Master/Slave I2C (0) PMU_RGU_RSTB	DVDD_IO_1
B11	GPIO6	DIO	TYPE1	General purpose input/output, Pin 6 Default pull-down	SPI Slave (0) SPI Master (0) UART (1) External frontend support I2S Master/Slave I2C (0)	DVDD_IO_1
A13	GPIO10	DIO	TYPE1	General purpose input/output, Pin 10 Default pull-down	UART (2) PWM (2) PMU_RGU_RST	DVDD_IO_1

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
					B PMU_GOTO_SLEEP External frontend support SDA0	
L1	GPIO11	DIO	TYPE2	General purpose input/output, Pin 11 Default pull-down	PWM (3) UART (2) SDIO Master SDIO Slave CLKO2 External front-end support I2S Master/Slave	DVDD_IO_0
L3	GPIO12	DIO	TYPE2	General purpose input/output, Pin 12 Default pull-down	SPI Slave (1) SPI Master (1) UART (2) SDIO Master SDIO Slave External front-end support I2S Master/Slave	DVDD_IO_0
L2	GPIO13	DIO	TYPE2	General purpose input/output, Pin 13 Default pull-down	SPI Slave (1) SPI Master (1) UART (2) SDIO Master SDIO Slave CLKO4 I2S Master/Slave	DVDD_IO_0
N1	GPIO14	DIO	TYPE2	General purpose input/output, Pin 14 Default pull-down	SPI Slave (1) SPI Master (1) I2S Master/Slave SDIO Master SDIO Slave PWM (4) CLKO4	DVDD_IO_0
N2	GPIO15	DIO	TYPE2	General purpose input/output, Pin 15	SPI Slave (1)	DVDD_IO_0

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
				Default pull-down	SPI Master (1) I2S Master/Slave SDIO Master SDIO Slave I2C (1) PWM (3)	
M2	GPIO16	DIO	TYPE2	General purpose input/output, Pin 16 Default pull-down	SPI Slave (1) SPI Master (1) I2S Master/Slave SDIO Master SDIO Slave I2C (1)	DVDD_IO_0
K1	GPIO17	DIO	TYPE3	General purpose input/output, Pin 17 Default pull-down	SPI Slave (1) SPI Master (1) I2S Master/Slave PWM (5) CLKO3 AUXADC0 BT_PRI0	DVDD_IO_0
H5	GPIO18	DIO	TYPE3	General purpose input/output, Pin 18 Default no pull	PMU_GOTO_SLEEP I2S Master/Slave CLKO4 I2C (1) ZCV CLKO3 PMU_RGU_RSTB	DVDD_IO_0
H3	GPIO19	DIO	TYPE3	General purpose input/output, Pin 19 Default pull-up	UART (0) I2C (1) PWM (5) AUXADC2	DVDD_IO_0
G4	GPIO20	DIO	TYPE3	General purpose input/output, Pin 20 Default no pull	UART (0) AUXADC3	DVDD_IO_0
L5	GPIO21	DIO	TYPE3	General purpose input/output, Pin 21 Default pull-up	UART (0)	DVDD_IO_0

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
L4	GPIO22	DIO	TYPE3	General purpose input/output, Pin 22 Default no pull	UART (0)	DVDD_IO_0
BT control interface						
B9	BTRF	AIO		BT RF IO		
K10	DEVICE_MODE	G		BT mode for FT testing		
H11	BTRST_N	DI		BT global reset, active low	Pull high resistor: 137K ohm	
J11	BTREGEN	AI		BT power ready		
J12	BTVBAT	Supply, 2.97V~ 3.63V		VCC for LDO and Buck		
H4	BT_UART_TX	DO		BT UART TX		
H6	BT_UART_RX	DI		BT UART RX		
G11	XTAL_IN_XO32M	AIO		Crystal input	XO32M_IN	
G12	XTAL_OUT_XO32M	AIO		Crystal output	XO32M_OUT	
K9	VREG_OUT15	AIO		LDO1.5V output		
M11	VREG_IN	AIO		Switch regulator feedback path/ LDO output	Switching Regulator output	
P13	LX	AIO		Switching Regulator output		
J10	TESTMODE			BT TESTMODE		
Limited output						
E6	GPIO0_B	DIO	TYPE4	limited output, Default pull-down		
B2	GPIO1_B	DIO	TYPE4	limited output, Default pull-down		
B1	GPIO2_B	DIO	TYPE4	limited output, Default pull-down		
E5	GPIO3_B	DIO	TYPE4	limited output, Default pull-down		
A2	GPIO4_B	DIO	TYPE4	limited output, Default pull-down		
C2	GPIO6_B	DIO	TYPE4	limited output, Default pull-down		
L6	GPIO7_B	DIO	TYPE4	limited output, Default pull-down		
K6	GPIO8_B	DIO	TYPE4	limited output,		

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
				Default pull-down		
N5	GPIO9_B	DIO	TYPE4	limited output, Default pull-down		
N4	GPIO10_B	DIO	TYPE4	limited output, Default pull-down		
M4	GPIO11_B	DIO	TYPE4	limited output, Default pull-down		
N3	GPIO12_B	DIO	TYPE4	limited output, Default pull-down		
P5	GPIO13_B	DIO	TYPE4	limited output, Default pull-down		
P6	GPIO14_B	DIO	TYPE4	limited output, Default pull-down		
M6	GPIO15_B	DIO	TYPE4	limited output, Default pull-down		
H12	GPIO18_B	DIO	TYPE4	limited output, Default pull-down		
H13	GPIO19_B	DIO	TYPE4	limited output, Default pull-down		
H14	GPIO20_B	DIO	TYPE4	limited output, Default pull-down		
G14	GPIO21_B	DIO	TYPE4	limited output, Default pull-down		
K2	OD_GPIO0_B	DIO	OD	limited output, Default open-drain, external pull-up is necessary		
J2	OD_GPIO1_B	DIO	OD	limited output, Default open-drain, external pull-up is necessary		
H2	OD_GPIO2_B	DIO	OD	limited output, Default open-drain, external pull-up is necessary		
Digital IO power/core power of Wi-Fi						
C12	DVDD_IO_1	P	-	Power input of GPIO left group (VIO_1)	-	-
P2	DVDD_IO_0	P	-	Power input of GPIO right group (VIO_0)	-	-
F13	DVDD18_MLDO	P	-	Power input of SF/EMI	-	-
A6	DVDD_CORE	P	-	Core power	-	-

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
P3	DVDD_CORE	P	-	Core power	-	-
Digital IO power/core power of BT						
N9	VCCDIG	Supply, 1.5V		VCC Digital Supply LDO1.5V output	Need Capacitor for regulated	
P9	VCCIO	Supply, 1.7V~ 3.6V		VCC for IO		
F9	VCCRF	Supply, 1.7V/ 1.9V		VCC for RF		
E11	VCCANA	Supply, 1.5V		VCC for Analog		
Ground						
E1	AVSS_WFRF	G		WiFi RF ground		
E2	AVSS_WFRF	G		WiFi RF ground		
F2	AVSS_WFRF	G		WiFi RF ground		
G1	AVSS_WFRF	G		WiFi RF ground		
A8	VSSLNA	G		RF LNA ground		
A10	VSSLNA	G		RF LNA ground		
B8	VSSLNA	G		RF LNA ground		
B10	VSSLNA	G		RF LNA ground		
D8	VSSLNA	G		LNA ground		
E12	GND	G		ground		
F7	GND	G		ground		
F8	GND	G		ground		
G7	GND	G		ground		
G8	GND	G		ground		
N6	GND	G		ground		
P8	GND	G		ground		
A4	AVSS15_WF0_LF	G		WiFi RF ground		
B5	AVSS15_WF0_LF	G		WiFi RF ground		
G9	VSSANA	G		ground for Analog		
G10	VSSANA	G		ground for Analog		
L11	AVSS33_MISC	G		ground for MISC		
M12	VSSBUCK	G		ground for BUCK		
N12	AVSS33_MISC	G		ground for MISC		
N13	VSSBUCK	G		ground for BUCK		

Pin Number	Pin Name	Pin Type	I/O Structure	Pin Description	Alternate Pin Functions	Power domain
No Connection						
A1	NC			No connection		
A14	NC			No connection		
P1	NC			No connection		
P14	NC			No connection		

11.3. AW7698N series pin multiplexing

The AW7698N series platform offers 16 GPIO pins. By setting up the control registers, the MCU software can control the direction, the output value and read the input values on the pins. The GPIOs and GPOs are multiplexed with other functions to reduce the pin count. To facilitate application use, the software can configure which clock to send outside the chip. There are five clock-out ports embedded in GPIO pins and each clock-out can be programmed to output an appropriate clock source. In addition, when two GPIOs function for the same peripheral IP, the smaller GPIO serial number has higher priority over the bigger one.

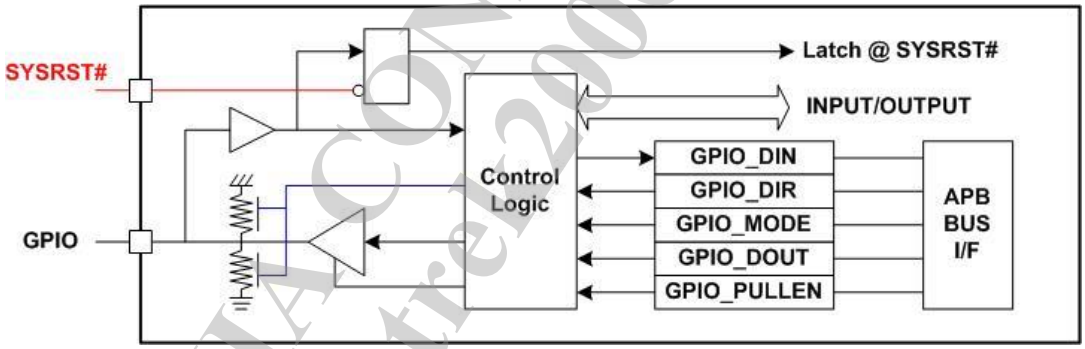


Figure 11.3-1. GPIO block diagram

The AW7698N series has rich peripheral functions and the peripheral signals are shown in Table 11.3-1. The SDIO, SPI Master and SPI Slave can support signal group allocate on different pins.

Table 11.3-1. Peripheral functions and signals

Alternate Function	Signal List
SDIO Master	MA_MC0_CK
	MA_MC0_CM0
	MA_MC0_DA0
	MA_MC0_DA1
	MA_MC0_DA2
	MA_MC0_DA3

Alternate Function	Signal List
SDIO Slave	SLV_MC0_CK SLV _MC0_CM0 SLV _MC0_DA0 SLV _MC0_DA1 SLV _MC0_DA2 SLV _MC0_DA3
UART (0)	URXD0 UTXD0 U0RTS U0CTS
UART (1)	URXD1 UTXD1 U1RTS U1CTS
UART (2)	URXD2 UTXD2 U2RTS U2CTS
I2C (0)	SCL0 SDA0
I2C (1)	SCL1 SDA1
I2C (2)	SCL2 SDA2
I2S Master/Slave	I2S_RX I2S_TX I2S_WS I2S_CK
I2S Master/Slave	TDM_RX TDM_TX TDM_WS TDM_CK TDM_MCLK
SPI Master (0)	SPIMST_A_SCK SPIMST_A_CS SPIMST_A_SIO0 SPIMST_A_SIO1 SPIMST_A_SIO2 SPIMST_A_SIO3
SPI Master (1)	SPIMST_B_SCK SPIMST_B_CS SPIMST_B_SIO0 SPIMST_B_SIO1

Alternate Function	Signal List
	SPIMST_B_SIO2 SPIMST_B_SIO3
SPI Slave (0)	SPISLV_A_SCK SPISLV_A_CS SPISLV_A_SIO0 SPISLV_A_SIO1 SPISLV_A_SIO2 SPISLV_A_SIO3
SPI Slave (1)	SPISLV_B_SCK SPISLV_B_CS SPISLV_B_SIO0 SPISLV_B_SIO1 SPISLV_B_SIO2 SPISLV_B_SIO3
PWM (0)	PWM0
PWM (1)	PWM1
PWM (2)	PWM2
PWM (3)	PWM3
PWM (4)	PWM4
PWM (5)	PWM5
AUXADC	AUXADCIN_0 AUXADCIN_1 AUXADCIN_2 AUXADCIN_3
CM4 JTAG	JTDI JTMS JTCK JTRST_B JTDO
External frontend support	WIFI_ANT_SEL0 WIFI_ANT_SEL1 WIFI_ANT_SEL2 WIFI_ANT_SEL3 WIFI_ANT_SEL4
timer32 (0)	timer32_0_cap0 (in) timer32_0_cap1 (in)
timer32 (1)	timer32_0_em0 (out) timer32_0_em1 (out) timer32_0_em2 (out) timer32_0_em3 (out)
SPI_B	SPI_CSN SPI_MOSI SPI_MISO

Alternate Function	Signal List
	SPI_CLK
XOUT_32K	XOUT_32K_in XOUT_32K_out

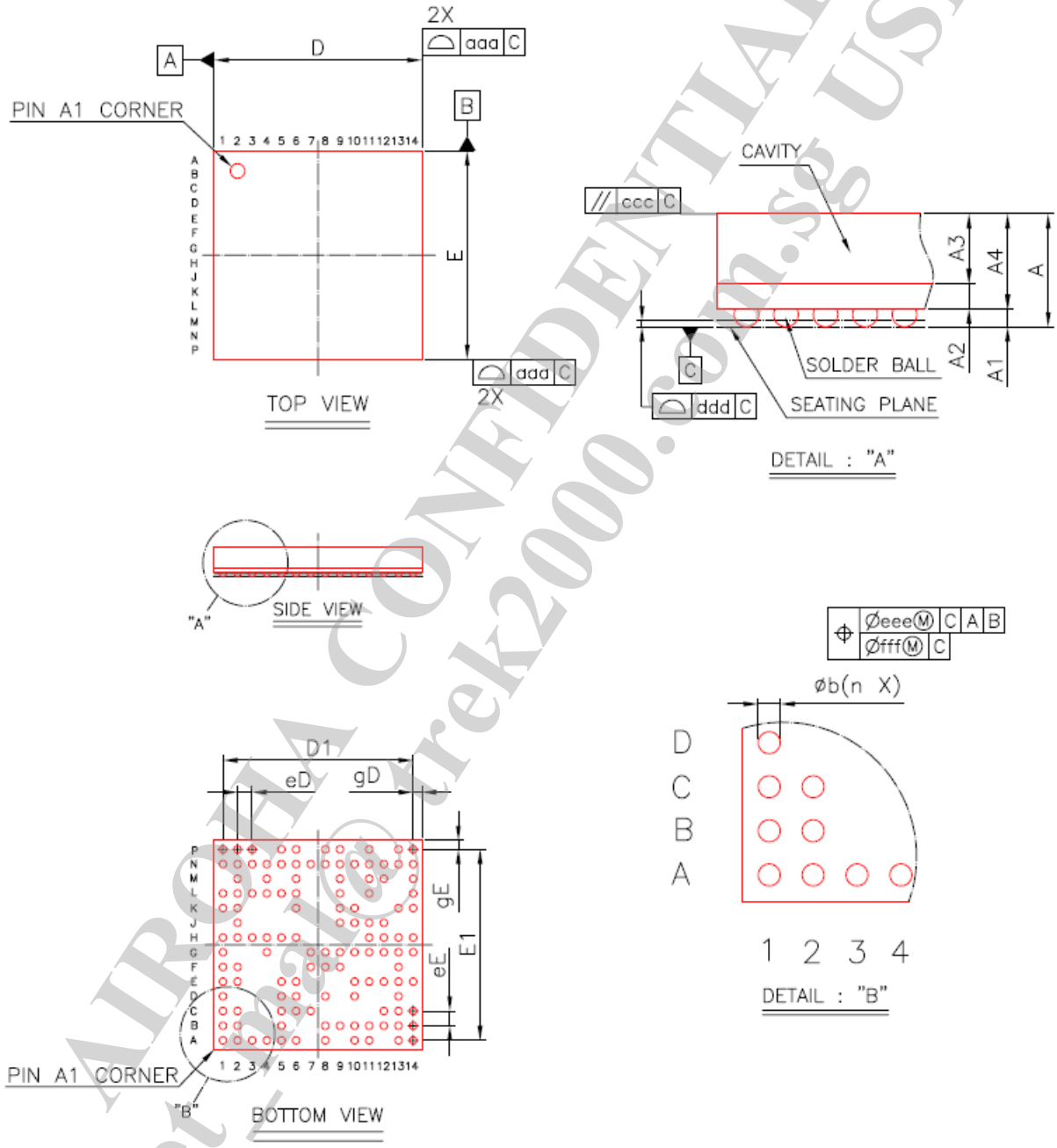
Table 11.3-2. PinMux description

Ball Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3	Aux Func.4	Aux Func.5	Aux Func.6	Aux Func.7	Aux Func.8	Aux Func.9	Aux Func.10
GPIO_0	GPIO0	EINT0		U1RTS	SCL1	I2S_RX	JTDI		WIFI_ANT_SEL0	BT_PRI1	PWM0
GPIO_1	GPIO1	EINT1		U1CTS	SDA1	I2S_TX	JTMS		WIFI_ANT_SEL1	BT_PRI3	PWM1
GPIO_2	GPIO2	EINT2		URXD0	PWM0	I2S_WS	JTCK	CLKO0		BT_PRI0	WIFI_ANT_SEL4
GPIO_3	GPIO3	EINT3		UTXD0	PWM1	I2S_CK	JTRST_B			WIFI_ANT_SEL2	I2S_CK
GPIO_4	GPIO4	SPISLV_A_SIO2	SPIMST_A_SIO2	EINT4		I2S_MCLK	JTDO			WIFI_ANT_SEL3	I2S_MCLK
GPIO_5	GPIO5	SPISLV_A_SIO3	SPIMST_A_SIO3	EINT5	URXD1	WIFI_ANT_SEL0	TDM_RX			SCL0	PMU_RGU_RSTB
GPIO_6	GPIO6	SPISLV_A_CS	SPIMST_A_CS	EINT6	UTXD1	WIFI_ANT_SEL1	TDM_TX			SDA0	
GPIO_7	GPIO7	SPISLV_A_SCK	SPIMST_A_SCK	EINT7	CLKO1	WIFI_ANT_SEL2	TDM_WS			BT_PRI3	
GPIO_8	GPIO8	SPISLV_A_SIO0	SPIMST_A_SIO0	EINT8	SCL0	U0RTS	TDM_CK		BT_PRI0		
GPIO_9	GPIO9	SPISLV_A_SIO1	SPIMST_A_SIO1	EINT9	SDA0	U0CTS	TDM_MCLK		WIFI_ANT_SEL3	BT_PRI1	
GPIO_10	GPIO10	EINT10	SDA0	U2CTS	PWM2	PMU_RGU_RSTB	PMU_GOTO_SLEEP		WIFI_ANT_SEL4		SDA0
GPIO_11	GPIO11	EINT11	PWM3	URXD2	MA_MC0_CK	SLV_MC0_CK	CLKO2			WIFI_ANT_SEL0	I2S_RX
GPIO_12	GPIO12	SPISLV_B_SIO3	SPIMST_B_SIO3	U2RTS	MA_MC0_CM0	SLV_MC0_CM0	EINT12			WIFI_ANT_SEL1	I2S_TX
GPIO_13	GPIO13	SPISLV_B_SIO2	SPIMST_B_SIO2	UTXD2	MA_MC0_DA0	SLV_MC0_DA0	CLKO4		EINT13		I2S_WS
GPIO_14	GPIO14	SPISLV_B_SIO1	SPIMST_B_SIO1	TDM_RX	MA_MC0_DA1	SLV_MC0_DA1	PWM4		EINT14		CLKO4
GPIO_15	GPIO15	SPISLV_B_SIO0	SPIMST_B_SIO0	TDM_TX	MA_MC0_DA2	SLV_MC0_DA2	SCL1		EINT15		PWM3
GPIO_16	GPIO16	SPISLV_B_SCK	SPIMST_B_SCK	TDM_WS	MA_MC0_DA3	SLV_MC0_DA3	SDA1		EINT16		
GPIO_17	GPIO17	SPISLV_B_CS	SPIMST_B_CS	TDM_CK	PWM5	CLKO3	AUXADC0		EINT17		BT_PRI0

GPIO_18	GPIO18	PMU_GOTO_SLEEP		TDM_MCLK	CLKO4	SDA1	ZCV (SW set AUXADC1)		EINT18	CLKO3	PMU_RGU_RSTB
GPIO_19	GPIO19	URXD0	EINT19	SCL1			AUXADC2				
GPIO_20	GPIO20	UTXD0	EINT20				AUXADC3				
GPIO_21	GPIO21	URXD0	EINT19	SCL1							
GPIO_22	GPIO22	UTXD0	EINT20								
GPIO0_B											
GPIO1_B											
GPIO2_B											
GPIO3_B											
GPIO4_B											
GPIO6_B											
GPIO7_B											
GPIO8_B											
GPIO9_B											
GPIO10_B											
GPIO11_B		GPIO11									
GPIO12_B											
GPIO13_B											
GPIO14_B											
GPIO15_B											
GPIO18_B											
GPIO19_B									GPIO8		
GPIO20_B										GPIO7	
GPIO21_B		GPIO21								GPIO9	
OD_GPIO0_B											
OD_GPIO1_B											
OD_GPIO2_B											

12. Package Description

12.1. AW7698N mechanical data of the package



Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			TFBGA		
Body Size	X	D	7.05	7.10	7.15
	Y	E	7.05	7.10	7.15
Ball Pitch	X	eD	0.50		
	Y	eE	0.50		
Mold Thickness		A3	0.70 Ref.		
Substrate Thickness		A2	0.13 Ref.		
Substrate+Mold Thickness		A4	0.78	0.83	0.88
Total Thickness		A	–	–	1.05
Ball Diameter			0.25		
Ball Stand Off		A1	0.10	0.15	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	122		
Edge Ball Center to Center	X	D1	6.50		
	Y	E1	6.50		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

Figure 12.1-1. Outlines and dimensions of AW7698N 7.1-mm x 7.1-mm x 1.05-mm 122 balls TFBGA package

12.2. AW7698N thermal operating specifications

Table 12.2-1. AW7698N thermal performance

Description	Value	Unit
Maximum Junction Temperature(Plastic Package)	125	°C
Theta JA	59.8	°C/W
Theta JC	21.1	°C/W
Theta JB	50.7	°C/W
Psi JT	0.99	°C/W

12.3. Lead-frame packaging

The AW7698N platform is provided in a lead-frame package and meets RoHS requirements.

13. Ordering Information

13.1. AW7698N top marking definition

Line1: device name
Line2: date code & fab code
Line3: assembly code & U1 wafer lot
Line4: fab code & U2 wafer lot

Figure 13.1-1. Mass production top marking of AW7698N

Table 13.1-1. Ordering information

Product number	Package	Description
AW7698N	TFBGA	7.1-mm x 7.1-mm x 1.05-mm 122 balls with 0.5-mm ball pitch