

AW7698 Efuse Content Guideline

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Document revision history

Revision	Date	Description
1.0	23 May 2019	Initial release
1.1	22 Oct 2019	Update BT address and eFEM efuse part
1.2	07 Nov 2019	Add note on WIFI/BT MAC page





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1. Introduction

The AW7698 E-FUSE layout provides configuration for vendor/product ID, SW setting, RF setting.



2. Efuse Address Map

2.1. Register map

Security control and status registers are available over APB bus interface and corresponding address map is as shown in Table 1. Base address is specific to the project AW7698.

Table 1. Register map

Offset	Value	Description	Write owner	Value
A20A0140		Customer_CTRL	Customer	Option
A20A0204		WLAN MAC Address	Customer	Option
A20A0208		WLAN MAC Address	Customer	Option
Offset 0x890		BT Address	Customer	Option
Offset 0x894		BT Address	Customer	Option
A20A0230		Crystal_Trim	Customer	Option
A20A0404		WIFI_EFUSE1	Customer	Option
A20A0408		WIFI_EFUSE2	Customer	Option
A20A0410		WIFI_EFUSE4	Customer	Option
A20A0414		WIFI_EFUSE5	Customer	Option



3. Register Definitions

3.1. A20A0140 Customer_CTRL

A20A0	140	<u>C_C1</u>	<u>rrl</u>			(Custo	mer_	CTRL		/				000	00000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														C_C	TRL	
Type												y ,				
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								C_C	TRL			7				
Type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 2. Description of C_CTRL

Bit(s)	Name	Description
		2: EFUSE_SDIO_TIMEOUT_ENLARGE
		0: the timeout of XBoot over SDIO is 2 seconds.
19:0	C_CTRL	1: the timeout of XBoot over SDIO is 10 seconds.
		Note: If the product does not need XBoot over SDIO, the customer does not need to use the
		eFuse bit.
		5: EFUSE_RTC_MODE_ULTRA_DEEP_SLEEP
		1: BROM skips some process when the system wakes up from retention mode.
		Note: When the eFuse bit is burned and RTC bit is set, then BROM will skip 150ms waiting time for command mode.
		8: SF IS SPI QUAD MODE
		0: configure serial flash as SPI mode in BROM.
		1: configure serial flash as SPI Quad mode in BROM.
		Note: If we configure as SPI mode, it spends approximately 30 ms to copy the 64KB
		bootloader. If we configure as SPI Quad mode, it spends approximately 16 ms to copy 64KB
		bootloader
		9: EFUSE_SF_FAST_BOOT_DIS
		0: reduce boot time by improving status check in SF. The waiting time for flash ready is
		approximately 1 ms.
		1: disable the improvement. Apply the legacy check. The waiting time for flash ready is
		approximately 40 ms.
		10: EFUSE_BROM_LOG_DIS
		0: BROM prints log to show execution result. It spends approximately 10 ms.
		1: disable the BROM log to reduce boot time by approximately 10 ms.
	V'	11~13: EFUSE_SF_VENDDOR_ID
	y	0: MXIC
		1: Winbond
		2: GD
		3: MICRON
		4 ~ 7: reserved
		14: EFUSE_SF_CHECK_ID_EN
	7	1: enable the check of EFUSE_SF_VENDDOR_ID and SF manufactory ID.
		Note: If the eFuse bit is burned, BROM checks whether the SF ID is matched to



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Bit(s)	Name	Description	
		EFUSE_SF_VENDDOR_ID.	
		If the check is failed, SF is configured as SPI mode.	7

3.2. A20A0204 WLAN MAC Address

A20A0	204	<u>WLA</u>	<u>N0</u>			1	WLAN	MAC			<i>)</i>		000	00000		
Bit	31	30	29	28	28 27 26 25 24 23 22 21 20 19									18	17	16
Name			WLAN0													
Type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WLAN0															
Type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3. Description of WLAN MAC Address

Bit(s)	Name	Description			
31:0	WLAN0	WLAN MAC Address [47:16].	Y		

3.3. A20A0208 WLAN MAC Address

A20A0	208	8 WLAN MAC Address										00000000				00000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		WLAN0														
Type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4. Description of WLAN MAC Address

Bit(s)	Name	Description
15:0	WLAN0	WLAN MAC Address [15:0].

Note:

MAC_ADDRESS[1st] = Efuse offset 0x207
MAC_ADDRESS[2nd] = Efuse offset 0x206
MAC_ADDRESS[3rd] = Efuse offset 0x205
MAC_ADDRESS[4th] = Efuse offset 0x204
MAC_ADDRESS[5th] = Efuse offset 0x209
MAC_ADDRESS[6th] = Efuse offset 0x208

3.4. Offset 0x890 BT MAC Address

0x890		BD_	ADDR	<u> </u>	Bluetooth Address										0000	00000
Bit	31 30 29 28 27 26 25 24 23 22 21 20 19										18	17	16			
Name	BD_ADDR											,				
Type																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								BD_A	DDR			77		\ \ \		
Type	(A) Y															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5. Description of Bluetooth Address

Bit(s)	Name	Description	
31:0	BD_ADDR	BT Address [47:16].	

3.5. Offset 0x894 BT MAC Address

0x894		BD A	ADDR	<u> </u>		E	0000000									
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						X										
Type							Y									
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							M	BD_A	ADDR							
Type								Y								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6. Description of Bluetooth Address

Bit(s)	Name	Description
15:0	BD ADDR	BT Address [15:0].

Note

BT_ADDRESS[1st] = Efuse offset 0x895

BT_ADDRESS[2nd] = Efuse offset 0x894

BT_ADDRESS[3rd] = Efuse offset 0x893

BT_ADDRESS[4th] = Efuse offset 0x892

BT ADDRESS[5th] = Efuse offset 0x891

BT_ADDRESS[6th] = Efuse offset 0x890



3.6. A20A0230 Crystal Trim

A20A0	230	XO_	<u>Trim</u>			(Crysta	l Trin	1	0000000						
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								XO_1	RIM						,	
Type												_				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								XO_1	RIM			77		\ \ \		
Type												Y				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7. Description of crystal trim

Bit(s)	Name	Description
31:0	XO_TRIM	16~23:XTAL_TRIM_2 24~31:XTAL_TRIM_3 [23:16]/[31:24] is used for crystal re-calibration purpose in customer production line If customers want to re-do frequency trimming on the customer production line, please use [23:16]/[31:24] as second /third frequency offset. The rom/firmware code checks Bit23 and Bit31 to determine whether the crystal trim code must be updated or not. Here is the formula: If (0xA20A0230[31] == 1) XTAL_CTL4[14:8] = 0xA20A0230[30:24]; Else if (0xA20A0230[23] == 1) XTAL_CTL4[14:8] = 0xA2020230[22:16]; Else Use default vale.



Reset

3.7. A20A0404 WIFI_EFUSE1

A20A040	04 <u>W</u>	IFI_E	FUS	<u>E1</u>		W	/IFI_EF	USE1	00000000								
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	WIFI _EFU SE1_ VALI D			TX_s hapin g_typ e	_	_PA nfig	TSSI _ena ble_b it	TX_D PD_C alibra tion_ enabl e			O_Cali O_offs		Ther	mal_sl n_d	lope_o lrop	f_gai	
Type	RO			RO	R	.0	RO	RO]	RO	7/	RO				
Reset	0			0	0	0	1	1	0	0	0	/ 0 /	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	WF_ LDO_ EFUS E_VA LID							A	RG.		DIV VS	LDO	RG_V	WFo_7	FRXLD S	00_V	
Type	RO									/ 1	RO_			D	\circ		

Table 8. Description of WIFI_EFUSE1

Bit(s)	Name	Description
31	WIFI_EFUSE1_VALID	Valid bit of WIFI_EFUSE1
		1'bo: not valid 1'b1: valid
28	TX_shaping_type	TX_shaping_type
27:26	TX_PA_config	TX PA config
		00: FPA 01: HPA
		10: MPA
		11: dynamic PA
25	TSSI_enable_bit	TSSI enable/disable bit
24	TX_DPD_Calibration_enable	2G TX DPD Calibration (enable/disable bit)
23:20	TX_DPD_Calibration_Go_offset	2G TX DPD Calibration (Go offset[3:0])
19:16	Thermal_slope_of_gain_drop	Thermal slope of gain drop,bit3~0: FPA, 0.25dB/step
15	WF_LDO_EFUSE_VALID	Valid bit of wifi RF LDO EFUSE
		1'bo: not valid 1'b1: valid
7:4	RG_WFo_DIVLDO_VS	For laser RTP issue, 1.225V tuning
3:0	RG WFo TRXLDO VS	For laser RTP issue, 1.3V tuning



3.8. A20A0408 WIFI_EFUSE2

A20A0)408 <u>WIFI</u>	EFUS	<u>SE2</u>	W							00000000					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WIFI_ EFUSE2_ VALID		ePA_ enable	eLNA_ enable	iPA _.		_Gba loss	nd_	Ex	cterna /	al_bypa	ass_P	1dB	- N	cterna bass_g	_
Type	RO		RO	RO		R	0	RO						RO		
Reset	0		0	0	0	0	0	0	0	0	7-0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	External_bypa gain	ass_	Exte	rnal_LNA_		Ext	ernal	_LNA	_gain		eP	ePA_gain				
Туре	RO			RO				X	F	RO				RO		
Reset	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0

Table 9. Description of WIFI_EFUSE2

Bit(s)	Name	Description
31	WIFI_EFUSE2_VALID	Valid bit of WIFI_EFUSE2
		1'b0: not valid
		1'b1: valid
29	ePA_enable	ePA enable
		1'b0: disable
		1'b1: enable
28	eLNA_enable	eLNA enable
	_	1'b0: disable
		1'b1: enable
27:24	iPA_ePA_Gband_FE_loss	iPA/ePA Gband FE loss between Ant and Chip out
23:19	External_bypass_P1dB	External bypass P1dB for 2G
18:14	External_bypass_gain	External bypass gain for 2G
13:10	External_LNA_P1dB	External LNA P1dB for 2G
8:5	External_LNA_gain	External LNA gain for 2G
4:0	ePA_gain	ePA gain for 2G



Note: there is no complete verification on WIFI_EFUSE2; If enabling the external PA/LNA function is necessary, please contact an Airoha engineer for assistance.

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3.9. A20A0410 WIFI_EFUSE4

A20A0	410	WIF	_EFU	SE4		1	WIFI_	EFUSE4 0000								00000	
Bit	31	30	29	28	27	26	25	24	23 22 21 20 19 18 17 16								
Name	WIFI_ EFUSE4_ VALID								TX_power_offset_middle								
Type																	
Reset	0								0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name		7	TX_pov	ver_of	fset_lc	w						TX_p	ower				
Туре																	
Reset	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	

Table 10. Description of WIFI_EFUSE4

Bit(s)	Name	Description
		Valid bit of WIFI_EFUSE4
31	WIFI_EFUSE4_VALID	1'b0: not valid
		1'b1: valid
23:16	TX_power_offset_middle	TX0 2.4G TX power offset middle (CH6~10) (delta, dB)
		B23: valid bit
		B22: 0: decrease power; 1: increase power
		B21~B16 is Power delta related to origin target power. Unit: 0.5dB
15:8	TX power offset low	TX0 2.4G TX power offset low (CH1~5) (delta, dB)
		B15: valid bit
		B14: 0: decrease power; 1: increase power
		B13~B8 is Power delta related to origin target power. Unit: 0.5dB
7:0	TX_power	TXO 2.4G TX power (54Mbps, dBm absolute value)
		B7 is valid bit
		B6 is sign bit, 0 is negative, 1 is positive
		B5~B0 is power
		1step = 0.5dB.
		For example, if set as 0x800000E0, 54MBps Tx power is 16dBm.

3.10. A20A0414 WIFI_EFUSE5

A20A	0414	WIF	_EFU	<u>SE5</u>		1	WIFI_	EFUSI	E5		00000000					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WIFI_ EFUSE5_ VALID								TX02	G_PA_	TSSI_	offset	, ,	E	>	
Type	RO									R	0			7		
Reset	0				1	1	0	0	1	0	1	1 .	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			TXo	2G_P	A_TSS	_slop	e	=			TX_p	ower_	offset	_high		
Туре					RO RO											
Reset		1	0	1	0	1	0	1	0	1 /	0	1	0	1	0	1

Table 11. Description of WIFI_EFUSE5

Bit(s)	Name	Description
31	WIFI_EFUSE5_VALID	Valid bit of WIFI_EFUSE5 1'bo: not valid 1'b1: valid
27:16	TX02G_PA_TSSI_offset	TX0 2.4G PA TSSI offset
14:8	TXo2G_PA_TSSI_slope	TXo 2.4G PA TSSI slope
7:0	TX_power_offset_high	TX0 2.4G TX power offset high(CH11~14)(delta,dB)