Main Memory (Part II)

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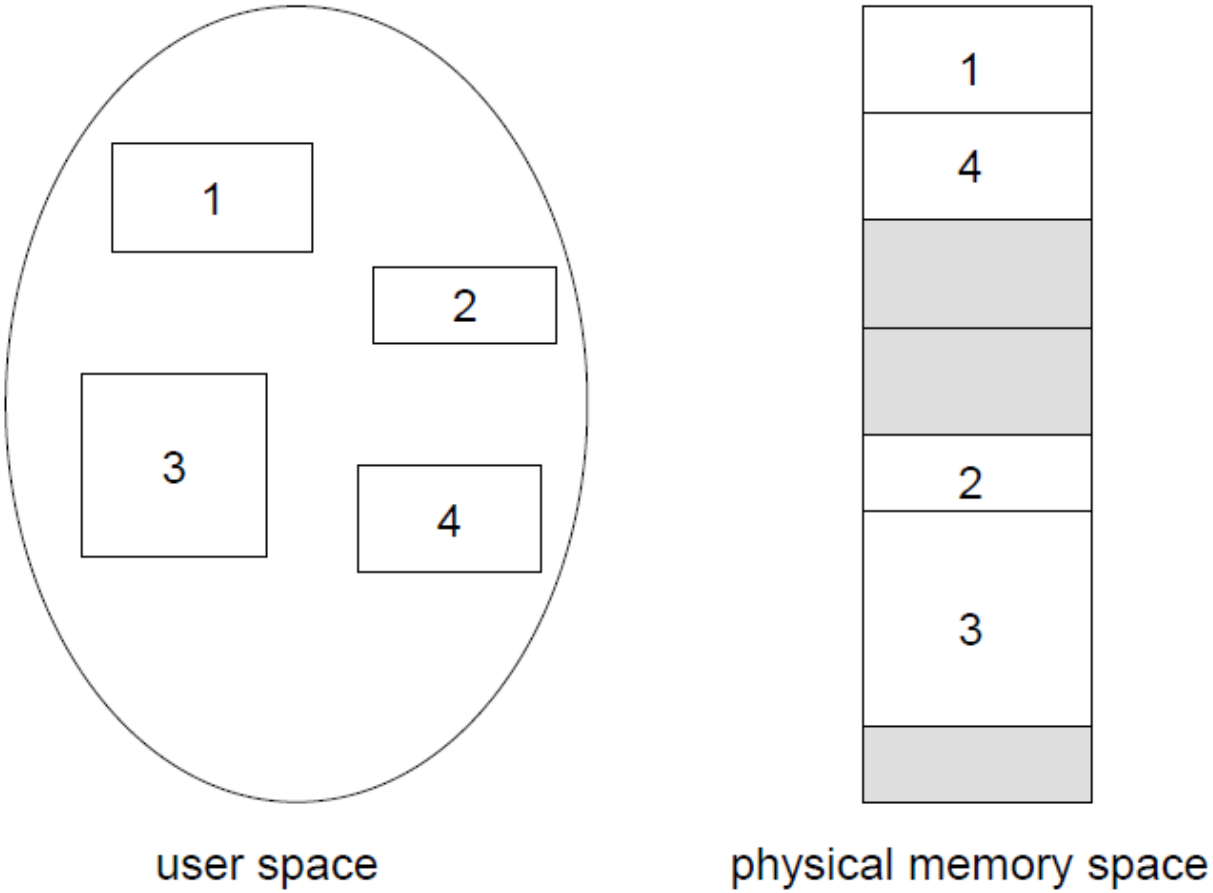
Reminder

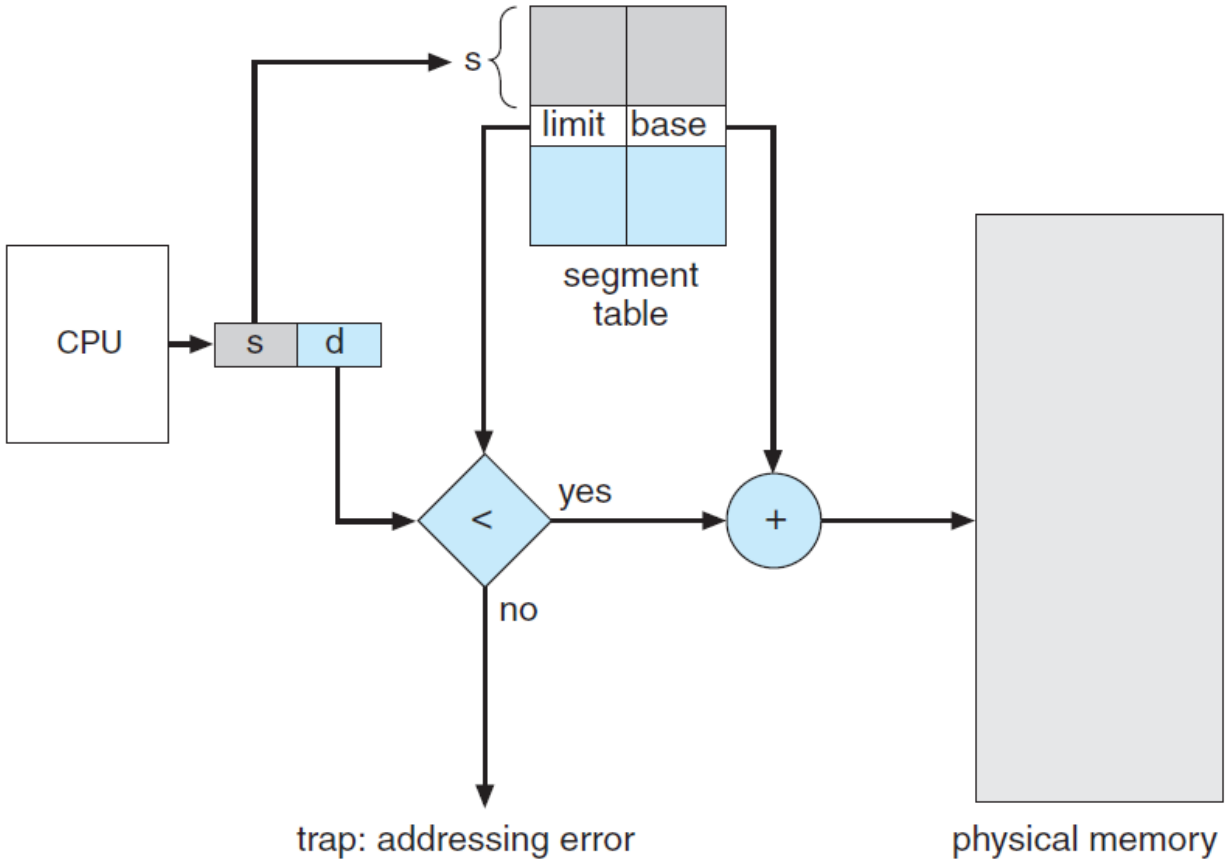
Reminder (1/3)

- External fragmentation vs. internal fragmentation
- Compaction: shuffle memory contents to place all free memory together in one large block.
- Other solutions:
  - Segmentation
  - Paging

Reminder (2/3)



Reminder (3/3)


s
limit
base
segment table
CPU
s
d
<
yes
+
no
trap: addressing error
physical memory

Paging

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- Paging avoids external fragmentation and the need for compaction, whereas segmentation does not.

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- To run a program of size N pages, need to find N free frames and load program.
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- Still have internal fragmentation.

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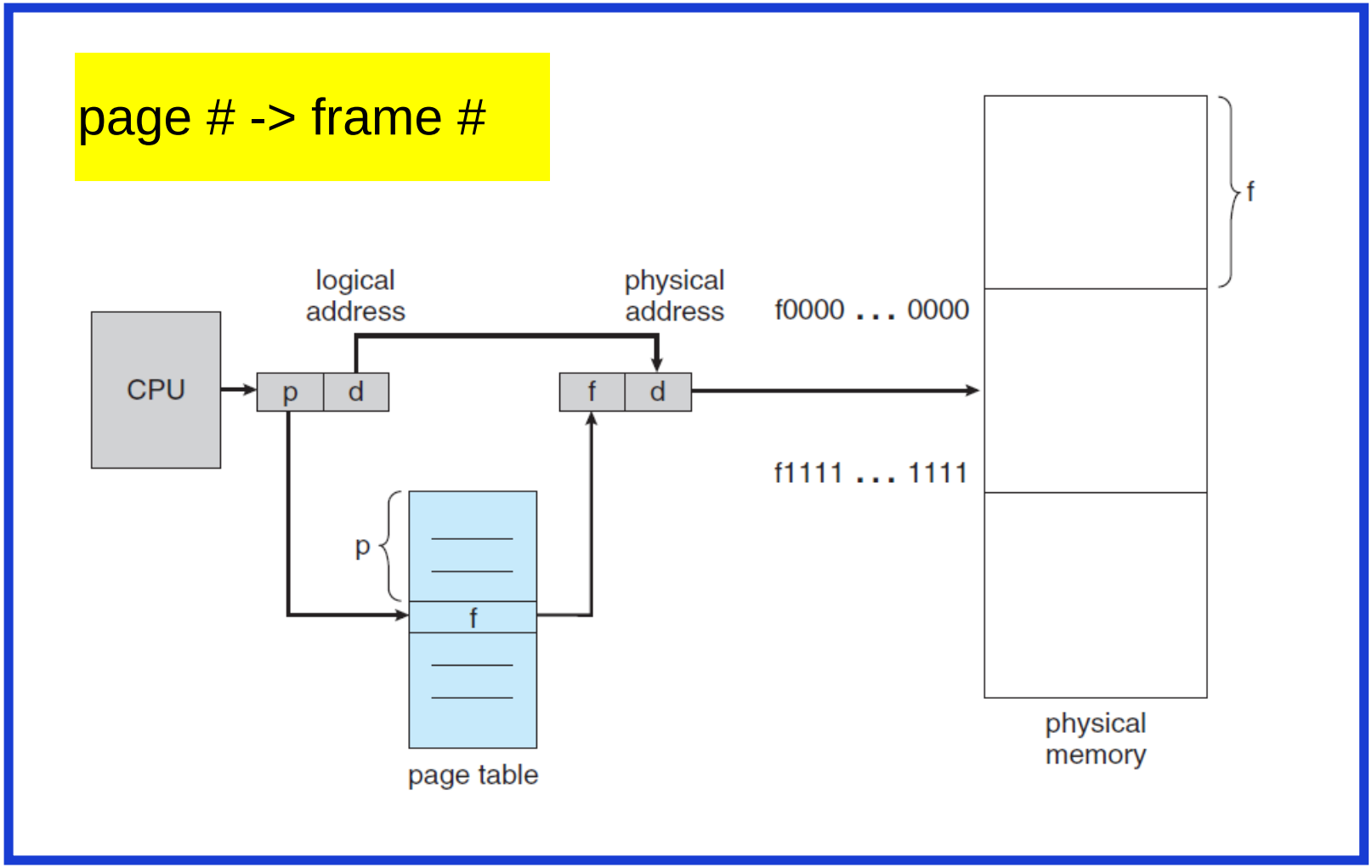
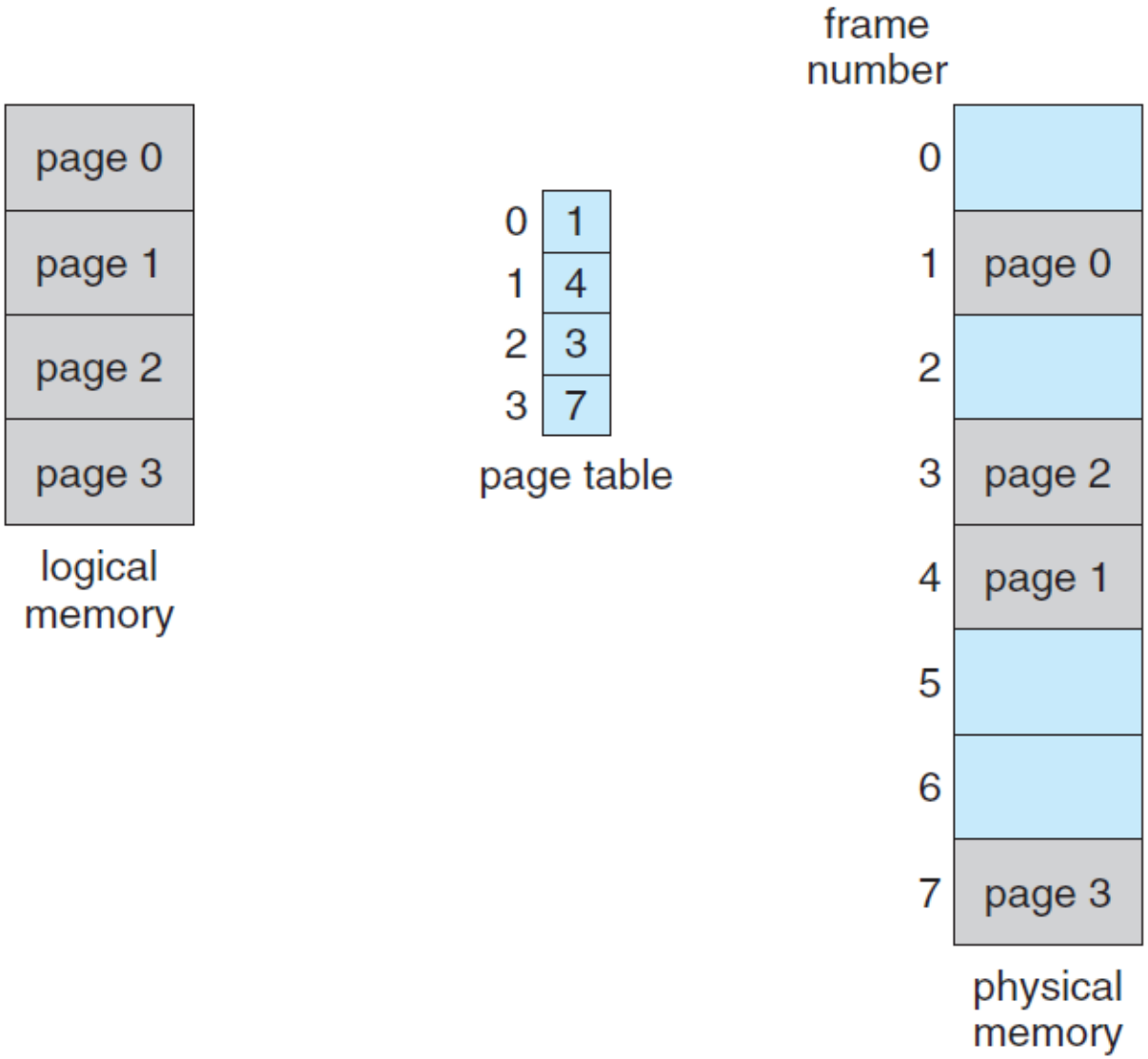
- For given logical address space 2^m and page size 2^n.

Paging Hardware



Paging Model of Logical and Physical Memory



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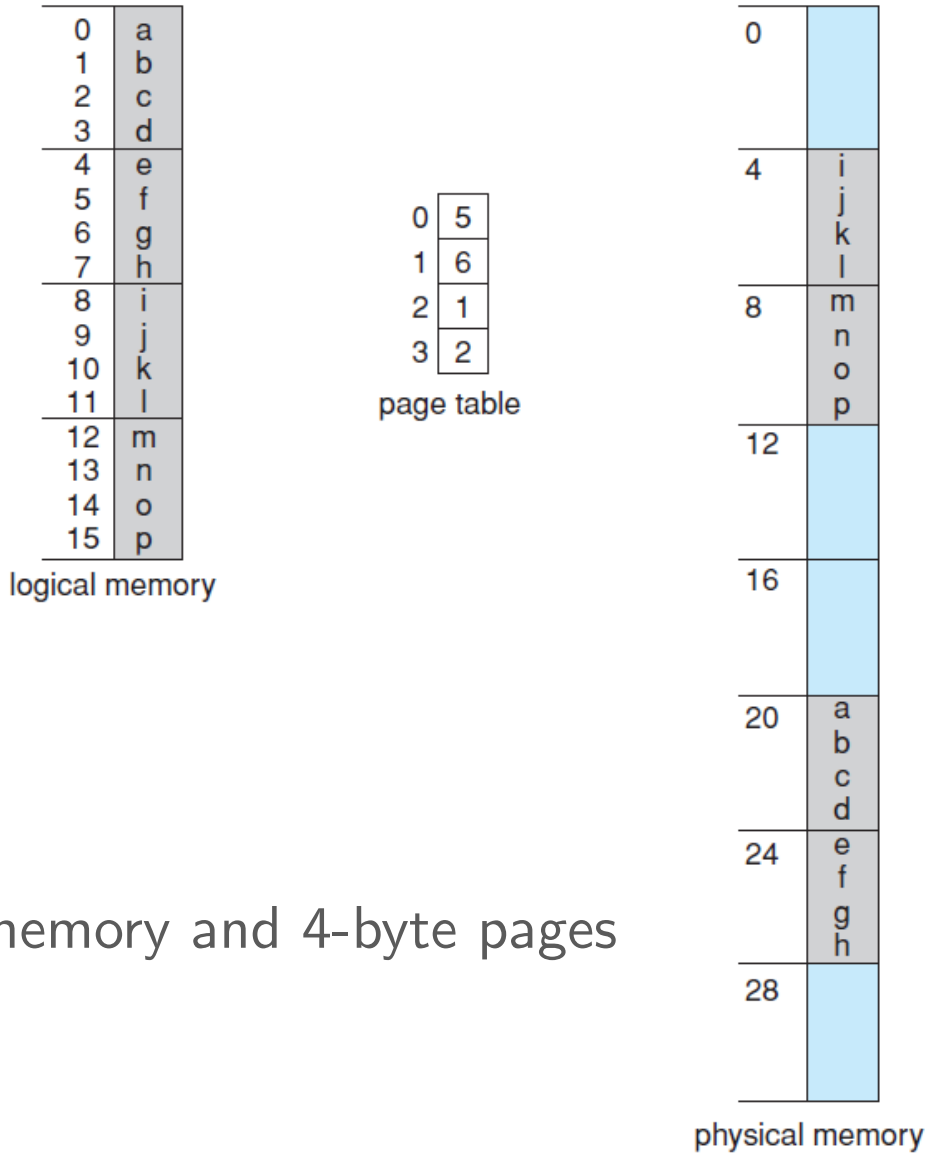
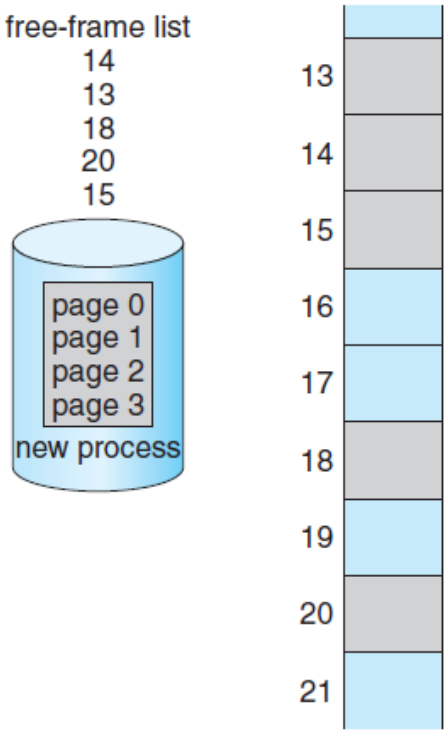
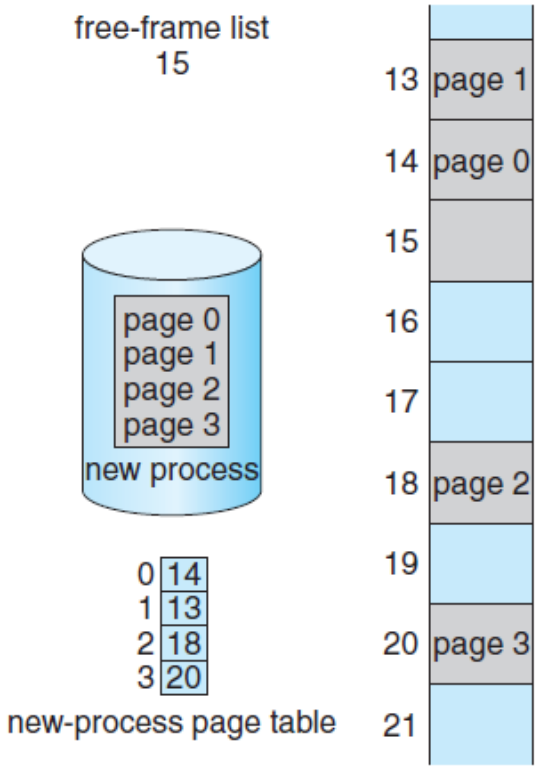


- $n = 2$ and $m = 4$, 32-byte memory and 4-byte pages

Free Frames



before allocation



after allocation

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- Pages typically are between 4 KB and 8 KB in size.

```
getconf PAGESIZE
```

Page Table Implementation

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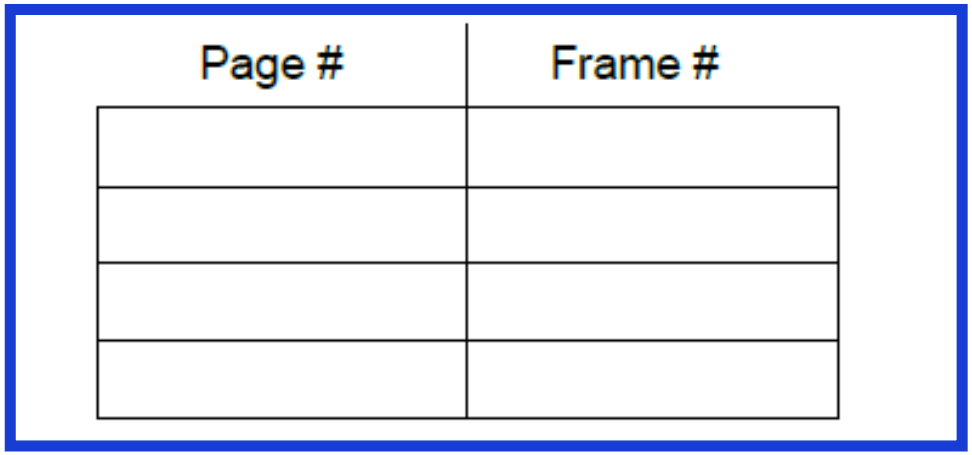
  - One for the page table and one for the data/instruction.

Translation Look-aside Buffers (TLB)

- The two memory access problem can be solved by the use of a special fast-lookup hardware cache called associative memory or translation look-aside buffers (TLBs).

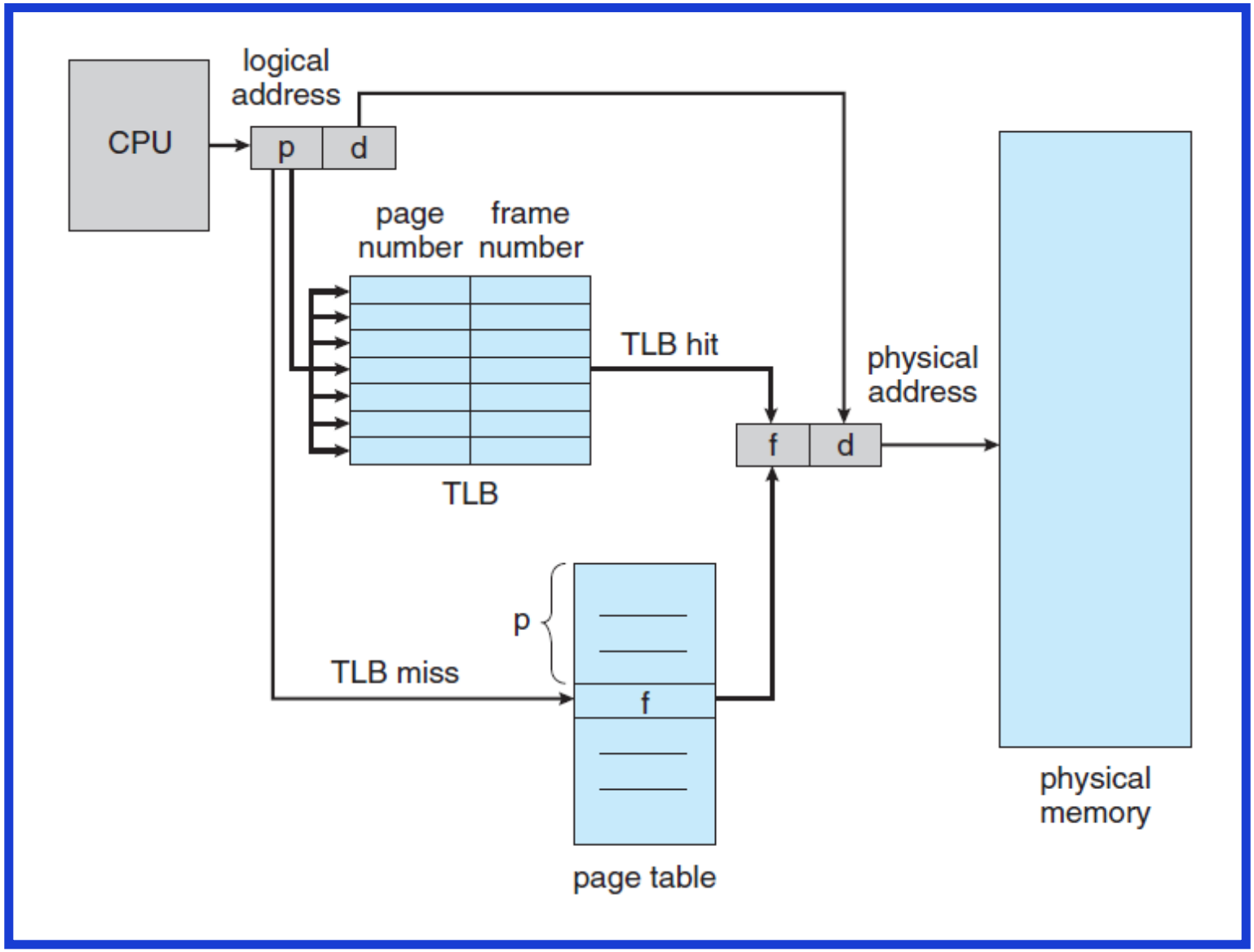
Associative Memory

- Associative memory: parallel search



- Address translation (p, d)
  - If p is in associative register, get *frame#* out
  - Otherwise, get *frame#* from page table in memory

Paging Hardware With TLB



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- On a TLB miss, value is loaded into the TLB for faster access next time.
  - Replacement policies must be considered.

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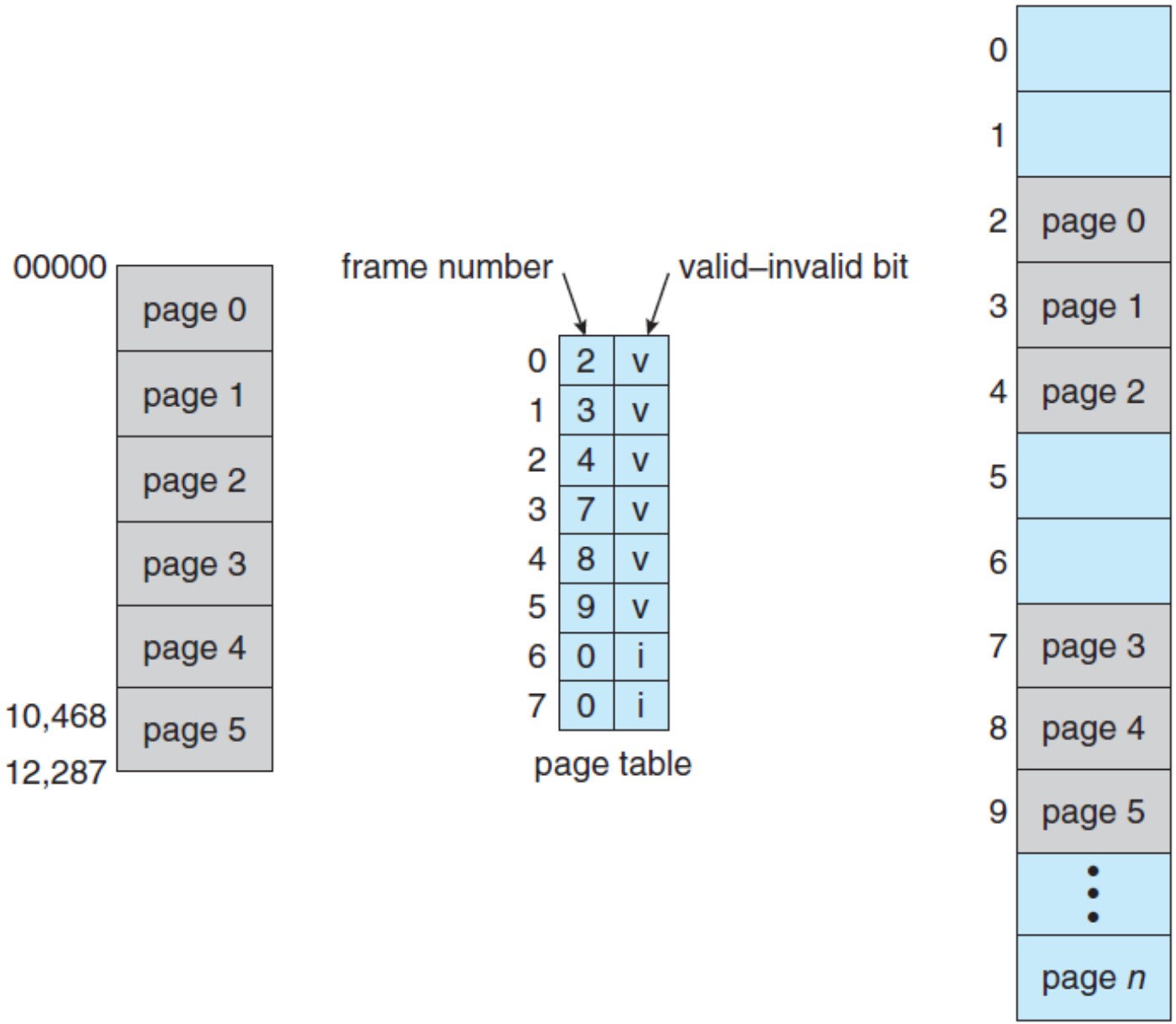
- Any violations result in a trap to the kernel.

Valid/Invalid Bit In A Page Table



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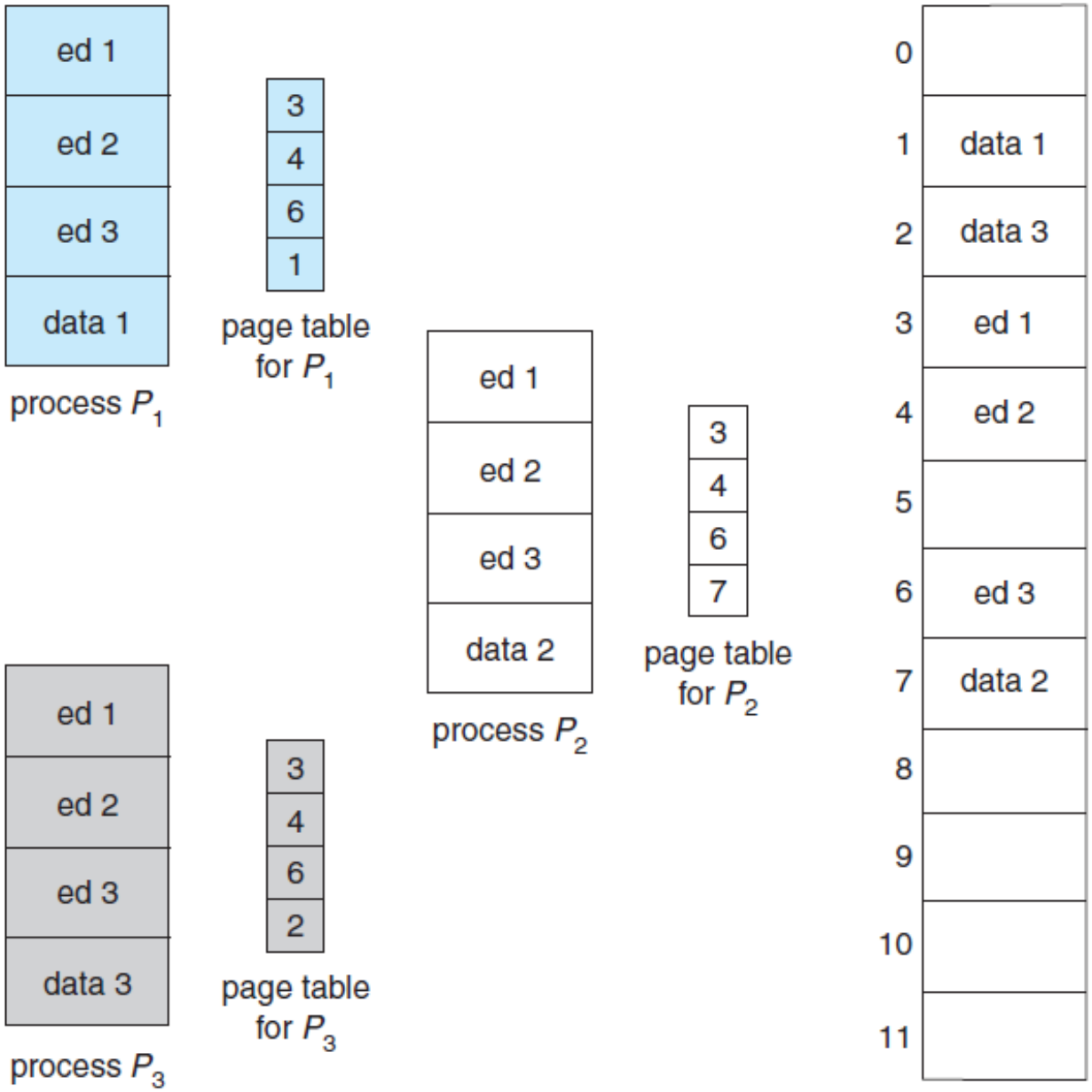
- Private code and data
  - Each process keeps a separate copy of the code and data.
  - The pages for the private code and data can appear anywhere in the logical address space.

Shared Pages Example



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  - Don't want to allocate that contiguously in main memory.

Structure of the Page Table (2/2)

- Hierarchical Paging
- Hashed Page Tables
- Inverted Page Tables

Hierarchical Paging

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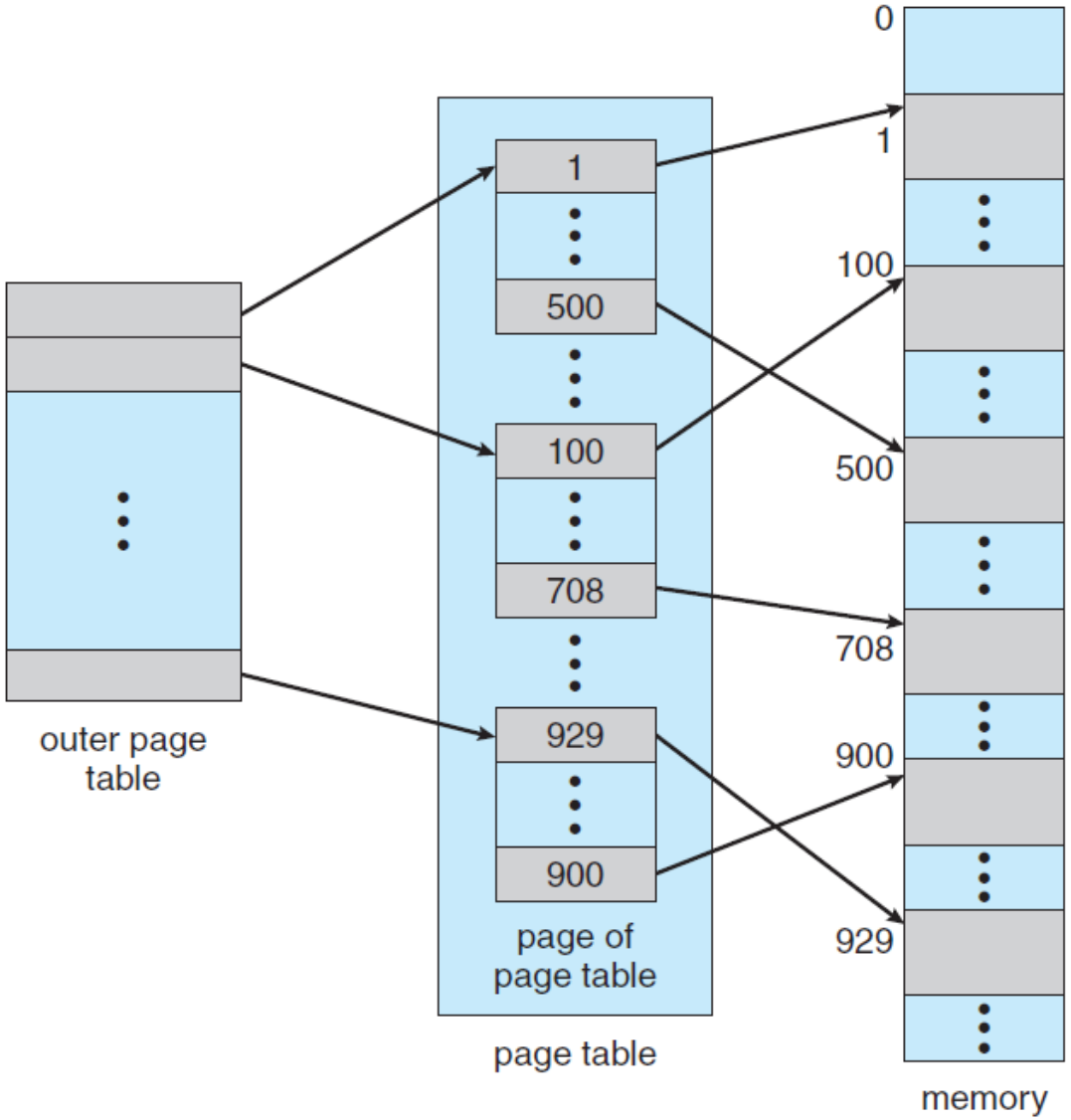
- Break up the logical address space into multiple page tables.
- A simple technique is a two-level page table.
- We then page the page table.

Two-Level Page-Table Scheme



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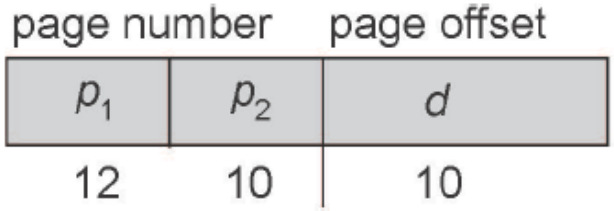

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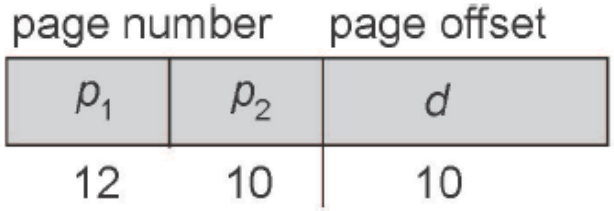

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- Known as forward-mapped page table.

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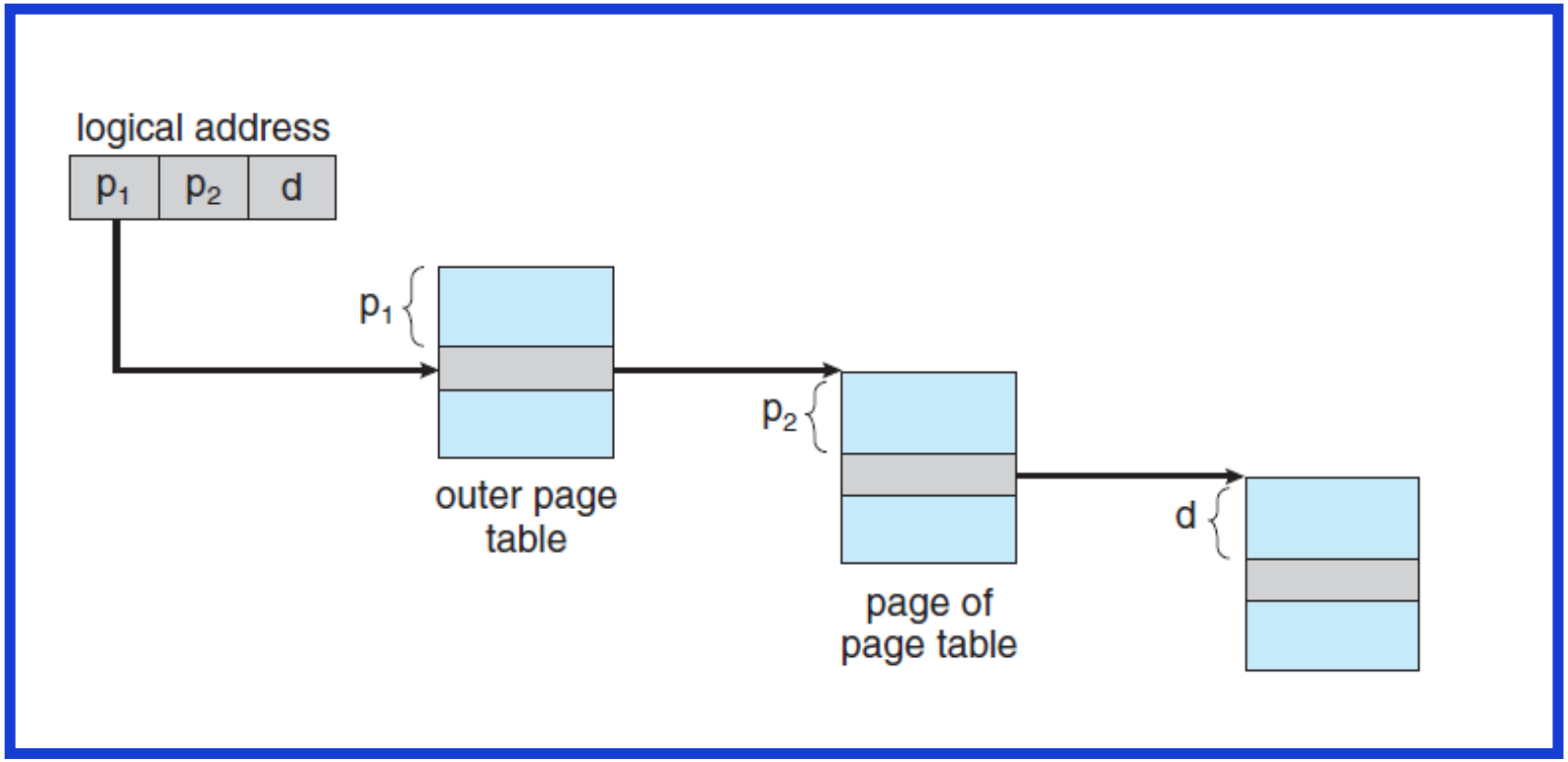

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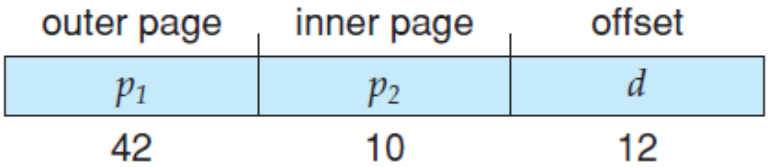

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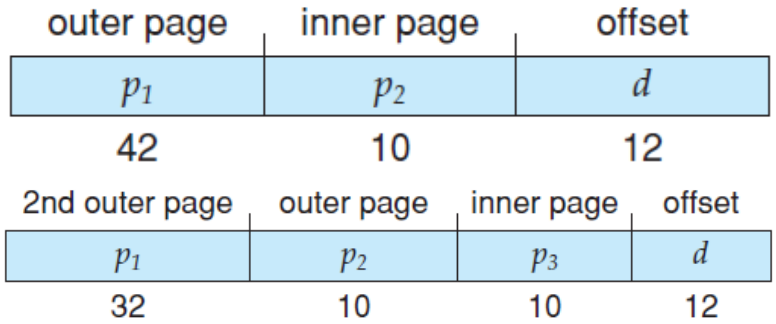
- And possibly 4 memory access to get to one physical memory location.



Hashed Page Tables

Hashed Page Tables (1/2)

- Common in address spaces > 32 bits
- The logical page number is hashed into a page table.
- This page table contains a chain of elements hashing to the same location.

Hashed Page Tables (2/2)

- Each element contains
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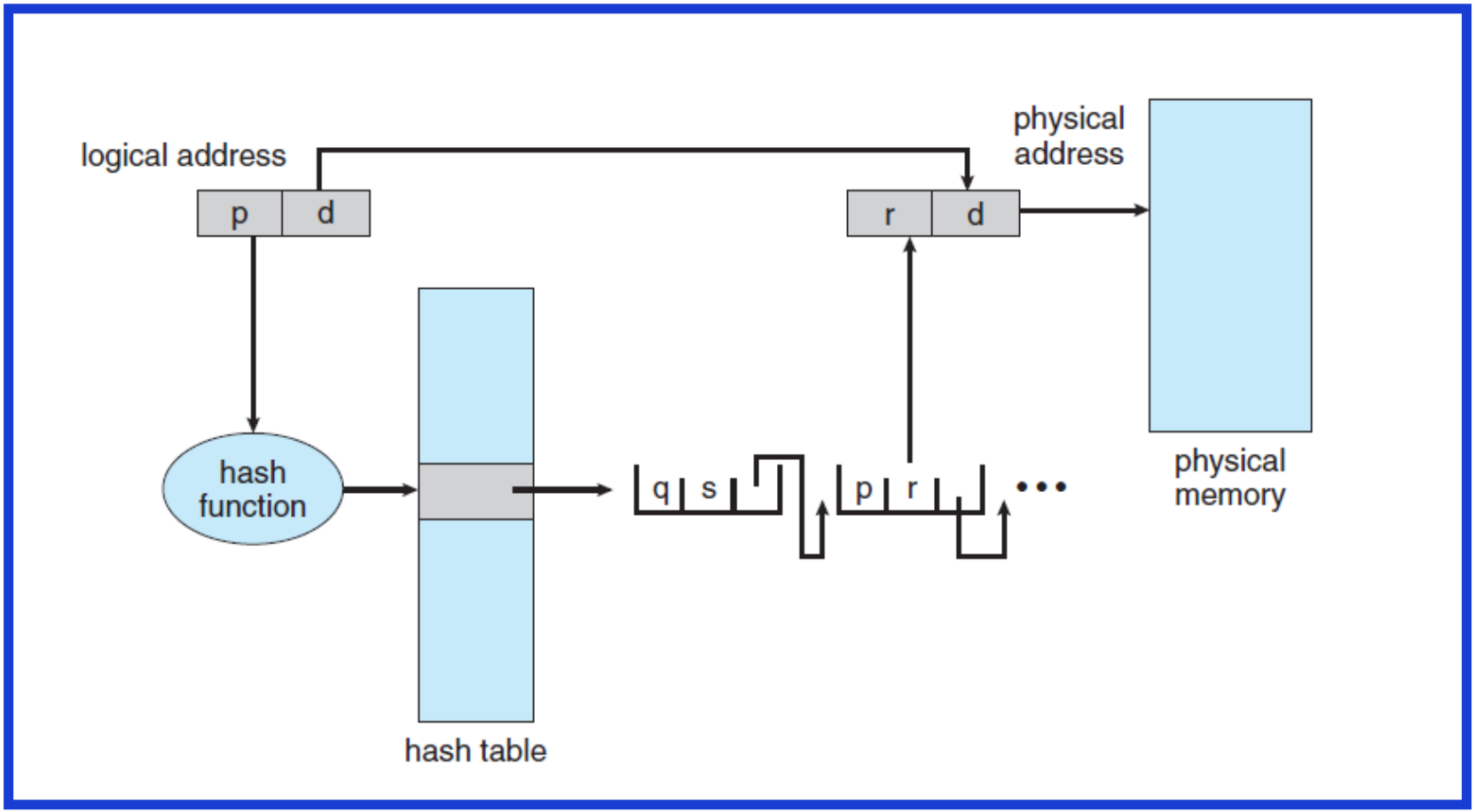
- Logical page numbers are compared in this chain searching for a match.
  - If a match is found, the corresponding physical frame is extracted.

!

Hashed Page Table Architecture



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- Entry consists of the virtual address of the page stored in that real memory location, with information about the process that owns that page.

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- But how to implement shared memory?
  - One mapping of a virtual address to the shared physical address

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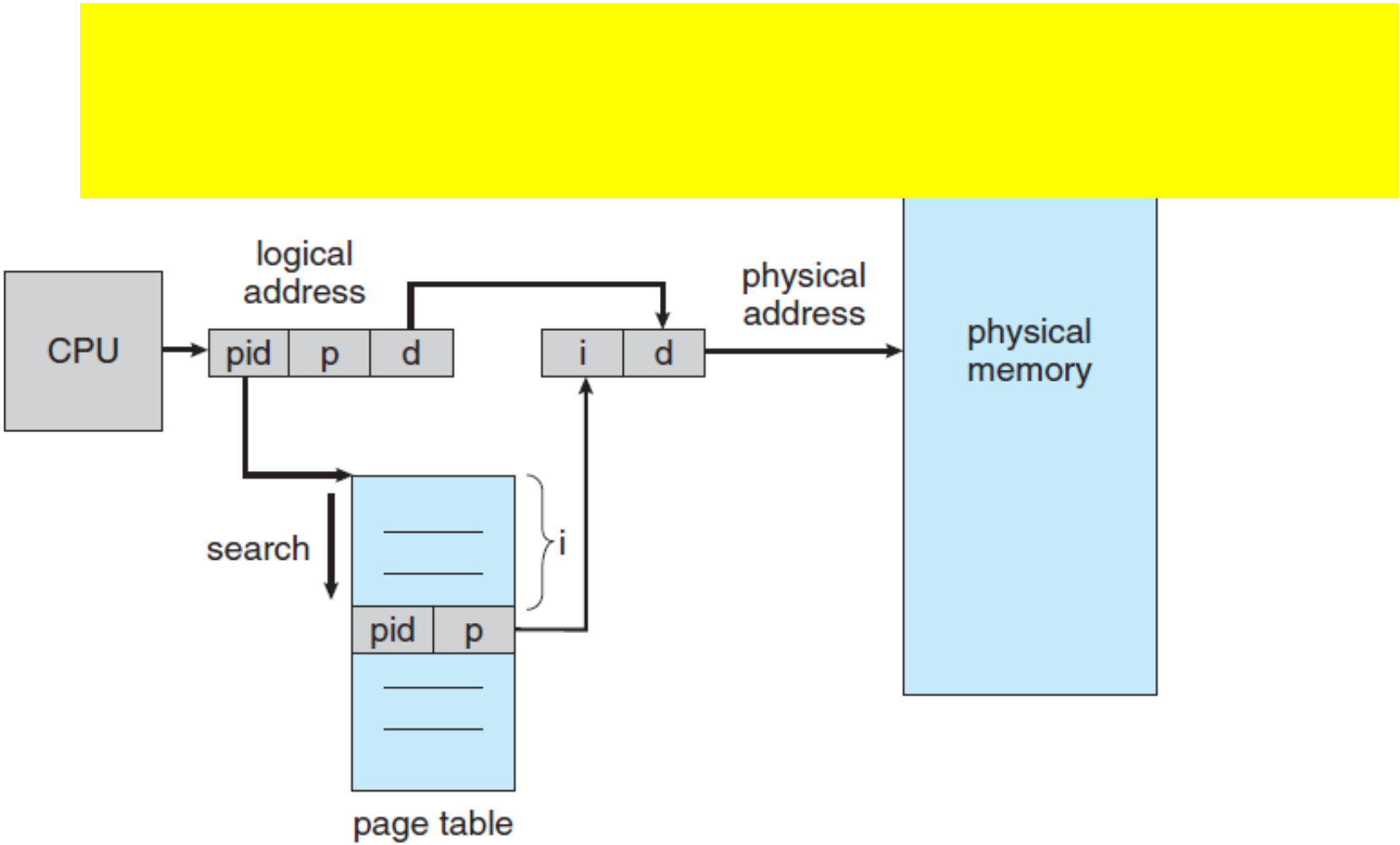

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- Page table structure: hierarchical paging, hashed page tables, inverted page tables

Questions?

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