# CA Assignment 3 Report

**For direct mapped as well as set associative**:-

1 block
---------- x 256 x $2^{10}$ bytes = number of blocks
4 bytes

=> number of blocks = $2^{16}$
Each block contains 4 bytes.
=> *bytes offset bit-width* = 2 bits

**Calculations for direct mapped cache**:-

1 row
---------- x $2^{16}$ block = number of rows
1 block

=> number of rows = $2^{16}$
=> *index bit-width* = 16
=> *tag bit-width* = 32 – (16 + 2) = 14

**Calculations for 4-way set associative cache**:-

1 set
---------- x $2^{16}$ block = number of sets
4 block

=> number of sets = $2^{14}$
=> *index bit-width* = 14
=> *tag bit-width* = 32 – (14 + 2) = 16

**Terminal commands:-**

1. *To compile, enter*:-

>> javac Block.java Set.java DirectMappedCache.java Main.java SetAssociativeCache.java

2. *To run the code, enter*:-

>> java Main

**NOTE:-** For replacement in cache, “LRU” (Least recently used) policy has been used

**Code outputs for direct mapped cache:-**

| | gcc.trace | gzip.trace | mcf.trace | swim.trace | twolf.trace |
|---|---|---|---|---|---|
| Number of accesses | 515683 | 481044 | 727230 | 303193 | 482824 |
| Number of hits | 483504 | 320883 | 7505 | 280738 | 476770 |
| Number of misses | 32179 | 160161 | 719725 | 22455 | 6054 |
| Hit rate | 0.93759 | 0.66705 | 0.01031 | 0.92593 | 0.98746 |
| Miss rate | 0.06240 | 0.33294 | 0.98968 | 0.07406 | 0.01253 |
| Hit to miss ratio | 15.02545 | 2.00350 | 0.01042 | 12.50224 | 78.75289 |

**Code outputs for 4-way set associative cache:-**

| | gcc.trace | gzip.trace | mcf.trace | swim.trace | twolf.trace |
|---|---|---|---|---|---|
| Number of accesses | 515683 | 481044 | 727230 | 303193 | 482824 |
| Number of hits | 483871 | 320883 | 7508 | 280825 | 476844 |
| Number of misses | 31812 | 160161 | 719722 | 22368 | 5980 |
| Hit rate | 0.93831 | 0.66705 | 0.01032 | 0.92622 | 0.98761 |
| Miss rate | 0.06168 | 0.33294 | 0.98967 | 0.07377 | 0.01238 |
| Hit to miss ratio | 15.21032 | 2.00350 | 0.01043 | 12.55476 | 79.73979 |

**Observations:-**

1. Hit rates for all the input files for 4-way set associative, are greater than or equal to the hit rates of direct mapped cache. So are the hit to miss ratio. This observation agrees to what we’d predict considering the “spatial locality” of memory.

2. Logical implementation of 4-way set associative cache is a bit more complex than that of direct mapped cache as can be seen in the code too.