Q.> Write a behavioral Verilog module for a modified form of traffic light controller FSM. It has 2 sensor inputs T_A and T_B and 6 traffic light outputs – 3 per lane (and a clock CLK and reset RST). The FSM behaves similar to the TLC FSM described in the text book with the difference that a YELLOW signal condition for a lane is for 2 cycles. Therefore the total number of states is 6 (S0 – S5). Draw the state-diagram for the FSM. Write a test-bench that covers the usual traffic conditions. Use **parameter** statement for describing the state constants to simplify the code. Write a test-bench that illustrates the correct operation of the FSM. Include gtkwave waveforms in your report.