VOTING MACHINE

Git_hub_Link: https://github.com/vardhan3003/Voting_Machine_on_FPGA

P.HARSHAVARDHAN BABU

Electronics and Communication Engineering, KL University

1.INTRODUCTION

This Verilog module simulates a voting machine, handling vote counting and confirmation for three categories: Bharatiya Janata Party(BJP), Congress (CONG), and None of the Above (NOTA). The module also interfaces with a seven-segment display, and confirming the vote cast for each option with led.

2. Working Principle

The design is composed of three main modules:

- 1. **Digits Module**: Handles the conversion of count values into digit representations.
- 2. **Seven Segment Display Module**: Manages the display of digit values on a seven-segment display.
- 3. **Voting Machine Module**: Integrates the counting logic, vote confirmation, and interfacing with the other two modules.

2.1 Digits Module

The digits module takes the vote counts as inputs and converts them into four-digit representations (ones, tens, hundreds, thousands). This module ensures that the correct count is selected based on the figure select signals (BJP_FIG, CONG_FIG, NOTA_FIG).

2.2 Seven Segment Display Module

The seven_seg module handles the multiplexing of the four-digit values onto a single seven-segment display. It cycles through each digit rapidly to give the appearance of all digits being displayed simultaneously.

2.3 Voting Machine Module

The voting_machine module integrates the entire system, handling the voting logic, counters, and interfacing with the digits and seven_seg modules. It includes debounce logic to ensure stable input reading and increments the corresponding vote count when a vote is cast.

3. Constraints on Board

- **Push Buttons:** Used to cast votes for BJP, CONG, and NOTA. Each button press increments the respective vote count.
- **LEDs**: Used to confirm that a vote has been cast for BJP, CONG, or NOTA.
- **Switches**: Used to select which vote count (BJP, CONG, or NOTA) is displayed on the seven-segment display.
- **Seven-Segment Display**: Digits (digit [3:0]) to select which digit to display. Segments (seg [6:0]) to display the corresponding value.

4. Outputs on Basys3 Board

Drive link:

https://drive.google.com/file/d/1DFImQKZBX74 JyveYWtqo8qSF9eHdibXh/view?usp=drivesdk

5. Conclusion

The voting machine implemented on the Basys3 FPGA board using Xilinx Vivado provides a reliable and efficient means of collecting and displaying votes for three options: BJP, CONG, and NOTA. The design leverages the FPGA's versatility to handle real-time inputs from push buttons for voting, confirm votes using LEDs, and display the vote counts on a seven-segment display.