

Paging multi-level

PDE → PT → PTE → PFN

↓ ↓ ↓ ↴
Page directory entry Page table Page table entry Page frame number

$$\text{Page-size} = 32B$$

$$\text{asize} = 32KB = 1024 \text{ pages}$$

$$\text{Phy mem} = 128 \text{ pages} = 128 \times 32B$$

$$VA = 10 \text{ bits} + 5 \text{ bits}$$

$$\begin{array}{c} \text{VPN} \\ 2^{10} \end{array} \quad \begin{array}{c} \text{offset} \\ 2^5 \end{array}$$

$$PA = 7 \text{ bits} + 5 \text{ bits}$$

$$\begin{array}{c} \text{PFN} \\ 2^7 \end{array} \quad \begin{array}{c} \text{offset} \\ 2^5 \end{array}$$

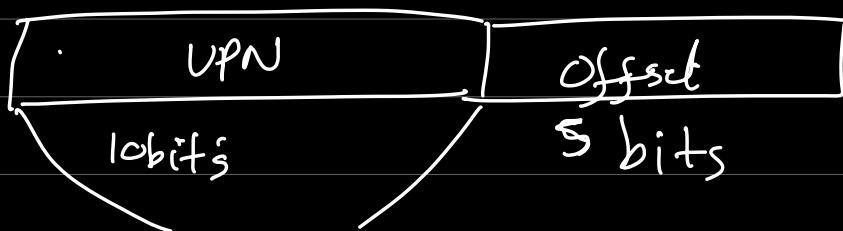
5 bits = 2^5 (page-size) \Rightarrow index into a page directory

PDBR \Rightarrow 108 (decimal) \Rightarrow page directory is

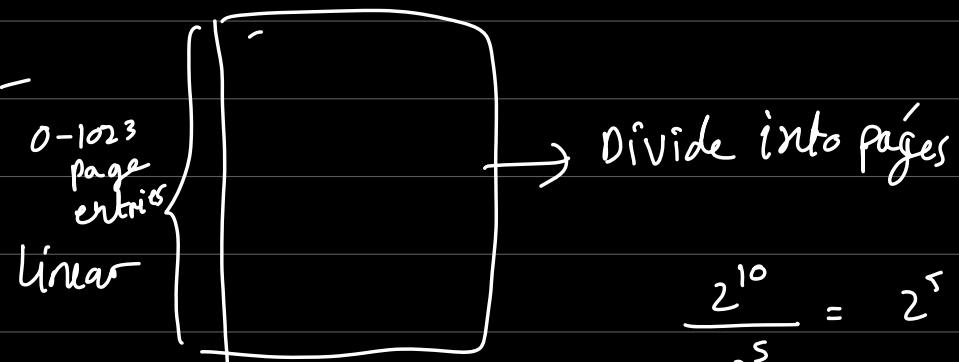
page directory
base register

in this page

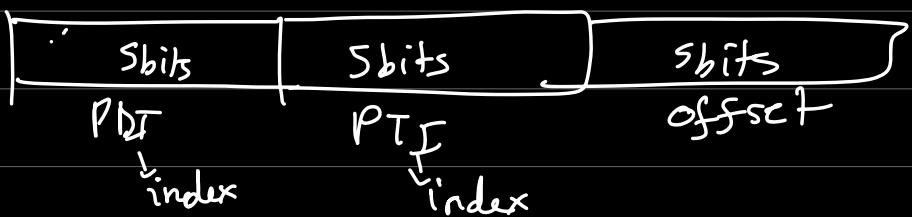
VA 611C =>



PD \Rightarrow Will contain one entry per page
of the page table



PD
↓
5 bits



$611c \Rightarrow \text{Ob} \underbrace{1000}_{\downarrow} \underbrace{000}_{\text{valid}} \underbrace{(1100)}_{\text{size}} \rightarrow 0x1c (28)$
 $\text{PDI} = 2^4 \Rightarrow$

$$\text{PTI} = 8$$

(2)

$\text{PDBR} = 83fee0da7fd47febbe9ed5ade4ac90d6$

$2^{9\text{th}} \text{ byte} \Rightarrow (\$8 \text{ in } 4^{\text{th}} \text{ bit}) = 0xa$

$\text{Ob} \underbrace{1000}_{\text{valid}}$.
 $\text{PFN} \Rightarrow 33 (0x21)$

$(0x21 << 5) + (0x8 * 3)$
 $= 0x460$

$\text{Ob} \underbrace{1000}_{\text{valid}}$.
 1100000 $\cancel{\text{bits}}$ size
should be bytes

$1064 \Rightarrow 33^{\text{rd}}$ page 8^{th} byte (starting index
 $= 0xb5$)

$\text{Ob} \underbrace{1010101}_{\downarrow \text{valid}} \rightarrow \text{PFN} = 0x35 (53)$

$(PTE = N \ll S) + \text{offset}$

= $0x6BC$ → Physical address

↓
 $(1724) \Rightarrow 53^{\text{rd}} \text{page} + 28^{\text{th}} \text{byte}$

= $0x08$ → value

VA 3da8 ⇒ 5 bits + 5 bits + 5 bits

PDI PTI offset
 \underbrace{\hspace{1cm}}_{VPN}

3da8 ⇒ 0b01110110101000
↓ ↓ ↓
PDI PTL offset

PDT ⇒ 15 ($0xf$)

↳ byte on PDBR page

↓ ↗
(216) $0xd6 \Rightarrow 0b$ 1010110
 ↑ ↗
 entry valid
(PDT) ↳ PFN
 0x56 (86)

. 8 bits

$$PTE_{addr} = \left(PDE.PFN \ll 5 \right) + \left(PTI * \frac{1}{\text{page size}(2^r)} \right)$$

$$PTE_{addr} = \frac{0xacd}{\Downarrow}$$

2765 byte in dump

$$\text{Find page} = \frac{2765}{32 \rightarrow \text{pagesize}} = 86 \text{ page}$$

+ 13th byte

\Downarrow
0x7f (127)

0b0111111

invalid

Fault (page table entry not valid)

VA 17f5 \Rightarrow 0b010111110101
 \Downarrow \Downarrow \Downarrow
 PDI PTI offset

$0x5(5)$ $0x1f(31)$ $0x15(21)$
 \Downarrow

5th byte on PDBR page
PDE 0xd4

↓
0b100100
valid

↓
PFN
0x54 (84)

(PDE.PFN << 5) + (0xf x 1)
↓

PTE_{addr} = 0xa9f (2719)

2719 = 84th page + 31st byte
32
↓

0xcc
↓

PTE = 0b1001110,
— valid PFN

0xfe (28)

(PTE.PFN << 5) + offset
(0xfe << 5) + 0x15

Physical addr \Rightarrow 0x9D5 (2517)

$\frac{2517}{32} = 78^{\text{th}}$ page and 2st byte

0x/c \Rightarrow value

VA 7f6c \Rightarrow ob1111110101100
↓ ↓ ↓
PDI PTI offset

0x1f(31) 0x1b(27)

31st byte on PDBR \Rightarrow 0x ff
↓

ob111111
↓ ↓
valid PFN

$$\begin{aligned}\text{PTEaddr} &= (\text{PTE.PFN} \ll 5) + (\text{PTI} * \text{size of PTE}) \\ &= 0x \text{ff}b (4091) \\ \frac{4091}{32} &= 127^{\text{th}} \text{ page} + 27^{\text{th}} \text{ byte}\end{aligned}$$

0x7f
↓
invalid
ob011111

fault

VA \times bad \Rightarrow 0b $\underline{0010}\underline{11010110}$
PDI PTI offset
 $0x2(2)$ ~~$0x10(29)$~~ $0xD13$

2nd byte on PDBR \Rightarrow

$0x7f$, invalid
0b $\underline{011111}$

fault PDE

VA $6d60 \Rightarrow$ 0b $\underline{1011010111}\underline{000000}$
PDI PTI offset
 $0x1b(27)$ $0xb0(1)$ $0x0$

27th byte of PDBR \Rightarrow $0x7f$

$0x7f \Rightarrow$ 0b $\underline{01111111}$, invalid

fault PDE

VA $2a5b \Rightarrow$ 0b $\underline{01010}\underline{001011011}$,

\downarrow PDI \downarrow PTI \downarrow offset
0xa(f0) 0x12(18) 0x1b(27)

10th byte on PDBR \Rightarrow 0x7f

0b011111
 \downarrow invalid

fault PDE

VA 4c5e \Rightarrow 0b10011000101110,

\downarrow PDI \downarrow PTI \downarrow offset
 \downarrow \downarrow \downarrow

0x13(19) 0x2(2) 0x1e(30)

19th byte on PDBR \Rightarrow 0x7f

\downarrow invalid
0b0111111

fault PDE

VA 2592 \Rightarrow

9th byte on PDBR \Rightarrow 0x7f

Used wrong
page 1 ..

invalid
PDBR value
otherwise would
have valid
redone, in the
end.

fault PDE

VA 3e99 \Rightarrow Ob01111010011001
 \downarrow \downarrow \downarrow
PDI PTE offset
 \Downarrow \downarrow \downarrow
0xf(15) 0x14(20) 0x19(25)

15th byte on PDBR \Rightarrow 0xd6
 \Downarrow

Ob1010110,
 \downarrow \rightarrow
valid PFN
 \Downarrow

0x56 (86)

$$\begin{aligned} \text{PTE addr} &= \text{PFN} \ll 5 + 0x14 \\ &= 0x104 (272) \end{aligned}$$

272
32 = 86th page + 20th byte

PTE . \Rightarrow 0xca

\Downarrow \nearrow valid
Ob11001010
1 0 1

\downarrow PFN

$0x4a$ (74)

$$\begin{aligned}\text{Physical address} &= (0x4a \ll 5) + 0x19 \\ &= 0x959 \quad (2393)\end{aligned}$$

$\frac{2393}{32} = 74^{\text{th}} \text{ page} + 25^{\text{th}} \text{ byte}$

$= 0x1e$

\downarrow

value

VA $0x2592 = 0b1001010010010$

\downarrow PDI \downarrow PTI \downarrow offset
 ↓ ↓ ↓

$0x9(9) \quad 0x1(2) \quad 0x12(13)$

9^{th} byte in PDBR $\Rightarrow 0x9e$

\downarrow

$0b1001110$
 \downarrow valid \downarrow PFN
 ↓ ↓
 $0x1e(30)$

$\text{PTEaddr} = (0x1e \ll 5) + 0xc$

$$= 0x3d \text{cc } (972)$$

$$\frac{972}{32} = 30^{\text{th}} \text{ page} + 12^{\text{th}} \text{ byte}$$

$$\text{PTE} = 0xb \downarrow$$

Ob10\underline{111101}

valid PFN

$$0x3d \text{ (61)}$$

$$\begin{aligned}\text{Physical addr} &= (0x3d \ll 5) + 0x12 \rightarrow \text{offset} \\ &= 0x7b2 \text{ (1970)}\end{aligned}$$

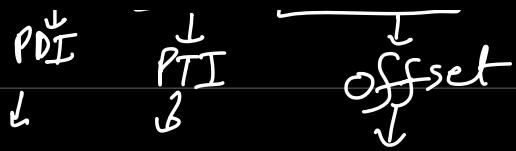
$$\frac{1970}{32} = 61^{\text{st}} \text{ page} + 18^{\text{th}} \text{ byte}$$

$$\text{value} = 0x1b$$

with seed = 1

$$\text{PDBR} = 17^{\text{th}} \text{ page}$$

$$\text{VA } 6c74 \Rightarrow \text{Ob } \underline{1011} \underline{0001} \underline{10100},$$



$0x1b(27)$ $0x3(3)$ $0x14(20)$

27th byte in PDBR \Rightarrow $0xa0_{(160)}$ PDE

$0b\ 10100000$

\downarrow valid \downarrow PFN

$0x20(32)$

$$\begin{aligned} \text{PTE addr} &= 0x20 \ll 5 + 0x3 \\ &= 0x403 \end{aligned}$$

$$\frac{1027}{32} = 32^{\text{nd}} \text{ page} + 3^{\text{rd}} \text{ byte}$$

$= 0xe1_{(225)}$ PTE

$0b\ 1100001$

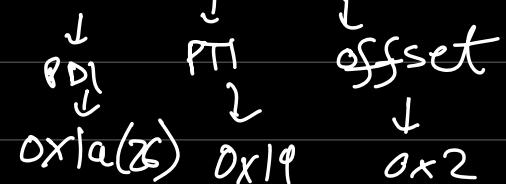
\downarrow valid \downarrow PFN

$0x61(97)$

$$\text{Physical addr} = 0x61 \ll 5 + 0x14 \\ = 0xc34 (3124)$$

$\frac{3124}{32} = 97^{\text{th}} \text{ page} + 20^{\text{th}} \text{ byte}$

$$\text{value} = 0x06$$

VA $0x6b22 \Rightarrow 0b110101100100010,$

 ↓
 PDI
 $0x1a(2)$
 ↓
 PTI
 $0x19$
 ↓
 offset
 $0x2$

26^{th} byte in PDBR $\Rightarrow 0xd2 \quad \text{PDE}$
 ↓

$0b1\underbrace{010010},$
 ↓
 valid
 PFN

$0x52(82)$

$$\text{PTE addr} = 0x52 \ll 5 + 0x19 \\ = 0xa59 (2649)$$

$\frac{2649}{32} = 82^{\text{nd}} \text{ page} + 25^{\text{th}} \text{ byte}$

$$= 0xc7 \quad \text{PTE}$$

$0b1000111$
 valid ↓
 PFN
 $0x47\ (71)$

Physical addr = $(0x47 \ll 5) + 0x2$ \rightarrow offset
 $= 0x8e2\ (2274)$

$\frac{2274}{32} = 71^{\text{st}} \text{ page} + 2^{\text{nd}} \text{ byte}$
 $= 0x1a \text{ value}$

With seed = 2

PDBR is 122nd page

VA 7570 \Rightarrow $0b1101010110000$,
 ↓ ↓ ↓
 PDI PTE Offset
 $0x1d(29)$ $0xb(11)$ $0x1a(16)$
 2nd byte on PDBR \Rightarrow $0xb3$ PDE
 ↴

$0b10110011$
valid PFN

$0x33(5)$

$$\begin{aligned} \text{PTE addr} &= (0x33 \ll 5) + 0xb \rightarrow \text{PTI} \\ &= 0x66b (1643) \end{aligned}$$

$\underline{1643} = 5^{\text{st}} \text{ page} + 11^{\text{th}} \text{ byte}$

32

$$= 0x7f$$

\Downarrow invalid
 $0b01111111$

fault PTE invalid

$$\begin{aligned} \text{VA } 0x7268 \Rightarrow 0b111001001101000, \\ \downarrow \quad \downarrow \quad \downarrow \\ \text{PDI} \quad \text{PTI} \quad \text{offset} \\ 0xc(28) \quad 0x13 \quad 0x8 \end{aligned}$$

28^{th} byte on PDIR $\Rightarrow 0xde$

$0b11011110,$

valid PFN

0x5e (94)

$$\begin{aligned} \text{PTE addr} &= 0x5e \ll 5 + 0x13 \xrightarrow{\text{PTI}} \\ &= 0xb03 (3027) \end{aligned}$$

$$\frac{3027}{32} = 9^{\text{th}} \text{ page} + 1^{\text{st}} \text{ byte}$$

$$= 0xe5 \text{ PTE}$$

↓

0b11100101
valid PFN

0x65 (101)

$$\begin{aligned} \text{Physical addr} &= (0x65 \ll 5) + 0x8 \xrightarrow{\text{offset}} \\ &= 0xc08 (3240) \end{aligned}$$

$$\frac{3240}{32} = 10^{\text{th}} \text{ page} + 8^{\text{th}} \text{ byte}$$

= 0x16 value

- 3 memory references to perform lookup
 - Page directory
 - Page table
 - Access data at physical address

① For two-level, three-level...
 will continue to need just
 one register like linear page table.

- To store the base address of
 page directory or page table
 in case of linear paging.
 Only no. of memory accesses increases
 with the level.

③ With multi-level page table, the
 chances of cache miss increases
 due to more memory accesses instead
 of just one in case of linear paging.
 But the size of cache is reduced
 in case of multi-level, specifically can
 cache PDEs & PTEs frequently used.
 Compared to large page table with

all PTEs of a process.