Ioannis Vardas

Vienna University of Technology - Faculty of Informatics

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Education

Vienna University of Technology
Austria

Doctoral programme in Engineering Sciences and Computer Science — *October 2021 - Present*

- **PhD Thesis**: TBD, Advisor: Prof. Jesper Larsson Träff
- **Coursework**: High Performance Computing; Scientific Programming with Python; Software Testing: From Basic Concepts to Advanced Topics; Fundamental research methods for doctoral students;

University of Crete
Greece

M.Sc. in Computer Science and Engineering, GPA: 8.79/10 — *November 2019*

- **MSc Thesis**: Process Placement Optimizations and Heterogeneity Extensions to the Slurm Resource Manager[4]. Advisor: Prof. Manolis G.H. Katevenis, Co-Advisor: Dr. Manolis Marazakis
- **Graduate Coursework**: Embedded Systems Lab; Principles of Distributed Computing; Internet Systems and Technologies; Computer Architecture; Parallel Computer Architecture; Managed Runtime Systems; Digital Circuits Design Lab Using EDA Tools;

University of Crete
Greece

B.Sc. in Computer Science, GPA: 7.03/10 — *March 2016*

- **Graduate Thesis**: Memory Testing through an FPGA with an embedded Processor

Stanford Online
Coursera

Machine Learning course certificate — *April 2022*

- Machine Learning Certificate

Research

Vienna University of Technology

- Performance analysis and optimization of HPC applications
- Mapping of parallel (MPI) applications to HPC system topologies and the role of MPI communicators
- mpisee: MPI Profiling for Communication and Communicator Structure, presented at the HIPS Workshop of IPDPS 2022
- In-depth analysis of the overhead of MPI profiling and tracing tools [1]

ICS-FORTH

- Improving the resilience of parallel applications via fault-aware mappings [3], [2].
- Process Placement Optimizations and Heterogeneity Extensions to Slurm RJMS [4]
- Simulating the behavior of Accurate congestion control for RDMA Transfers [5]

Skills

Development and Design Skills	Parallel Programming, Machine Learning, Linux Device Drivers/Modules, Hardware design
Programming Languages	C, C++, Python, Bash, Octave, System-Verilog, ARM and MIPS Assembly, Java
Frameworks and Libraries	MPI, OpenMP, CUDA, NumPy, Scikit-learn, Pandas, Matplotlib
Operating Systems	Linux(Gentoo, RHEL, Debian, Arch), FreeBSD, Microsoft Windows
Virtualization Platforms	QEMU, Virtual Box, Microsoft Hyper-V
Languages besides native(Greek)	English C2 level. University of Michigan, Certificate of Proficiency in English

Employment history

Vienna University of Technology - Faculty of Informatics
Austria

Pre-Doctoral Researcher — *June 2021 - Present*

- Pre-Doctoral Researcher, Parallel Computing Group

ICS-FORTH *Greece*

Research Engineer *Dec. 2019 - May 2021*

- Research staff, Computer Architecture and VLSI Systems (CARV) Laboratory

ICS-FORTH *Greece*

Graduate Research Assistant *Sept 2017 - Nov 2019*

- Master's degree Scholarship, Computer Architecture and VLSI Systems (CARV) Laboratory

Hellenic Army *Greece*

Served in the Hellenic Armed Forces *Dec. 2016 - Aug 2017*

- Served in the Hellenic Army, Research and Informatics Corps

ICS-FORTH *Greece*

Research Scholarship *Aug. 2016 - Nov. 2016*

- Research Scholarship, Computer Architecture and VLSI Systems (CARV) Laboratory

Teaching Experience

Teaching Assistant *CSD, University of Crete, Greece*

Computer Organization (cs-225) *Spring 2018, 2019*

- Developed YAC Simulator, a cache simulator written in C/C++ for a simple cache scheme

Digital Design (cs-120) *Fall 2018, 2019*

Packet Switch Architecture (cs-534) *Spring 2016*

Attended Summer School

HiPEAC Summer School - ACACES *Fiuggi, Italy*

Coursework *July 2018*

- Memory Systems and Memory-Centric Computing Systems: Challenges and Opportunities by Onur Mutlu
- Distributed memory programming and algorithms by Johannes Langguth
- GPU Architectures: From Basic to Advanced Concepts by Adwait Jog
- Architectural Support for Virtual Memory by Abhishek Bhattacharjee

Presented Poster

- Extending Slurm to support Running Workloads in Virtual Machines or VINO-Slurm: Virtual NOdes in Slurm

Side Project

Design of a RISC-V core in System Verilog

- Implementation of RV32IC standard with support for stream instructions
- Developed using Synopsys EDA tools for the purposes of Digital Circuits Design Lab Using EDA Tools

References

- Prof. Jesper L. Traff, traff@par.tuwien.ac.at
- Ass. Prof. Sascha Hunold, hunold@par.tuwien.ac.at
- Prof. Manolis G.H. Katevenis, kateveni@ics.forth.gr
- Dr. Manolis Marazakis, maraz@ics.forth.gr

Publications

[1] Sascha Hunold et al. “An Overhead Analysis of MPI Profiling and Tracing Tools”. In: New York, NY, USA: Association for Computing Machinery, 2022.

[2] Ioannis Vardas, Manolis Ploumidis, and Manolis Marazakis. “Exploring the Impact of Node Failures on the Resource Allocation for Parallel Jobs”. In: *Euro-Par 2021: Parallel Processing Workshops*. Ed. by Ricardo Chaves et al. Springer International Publishing, 2022, pp. 298–309.

[3] I. Vardas, M. Ploumidis, and M. Marazakis. “Towards Communication Profile, Topology and Node Failure Aware Process Placement”. In: *2020 IEEE 32nd International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*. 2020, pp. 241–248.

[4] Ioannis Vardas. “Process Placement Optimizations and Heterogeneity Extensions to the Slurm Resource Manager”. 2019. URL: https://tinyurl.com/mwujn46s.

[5] Dimitris Giannopoulos et al. “Accurate Congestion Control for RDMA Transfers”. In: *Proceedings of the Twelfth IEEE/ACM International Symposium on Networks-on-Chip*. NOCS ’18. Torino, Italy: IEEE Press, 2018. ISBN: 9781538648933.