Ioannis Vardas

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Education

Technical University of Vienna — *Austria*

PhD in Engineering Sciences and Computer Sciences — *October 2021*

- **PhD Thesis**: TBD, Advisor: Prof. Jesper Larsson Träff
- **Coursework**: High Performance Computing; Scientific Programming with Python;

University of Crete — *Greece*

M.Sc. in Computer Science and Engineering, GPA: 8.79/10 — *November 2019*

- **MSc Thesis**: Process Placement Optimizations and Heterogeneity Extensions to the Slurm Resource Manager[2]. Advisor: Prof. Manolis G.H. Katevenis, Co-Advisor: Dr. Manolis Marazakis
- **Graduate Coursework**: Embedded Systems Lab; Principles of Distributed Computing; Internet Systems and Technologies; Computer Architecture; Parallel Computer Architecture; Managed Runtime Systems; Digital Circuits Design Lab Using EDA Tools;

University of Crete — *Greece*

B.Sc. in Computer Science, GPA: 7.03/10 — *March 2016*

- **Graduate Thesis**: Memory Testing through an FPGA with an embedded Processor

Research

ICS-FORTH — *Greece*

Exploring the impact of node failures on the resource allocation for parallel jobs — *September 2021*

- This work enables the evaluation of different resource allocation methods under different failure conditions in a controlled and configurable manner
- This work includes a simulation environment based on a synthetic trace generator for node failures
- It is able to evaluate resource allocation methods for a Torus topology by simulating parallel job runs
- The following were implemented:
  - A generator for node failure traces which assumes a Weibull distribution of failures for each Node
  - Three resource allocation methods for Torus topologies
  - Job durations derived from an exponential distribution
  - Developed in C using GSL (Gnu Scientific Library) and Python
- This work was presented in the 14th Workshop on Resiliency in High Performance Computing held in conjunction with the Euro-Par 2021

ICS-FORTH — *Greece*

Towards Communication Profile, Topology and Node Failure Aware Process Placement — *October 2020*

- The main goal is to reduce the average job completion time by avoiding errors due to node failures, while also reducing the cost of communication of the parallel processes by optimizing their mapping to the parallel system.
- In brief, I implemented the following:
  - Profiler for MPI applications that captures bytes and messages exchanged between the MPI processes via MPI point to point and collective calls
  - Fault Aware Node Selection heuristic for 3D Torus written in C language
  - Interface with Scotch Graph mapping library written in C language
  - Evaluation platform for SimGrid Simulator written in Python and C/C++
- For the evaluation I simulated several MPI applications using SimGrid. including NAS parallel benchmarks, LAMMPS and HPL
- Part of this research was published in [1]

Process Placement Optimizations and Heterogeneity Extensions to Slurm RJMS

Sept. 2017 - Nov. 2019

- This is the topic of my MSc thesis [2] which introduces three extensions to Slurm Resource and Job Managing System:
  1. A new plugin that enables Slurm to support FPGA-based accelerators as a resource
  2. Enable Slurm to support running workloads in Virtual Machines using QEMU
  3. This extension introduces a number of plugins to Slurm that enable it to map a parallel job to the topology while also avoiding potential faulty nodes

  For the implementation of the above extensions I developed several plugins for Slurm as well as extending its core functionality for the second extension which required an in-depth knowledge about Slurm internals. The first extension of Slurm was integrated in the ExaNeSt prototype. This work was supported by the European Union's Horizon 2020 Research and Innovation Programme, ExaNeSt, under grant agreement No. 671553.

Accurate congestion control for RDMA Transfers

Aug. 2016 - Nov. 2016

- This research introduces a congestion control protocol for dealing with traffic bursts. It attempts fair-share allocation of bandwidth between flows without keeping per-flow state in the network. I contributed to this project by extending the existing simulation environment using Omnet++ (discrete event simulation environment) and running simulations and tests. This project was published in [3].

Employment history

Technical University of Vienna - Faculty of Informatics — *Austria*

Pre-Doctoral Researcher — *June 2021 - Present*

- Pre-Doctoral Researcher, Parallel Computing Group

ICS-FORTH — *Greece*

Research staff — *Dec. 2019 - May 2021*

- Research staff, Computer Architecture and VLSI Systems (CARV) Laboratory

ICS-FORTH — *Greece*

Graduate Research Assistant — *Sept 2017 - Nov 2019*

- Master's degree Scolarship, Computer Architecture and VLSI Systems (CARV) Laboratory

Hellenic Army — *Greece*

Served in the Hellenic Armed Forces — *Dec. 2016 - Aug 2017*

- Served in the Hellenic Army, Research and Informatics Corps

ICS-FORTH — *Greece*

Research Scholarship — *Aug. 2016 - Nov. 2016*

- Research Scholarship, Computer Architecture and VLSI Systems (CARV) Laboratory

Teaching Experience

Teaching Assistant — *CSD-University of Crete, Greece*

Computer Organization (CS-225) — *Spring 2018, 2019*

- Oral Examination of students' exercises
- Marking and assessment of exercises
- Participating in marking and assessment of the final and midterm examinations
- Developed the YAC Simulator, a cache simulator written in C/C++ for a simple cache scheme. As I am aware, it is still used to this day for this course

Digital Design (CS-120) — *Fall 2018, 2019*

- Oral examinations of students during the CS-120 Laboratory exercises
- Answering questions both in mailing list and in person
- Participating in marking and assessment of the final and midterm examinations

Digital Design (cs-534)

Spring 2016

- Answering questions both in mailing list and in person
- Marking and assessment of students' exercises

Attended Summer School

HiPEAC Summer School - ACACES

Fiuggi, Italy

July 2018

Coursework

- Memory Systems and Memory-Centric Computing Systems: Challenges and Opportunities by Onur Mutlu
- Distributed memory programming and algorithms by Johannes Langguth
- GPU Architectures: From Basic to Advanced Concepts by Adwait Jog
- Architectural Support for Virtual Memory by Abhishek Bhattacharjee

Presented Poster

- Extending Slurm to support Running Workloads in Virtual Machines or VINO-Slurm: Virtual NOdes in Slurm

Side Project

Design of a RISC-V core in System Verilog

- Implementation of RV32IC standard with support for stream instructions
- Development done using Synopsys EDA tools for the purposes of Digital Circuits Design Lab Using EDA Tools

Skills

Languages	C, C++, Python, Bash, System-Verilog, ARM and MIPS Assembly, Java
Operating Systems	Linux(Gentoo, CentOS, Debian, Arch), FreeBSD, Microsoft Windows
Development and Design Skills	MPI applications, Linux Device Drivers and Modules, Hardware design using Synopsys EDA Tools, Git
Virtualization Platforms	QEMU, Virtual Box, Microsoft Hyper-V
Languages besides native(Greek)	English C2 level. University of Michigan, Certificate of Proficiency in English

References

- Dr. Manolis Marazakis, maraz@ics.forth.gr
- Dr. Manolis Ploumidis, ploumid@ics.forth.gr
- Prof. Manolis G.H. Katevenis, kateveni@ics.forth.gr
- Prof. Vassilis Papaefstathiou, papaef@ics.forth.gr

Publications

[1] I. Vardas, M. Ploumidis, and M. Marazakis. "Towards Communication Profile, Topology and Node Failure Aware Process Placement". In: *2020 IEEE 32nd International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*. 2020, pp. 241–248. DOI: 10.1109/SBAC-PAD49847.2020.00041.

[2] Ioannis Vardas. "Process Placement Optimizations and Heterogeneity Extensions to the Slurm Resource Manager". 2019. URL: https://publications.ics.forth.gr/tech-reports/2020/2020.TR477_MPI_parallel_jobs_Slurm_resource_manager_extensions.pdf.

[3] Dimitris Giannopoulos et al. "Accurate Congestion Control for RDMA Transfers". In: *Proceedings of the Twelfth IEEE/ACM International Symposium on Networks-on-Chip*. NOCS '18. Torino, Italy: IEEE Press, 2018. ISBN: 9781538648933.