Ioannis Vardas

TU Wien - Faculty of Informatics - Institute of Computer Engineering

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Summary

PhD Candidate in Computer Science (PhD thesis accepted, defense pending) with expertise in performance engineering for large-scale HPC systems. Proven ability to identify and resolve critical system inefficiencies by developing novel profiling tools from the ground up, such as mpisee, leading to significant, measurable application speedups. Experience covers key areas of high-performance computing, from contributing to core infrastructure like the Slurm resource manager to optimizing applications via topology-aware process mapping and simulating custom interconnects. A skilled communicator with experience collaborating across diverse domains, from HPC research to pharmaceutical science, driven to solve foundational systems challenges.

Professional Experience

TU Wien - Faculty of Informatics: Parallel Computing Research Unit
Austria

Pre-Doctoral Researcher
June 2021 - June 2025

- Designed and implemented a process mapping algorithm in Python to improve available memory bandwidth and reducing communication overheads for colocated large-scale MPI applications on real-world HPC systems [1, 2, 12].
- Designed and implemented mpisee in C++, a novel profiling tool for MPI applications that analyzes MPI communication per communicator [3, 11]. Utilized to identify performance bottlenecks in scientific applications by dissecting fundamental MPI operations. Made key design decisions about distributed communicator tracking, data collection methodology and analysis framework.
- Collaborated with pharmaceutical researchers to integrate and optimize LigandScout software for molecular screening on HPC systems, communicating technical constraints and identifying opportunities to improve task scheduling [10].
- Contributed to proposals for MPI library API and collective algorithm enhancements [9, 8, 7].
- Currently developing ncclsee in C, a lightweight profiling tool for measuring the time of NCCL operations of distributed GPU applications at large scale.

ICS-FORTH - Computer Architecture and VLSI Systems Laboratory
Greece

Research Engineer
Dec. 2019 - May 2021

- Conducted research on fault-aware process placement strategies to enhance the resilience of MPI applications on HPC systems [5, 4]. Implemented a simulation environment (using C and Python) for generating synthetic node failures based on the Weibull distribution in an HPC torus cluster.

ICS-FORTH - Computer Architecture and VLSI Systems Laboratory
Greece

Graduate Research Assistant
Sept. 2017 - Nov. 2019

- Extended the Slurm resource manager to support heterogeneous architectures (including FPGA-based accelerators) and optimize process placement, demonstrating ability to contribute to complex HPC runtime systems.

Hellenic Army
Greece

Served in the Hellenic Armed Forces
Dec. 2016 - Aug 2017

- Served in the Hellenic Army, Research and Informatics Corps

ICS-FORTH - Computer Architecture and VLSI Systems Laboratory
Greece

Research Scholarship
June 2016 - Nov. 2016

- Simulated the behavior of a novel Accurate congestion control for RDMA Transfers on HPC interconnects using Omnet++ [13].

Skills

HPC & Parallel Computing	MPI, CUDA, HIP, OpenMP, POSIX Threads, SIMD Vectorization
Programming Languages	C, C++ (C++11/17), Python
Performance Analysis Tools	Linux perf, gprof, PAPI, NVIDIA Nsight Systems, Score-P, HPCToolkit
Development Tools	Git, CMake, Bash scripting, CI/CD pipelines (GitHub Actions), GDB, LLDB, Valgrind
Machine Learning & Data Processing	PyTorch, R, PySpark
System Administration	Linux-based (RHEL, SLES, Debian), Docker, Singularity, QEMU, Spack
Languages	Greek (native), English (CEFR C2), German (Intermediate)

Education

TU Wien — *Austria*

Doctoral candidate in Engineering Sciences and Computer Sciences — *Present*

- **PhD Thesis** (thesis accepted, defense pending): Improving Colocated MPI Application Performance via Process Mapping in HPC Systems: Leveraging Hierarchical Process-to-core Mappings and Communicator-centric Profiling. Supervisor: Prof. Jesper Larsson Träff.

University of Crete — *Greece*

M.Sc. in Computer Science and Engineering — *Nov. 2019*

- **MSc Thesis**: Process Placement Optimizations and Heterogeneity Extensions to the Slurm Resource Manager[6]. Advisors: Prof. Manolis G.H. Katevenis, Co-Advisor: Dr. Manolis Marazakis.

University of Crete — *Greece*

B.Sc. in Computer Science — *Mar. 2016*

- **Bachelor Thesis**: Memory Testing through an FPGA with an embedded Processor

Further Education

Certificates

- Machine learning from Stanford Online by Andrew Ng.
- Modern C++ software design (advanced level) by Klaus Iglberger.

Summer Schools

- ACM Europe Summer School on HPC Computer Architectures for AI and Dedicated Applications, 2022: Program Schedule.
- International Summer School on Advanced Computer Architectures and Compilation for High-Perfomance and Embedded Systems (ACACES) 2018.

Other Activities

- Student Volunteer, SC'23 Conference, Denver, USA.

Other Projects

Design of a RISC-V core in System Verilog

- Implementation of RV32IC standard with support for stream instructions.
- Developed with Synopsys EDA tools for the purposes of Digital Circuits Design Lab Using EDA Tools.

Cache Simulator

- Designed and implemented YAC Simulator, a cache simulator written in C/C++ for a simple cache scheme.
- Developed for the purposes of the CS-255 Computer Organization course of the University of Crete.

List of Publications

[1] Ioannis Vardas et al. “Improved Parallel Application Performance and Makespan by Colocation and Topology-aware Process Mapping”. In: *IEEE/ACM 24th International Symposium on Cluster, Cloud and Internet Computing (CCGrid)*. 2024. DOI: 10.1109/CCGrid59990.2024.00023.

[2] Ioannis Vardas et al. “Exploring Mapping Strategies for Co-allocated HPC Applications”. In: *Euro-Par 2023: Parallel Processing Workshops*. Springer Nature Switzerland, 2024, pp. 271–276. DOI: 10.1007/978-3-031-48803-0_31.

[3] Ioannis Vardas et al. “mpisee: MPI Profiling for Communication and Communicator Structure”. In: *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*. 2022, pp. 520–529. DOI: 10.1109/IPDPSW55747.2022.00092.

[4] Ioannis Vardas, Manolis Ploumidis, and Manolis Marazakis. “Towards Communication Profile, Topology and Node Failure Aware Process Placement”. In: *SBAC-PAD*. 2020, pp. 241–248. DOI: 10.1109/SBAC-PAD49847.2020.00041.

[5] Ioannis Vardas, Manolis Ploumidis, and Manolis Marazakis. “Exploring the Impact of Node Failures on the Resource Allocation for Parallel Jobs”. In: *Euro-Par 2021: Parallel Processing Workshops*. Springer International Publishing, 2022, pp. 298–309. DOI: 10.1007/978-3-031-06156-1_24.

[6] Ioannis Vardas. “Process Placement Optimizations and Heterogeneity Extensions to the Slurm Resource Manager”. 2019. URL: https://tinyurl.com/mwujn46s.

[7] Jesper Larsson Träff, Ioannis Vardas, and Sascha Hunold. “Modes, Persistence and Orthogonality: Blowing MPI Up”. In: *Proceedings of the SC ’24 Workshops*. 2024, pp. 404–413. DOI: 10.1109/SCW63240.2024.00061.

[8] Jesper Larsson Träff and Ioannis Vardas. “Library Development with MPI: Attributes, Request Objects, Group Communicator Creation, Local Reductions, and Datatypes”. In: *Proceedings of the 30th European MPI Users’ Group Meeting*. EuroMPI ’23. ACM, 2023. DOI: 10.1145/3615318.3615323.

[9] Jesper Larsson Träff et al. “Uniform Algorithms for Reduce-scatter and (most) other Collectives for MPI”. In: *IEEE International Conference on Cluster Computing (CLUSTER)*. 2023, pp. 284–294. DOI: 10.1109/CLUSTER52292.2023.00031.

[10] Sascha Hunold et al. “Massively Scaling Molecular Screening Workloads on EuroHPC Supercomputers”. In: *Austrian-Slovenian HPC Meeting 2023 - ASHPC23*. 2023, pp. 51–51. DOI: 10.25365/phaidra.423.

[11] Sascha Hunold et al. “An Overhead Analysis of MPI Profiling and Tracing Tools”. In: *Proceedings of the PERMAVOST workshop*. ACM, 2022. DOI: 10.1145/3526063.3535353.

[12] Philippe Swartvagher et al. “Using Mixed-Radix Decomposition to Enumerate Computational Resources of Deeply Hierarchical Architectures”. In: *Proceedings of the SC ’23 Workshops*. SC-W ’23. ACM, 2023, pp. 405–415. DOI: 10.1145/3624062.3624109.

[13] Dimitris Giannopoulos et al. “Accurate Congestion Control for RDMA Transfers”. In: *Proceedings of the Twelfth IEEE/ACM International Symposium on Networks-on-Chip*. NOCS ’18. Torino, Italy, 2018. DOI: 10.1109/NOCS.2018.8512155.