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MCUXpresso SDK API Reference Manual

NXP Semiconductors



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Chapter 1

Introduction

The MCUXpresso Software Development Kit (MCUXpresso SDK) is a collection of software enablement for NXP Microcontrollers that includes peripheral drivers, multicore support and integrated RTOS support for FreeRTOS™. In addition to the base enablement, the MCUXpresso SDK is augmented with demo applications, driver example projects, and API documentation to help users quickly leverage the support provided by MCUXpresso SDK. The [MCUXpresso SDK Web Builder](#) is available to provide access to all MCUXpresso SDK packages. See the *MCUXpresso Software Development Kit (SDK) Release Notes* (document MCUXSDKRNN) in the Supported Devices section at [MCUXpresso-SDK: Software Development Kit for MCUXpresso](#) for details.

The MCUXpresso SDK is built with the following runtime software components:

- Arm® and DSP standard libraries, and CMSIS-compliant device header files which provide direct access to the peripheral registers.
- Peripheral drivers that provide stateless, high-performance, ease-of-use APIs. Communication drivers provide higher-level transactional APIs for a higher-performance option.
- RTOS wrapper driver built on top of MCUXpresso SDK peripheral drivers and leverage native RTOS services to better comply to the RTOS cases.
- Real time operation systems (RTOS) for FreeRTOS OS.
- Stacks and middleware in source or object formats including:
- CMSIS-DSP, a suite of common signal processing functions.
- The MCUXpresso SDK comes complete with software examples demonstrating the usage of the peripheral drivers, RTOS wrapper drivers, middleware, and RTOSes.

The peripheral drivers and RTOS driver wrappers can be used across multiple devices within the product family without modification. The configuration items for each driver are encapsulated into C language data structures. Device-specific configuration information is provided as part of the MCUXpresso SDK and need not be modified by the user. If necessary, the user is able to modify the peripheral driver and RTOS wrapper driver configuration during runtime. The driver examples demonstrate how to configure the drivers by passing the proper configuration data to the APIs. The folder structure is organized to reduce the total number of includes required to compile a project.

The rest of this document describes the API references in detail for the peripheral drivers and RTOS wrapper drivers. For the latest version of this and other MCUXpresso SDK documents, see the [mcuxpresso.nxp.com/apidoc/](#).

Deliverable	Location
Demo Applications	<install_dir>/boards/<board_name>/demo_apps
Driver Examples	<install_dir>/boards/<board_name>/driver_examples
Documentation	<install_dir>/docs
Middleware	<install_dir>/middleware
Drivers	<install_dir>/<device_name>/drivers/
CMSIS Standard Arm Cortex-M Headers, math and DSP Libraries	<install_dir>/CMSIS
Device Startup and Linker	<install_dir>/<device_name>/<toolchain>/
MCUXpresso SDK Utilities	<install_dir>/devices/<device_name>/utilities
RTOS Kernel Code	<install_dir>/rtos

MCUXpresso SDK Folder Structure

Chapter 2

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Chapter 3

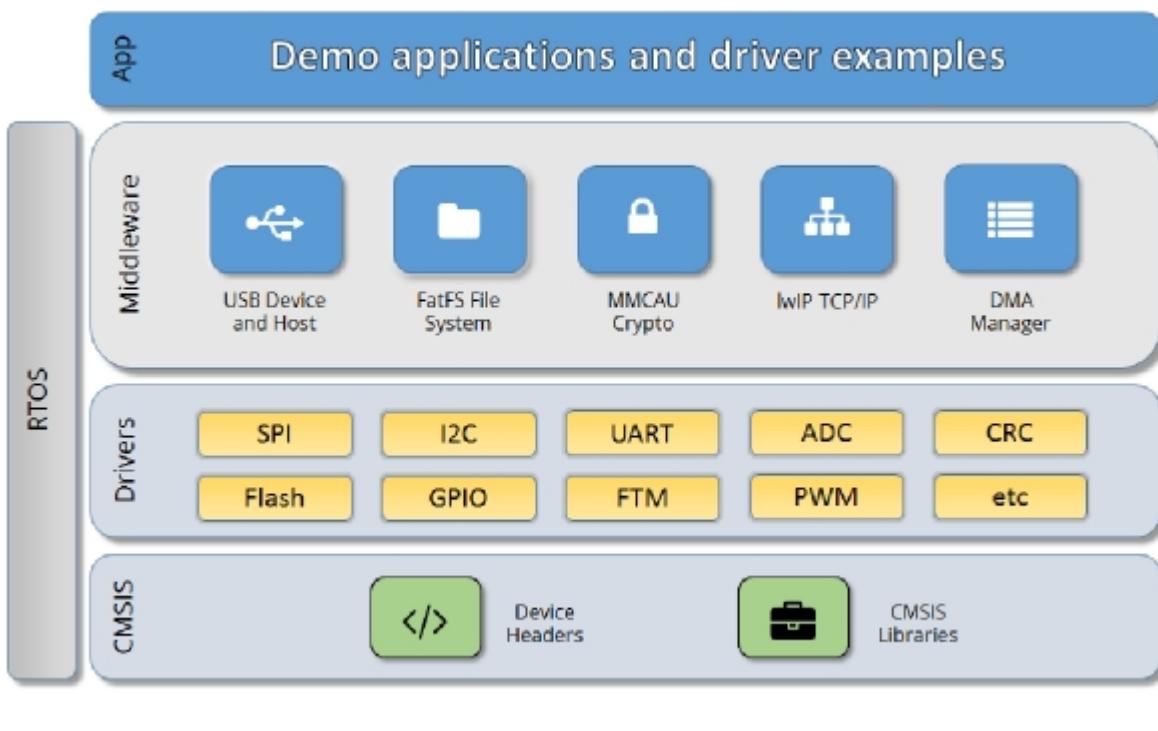
Architectural Overview

This chapter provides the architectural overview for the MCUXpresso Software Development Kit (MCUXpresso SDK). It describes each layer within the architecture and its associated components.

Overview

The MCUXpresso SDK architecture consists of five key components listed below.

1. The Arm Cortex Microcontroller Software Interface Standard (CMSIS) CORE compliance device-specific header files, SOC Header, and CMSIS math/DSP libraries.
2. Peripheral Drivers
3. Real-time Operating Systems (RTOS)
4. Stacks and Middleware that integrate with the MCUXpresso SDK
5. Demo Applications based on the MCUXpresso SDK



MCU header files

Each supported MCU device in the MCUXpresso SDK has an overall System-on Chip (SoC) memory-

mapped header file. This header file contains the memory map and register base address for each peripheral and the IRQ vector table with associated vector numbers. The overall SoC header file provides access to the peripheral registers through pointers and predefined bit masks. In addition to the overall SoC memory-mapped header file, the MCUXpresso SDK includes a feature header file for each device. The feature header file allows NXP to deliver a single software driver for a given peripheral. The feature file ensures that the driver is properly compiled for the target SOC.

CMSIS Support

Along with the SoC header files and peripheral extension header files, the MCUXpresso SDK also includes common CMSIS header files for the Arm Cortex-M core and the math and DSP libraries from the latest CMSIS release. The CMSIS DSP library source code is also included for reference.

MCUXpresso SDK Peripheral Drivers

The MCUXpresso SDK peripheral drivers mainly consist of low-level functional APIs for the MCU product family on-chip peripherals and also of high-level transactional APIs for some bus drivers/DM-A driver/eDMA driver to quickly enable the peripherals and perform transfers.

All MCUXpresso SDK peripheral drivers only depend on the CMSIS headers, device feature files, fsl_common.h, and fsl_clock.h files so that users can easily pull selected drivers and their dependencies into projects. With the exception of the clock/power-relevant peripherals, each peripheral has its own driver. Peripheral drivers handle the peripheral clock gating/ungating inside the drivers during initialization and deinitialization respectively.

Low-level functional APIs provide common peripheral functionality, abstracting the hardware peripheral register accesses into a set of stateless basic functional operations. These APIs primarily focus on the control, configuration, and function of basic peripheral operations. The APIs hide the register access details and various MCU peripheral instantiation differences so that the application can be abstracted from the low-level hardware details. The API prototypes are intentionally similar to help ensure easy portability across supported MCUXpresso SDK devices.

Transactional APIs provide a quick method for customers to utilize higher-level functionality of the peripherals. The transactional APIs utilize interrupts and perform asynchronous operations without user intervention. Transactional APIs operate on high-level logic that requires data storage for internal operation context handling. However, the Peripheral Drivers do not allocate this memory space. Rather, the user passes in the memory to the driver for internal driver operation. Transactional APIs ensure the NVIC is enabled properly inside the drivers. The transactional APIs do not meet all customer needs, but provide a baseline for development of custom user APIs.

Note that the transactional drivers never disable an NVIC after use. This is due to the shared nature of interrupt vectors on devices. It is up to the user to ensure that NVIC interrupts are properly disabled after usage is complete.

Interrupt handling for transactional APIs

A double weak mechanism is introduced for drivers with transactional API. The double weak indicates two levels of weak vector entries. See the examples below:

```
PUBWEAK SPI0_IRQHandler  
PUBWEAK SPI0_DriverIRQHandler  
SPI0_IRQHandler
```

```
LDR      R0, =SPI0_DriverIRQHandler  
BX      R0
```

The first level of the weak implementation are the functions defined in the vector table. In the devices/<DEVICE_NAME>/<TOOLCHAIN>/startup_<DEVICE_NAME>.s/.S file, the implementation of the first layer weak function calls the second layer of weak function. The implementation of the second layer weak function (ex. SPI0_DriverIRQHandler) jumps to itself (B). The MCUXpresso SDK drivers with transactional APIs provide the reimplementation of the second layer function inside of the peripheral driver. If the MCUXpresso SDK drivers with transactional APIs are linked into the image, the SPI0_DriverIRQHandler is replaced with the function implemented in the MCUXpresso SDK SPI driver.

The reason for implementing the double weak functions is to provide a better user experience when using the transactional APIs. For drivers with a transactional function, call the transactional APIs and the drivers complete the interrupt-driven flow. Users are not required to redefine the vector entries out of the box. At the same time, if users are not satisfied by the second layer weak function implemented in the MCUXpresso SDK drivers, users can redefine the first layer weak function and implement their own interrupt handler functions to suit their implementation.

The limitation of the double weak mechanism is that it cannot be used for peripherals that share the same vector entry. For this use case, redefine the first layer weak function to enable the desired peripheral interrupt functionality. For example, if the MCU's UART0 and UART1 share the same vector entry, redefine the UART0_UART1_IRQHandler according to the use case requirements.

Feature Header Files

The peripheral drivers are designed to be reusable regardless of the peripheral functional differences from one MCU device to another. An overall Peripheral Feature Header File is provided for the MCUXpresso SDK-supported MCU device to define the features or configuration differences for each sub-family device.

Application

See the *Getting Started with MCUXpresso SDK* document (MCUXSDKGSUG).

Chapter 4

AUDIOMIX Driver

4.1 Overview

AUDIOMIX driver provides APIs to control AUDIOMIX clock.

Macros

- `#define AUDIOMIX_ATTACH_ID(offset, mask, value) ((uint32_t)(offset) | ((uint32_t)(mask) << 16U) | ((uint32_t)(value) << 24U))`
AUDIOMIX attach id combination.

Typedefs

- `typedef enum _audiomix_attach_clk audiomix_attach_clk_t`
audio mix attach clk id

Enumerations

- enum _audiomix_attach_clk {

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI1_ROOT,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI2_ROOT,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI3_ROOT,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI5_ROOT,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI6_ROOT,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI7_ROOT,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI1_MCLK,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI2_MCLK,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI3_MCLK,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI5_MCLK,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI6_MCLK,

kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI7_MCLK,

kAUDIOMIX_Attach_SAI1_MCLK1_To_SAI1_ROOT,

kAUDIOMIX_Attach_SAI1_MCLK1_To_SAI1_MCLK,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI1_ROOT,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI2_ROOT,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI3_ROOT,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI5_ROOT,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI6_ROOT,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI7_ROOT,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI1_MCLK,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI2_MCLK,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI3_MCLK,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI5_MCLK,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI6_MCLK,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI7_MCLK,

kAUDIOMIX_Attach_SAI2_MCLK2_To_SPDIF_ExtCLK,

kAUDIOMIX_Attach_SAI2_MCLK1_To_SAI2_ROOT,

kAUDIOMIX_Attach_SAI2_MCLK1_To_SAI2_MCLK,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI1_ROOT,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI2_ROOT,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI3_ROOT,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI5_ROOT,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI6_ROOT,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI7_ROOT,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI1_MCLK,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI2_MCLK,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI3_MCLK,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI5_MCLK,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI6_MCLK,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI7_MCLK,

kAUDIOMIX_Attach_SAI3_MCLK2_To_SPDIF_ExtCLK,

kAUDIOMIX_Attach_SAI3_MCLK1_To_SAI3_ROOT,

kAUDIOMIX_Attach_SAI3_MCLK1_To_SAI3_MCLK,

```

U, 2U) }

    audio mix attach clk id
• enum _audiomix_power_ctrl {
    kAUDIOMIX_PowerCtrlEDMA = 1U,
    kAUDIOMIX_PowerCtrlSDMA2 = 2U,
    kAUDIOMIX_PowerCtrlSDMA3 = 4U,
    kAUDIOMIX_PowerCtrlPDM = 8U,
    kAUDIOMIX_PowerCtrlSAI1 = 16U,
    kAUDIOMIX_PowerCtrlSAI2 = 32U,
    kAUDIOMIX_PowerCtrlSAI3 = 64U,
    kAUDIOMIX_PowerCtrlSAI5 = 128U,
    kAUDIOMIX_PowerCtrlSAI6 = 256U,
    kAUDIOMIX_PowerCtrlSAI7 = 512U }

    audio mix power control

```

Driver version

- #define **FSL_AUDIOMIX_DRIVER_VERSION** (**MAKE_VERSION(2, 0, 1)**)
AUDIOMIX driver version 2.0.1.

AUDIOMIX clock Setting

- void **AUDIOMIX_AttachClk** (AUDIOMIX_Type *base, **audiomix_attach_clk_t** id)
audiomix attach clock.
- static uint32_t **AUDIOMIX_GetIPStopAck** (AUDIOMIX_Type *base, uint32_t ip)
audiomix low power ack bit status.
- static void **AUDIOMIX_SetIPStop** (AUDIOMIX_Type *base, uint32_t ip)
audiomix low power stop mode
- static void **AUDIOMIX_SetEARCReset** (AUDIOMIX_Type *base, bool enable)
audiomix earc reset
- static void **AUDIOMIX_SetEARCPHYReset** (AUDIOMIX_Type *base, bool enable)
audiomix earc PHY reset
- void **AUDIOMIX_InitAudioPll** (AUDIOMIX_Type *base, const **ccm_analog_frac_pll_config_t** *config)
Initializes the SAI PLL.
- void **AUDIOMIX_DeinitAudioPll** (AUDIOMIX_Type *base)
brief De-initialize the SAI PLL.
- uint32_t **AUDIOMIX_GetAudioPllFreq** (AUDIOMIX_Type *base)
Get the sai PLL output freq.

4.2 Macro Definition Documentation

4.2.1 #define FSL_AUDIOMIX_DRIVER_VERSION (MAKE_VERSION(2, 0, 1))

4.3 Enumeration Type Documentation

4.3.1 enum _audiomix_attach_clk

Enumerator

<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI1_ROOT</i>	attach SAI1 MCLK2 to SAI1 root
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI2_ROOT</i>	attach SAI1 MCLK2 to SAI2 root
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI3_ROOT</i>	attach SAI1 MCLK2 to SAI3 root
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI5_ROOT</i>	attach SAI1 MCLK2 to SAI5 root
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI6_ROOT</i>	attach SAI1 MCLK2 to SAI6 root
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI7_ROOT</i>	attach SAI1 MCLK2 to SAI7 root
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI1_MCLK</i>	attach SAI1 MCLK2 to SAI1 MCLK
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI2_MCLK</i>	attach SAI1 MCLK2 to SAI2 MCLK
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI3_MCLK</i>	attach SAI1 MCLK2 to SAI3 MCLK
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI5_MCLK</i>	attach SAI1 MCLK2 to SAI5 MCLK
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI6_MCLK</i>	attach SAI1 MCLK2 to SAI6 MCLK
<i>kAUDIOMIX_Attach_SAI1_MCLK2_To_SAI7_MCLK</i>	attach SAI1 MCLK2 to SAI7 MCLK
<i>kAUDIOMIX_Attach_SAI1_MCLK1_To_SAI1_ROOT</i>	attach SAI1 MCLK1 to SAI1 root
<i>kAUDIOMIX_Attach_SAI1_MCLK1_To_SAI1_MCLK</i>	attach SAI1 MCLK1 to SAI1 MCLK
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI1_ROOT</i>	attach SAI2 MCLK2 to SAI1 root
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI2_ROOT</i>	attach SAI2 MCLK2 to SAI2 root
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI3_ROOT</i>	attach SAI2 MCLK2 to SAI3 root
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI5_ROOT</i>	attach SAI2 MCLK2 to SAI5 root
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI6_ROOT</i>	attach SAI2 MCLK2 to SAI6 root
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI7_ROOT</i>	attach SAI2 MCLK2 to SAI7 root
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI1_MCLK</i>	attach SAI2 MCLK2 to SAI1 MCLK
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI2_MCLK</i>	attach SAI2 MCLK2 to SAI2 MCLK
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI3_MCLK</i>	attach SAI2 MCLK2 to SAI3 MCLK
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI5_MCLK</i>	attach SAI2 MCLK2 to SAI5 MCLK
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI6_MCLK</i>	attach SAI2 MCLK2 to SAI6 MCLK
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SAI7_MCLK</i>	attach SAI2 MCLK2 to SAI7 MCLK
<i>kAUDIOMIX_Attach_SAI2_MCLK2_To_SPDIF_ExtCLK</i>	attach SAI2 MCLK2 to SPDIF EXTC-LK
<i>kAUDIOMIX_Attach_SAI2_MCLK1_To_SAI2_ROOT</i>	attach SAI2 MCLK1 to SAI2 root
<i>kAUDIOMIX_Attach_SAI2_MCLK1_To_SAI2_MCLK</i>	attach SAI2 MCLK1 to SAI2 MCLK
<i>kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI1_ROOT</i>	attach SAI3 MCLK2 to SAI1 root
<i>kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI2_ROOT</i>	attach SAI3 MCLK2 to SAI2 root
<i>kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI3_ROOT</i>	attach SAI3 MCLK2 to SAI3 root
<i>kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI5_ROOT</i>	attach SAI3 MCLK2 to SAI5 root
<i>kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI6_ROOT</i>	attach SAI3 MCLK2 to SAI6 root
<i>kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI7_ROOT</i>	attach SAI3 MCLK2 to SAI7 root
<i>kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI1_MCLK</i>	attach SAI3 MCLK2 to SAI1 MCLK
<i>kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI2_MCLK</i>	attach SAI3 MCLK2 to SAI2 MCLK
<i>kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI3_MCLK</i>	attach SAI3 MCLK2 to SAI3 MCLK
<i>kAUDIOMIX_Attach_SAI3_MCLK2_To_SAI5_MCLK</i>	attach SAI3 MCLK2 to SAI5 MCLK

<i>KAUDIOMIX_Attach_SAI3_MCLK2_To_SAI6_MCLK</i>	attach SAI3 MCLK2 to SAI6 MCLK
<i>KAUDIOMIX_Attach_SAI3_MCLK2_To_SAI7_MCLK</i>	attach SAI3 MCLK2 to SAI7 MCLK
<i>KAUDIOMIX_Attach_SAI3_MCLK2_To_SPDIF_ExtCLK</i>	attach SAI3 MCLK2 to SPDIF EXTC-LK
<i>KAUDIOMIX_Attach_SAI3_MCLK1_To_SAI3_ROOT</i>	attach SAI3 MCLK1 to SAI3 root
<i>KAUDIOMIX_Attach_SAI3_MCLK1_To_SAI3_MCLK</i>	attach SAI3 MCLK1 to SAI3 MCLK
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI1_ROOT</i>	attach SAI5 MCLK2 to SAI1 root
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI2_ROOT</i>	attach SAI5 MCLK2 to SAI2 root
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI3_ROOT</i>	attach SAI5 MCLK2 to SAI3 root
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI5_ROOT</i>	attach SAI5 MCLK2 to SAI5 root
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI6_ROOT</i>	attach SAI5 MCLK2 to SAI6 root
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI7_ROOT</i>	attach SAI5 MCLK2 to SAI7 root
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI1_MCLK</i>	attach SAI5 MCLK2 to SAI1 MCLK
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI2_MCLK</i>	attach SAI5 MCLK2 to SAI2 MCLK
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI3_MCLK</i>	attach SAI5 MCLK2 to SAI3 MCLK
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI5_MCLK</i>	attach SAI5 MCLK2 to SAI5 MCLK
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI6_MCLK</i>	attach SAI5 MCLK2 to SAI6 MCLK
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SAI7_MCLK</i>	attach SAI5 MCLK2 to SAI7 MCLK
<i>KAUDIOMIX_Attach_SAI5_MCLK2_To_SPDIF_ExtCLK</i>	attach SAI5 MCLK2 to SPDIF EXTC-LK
<i>KAUDIOMIX_Attach_SAI5_MCLK1_To_SAI5_ROOT</i>	attach SAI5 MCLK1 to SAI5 root
<i>KAUDIOMIX_Attach_SAI5_MCLK1_To_SAI5_MCLK</i>	attach SAI5 MCLK1 to SAI5 MCLK
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI1_ROOT</i>	attach SAI6 MCLK2 to SAI1 root
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI2_ROOT</i>	attach SAI6 MCLK2 to SAI2 root
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI3_ROOT</i>	attach SAI6 MCLK2 to SAI3 root
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI5_ROOT</i>	attach SAI6 MCLK2 to SAI5 root
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI6_ROOT</i>	attach SAI6 MCLK2 to SAI6 root
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI7_ROOT</i>	attach SAI6 MCLK2 to SAI7 root
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI1_MCLK</i>	attach SAI6 MCLK2 to SAI1 MCLK
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI2_MCLK</i>	attach SAI6 MCLK2 to SAI2 MCLK
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI3_MCLK</i>	attach SAI6 MCLK2 to SAI3 MCLK
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI5_MCLK</i>	attach SAI6 MCLK2 to SAI5 MCLK
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI6_MCLK</i>	attach SAI6 MCLK2 to SAI6 MCLK
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SAI7_MCLK</i>	attach SAI6 MCLK2 to SAI7 MCLK
<i>KAUDIOMIX_Attach_SAI6_MCLK2_To_SPDIF_ExtCLK</i>	attach SAI6 MCLK2 to SPDIF EXTC-LK
<i>KAUDIOMIX_Attach_SAI6_MCLK1_To_SAI6_ROOT</i>	attach SAI6 MCLK2 to SAI6 root
<i>KAUDIOMIX_Attach_SAI6_MCLK1_To_SAI6_MCLK</i>	attach SAI6 MCLK2 to SAI6 MCLK
<i>KAUDIOMIX_Attach_SAI7_MCLK2_To_SAI1_ROOT</i>	attach SAI7 MCLK2 to SAI1 root
<i>KAUDIOMIX_Attach_SAI7_MCLK2_To_SAI2_ROOT</i>	attach SAI7 MCLK2 to SAI2 root
<i>KAUDIOMIX_Attach_SAI7_MCLK2_To_SAI3_ROOT</i>	attach SAI7 MCLK2 to SAI3 root
<i>KAUDIOMIX_Attach_SAI7_MCLK2_To_SAI5_ROOT</i>	attach SAI7 MCLK2 to SAI5 root
<i>KAUDIOMIX_Attach_SAI7_MCLK2_To_SAI6_ROOT</i>	attach SAI7 MCLK2 to SAI6 root
<i>KAUDIOMIX_Attach_SAI7_MCLK2_To_SAI7_ROOT</i>	attach SAI7 MCLK2 to SAI7 root
<i>KAUDIOMIX_Attach_SAI7_MCLK2_To_SAI1_MCLK</i>	attach SAI7 MCLK2 to SAI1 MCLK

kAUDIOMIX_Attach_SAI7_MCLK2_To_SAI2_MCLK attach SAI7 MCLK2 to SAI2 MCLK
kAUDIOMIX_Attach_SAI7_MCLK2_To_SAI3_MCLK attach SAI7 MCLK2 to SAI3 MCLK
kAUDIOMIX_Attach_SAI7_MCLK2_To_SAI5_MCLK attach SAI7 MCLK2 to SAI5 MCLK
kAUDIOMIX_Attach_SAI7_MCLK2_To_SAI6_MCLK attach SAI7 MCLK2 to SAI6 MCLK
kAUDIOMIX_Attach_SAI7_MCLK2_To_SAI7_MCLK attach SAI7 MCLK2 to SAI7 MCLK
kAUDIOMIX_Attach_SAI7_MCLK2_To_SPDIF_ExtCLK attach SAI7 MCLK2 to SPDIF_ExtC-LK
kAUDIOMIX_Attach_SAI7_MCLK1_To_SAI7_ROOT attach SAI7 MCLK1 to SAI7 root
kAUDIOMIX_Attach_SAI7_MCLK1_To_SAI7_MCLK attach SAI7 MCLK1 to SAI7 MCLK
kAUDIOMIX_Attach_PDM_Root_to_CCM_PDM attach PDM ROOT to CCM PDM clock
kAUDIOMIX_Attach_PDM_Root_to_SAI_PLL_DVI2 attach PDM ROOT to sai pll div2
kAUDIOMIX_Attach_PDM_Root_to_SAI1_MCLK attach PDM ROOT to SAI1 mclk

4.3.2 enum _audiomix_power_ctrl

Enumerator

kAUDIOMIX_PowerCtrlEDMA edma power control
kAUDIOMIX_PowerCtrlSDMA2 SDMA2 power control.
kAUDIOMIX_PowerCtrlSDMA3 SDMA3 power control.
kAUDIOMIX_PowerCtrlPDM PDM power control.
kAUDIOMIX_PowerCtrlSAI1 SAI1 power control.
kAUDIOMIX_PowerCtrlSAI2 SAI2 power control.
kAUDIOMIX_PowerCtrlSAI3 SAI3 power control.
kAUDIOMIX_PowerCtrlSAI5 SAI5 power control.
kAUDIOMIX_PowerCtrlSAI6 SAI6 power control.
kAUDIOMIX_PowerCtrlSAI7 SAI7 power control.

4.4 Function Documentation

4.4.1 void AUDIOMIX_AttachClk (**AUDIOMIX_Type** * *base*, **audiomix_attach_clk_t id)**

Parameters

<i>base</i>	audiomix base address.
<i>id</i>	attach clock id.

4.4.2 static uint32_t AUDIOMIX_GetIPStopAck (**AUDIOMIX_Type** * *base*, **uint32_t ip**) [inline], [static]

Parameters

<i>base</i>	audiomix base address.
<i>ip</i>	reference _audiomix_power_ctrl, can be a value or combine value in _audiomix_-power_ctrl

4.4.3 static void AUDIOMIX_SetIPStop (AUDIOMIX_Type * *base*, uint32_t *ip*) [inline], [static]

Parameters

<i>base</i>	audiomix base address.
<i>ip</i>	reference _audiomix_power_ctrl, can be a value or combine value in _audiomix_-power_ctrl

4.4.4 static void AUDIOMIX_SetEARCReset (AUDIOMIX_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	audiomix base address.
<i>enable</i>	true is reset, flase is release.

4.4.5 static void AUDIOMIX_SetEARCPhyReset (AUDIOMIX_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	audiomix base address.
<i>enable</i>	true is reset, flase is release.

4.4.6 void AUDIOMIX_InitAudioPII (AUDIOMIX_Type * *base*, const ccm_analog_frac_pll_config_t * *config*)

note This function can't detect whether the AUDIO PLL has been enabled and used by some IPs.

Parameters

<i>base</i>	audiomix base address.
<i>config</i>	Pointer to the configuration structure(see ref ccm_analog_frac_pll_config-t enumeration).

4.4.7 uint32_t AUDIOMIX_GetAudioPIIFreq (AUDIOMIX_Type * *base*)

Return values

<i>sai</i>	pll output freq.
------------	------------------

Chapter 5

Clock Driver

5.1 Overview

The MCUXpresso SDK provides APIs for MCUXpresso SDK devices' clock operation.

The clock driver supports:

- Clock generator (PLL, FLL, and so on) configuration
- Clock mux and divider configuration
- Getting clock frequency

Data Structures

- struct `_ccm_analog_frac_pll_config`
Fractional-N PLL configuration. [More...](#)
- struct `_ccm_analog_integer_pll_config`
Integer PLL configuration. [More...](#)

Macros

- `#define OSC24M_CLK_FREQ 24000000U`
XTAL 24M clock frequency.
- `#define CLKPAD_FREQ 0U`
pad clock frequency.
- `#define ECSPI_CLOCKS`
Clock ip name array for ECSPI.
- `#define EDMA_CLOCKS`
Clock ip name array for EDMA.
- `#define ENET_CLOCKS`
Clock ip name array for ENET.
- `#define ENETQOS_CLOCKS`
Clock ip name array for ENET_QOS.
- `#define FLEXCAN_CLOCKS`
Clock ip name array for FLEXCAN.
- `#define GPIO_CLOCKS`
Clock ip name array for GPIO.
- `#define GPT_CLOCKS`
Clock ip name array for GPT.
- `#define I2C_CLOCKS`
Clock ip name array for I2C.
- `#define IOMUX_CLOCKS`
Clock ip name array for IOMUX.
- `#define IPMUX_CLOCKS`
Clock ip name array for IPMUX.
- `#define PWM_CLOCKS`
Clock ip name array for PWM.

- #define **RDC_CLOCKS**
Clock ip name array for RDC.
- #define **SAI_CLOCKS**
Clock ip name array for SAI.
- #define **RDC_SEMA42_CLOCKS**
Clock ip name array for RDC SEMA42.
- #define **UART_CLOCKS**
Clock ip name array for UART.
- #define **USDHC_CLOCKS**
Clock ip name array for USDHC.
- #define **WDOG_CLOCKS**
Clock ip name array for WDOG.
- #define **TMU_CLOCKS**
Clock ip name array for TEMPSENSOR.
- #define **SDMA_CLOCKS**
Clock ip name array for SDMA.
- #define **MU_CLOCKS**
Clock ip name array for MU.
- #define **QSPI_CLOCKS**
Clock ip name array for QSPI.
- #define **PDM_CLOCKS**
Clock ip name array for PDM.
- #define **ASRC_CLOCKS**
Clock ip name array for ASRC.
- #define **CCM_BIT_FIELD_EXTRACTION**(val, mask, shift) (((val) & (mask)) >> (shift))
CCM reg macros to extract corresponding registers bit field.
- #define **CCM_REG_OFF**(root, off) (*((volatile uint32_t *)((uintptr_t)(root) + (off))))
CCM reg macros to map corresponding registers.
- #define **AUDIO_PLL1_GEN_CTRL_OFFSET** 0x00
CCM Analog registers offset.
- #define **CCM_ANALOG_TUPLE**(reg, shift) (((reg)&0xFFFFU) << 16U) | ((shift))
CCM ANALOG tuple macros to map corresponding registers and bit fields.
- #define **CLOCK_GATE_IN_AUDIOMIX** (1U)
CCM CCGR and root tuple.
- #define **AUDIOMIX_TUPLE**(offset, gate, root) (((**CLOCK_GATE_IN_AUDIOMIX**) << 28U) | ((offset)&0xFU) << 24U) | (((gate)&0xFFU) << 16U) | ((root)&0xFFFFU))
audio mix CCGR
- #define **CLOCK_ROOT_SOURCE**
clock root source
- #define **kCLOCK_CoreSysClk** **kCLOCK_CoreM7Clk**
For compatible with other platforms without CCM.
- #define **CLOCK_GetCoreSysClkFreq** **CLOCK_GetCoreM7Freq**
For compatible with other platforms without CCM.

Typedefs

- typedef enum **_clock_name** **clock_name_t**
Clock name used to get clock frequency.
- typedef enum **_clock_ip_name** **clock_ip_name_t**
CCM CCGR gate control.
- typedef enum **_clock_root_control** **clock_root_control_t**

- `ccm root name used to get clock frequency.`
- `typedef enum _clock_root clock_root_t`
`ccm clock root used to get clock frequency.`
- `typedef enum _clock_rootmux_m7_clk_sel clock_rootmux_m7_clk_sel_t`
`Root clock select enumeration for ARM Cortex-M7 core.`
- `typedef enum _clock_rootmux_axi_clk_sel clock_rootmux_axi_clk_sel_t`
`Root clock select enumeration for MAIN AXI bus.`
- `typedef enum _clock_rootmux_ahb_clk_sel clock_rootmux_ahb_clk_sel_t`
`Root clock select enumeration for AHB bus.`
- `typedef enum _clock_rootmux_audio_ahb_clk_sel clock_rootmux_audio_ahb_clk_sel_t`
`Root clock select enumeration for Audio AHB bus.`
- `typedef enum _clock_rootmux_qspi_clk_sel clock_rootmux_qspi_clk_sel_t`
`Root clock select enumeration for QSPI peripheral.`
- `typedef enum _clock_rootmux_ecspi_clk_sel clock_rootmux_ecspi_clk_sel_t`
`Root clock select enumeration for ECSPI peripheral.`
- `typedef enum _clock_rootmux_enet_axi_clk_sel clock_rootmux_enet_axi_clk_sel_t`
`Root clock select enumeration for ENET AXI bus.`
- `typedef enum _clock_rootmux_enet_qos_clk_sel clock_rootmux_enet_qos_clk_sel_t`
`Root clock select enumeration for ENET QOS Clcok.`
- `typedef enum _clock_rootmux_enet_ref_clk_sel clock_rootmux_enet_ref_clk_sel_t`
`Root clock select enumeration for ENET REF Clcok.`
- `typedef enum _clock_rootmux_enet_qos_timer_clk_sel clock_rootmux_enet_qos_timer_clk_sel_t`
`Root clock select enumeration for ENET QOS TIMER Clcok.`
- `typedef enum _clock_rootmux_enet_timer_clk_sel clock_rootmux_enet_timer_clk_sel_t`
`Root clock select enumeration for ENET TIMER Clcok.`
- `typedef enum _clock_rootmux_enet_phy_clk_sel clock_rootmux_enet_phy_clk_sel_t`
`Root clock select enumeration for ENET PHY Clcok.`
- `typedef enum _clock_rootmux_flexcan_clk_sel clock_rootmux_flexcan_clk_sel_t`
`Root clock select enumeration for FLEXCAN peripheral.`
- `typedef enum _clock_rootmux_i2c_clk_sel clock_rootmux_i2c_clk_sel_t`
`Root clock select enumeration for I2C peripheral.`
- `typedef enum _clock_rootmux_uart_clk_sel clock_rootmux_uart_clk_sel_t`
`Root clock select enumeration for UART peripheral.`
- `typedef enum _clock_rootmux_gpt clock_rootmux_gpt_t`

- *Root clock select enumeration for GPT peripheral.*
• `typedef enum _clock_rootmux_wdog_clk_sel clock_rootmux_wdog_clk_sel_t`
Root clock select enumeration for WDOG peripheral.
- `typedef enum _clock_rootmux_pwm_clk_sel clock_rootmux_Pwm_clk_sel_t`
Root clock select enumeration for PWM peripheral.
- `typedef enum _clock_rootmux_sai_clk_sel clock_rootmux_sai_clk_sel_t`
Root clock select enumeration for SAI peripheral.
- `typedef enum _clock_rootmux_pdm_clk_sel clock_rootmux_pdm_clk_sel_t`
Root clock select enumeration for PDM peripheral.
- `typedef enum _clock_rootmux_noc_clk_sel clock_rootmux_noc_clk_sel_t`
Root clock select enumeration for NOC CLK.
- `typedef enum _clock_pll_gate clock_pll_gate_t`
CCM PLL gate control.
- `typedef enum _clock_gate_value clock_gate_value_t`
CCM gate control value.
- `typedef enum _clock_pll_bypass_ctrl clock_pll_bypass_ctrl_t`
PLL control names for PLL bypass.
- `typedef enum _ccm_analog_pll_clke clock_pll_clke_t`
PLL clock names for clock enable/disable settings.
- `typedef enum _clock_pll_ctrl clock_pll_ctrl_t`
ANALOG Power down override control.
- `typedef struct _ccm_analog_frac_pll_config ccm_analog_frac_pll_config_t`
Fractional-N PLL configuration.
- `typedef struct _ccm_analog_integer_pll_config ccm_analog_integer_pll_config_t`
Integer PLL configuration.

Enumerations

- enum `_clock_name` {

 `kCLOCK_CoreM7Clk,`

 `kCLOCK_AxiClk,`

 `kCLOCK_AhbClk,`

 `kCLOCK_IpgClk,`

 `kCLOCK_PerClk,`

 `kCLOCK_EnetIpgClk,`

 `kCLOCK_Osc24MClk,`

 `kCLOCK_ArmPllClk,`

 `kCLOCK_DramPllClk,`

 `kCLOCK_VpuPllClk,`

 `kCLOCK_SysPll1Clk,`

 `kCLOCK_SysPll1Div2Clk,`

 `kCLOCK_SysPll1Div3Clk,`

 `kCLOCK_SysPll1Div4Clk,`

 `kCLOCK_SysPll1Div5Clk,`

 `kCLOCK_SysPll1Div6Clk,`

 `kCLOCK_SysPll1Div8Clk,`

 `kCLOCK_SysPll1Div10Clk,`

 `kCLOCK_SysPll1Div20Clk,`

 `kCLOCK_SysPll2Clk,`

 `kCLOCK_SysPll2Div2Clk,`

 `kCLOCK_SysPll2Div3Clk,`

 `kCLOCK_SysPll2Div4Clk,`

 `kCLOCK_SysPll2Div5Clk,`

 `kCLOCK_SysPll2Div6Clk,`

 `kCLOCK_SysPll2Div8Clk,`

 `kCLOCK_SysPll2Div10Clk,`

 `kCLOCK_SysPll2Div20Clk,`

 `kCLOCK_SysPll3Clk,`

 `kCLOCK_AudioPll1Clk,`

 `kCLOCK_AudioPll2Clk,`

 `kCLOCK_VideoPll1Clk,`

 `kCLOCK_ExtClk1,`

 `kCLOCK_ExtClk2,`

 `kCLOCK_ExtClk3,`

 `kCLOCK_ExtClk4,`

 `kCLOCK_NoneName }`

 Clock name used to get clock frequency.
- enum `_clock_ip_name` { ,

```
kCLOCK_Debug = CCM_TUPLE(4U, 32U),
kCLOCK_Dram = CCM_TUPLE(5U, 64U),
kCLOCK_Ecspi1 = CCM_TUPLE(7U, 101U),
kCLOCK_Ecspi2 = CCM_TUPLE(8U, 102U),
kCLOCK_Ecspi3 = CCM_TUPLE(9U, 131U),
kCLOCK_Enet1 = CCM_TUPLE(10U, 17U),
kCLOCK_Gpio1 = CCM_TUPLE(11U, 33U),
kCLOCK_Gpio2 = CCM_TUPLE(12U, 33U),
kCLOCK_Gpio3 = CCM_TUPLE(13U, 33U),
kCLOCK_Gpio4 = CCM_TUPLE(14U, 33U),
kCLOCK_Gpio5 = CCM_TUPLE(15U, 33U),
kCLOCK_Gpt1 = CCM_TUPLE(16U, 107U),
kCLOCK_Gpt2 = CCM_TUPLE(17U, 108U),
kCLOCK_Gpt3 = CCM_TUPLE(18U, 109U),
kCLOCK_Gpt4 = CCM_TUPLE(19U, 110U),
kCLOCK_Gpt5 = CCM_TUPLE(20U, 111U),
kCLOCK_Gpt6 = CCM_TUPLE(21U, 112U),
kCLOCK_I2c1 = CCM_TUPLE(23U, 90U),
kCLOCK_I2c2 = CCM_TUPLE(24U, 91U),
kCLOCK_I2c3 = CCM_TUPLE(25U, 92U),
kCLOCK_I2c4 = CCM_TUPLE(26U, 93U),
kCLOCK_I2c5 = CCM_TUPLE(51U, 73U),
kCLOCK_I2c6 = CCM_TUPLE(52U, 74U),
kCLOCK_Can1 = CCM_TUPLE(53U, 68U),
kCLOCK_Can2 = CCM_TUPLE(54U, 69U),
kCLOCK_Enet_Qos = CCM_TUPLE(59U, 81U),
kCLOCK_Iomux = CCM_TUPLE(27U, 33U),
kCLOCK_Ipmux1 = CCM_TUPLE(28U, 33U),
kCLOCK_Ipmux2 = CCM_TUPLE(29U, 33U),
kCLOCK_Ipmux3 = CCM_TUPLE(30U, 33U),
kCLOCK_Mu = CCM_TUPLE(33U, 33U),
kCLOCK_Ocram = CCM_TUPLE(35U, 33U),
kCLOCK_OcramS = CCM_TUPLE(36U, 32U),
kCLOCK_Pwm1 = CCM_TUPLE(40U, 103U),
kCLOCK_Pwm2 = CCM_TUPLE(41U, 104U),
kCLOCK_Pwm3 = CCM_TUPLE(42U, 105U),
kCLOCK_Pwm4 = CCM_TUPLE(43U, 106U),
kCLOCK_Qspi = CCM_TUPLE(47U, 87U),
kCLOCK_Nand = CCM_TUPLE(48U, 86U),
kCLOCK_Rdc = CCM_TUPLE(49U, 33U),
kCLOCK_Sdma1 = CCM_TUPLE(58U, 33U),
kCLOCK_Sec_Debug = CCM_TUPLE(60U, 33U),
kCLOCK_Sema42_1 = CCM_TUPLE(61U, 33U),
kCLOCK_Sema42_2 = CCM_TUPLE(62U, 33U),
kCLOCK_Sim_enet = CCM_TUPLE(64U, 17U),
kCLOCK_Sim_m = CCM_TUPLE(65U, 32U),
```

```

kCLOCK_Ocram_A = AUDIOMIX_TUPLE(4U, 0U, 0xFFFF) }

CCM CCGR gate control.
• enum _clock_root_control {
    kCLOCK_RootM7,
    kCLOCK_RootHsioAxi,
    kCLOCK_RootMainAxi,
    kCLOCK_RootEnetAxi,
    kCLOCK_RootNandUsdhcBus,
    kCLOCK_RootVpuBus,
    kCLOCK_RootMediaAxi,
    kCLOCK_RootMediaApb,
    kCLOCK_RootHdmiApb,
    kCLOCK_RootNoc = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[26].TARGET_ROO-
T),
    kCLOCK_RootAhb = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[32].TARGET_ROO-
T),
    kCLOCK_RootIpg = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[33].TARGET_ROO-
T),
    kCLOCK_RootAudioAhb,
    kCLOCK_RootAudioIpg,
    kCLOCK_RootDramAlt,
    kCLOCK_RootFlexCan1,
    kCLOCK_RootFlexCan2,
    kCLOCK_RootSai1 = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[75].TARGET_ROO-
T),
    kCLOCK_RootSai2 = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[76].TARGET_ROO-
T),
    kCLOCK_RootSai3 = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[77].TARGET_ROO-
T),
    kCLOCK_RootSai5 = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[79].TARGET_ROO-
T),
    kCLOCK_RootSai6 = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[80].TARGET_ROO-
T),
    kCLOCK_RootSai7 = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[134].TARGET_ROO-
OT),
    kCLOCK_RootEnetQos,
    kCLOCK_RootEnetQosTimer,
    kCLOCK_RootEnetRef = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[83].TARGET_R-
OOT),
    kCLOCK_RootEnetTimer,
    kCLOCK_RootEnetPhy,
    kCLOCK_RootNand = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[86].TARGET_ROO-
OT),
    kCLOCK_RootQspi = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[87].TARGET_ROO-

```

T),
`kCLOCK_RootUsdhc1`,
`kCLOCK_RootUsdhc2`,
`kCLOCK_RootUsdhc3`,
`kCLOCK_RootI2c1` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[90].TARGET_ROOT),
`kCLOCK_RootI2c2` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[91].TARGET_ROOT),
`kCLOCK_RootI2c3` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[92].TARGET_ROOT),
`kCLOCK_RootI2c4` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[93].TARGET_ROOT),
`kCLOCK_RootI2c5` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[73].TARGET_ROOT),
`kCLOCK_RootI2c6` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[74].TARGET_ROOT),
`kCLOCK_RootUart1` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[94].TARGET_ROOT),
`kCLOCK_RootUart2` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[95].TARGET_ROOT),
`kCLOCK_RootUart3` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[96].TARGET_ROOT),
`kCLOCK_RootUart4` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[97].TARGET_ROOT),
`kCLOCK_RootGic` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[100].TARGET_ROOT),
`kCLOCK_RootEspi1`,
`kCLOCK_RootEspi2`,
`kCLOCK_RootEspi3`,
`kCLOCK_RootPwm1` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[103].TARGET_ROOT),
`kCLOCK_RootPwm2` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[104].TARGET_ROOT),
`kCLOCK_RootPwm3` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[105].TARGET_ROOT),
`kCLOCK_RootPwm4` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[106].TARGET_ROOT),
`kCLOCK_RootGpt1` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[107].TARGET_ROOT),
`kCLOCK_RootGpt2` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[108].TARGET_ROOT),
`kCLOCK_RootGpt3` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[109].TARGET_ROOT),
`kCLOCK_RootGpt4` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[110].TARGET_ROOT)

OT),
`kCLOCK_RootGpt5` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[111].TARGET_ROOT),
`kCLOCK_RootGpt6` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[112].TARGET_ROOT),
`kCLOCK_RootWdog` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[114].TARGET_ROOT),
`kCLOCK_RootPdm` = (uintptr_t)CCM_BASE + offsetof(CCM_Type, ROOT[132].TARGET_ROOT) }

ccm root name used to get clock frequency.

- enum `_clock_root` {

kCLOCK_M7ClkRoot = 0,
kCLOCK_HsioAxiClkRoot,
kCLOCK_MainAxiClkRoot,
kCLOCK_EnetAxiClkRoot,
kCLOCK_NandUsdhcBusClkRoot,
kCLOCK_VpuBusClkRoot,
kCLOCK_MediaAxiClkRoot,
kCLOCK_MediaApbClkRoot,
kCLOCK_HdmiApbClkRoot,
kCLOCK_NocClkRoot,
kCLOCK_AhbClkRoot,
kCLOCK_IpgClkRoot,
kCLOCK_AudioAhbClkRoot,
kCLOCK_AudioIpgClkRoot,
kCLOCK_DramAltClkRoot,
kCLOCK_FlexCan1ClkRoot,
kCLOCK_FlexCan2ClkRoot,
kCLOCK_Sai1ClkRoot,
kCLOCK_Sai2ClkRoot,
kCLOCK_Sai3ClkRoot,
kCLOCK_Sai5ClkRoot,
kCLOCK_Sai6ClkRoot,
kCLOCK_Sai7ClkRoot,
kCLOCK_EnetQosClkRoot,
kCLOCK_EnetQosTimerClkRoot,
kCLOCK_EnetRefClkRoot,
kCLOCK_EnetTimerClkRoot,
kCLOCK_EnetPhyClkRoot,
kCLOCK_NandClkRoot,
kCLOCK_QspiClkRoot,
kCLOCK_Usdhc1ClkRoot,
kCLOCK_Usdhc2ClkRoot,
kCLOCK_Usdhc3ClkRoot,
kCLOCK_I2c1ClkRoot,
kCLOCK_I2c2ClkRoot,
kCLOCK_I2c3ClkRoot,
kCLOCK_I2c4ClkRoot,
kCLOCK_I2c5ClkRoot,
kCLOCK_I2c6ClkRoot,
kCLOCK_Uart1ClkRoot,
kCLOCK_Uart2ClkRoot,
kCLOCK_Uart3ClkRoot,
kCLOCK_Uart4ClkRoot,
kCLOCK_GicClkRoot,
kCLOCK_Ecspi1ClkRoot,
kCLOCK_Ecspi2ClkRoot,

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kCLOCK_Pwm1ClkRoot,
kCLOCK_Pwm2ClkRoot,

- ```

kCLOCK_PdmClkRoot }

ccm clock root used to get clock frequency.
• enum _clock_rootmux_m7_clk_sel {
 kCLOCK_M7RootmuxOsc24M = 0U,
 kCLOCK_M7RootmuxSysPll2Div5 = 1U,
 kCLOCK_M7RootmuxSysPll2Div4 = 2U,
 kCLOCK_M7RootmuxSysVpuPll = 3U,
 kCLOCK_M7RootmuxSysPll1 = 4U,
 kCLOCK_M7RootmuxAudioPll1 = 5U,
 kCLOCK_M7RootmuxVideoPll1 = 6U,
 kCLOCK_M7RootmuxSysPll3 = 7U }

Root clock select enumeration for ARM Cortex-M7 core.
• enum _clock_rootmux_axi_clk_sel {
 kCLOCK_AxiRootmuxOsc24M = 0U,
 kCLOCK_AxiRootmuxSysPll2Div3 = 1U,
 kCLOCK_AxiRootmuxSysPll1 = 2U,
 kCLOCK_AxiRootmuxSysPll2Div4 = 3U,
 kCLOCK_AxiRootmuxSysPll2 = 4U,
 kCLOCK_AxiRootmuxAudioPll1 = 5U,
 kCLOCK_AxiRootmuxVideoPll1 = 6U,
 kCLOCK_AxiRootmuxSysPll1Div8 = 7U }

Root clock select enumeration for MAIN AXI bus.
• enum _clock_rootmux_ahb_clk_sel {
 kCLOCK_AhbRootmuxOsc24M = 0U,
 kCLOCK_AhbRootmuxSysPll1Div6 = 1U,
 kCLOCK_AhbRootmuxSysPll1 = 2U,
 kCLOCK_AhbRootmuxSysPll1Div2 = 3U,
 kCLOCK_AhbRootmuxSysPll2Div8 = 4U,
 kCLOCK_AhbRootmuxSysPll3 = 5U,
 kCLOCK_AhbRootmuxAudioPll1 = 6U,
 kCLOCK_AhbRootmuxVideoPll1 = 7U }

Root clock select enumeration for AHB bus.
• enum _clock_rootmux_audio_ahb_clk_sel {
 kCLOCK_AudioAhbRootmuxOsc24M = 0U,
 kCLOCK_AudioAhbRootmuxSysPll2Div2 = 1U,
 kCLOCK_AudioAhbRootmuxSysPll1 = 2U,
 kCLOCK_AudioAhbRootmuxSysPll2 = 3U,
 kCLOCK_AudioAhbRootmuxSysPll2Div6 = 4U,
 kCLOCK_AudioAhbRootmuxSysPll3 = 5U,
 kCLOCK_AudioAhbRootmuxAudioPll1 = 6U,
 kCLOCK_AudioAhbRootmuxVideoPll1 = 7U }

Root clock select enumeration for Audio AHB bus.
• enum _clock_rootmux_qspi_clk_sel {

```

```
kCLOCK_QspiRootmuxOsc24M = 0U,
kCLOCK_QspiRootmuxSysPll1Div2 = 1U,
kCLOCK_QspiRootmuxSysPll2Div3 = 2U,
kCLOCK_QspiRootmuxSysPll2Div2 = 3U,
kCLOCK_QspiRootmuxAudioPll2 = 4U,
kCLOCK_QspiRootmuxSysPll1Div3 = 5U,
kCLOCK_QspiRootmuxSysPll3 = 6,
kCLOCK_QspiRootmuxSysPll1Div8 = 7U }
```

*Root clock select enumeration for QSPI peripheral.*

- enum `_clock_rootmux_ecspi_clk_sel` {
   
kCLOCK\_EcspiRootmuxOsc24M = 0U,
   
kCLOCK\_EcspiRootmuxSysPll2Div5 = 1U,
   
kCLOCK\_EcspiRootmuxSysPll1Div20 = 2U,
   
kCLOCK\_EcspiRootmuxSysPll1Div5 = 3U,
   
kCLOCK\_EcspiRootmuxSysPll1 = 4U,
   
kCLOCK\_EcspiRootmuxSysPll3 = 5U,
   
kCLOCK\_EcspiRootmuxSysPll2Div4 = 6U,
   
kCLOCK\_EcspiRootmuxAudioPll2 = 7U }

*Root clock select enumeration for ECSPI peripheral.*

- enum `_clock_rootmux_enet_axi_clk_sel` {
   
kCLOCK\_EnetAxiRootmuxOsc24M = 0U,
   
kCLOCK\_EnetAxiRootmuxSysPll1Div3 = 1U,
   
kCLOCK\_EnetAxiRootmuxSysPll1 = 2U,
   
kCLOCK\_EnetAxiRootmuxSysPll2Div4 = 3U,
   
kCLOCK\_EnetAxiRootmuxSysPll2Div5 = 4U,
   
kCLOCK\_EnetAxiRootmuxAudioPll1 = 5U,
   
kCLOCK\_EnetAxiRootmuxVideoPll1 = 6U,
   
kCLOCK\_EnetAxiRootmuxSysPll3 = 7U }

*Root clock select enumeration for ENET AXI bus.*

- enum `_clock_rootmux_enet_qos_clk_sel` {
   
kCLOCK\_EnetQosRootmuxOsc24M = 0U,
   
kCLOCK\_EnetQosRootmuxSysPll2Div8 = 1U,
   
kCLOCK\_EnetQosRootmuxSysPll2Div20 = 2U,
   
kCLOCK\_EnetQosRootmuxSysPll2Div10 = 3U,
   
kCLOCK\_EnetQosRootmuxSysPll1Div5 = 4U,
   
kCLOCK\_EnetQosRootmuxAudioPll1 = 5U,
   
kCLOCK\_EnetQosRootmuxVideoPll1 = 6U,
   
kCLOCK\_EnetQosRootmuxExtClk4 = 7U }

*Root clock select enumeration for ENET QOS Clck.*

- enum `_clock_rootmux_enet_ref_clk_sel` {

```
kCLOCK_EnetRefRootmuxOsc24M = 0U,
kCLOCK_EnetRefRootmuxSysPll2Div8 = 1U,
kCLOCK_EnetRefRootmuxSysPll2Div20 = 2U,
kCLOCK_EnetRefRootmuxSysPll2Div10 = 3U,
kCLOCK_EnetRefRootmuxSysPll1Div5 = 4U,
kCLOCK_EnetRefRootmuxAudioPll1 = 5U,
kCLOCK_EnetRefRootmuxVideoPll1 = 6U,
kCLOCK_EnetRefRootmuxExtClk4 = 7U }
```

*Root clock select enumeration for ENET REF Clck.*

- enum `_clock_rootmux_enet_qos_timer_clk_sel` {
   
kCLOCK\_EnetQosTimerRootmuxOsc24M = 0U,
   
kCLOCK\_EnetQosTimerRootmuxSysPll2Div10 = 1U,
   
kCLOCK\_EnetQosTimerRootmuxAudioPll1 = 2U,
   
kCLOCK\_EnetQosTimerRootmuxExtClk1 = 3U,
   
kCLOCK\_EnetQosTimerRootmuxExtClk2 = 4U,
   
kCLOCK\_EnetQosTimerRootmuxExtClk3 = 5U,
   
kCLOCK\_EnetQosTimerRootmuxExtClk4 = 6U,
   
kCLOCK\_EnetQosTimerRootmuxVideoPll1 = 7U }

*Root clock select enumeration for ENET QOS TIMER Clck.*

- enum `_clock_rootmux_enet_timer_clk_sel` {
   
kCLOCK\_EnetTimerRootmuxOsc24M = 0U,
   
kCLOCK\_EnetTimerRootmuxSysPll2Div10 = 1U,
   
kCLOCK\_EnetTimerRootmuxAudioPll1 = 2U,
   
kCLOCK\_EnetTimerRootmuxExtClk1 = 3U,
   
kCLOCK\_EnetTimerRootmuxExtClk2 = 4U,
   
kCLOCK\_EnetTimerRootmuxExtClk3 = 5U,
   
kCLOCK\_EnetTimerRootmuxExtClk4 = 6U,
   
kCLOCK\_EnetTimerRootmuxVideoPll1 = 7U }

*Root clock select enumeration for ENET TIMER Clck.*

- enum `_clock_rootmux_enet_phy_clk_sel` {
   
kCLOCK\_EnetPhyRootmuxOsc24M = 0U,
   
kCLOCK\_EnetPhyRootmuxSysPll2Div20 = 1U,
   
kCLOCK\_EnetPhyRootmuxSysPll2Div8 = 2U,
   
kCLOCK\_EnetPhyRootmuxSysPll2Div5 = 3U,
   
kCLOCK\_EnetPhyRootmuxSysPll2Div2 = 4U,
   
kCLOCK\_EnetPhyRootmuxAudioPll1 = 5U,
   
kCLOCK\_EnetPhyRootmuxVideoPll1 = 6U,
   
kCLOCK\_EnetPhyRootmuxAudioPll2 = 7U }

*Root clock select enumeration for ENET PHY Clck.*

- enum `_clock_rootmux_flexcan_clk_sel` {

```
kCLOCK_FlexCanRootmuxOsc24M = 0U,
kCLOCK_FlexCanRootmuxSysPll2Div5 = 1U,
kCLOCK_FlexCanRootmuxSysPll1Div20 = 2U,
kCLOCK_FlexCanRootmuxSysPll1Div5 = 3U,
kCLOCK_FlexCanRootmuxSysPll1 = 4U,
kCLOCK_FlexCanRootmuxSysPll3 = 5U,
kCLOCK_FlexCanRootmuxSysPll2Div4 = 6U,
kCLOCK_FlexCanRootmuxAudioPll2 = 7U }
```

*Root clock select enumeration for FLEXCAN peripheral.*

- enum `_clock_rootmux_i2c_clk_sel` {
 

```
kCLOCK_I2cRootmuxOsc24M = 0U,
kCLOCK_I2cRootmuxSysPll1Div5 = 1U,
kCLOCK_I2cRootmuxSysPll2Div20 = 2U,
kCLOCK_I2cRootmuxSysPll3 = 3U,
kCLOCK_I2cRootmuxAudioPll1 = 4U,
kCLOCK_I2cRootmuxVideoPll1 = 5U,
kCLOCK_I2cRootmuxAudioPll2 = 6U,
kCLOCK_I2cRootmuxSysPll1Div6 = 7U }
```

*Root clock select enumeration for I2C peripheral.*

- enum `_clock_rootmux_uart_clk_sel` {
 

```
kCLOCK_UartRootmuxOsc24M = 0U,
kCLOCK_UartRootmuxSysPll1Div10 = 1U,
kCLOCK_UartRootmuxSysPll2Div5 = 2U,
kCLOCK_UartRootmuxSysPll2Div10 = 3U,
kCLOCK_UartRootmuxSysPll3 = 4U,
kCLOCK_UartRootmuxExtClk2 = 5U,
kCLOCK_UartRootmuxExtClk34 = 6U,
kCLOCK_UartRootmuxAudioPll2 = 7U }
```

*Root clock select enumeration for UART peripheral.*

- enum `_clock_rootmux_gpt` {
 

```
kCLOCK_GptRootmuxOsc24M = 0U,
kCLOCK_GptRootmuxSystemPll2Div10 = 1U,
kCLOCK_GptRootmuxSysPll1Div2 = 2U,
kCLOCK_GptRootmuxSysPll1Div20 = 3U,
kCLOCK_GptRootmuxVideoPll1 = 4U,
kCLOCK_GptRootmuxSystemPll1Div10 = 5U,
kCLOCK_GptRootmuxAudioPll1 = 6U,
kCLOCK_GptRootmuxExtClk123 = 7U }
```

*Root clock select enumeration for GPT peripheral.*

- enum `_clock_rootmux_wdog_clk_sel` {

```
kCLOCK_WdogRootmuxOsc24M = 0U,
kCLOCK_WdogRootmuxSysPlI1Div6 = 1U,
kCLOCK_WdogRootmuxSysPlI1Div5 = 2U,
kCLOCK_WdogRootmuxVpuPlI = 3U,
kCLOCK_WdogRootmuxSystemPlI2Div8 = 4U,
kCLOCK_WdogRootmuxSystemPlI3 = 5U,
kCLOCK_WdogRootmuxSystemPlI1Div10 = 6U,
kCLOCK_WdogRootmuxSystemPlI2Div6 = 7U }
```

*Root clock select enumeration for WDOG peripheral.*

- enum `_clock_rootmux_pwm_clk_sel` {
 

```
kCLOCK_PwmRootmuxOsc24M = 0U,
kCLOCK_PwmRootmuxSysPlI2Div10 = 1U,
kCLOCK_PwmRootmuxSysPlI1Div5 = 2U,
kCLOCK_PwmRootmuxSysPlI1Div20 = 3U,
kCLOCK_PwmRootmuxSystemPlI3 = 4U,
kCLOCK_PwmRootmuxExtClk12 = 5U,
kCLOCK_PwmRootmuxSystemPlI1Div10 = 6U,
kCLOCK_PwmRootmuxVideoPlI1 = 7U }
```

*Root clock select enumeration for PWM peripheral.*

- enum `_clock_rootmux_sai_clk_sel` {
 

```
kCLOCK_SaiRootmuxOsc24M = 0U,
kCLOCK_SaiRootmuxAudioPlI1 = 1U,
kCLOCK_SaiRootmuxAudioPlI2 = 2U,
kCLOCK_SaiRootmuxVideoPlI1 = 3U,
kCLOCK_SaiRootmuxSysPlI1Div6 = 4U,
kCLOCK_SaiRootmuxOsc26m = 5U,
kCLOCK_SaiRootmuxExtClk1 = 6U,
kCLOCK_SaiRootmuxExtClk2 = 7U }
```

*Root clock select enumeration for SAI peripheral.*

- enum `_clock_rootmux_pdm_clk_sel` {
 

```
kCLOCK_PdmRootmuxOsc24M = 0U,
kCLOCK_PdmRootmuxSysPlI2Div10 = 1U,
kCLOCK_PdmRootmuxAudioPlI1 = 2U,
kCLOCK_PdmRootmuxSysPlI1 = 3U,
kCLOCK_PdmRootmuxSysPlI2 = 4U,
kCLOCK_PdmRootmuxSysPlI3 = 5U,
kCLOCK_PdmRootmuxExtClk3 = 6U,
kCLOCK_PdmRootmuxAudioPlI2 = 7U }
```

*Root clock select enumeration for PDM peripheral.*

- enum `_clock_rootmux_noc_clk_sel` {

```
kCLOCK_NocRootmuxOsc24M = 0U,
kCLOCK_NocRootmuxSysPll1 = 1U,
kCLOCK_NocRootmuxSysPll3 = 2U,
kCLOCK_NocRootmuxSysPll2 = 3U,
kCLOCK_NocRootmuxSysPll2Div2 = 4U,
kCLOCK_NocRootmuxAudioPll1 = 5U,
kCLOCK_NocRootmuxVideoPll1 = 6U,
kCLOCK_NocRootmuxAudioPll2 = 7U }
```

*Root clock select enumeration for NOC CLK.*

- enum `_clock_pll_gate` {
   
`kCLOCK_ArmPllGate` = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[12].PLL\_C-TRL),
   
`kCLOCK_GpuPllGate` = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[13].PLL\_C-TRL),
   
`kCLOCK_VpuPllGate` = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[14].PLL\_C-TRL),
   
`kCLOCK_DramPllGate` = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[15].PLL\_C-TRL),
   
`kCLOCK_SysPll1Gate` = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[16].PLL\_C-TRL),
   
`kCLOCK_SysPll1Div2Gate`,
   
`kCLOCK_SysPll1Div3Gate`,
   
`kCLOCK_SysPll1Div4Gate`,
   
`kCLOCK_SysPll1Div5Gate`,
   
`kCLOCK_SysPll1Div6Gate`,
   
`kCLOCK_SysPll1Div8Gate`,
   
`kCLOCK_SysPll1Div10Gate`,
   
`kCLOCK_SysPll1Div20Gate`,
   
`kCLOCK_SysPll2Gate` = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[25].PLL\_C-TRL),
   
`kCLOCK_SysPll2Div2Gate`,
   
`kCLOCK_SysPll2Div3Gate`,
   
`kCLOCK_SysPll2Div4Gate`,
   
`kCLOCK_SysPll2Div5Gate`,
   
`kCLOCK_SysPll2Div6Gate`,
   
`kCLOCK_SysPll2Div8Gate`,
   
`kCLOCK_SysPll2Div10Gate`,
   
`kCLOCK_SysPll2Div20Gate`,
   
`kCLOCK_SysPll3Gate` = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[34].PLL\_C-TRL),
   
`kCLOCK_AudioPll1Gate` = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[35].PLL\_C-CTRL),
   
`kCLOCK_AudioPll2Gate` = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[36].PLL\_C-CTRL),
   
`kCLOCK_VideoPll1Gate` = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[37].PLL\_C-CTRL)
 }

- CTRL),  
**kCLOCK\_VideoPll2Gate** = (uintptr\_t)CCM\_BASE + offsetof(CCM\_Type, PLL\_CTRL[38].PLL\_-  
CTRL) }
- CCM PLL gate control.*
- enum **\_clock\_gate\_value** {
 **kCLOCK\_ClockNotNeeded** = 0x0U,  
**kCLOCK\_ClockNeededRun** = 0x1111U,  
**kCLOCK\_ClockNeededRunWait** = 0x2222U,  
**kCLOCK\_ClockNeededAll** = 0x3333U }
- CCM gate control value.*
- enum **\_clock\_pll\_bypass\_ctrl** {
 **kCLOCK\_AudioPll1BypassCtrl**,  
**kCLOCK\_AudioPll2BypassCtrl**,  
**kCLOCK\_VideoPll1BypassCtrl**,  
**kCLOCK\_DramPllInternalPll1BypassCtrl**,  
**kCLOCK\_ArmPllPwrBypassCtrl**,  
**kCLOCK\_SysPll1InternalPll1BypassCtrl**,  
**kCLOCK\_SysPll2InternalPll1BypassCtrl**,  
**kCLOCK\_SysPll3InternalPll1BypassCtrl** }
- PLL control names for PLL bypass.*
- enum **\_ccm\_analog\_pll\_clke** {
 **kCLOCK\_AudioPll1Clke**,  
**kCLOCK\_AudioPll2Clke**,  
**kCLOCK\_VideoPll1Clke**,  
**kCLOCK\_DramPllClke**,  
**kCLOCK\_ArmPllClke**,  
**kCLOCK\_SystemPll1Clke**,  
**kCLOCK\_SystemPll1Div2Clke**,  
**kCLOCK\_SystemPll1Div3Clke**,  
**kCLOCK\_SystemPll1Div4Clke**,  
**kCLOCK\_SystemPll1Div5Clke**,  
**kCLOCK\_SystemPll1Div6Clke**,  
**kCLOCK\_SystemPll1Div8Clke**,  
**kCLOCK\_SystemPll1Div10Clke**,  
**kCLOCK\_SystemPll1Div20Clke**,  
**kCLOCK\_SystemPll2Clke**,  
**kCLOCK\_SystemPll2Div2Clke**,  
**kCLOCK\_SystemPll2Div3Clke**,  
**kCLOCK\_SystemPll2Div4Clke**,  
**kCLOCK\_SystemPll2Div5Clke**,  
**kCLOCK\_SystemPll2Div6Clke**,  
**kCLOCK\_SystemPll2Div8Clke**,  
**kCLOCK\_SystemPll2Div10Clke**,  
**kCLOCK\_SystemPll2Div20Clke**,  
**kCLOCK\_SystemPll3Clke** }

- *PLL clock names for clock enable/disable settings.*
- enum `_clock_pll_ctrl`  
*ANALOG Power down override control.*
- enum {  
  `kANALOG_PlIRefOsc24M` = 0U,  
  `kANALOG_PlIPadClk` = 1U }  
*PLL reference clock select.*

## Driver version

- `#define FSL_CLOCK_DRIVER_VERSION (MAKE_VERSION(2, 2, 0))`  
*CLOCK driver version 2.2.0.*

## CCM Root Clock Setting

- static void `CLOCK_SetRootMux (clock_root_control_t rootClk, uint32_t mux)`  
*Set clock root mux.*
- static uint32\_t `CLOCK_GetRootMux (clock_root_control_t rootClk)`  
*Get clock root mux.*
- static void `CLOCK_EnableRoot (clock_root_control_t rootClk)`  
*Enable clock root.*
- static void `CLOCK_DisableRoot (clock_root_control_t rootClk)`  
*Disable clock root.*
- static bool `CLOCK_IsRootEnabled (clock_root_control_t rootClk)`  
*Check whether clock root is enabled.*
- void `CLOCK_UpdateRoot (clock_root_control_t ccmRootClk, uint32_t mux, uint32_t pre, uint32_t post)`  
*Update clock root in one step, for dynamical clock switching Note: The PRE and POST dividers in this function are the actually divider, software will map it to register value.*
- void `CLOCK_SetRootDivider (clock_root_control_t ccmRootClk, uint32_t pre, uint32_t post)`  
*Set root clock divider Note: The PRE and POST dividers in this function are the actually divider, software will map it to register value.*
- static uint32\_t `CLOCK_GetRootPreDivider (clock_root_control_t rootClk)`  
*Get clock root PRE\_PODF.*
- static uint32\_t `CLOCK_GetRootPostDivider (clock_root_control_t rootClk)`  
*Get clock root POST\_PODF.*

## CCM Gate Control

- static void `CLOCK_ControlGate (uintptr_t ccmGate, clock_gate_value_t control)`  
*Set PLL or CCGR gate control.*
- void `CLOCK_EnableClock (clock_ip_name_t ccmGate)`  
*Enable CCGR clock gate and root clock gate for each module User should set specific gate for each module according to the description of the table of system clocks, gating and override in CCM chapter of reference manual.*
- void `CLOCK_DisableClock (clock_ip_name_t ccmGate)`  
*Disable CCGR clock gate for the each module User should set specific gate for each module according to the description of the table of system clocks, gating and override in CCM chapter of reference manual.*

## CCM Analog PLL Operation Functions

- static void **CLOCK\_PowerUpPll** (CCM\_ANALOG\_Type \*base, **clock\_pll\_ctrl\_t** pllControl)
 

*Power up PLL.*
- static void **CLOCK\_PowerDownPll** (CCM\_ANALOG\_Type \*base, **clock\_pll\_ctrl\_t** pllControl)
 

*Power down PLL.*
- static void **CLOCK\_SetPllBypass** (CCM\_ANALOG\_Type \*base, **clock\_pll\_bypass\_ctrl\_t** pllControl, bool bypass)
 

*PLL bypass setting.*
- static bool **CLOCK\_IsPllBypassed** (CCM\_ANALOG\_Type \*base, **clock\_pll\_bypass\_ctrl\_t** pllControl)
 

*Check if PLL is bypassed.*
- static bool **CLOCK\_IsPllLocked** (CCM\_ANALOG\_Type \*base, **clock\_pll\_ctrl\_t** pllControl)
 

*Check if PLL clock is locked.*
- static void **CLOCK\_EnableAnalogClock** (CCM\_ANALOG\_Type \*base, **clock\_pll\_clke\_t** pllClock)
 

*Enable PLL clock.*
- static void **CLOCK\_DisableAnalogClock** (CCM\_ANALOG\_Type \*base, **clock\_pll\_clke\_t** pllClock)
 

*Disable PLL clock.*
- static void **CLOCK\_OverridePllClke** (CCM\_ANALOG\_Type \*base, **clock\_pll\_clke\_t** ovClock, bool override)
 

*Override PLL clock output enable.*
- static void **CLOCK\_OverridePllPd** (CCM\_ANALOG\_Type \*base, **clock\_pll\_ctrl\_t** pdClock, bool override)
 

*Override PLL power down.*
- void **CLOCK\_InitArmPll** (const **ccm\_analog\_integer\_pll\_config\_t** \*config)
 

*Initializes the ANALOG ARM PLL.*
- void **CLOCK\_DeinitArmPll** (void)
 

*De-initialize the ARM PLL.*
- void **CLOCK\_InitSysPll1** (const **ccm\_analog\_integer\_pll\_config\_t** \*config)
 

*Initializes the ANALOG SYS PLL1.*
- void **CLOCK\_DeinitSysPll1** (void)
 

*De-initialize the System PLL1.*
- void **CLOCK\_InitSysPll2** (const **ccm\_analog\_integer\_pll\_config\_t** \*config)
 

*Initializes the ANALOG SYS PLL2.*
- void **CLOCK\_DeinitSysPll2** (void)
 

*De-initialize the System PLL2.*
- void **CLOCK\_InitSysPll3** (const **ccm\_analog\_integer\_pll\_config\_t** \*config)
 

*Initializes the ANALOG SYS PLL3.*
- void **CLOCK\_DeinitSysPll3** (void)
 

*De-initialize the System PLL3.*
- void **CLOCK\_InitAudioPll1** (const **ccm\_analog\_frac\_pll\_config\_t** \*config)
 

*Initializes the ANALOG AUDIO PLL1.*
- void **CLOCK\_DeinitAudioPll1** (void)
 

*De-initialize the Audio PLL1.*
- void **CLOCK\_InitAudioPll2** (const **ccm\_analog\_frac\_pll\_config\_t** \*config)
 

*Initializes the ANALOG AUDIO PLL2.*
- void **CLOCK\_DeinitAudioPll2** (void)
 

*De-initialize the Audio PLL2.*
- void **CLOCK\_InitVideoPll1** (const **ccm\_analog\_frac\_pll\_config\_t** \*config)

- `void CLOCK_DeinitVideoPll1 (void)`  
*De-initialize the Video PLL.*
- `void CLOCK_InitIntegerPll (CCM_ANALOG_Type *base, const ccm_analog_integer_pll_config_t *config, clock_pll_ctrl_t type)`  
*Initializes the ANALOG Integer PLL.*
- `uint32_t CLOCK_GetIntegerPllFreq (CCM_ANALOG_Type *base, clock_pll_ctrl_t type, uint32_t refClkFreq, bool pll1Bypass)`  
*Get the ANALOG Integer PLL clock frequency.*
- `void CLOCK_InitFracPll (CCM_ANALOG_Type *base, const ccm_analog_frac_pll_config_t *config, clock_pll_ctrl_t type)`  
*Initializes the ANALOG Fractional PLL.*
- `uint32_t CLOCK_GetFracPllFreq (CCM_ANALOG_Type *base, clock_pll_ctrl_t type, uint32_t refClkFreq)`  
*Gets the ANALOG Fractional PLL clock frequency.*
- `uint32_t CLOCK_GetPllFreq (clock_pll_ctrl_t pll)`  
*Gets PLL clock frequency.*
- `uint32_t CLOCK_GetPllRefClkFreq (clock_pll_ctrl_t ctrl)`  
*Gets PLL reference clock frequency.*

## CCM Get frequency

- `uint32_t CLOCK_GetFreq (clock_name_t clockName)`  
*Gets the clock frequency for a specific clock name.*
- `uint32_t CLOCK_GetClockRootFreq (clock_root_t clockRoot)`  
*Gets the frequency of selected clock root.*
- `uint32_t CLOCK_GetCoreM7Freq (void)`  
*Get the CCM Cortex M7 core frequency.*
- `uint32_t CLOCK_GetAxiFreq (void)`  
*Get the CCM Axi bus frequency.*
- `uint32_t CLOCK_GetAhbFreq (void)`  
*Get the CCM Ahb bus frequency.*
- `uint32_t CLOCK_GetEnetAxiFreq (void)`  
*brief Get the CCM Enet AXI bus frequency.*

## 5.2 Data Structure Documentation

### 5.2.1 struct \_ccm\_analog\_frac\_pll\_config

Note: all the dividers in this configuration structure are the actually divider, software will map it to register value

## Data Fields

- `uint8_t refSel`  
*pll reference clock sel*
- `uint32_t mainDiv`  
*Value of the 10-bit programmable main-divider, range must be 64~1023.*

- `uint32_t dsm`  
*Value of 16-bit DSM.*
- `uint8_t preDiv`  
*Value of the 6-bit programmable pre-divider, range must be 1~63.*
- `uint8_t postDiv`  
*Value of the 3-bit programmable Scaler, range must be 0~6.*

## 5.2.2 struct \_ccm\_analog\_integer\_pll\_config

Note: all the dividers in this configuration structure are the actually divider, software will map it to register value

### Data Fields

- `uint8_t refSel`  
*pll reference clock sel*
- `uint32_t mainDiv`  
*Value of the 10-bit programmable main-divider, range must be 64~1023.*
- `uint8_t preDiv`  
*Value of the 6-bit programmable pre-divider, range must be 1~63.*
- `uint8_t postDiv`  
*Value of the 3-bit programmable Scaler, range must be 0~6.*

## 5.3 Macro Definition Documentation

### 5.3.1 #define FSL\_CLOCK\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 0))

### 5.3.2 #define ECSPI\_CLOCKS

#### Value:

```
{
 kCLOCK_IpInvalid, kCLOCK_Ecspil, kCLOCK_Ecspi2,
 kCLOCK_Ecspi3, \
}
```

### 5.3.3 #define EDMA\_CLOCKS

#### Value:

```
{
 kCLOCK_Edma, \
}
```

### 5.3.4 #define ENET\_CLOCKS

**Value:**

```
{
 kCLOCK_Enet1, \
}
```

### 5.3.5 #define ENETQOS\_CLOCKS

**Value:**

```
{
 kCLOCK_Enet_Qos \
}
```

### 5.3.6 #define FLEXCAN\_CLOCKS

**Value:**

```
{
 kCLOCK_IpInvalid, kCLOCK_Can1, kCLOCK_Can2, \
}
```

### 5.3.7 #define GPIO\_CLOCKS

**Value:**

```
{
 kCLOCK_IpInvalid, kCLOCK_Gpio1, kCLOCK_Gpio2,
 kCLOCK_Gpio3, kCLOCK_Gpio4, kCLOCK_Gpio5, \
}
```

### 5.3.8 #define GPT\_CLOCKS

**Value:**

```
{
 kCLOCK_IpInvalid, kCLOCK_Gpt1, kCLOCK_Gpt2,
 kCLOCK_Gpt3, kCLOCK_Gpt4, kCLOCK_Gpt5,
 kCLOCK_Gpt6, \
}
```

### 5.3.9 #define I2C\_CLOCKS

**Value:**

```
{
 kCLOCK_IpInvalid, kCLOCK_I2c1, kCLOCK_I2c2,
 kCLOCK_I2c3, kCLOCK_I2c4, kCLOCK_I2c5,
 kCLOCK_I2c6, \
}
```

### 5.3.10 #define IOMUX\_CLOCKS

**Value:**

```
{
 kCLOCK_Iomux, \
}
```

### 5.3.11 #define IPMUX\_CLOCKS

**Value:**

```
{
 kCLOCK_Ipmux1, kCLOCK_Ipmux2,
 kCLOCK_Ipmux3, \
}
```

### 5.3.12 #define PWM\_CLOCKS

**Value:**

```
{
 kCLOCK_IpInvalid, kCLOCK_Pwm1, kCLOCK_Pwm2,
 kCLOCK_Pwm3, kCLOCK_Pwm4, \
}
```

### 5.3.13 #define RDC\_CLOCKS

**Value:**

```
{
 kCLOCK_Rdc, \
}
```

### 5.3.14 #define SAI\_CLOCKS

**Value:**

```
{
 kCLOCK_IpInvalid, kCLOCK_Sai1, kCLOCK_Sai2,
 kCLOCK_Sai3, kCLOCK_IpInvalid, kCLOCK_Sai5, kCLOCK_Sai6,
 \
 kCLOCK_Sai7
}
```

### 5.3.15 #define RDC\_SEMA42\_CLOCKS

**Value:**

```
{
 kCLOCK_IpInvalid, kCLOCK_Sema42_1, kCLOCK_Sema42_2 \
}
```

### 5.3.16 #define UART\_CLOCKS

**Value:**

```
{
 kCLOCK_IpInvalid, kCLOCK_Uart1, kCLOCK_Uart2,
 kCLOCK_Uart3, kCLOCK_Uart4, \
}
```

### 5.3.17 #define USDHC\_CLOCKS

**Value:**

```
{
 kCLOCK_IpInvalid, kCLOCK_Usdhc1, kCLOCK_Usdhc2,
 kCLOCK_Usdhc3 \
}
```

### 5.3.18 #define WDOG\_CLOCKS

**Value:**

```
{
 kCLOCK_IpInvalid, kCLOCK_Wdog1, kCLOCK_Wdog2,
 kCLOCK_Wdog3 \
}
```

### 5.3.19 #define TMU\_CLOCKS

**Value:**

```
{
 kCLOCK_TempSensor, \
}
```

### 5.3.20 #define SDMA\_CLOCKS

**Value:**

```
{
 kCLOCK_Sdma1, kCLOCK_Sdma2, kCLOCK_Sdma3, \
}
```

### 5.3.21 #define MU\_CLOCKS

**Value:**

```
{
 kCLOCK_Mu \
}
```

### 5.3.22 #define QSPI\_CLOCKS

**Value:**

```
{
 kCLOCK_Qspi \
}
```

### 5.3.23 #define PDM\_CLOCKS

**Value:**

```
{
 kCLOCK_Pdm \
}
```

### 5.3.24 #define ASRC\_CLOCKS

**Value:**

```
{
 kCLOCK_Asrc \
}
```

### 5.3.25 #define kCLOCK\_CoreSysClk kCLOCK\_CoreM7Clk

### 5.3.26 #define CLOCK\_GetCoreSysClkFreq CLOCK\_GetCoreM7Freq

## 5.4 Typedef Documentation

5.4.1 **typedef enum \_clock\_name clock\_name\_t**

5.4.2 **typedef enum \_clock\_ip\_name clock\_ip\_name\_t**

5.4.3 **typedef enum \_clock\_root\_control clock\_root\_control\_t**

5.4.4 **typedef enum \_clock\_root clock\_root\_t**

5.4.5 **typedef enum \_clock\_rootmux\_m7\_clk\_sel clock\_rootmux\_m7\_clk\_sel\_t**

5.4.6 **typedef enum \_clock\_rootmux\_axi\_clk\_sel clock\_rootmux\_axi\_clk\_sel\_t**

5.4.7 **typedef enum \_clock\_rootmux\_ahb\_clk\_sel clock\_rootmux\_ahb\_clk\_sel\_t**

5.4.8 **typedef enum \_clock\_rootmux\_audio\_ahb\_clk\_sel clock\_rootmux\_audio\_-ahb\_clk\_sel\_t**

5.4.9 **typedef enum \_clock\_rootmux\_qspi\_clk\_sel clock\_rootmux\_qspi\_clk\_sel\_t**

5.4.10 **typedef enum \_clock\_rootmux\_ecspi\_clk\_sel clock\_rootmux\_ecspi\_clk\_sel\_t**

5.4.11 **typedef enum \_clock\_rootmux\_enet\_axi\_clk\_sel clock\_rootmux\_enet\_axi\_-clk\_sel\_t**

5.4.12 **typedef enum \_clock\_rootmux\_enet\_qos\_clk\_sel clock\_rootmux\_enet\_qos\_-clk\_sel\_t**

5.4.13 **typedef enum \_clock\_rootmux\_enet\_ref\_clk\_sel clock\_rootmux\_enet\_ref\_-clk\_sel\_t**

5.4.14 **typedef enum \_clock\_rootmux\_enet\_qos\_timer\_clk\_sel  
clock\_rootmux\_enet\_qos\_timer\_clk\_sel\_t**

5.4.15 **typedef enum \_clock\_rootmux\_enet\_timer\_clk\_sel clock\_rootmux\_enet\_-timer\_clk\_sel\_t**

5.4.16 **typedef enum \_clock\_rootmux\_enet\_phy\_clk\_sel clock\_rootmux\_enet\_phy\_-clk\_sel\_t**

5.4.17 **typedef enum \_clock\_rootmux\_flexcan\_clk\_sel clock\_rootmux\_flexcan\_clk\_-sel\_t**

- 0:15: REG offset to CCM\_ANALOG\_BASE in bytes.
- 16:20: bypass bit shift.

#### 5.4.29 `typedef enum _ccm_analog_pll_clke clock_pll_clke_t`

These constants define the PLL clock names for PLL clock enable/disable operations.

- 0:15: REG offset to CCM\_ANALOG\_BASE in bytes.
- 16:20: Clock enable bit shift.

#### 5.4.30 `typedef struct _ccm_analog_frac_pll_config ccm_analog_frac_pll_config_t`

Note: all the dividers in this configuration structure are the actually divider, software will map it to register value

#### 5.4.31 `typedef struct _ccm_analog_integer_pll_config ccm_analog_integer_pll_config_t`

Note: all the dividers in this configuration structure are the actually divider, software will map it to register value

### 5.5 Enumeration Type Documentation

#### 5.5.1 `enum _clock_name`

Enumerator

- kCLOCK\_CoreM7Clk* ARM M7 Core clock.
- kCLOCK\_AxiClk* Main AXI bus clock.
- kCLOCK\_AhbClk* AHB bus clock.
- kCLOCK\_IpgClk* IPG bus clock.
- kCLOCK\_PerClk* Peripheral Clock.
- kCLOCK\_EnetIpgClk* ENET IPG Clock.
- kCLOCK\_Osc24MClk* OSC 24M clock.
- kCLOCK\_ArmPllClk* Arm PLL clock.
- kCLOCK\_DramPllClk* Dram PLL clock.
- kCLOCK\_VpuPllClk* Vpu PLL clock.
- kCLOCK\_SysPll1Clk* Sys PLL1 clock.
- kCLOCK\_SysPll1Div2Clk* Sys PLL1 clock divided by 2.
- kCLOCK\_SysPll1Div3Clk* Sys PLL1 clock divided by 3.
- kCLOCK\_SysPll1Div4Clk* Sys PLL1 clock divided by 4.
- kCLOCK\_SysPll1Div5Clk* Sys PLL1 clock divided by 5.
- kCLOCK\_SysPll1Div6Clk* Sys PLL1 clock divided by 6.

*kCLOCK\_SysPll1Div8Clk* Sys PLL1 clock divided by 8.  
*kCLOCK\_SysPll1Div10Clk* Sys PLL1 clock divided by 10.  
*kCLOCK\_SysPll1Div20Clk* Sys PLL1 clock divided by 20.  
*kCLOCK\_SysPll2Clk* Sys PLL2 clock.  
*kCLOCK\_SysPll2Div2Clk* Sys PLL2 clock divided by 2.  
*kCLOCK\_SysPll2Div3Clk* Sys PLL2 clock divided by 3.  
*kCLOCK\_SysPll2Div4Clk* Sys PLL2 clock divided by 4.  
*kCLOCK\_SysPll2Div5Clk* Sys PLL2 clock divided by 5.  
*kCLOCK\_SysPll2Div6Clk* Sys PLL2 clock divided by 6.  
*kCLOCK\_SysPll2Div8Clk* Sys PLL2 clock divided by 8.  
*kCLOCK\_SysPll2Div10Clk* Sys PLL2 clock divided by 10.  
*kCLOCK\_SysPll2Div20Clk* Sys PLL2 clock divided by 20.  
*kCLOCK\_SysPll3Clk* Sys PLL3 clock.  
*kCLOCK\_AudioPll1Clk* Audio PLL1 clock.  
*kCLOCK\_AudioPll2Clk* Audio PLL2 clock.  
*kCLOCK\_VideoPll1Clk* Video PLL1 clock.  
*kCLOCK\_ExtClk1* External clock1.  
*kCLOCK\_ExtClk2* External clock2.  
*kCLOCK\_ExtClk3* External clock3.  
*kCLOCK\_ExtClk4* External clock4.  
*kCLOCK\_NoneName* None Clock Name.

### 5.5.2 enum \_clock\_ip\_name

Enumerator

*kCLOCK\_Debug* DEBUG Clock Gate.  
*kCLOCK\_Dram* DRAM Clock Gate.  
*kCLOCK\_Ecspi1* ECSPI1 Clock Gate.  
*kCLOCK\_Ecspi2* ECSPI2 Clock Gate.  
*kCLOCK\_Ecspi3* ECSPI3 Clock Gate.  
*kCLOCK\_Enet1* ENET1 Clock Gate.  
*kCLOCK\_Gpio1* GPIO1 Clock Gate.  
*kCLOCK\_Gpio2* GPIO2 Clock Gate.  
*kCLOCK\_Gpio3* GPIO3 Clock Gate.  
*kCLOCK\_Gpio4* GPIO4 Clock Gate.  
*kCLOCK\_Gpio5* GPIO5 Clock Gate.  
*kCLOCK\_Gpt1* GPT1 Clock Gate.  
*kCLOCK\_Gpt2* GPT2 Clock Gate.  
*kCLOCK\_Gpt3* GPT3 Clock Gate.  
*kCLOCK\_Gpt4* GPT4 Clock Gate.  
*kCLOCK\_Gpt5* GPT5 Clock Gate.  
*kCLOCK\_Gpt6* GPT6 Clock Gate.  
*kCLOCK\_I2c1* I2C1 Clock Gate.

*kCLOCK\_I2c2* I2C2 Clock Gate.  
*kCLOCK\_I2c3* I2C3 Clock Gate.  
*kCLOCK\_I2c4* I2C4 Clock Gate.  
*kCLOCK\_I2c5* I2C5 Clock Gate.  
*kCLOCK\_I2c6* I2C6 Clock Gate.  
*kCLOCK\_Can1* FlexCAN1 Clock Gate.  
*kCLOCK\_Can2* FlexCAN2 Clock Gate.  
*kCLOCK\_Enet\_Qos* ENET QOS Clock Gate.  
*kCLOCK\_Iomux* IOMUX Clock Gate.  
*kCLOCK\_Ipmux1* IPMUX1 Clock Gate.  
*kCLOCK\_Ipmux2* IPMUX2 Clock Gate.  
*kCLOCK\_Ipmux3* IPMUX3 Clock Gate.  
*kCLOCK\_Mu* MU Clock Gate.  
*kCLOCK\_Ocram* OCRAM Clock Gate.  
*kCLOCK\_OcramS* OCRAM S Clock Gate.  
*kCLOCK\_Pwm1* PWM1 Clock Gate.  
*kCLOCK\_Pwm2* PWM2 Clock Gate.  
*kCLOCK\_Pwm3* PWM3 Clock Gate.  
*kCLOCK\_Pwm4* PWM4 Clock Gate.  
*kCLOCK\_Qspi* QSPI Clock Gate.  
*kCLOCK\_Nand* NAND Clock Gate.  
*kCLOCK\_Rdc* RDC Clock Gate.  
*kCLOCK\_Sdma1* SDMA1 Clock Gate.  
*kCLOCK\_Sec\_Debug* SEC\_DEBUG Clock Gate.  
*kCLOCK\_Sema42\_1* RDC SEMA42 Clock Gate.  
*kCLOCK\_Sema42\_2* RDC SEMA42 Clock Gate.  
*kCLOCK\_Sim\_enet* SIM\_ENET Clock Gate.  
*kCLOCK\_Sim\_m* SIM\_M Clock Gate.  
*kCLOCK\_Sim\_main* SIM\_MAIN Clock Gate.  
*kCLOCK\_Sim\_s* SIM\_S Clock Gate.  
*kCLOCK\_Sim\_wakeup* SIM\_WAKEUP Clock Gate.  
*kCLOCK\_Gpu2D* GPU2D Clock Gate.  
*kCLOCK\_Gpu3D* GPU3D Clock Gate.  
*kCLOCK\_Uart1* UART1 Clock Gate.  
*kCLOCK\_Uart2* UART2 Clock Gate.  
*kCLOCK\_Uart3* UART3 Clock Gate.  
*kCLOCK\_Uart4* UART4 Clock Gate.  
*kCLOCK\_Usdhc1* USDHC1 Clock Gate.  
*kCLOCK\_Usdhc2* USDHC2 Clock Gate.  
*kCLOCK\_Wdog1* WDOG1 Clock Gate.  
*kCLOCK\_Wdog2* WDOG2 Clock Gate.  
*kCLOCK\_Wdog3* WDOG3 Clock Gate.  
*kCLOCK\_Vpu\_G1* VPU\_G1 Clock Gate.  
*kCLOCK\_Gpu* GPU Clock Gate.  
*kCLOCK\_Vpu\_Vc8ke* VPU\_VC8KE Clock Gate.

*kCLOCK\_Vpu\_G2* VPU\_G2 Clock Gate.  
*kCLOCK\_Npu* NPU Clock Gate.  
*kCLOCK\_Hsio* HSIO Clock Gate.  
*kCLOCK\_Media* MEDIA Clock Gate.  
*kCLOCK\_Usdhc3* USDHC3 Clock Gate.  
*kCLOCK\_Hdmi* HDMI Clock Gate.  
*kCLOCK\_TempSensor* TempSensor Clock Gate.  
*kCLOCK\_Audio* AUDIO Clock Gate.  
*kCLOCK\_Earc* EARC clock gate.  
*kCLOCK\_AudioDspDebug* AUDIO DSP DEBUG clock gate.  
*kCLOCK\_AudioDsp* audio dsp clock gate  
*kCLOCK\_Spba2* SPBA2 clock gate.  
*kCLOCK\_Sdma3* SDMA3 clock gate.  
*kCLOCK\_Sdma2* SDMA2 clock gate.  
*kCLOCK\_Pdm* PDM clock gate.  
*kCLOCK\_Asrc* ASRC clock gate.  
*kCLOCK\_Sai7\_Mclk3* SAI7 MCLK3 clock gate.  
*kCLOCK\_Sai7\_Mclk2* SAI7 MCLK2 clock gate.  
*kCLOCK\_Sai7\_Mclk1* SAI7 MCLK1 clock gate.  
*kCLOCK\_Sai7* SAI7 clock gate.  
*kCLOCK\_Sai6\_Mclk3* SAI6 MCLK3 clock gate.  
*kCLOCK\_Sai6\_Mclk2* SAI6 MCLK2 clock gate.  
*kCLOCK\_Sai6\_Mclk1* SAI6 MCLK1 clock gate.  
*kCLOCK\_Sai6* SAI6 clock gate.  
*kCLOCK\_Sai5\_Mclk3* SAI5 MCLK3 clock gate.  
*kCLOCK\_Sai5\_Mclk2* SAI5 MCLK2 clock gate  
*kCLOCK\_Sai5\_Mclk1* SAI5 MCLK1 clock gate.  
*kCLOCK\_Sai5* SAI5 clock gate.  
*kCLOCK\_Sai3\_Mclk3* SAI3 MCLK3 clock gate.  
*kCLOCK\_Sai3\_Mclk2* SAI3 MCLK2 clock gate.  
*kCLOCK\_Sai3\_Mclk1* SAI3 MCLK1 clock gate.  
*kCLOCK\_Sai3* SAI3 clock gate.  
*kCLOCK\_Sai2\_Mclk3* SAI2 MCLK3 clock gate.  
*kCLOCK\_Sai2\_Mclk2* SAI2 MCLK2 clock gate.  
*kCLOCK\_Sai2\_Mclk1* SAI2 MCLK1 clock gate.  
*kCLOCK\_Sai2* SAI2 clock gate.  
*kCLOCK\_Sai1\_Mclk3* SAI1 MCLK3 clock gate.  
*kCLOCK\_Sai1\_Mclk2* SAI1 MCLK2 clock gate.  
*kCLOCK\_Sai1\_Mclk1* SAI1 MCLK1 clock gate.  
*kCLOCK\_Sai1* SAI1 clock gate.  
*kCLOCK\_EarcPhy* EARC PHY clock gate.  
*kCLOCK\_Mu3* MU3 clock gate.  
*kCLOCK\_Mu2* MU2 clock gate.  
*kCLOCK\_Pl* PLL clock gate.  
*kCLOCK\_Edma* EDMA clock gate.

*kCLOCK\_Aud2htx* AUD2HTX clock gate.  
*kCLOCK\_Ocram\_A* OCRAM A clock gate.

### 5.5.3 enum \_clock\_root\_control

Enumerator

*kCLOCK\_RootM7* ARM Cortex-M7 Clock control name.  
*kCLOCK\_RootHsioAxi* HSIO AXI Clock control name.  
*kCLOCK\_RootMainAxi* MAIN AXI Clock control name.  
*kCLOCK\_RootEnetAxi* ENET AXI Clock control name.  
*kCLOCK\_RootNandUsdhcBus* NAND USDHC BUS Clock control name.  
*kCLOCK\_RootVpuBus* VPU BUS Clock control name.  
*kCLOCK\_RootMediaAxi* MEDIA AXI Clock control name.  
*kCLOCK\_RootMediaApb* MEDIA APB Clock control name.  
*kCLOCK\_RootHdmiApb* HDMI APB Clock control name.  
*kCLOCK\_RootNoc* NOC Clock control name.  
*kCLOCK\_RootAhb* AHB Clock control name.  
*kCLOCK\_RootIpq* IPG Clock control name.  
*kCLOCK\_RootAudioAhb* Audio AHB Clock control name.  
*kCLOCK\_RootAudioIpq* Audio IPG Clock control name.  
*kCLOCK\_RootDramAlt* DRAM ALT Clock control name.  
*kCLOCK\_RootFlexCan1* FLEXCAN1 Clock control name.  
*kCLOCK\_RootFlexCan2* FLEXCAN2 Clock control name.  
*kCLOCK\_RootSai1* SAI1 Clock control name.  
*kCLOCK\_RootSai2* SAI2 Clock control name.  
*kCLOCK\_RootSai3* SAI3 Clock control name.  
*kCLOCK\_RootSai5* SAI5 Clock control name.  
*kCLOCK\_RootSai6* SAI6 Clock control name.  
*kCLOCK\_RootSai7* SAI7 Clock control name.  
*kCLOCK\_RootEnetQos* ENET QOS Clock control name.  
*kCLOCK\_RootEnetQosTimer* ENET QOS TIMER Clock control name.  
*kCLOCK\_RootEnetRef* ENET Clock control name.  
*kCLOCK\_RootEnetTimer* ENET TIMER Clock control name.  
*kCLOCK\_RootEnetPhy* ENET PHY Clock control name.  
*kCLOCK\_RootNand* NAND Clock control name.  
*kCLOCK\_RootQspi* QSPI Clock control name.  
*kCLOCK\_RootUsdhc1* USDHC1 Clock control name.  
*kCLOCK\_RootUsdhc2* USDHC2 Clock control name.  
*kCLOCK\_RootUsdhc3* USDHC3 Clock control name.  
*kCLOCK\_RootI2c1* I2C1 Clock control name.  
*kCLOCK\_RootI2c2* I2C2 Clock control name.  
*kCLOCK\_RootI2c3* I2C3 Clock control name.  
*kCLOCK\_RootI2c4* I2C4 Clock control name.

*kCLOCK\_RootI2c5* I2C5 Clock control name.  
*kCLOCK\_RootI2c6* I2C6 Clock control name.  
*kCLOCK\_RootUart1* UART1 Clock control name.  
*kCLOCK\_RootUart2* UART2 Clock control name.  
*kCLOCK\_RootUart3* UART3 Clock control name.  
*kCLOCK\_RootUart4* UART4 Clock control name.  
*kCLOCK\_RootGic* GIC Clock control name.  
*kCLOCK\_RootEcspi1* ECSPi1 Clock control name.  
*kCLOCK\_RootEcspi2* ECSPi2 Clock control name.  
*kCLOCK\_RootEcspi3* ECSPi3 Clock control name.  
*kCLOCK\_RootPwm1* PWM1 Clock control name.  
*kCLOCK\_RootPwm2* PWM2 Clock control name.  
*kCLOCK\_RootPwm3* PWM3 Clock control name.  
*kCLOCK\_RootPwm4* PWM4 Clock control name.  
*kCLOCK\_RootGpt1* GPT1 Clock control name.  
*kCLOCK\_RootGpt2* GPT2 Clock control name.  
*kCLOCK\_RootGpt3* GPT3 Clock control name.  
*kCLOCK\_RootGpt4* GPT4 Clock control name.  
*kCLOCK\_RootGpt5* GPT5 Clock control name.  
*kCLOCK\_RootGpt6* GPT6 Clock control name.  
*kCLOCK\_RootWdog* WDOG Clock control name.  
*kCLOCK\_RootPdm* PDM Clock control name.

#### 5.5.4 enum \_clock\_root

Enumerator

*kCLOCK\_M7ClkRoot* ARM Cortex-M7 Clock control name.  
*kCLOCK\_HsioAxiClkRoot* HSIO AXI Clock control name.  
*kCLOCK\_MainAxiClkRoot* MAIN AXI Clock control name.  
*kCLOCK\_EnetAxiClkRoot* ENET AXI Clock control name.  
*kCLOCK\_NandUsdhcBusClkRoot* NAND USDHC BUS Clock control name.  
*kCLOCK\_VpuBusClkRoot* VPU BUS Clock control name.  
*kCLOCK\_MediaAxiClkRoot* MEDIA AXI Clock control name.  
*kCLOCK\_MediaApbClkRoot* MEDIA APB Clock control name.  
*kCLOCK\_HdmiApbClkRoot* HDMI APB Clock control name.  
*kCLOCK\_NocClkRoot* NOC Clock control name.  
*kCLOCK\_AhbClkRoot* AHB Clock control name.  
*kCLOCK\_IpgClkRoot* IPG Clock control name.  
*kCLOCK\_AudioAhbClkRoot* Audio AHB Clock control name.  
*kCLOCK\_AudioIpgClkRoot* Audio IPG Clock control name.  
*kCLOCK\_DramAltClkRoot* DRAM ALT Clock control name.  
*kCLOCK\_FlexCan1ClkRoot* FLEXCAN1 Clock control name.  
*kCLOCK\_FlexCan2ClkRoot* FLEXCAN2 Clock control name.

***kCLOCK\_Sai1ClkRoot*** SAI1 Clock control name.  
***kCLOCK\_Sai2ClkRoot*** SAI2 Clock control name.  
***kCLOCK\_Sai3ClkRoot*** SAI3 Clock control name.  
***kCLOCK\_Sai5ClkRoot*** SAI5 Clock control name.  
***kCLOCK\_Sai6ClkRoot*** SAI6 Clock control name.  
***kCLOCK\_Sai7ClkRoot*** SAI7 Clock control name.  
***kCLOCK\_EnetQosClkRoot*** ENET QOS Clock control name.  
***kCLOCK\_EnetQosTimerClkRoot*** ENET QOS TIMER Clock control name.  
***kCLOCK\_EnetRefClkRoot*** ENET Clock control name.  
***kCLOCK\_EnetTimerClkRoot*** ENET TIMER Clock control name.  
***kCLOCK\_EnetPhyClkRoot*** ENET PHY Clock control name.  
***kCLOCK\_NandClkRoot*** NAND Clock control name.  
***kCLOCK\_QspiClkRoot*** QSPI Clock control name.  
***kCLOCK\_Usdhc1ClkRoot*** USDHC1 Clock control name.  
***kCLOCK\_Usdhc2ClkRoot*** USDHC2 Clock control name.  
***kCLOCK\_Usdhc3ClkRoot*** USDHC3 Clock control name.  
***kCLOCK\_I2c1ClkRoot*** I2C1 Clock control name.  
***kCLOCK\_I2c2ClkRoot*** I2C2 Clock control name.  
***kCLOCK\_I2c3ClkRoot*** I2C3 Clock control name.  
***kCLOCK\_I2c4ClkRoot*** I2C4 Clock control name.  
***kCLOCK\_I2c5ClkRoot*** I2C5 Clock control name.  
***kCLOCK\_I2c6ClkRoot*** I2C6 Clock control name.  
***kCLOCK\_Uart1ClkRoot*** UART1 Clock control name.  
***kCLOCK\_Uart2ClkRoot*** UART2 Clock control name.  
***kCLOCK\_Uart3ClkRoot*** UART3 Clock control name.  
***kCLOCK\_Uart4ClkRoot*** UART4 Clock control name.  
***kCLOCK\_GicClkRoot*** GIC Clock control name.  
***kCLOCK\_Ecspi1ClkRoot*** ECSPI1 Clock control name.  
***kCLOCK\_Ecspi2ClkRoot*** ECSPI2 Clock control name.  
***kCLOCK\_Ecspi3ClkRoot*** ECSPI3 Clock control name.  
***kCLOCK\_Pwm1ClkRoot*** PWM1 Clock control name.  
***kCLOCK\_Pwm2ClkRoot*** PWM2 Clock control name.  
***kCLOCK\_Pwm3ClkRoot*** PWM3 Clock control name.  
***kCLOCK\_Pwm4ClkRoot*** PWM4 Clock control name.  
***kCLOCK\_Gpt1ClkRoot*** GPT1 Clock control name.  
***kCLOCK\_Gpt2ClkRoot*** GPT2 Clock control name.  
***kCLOCK\_Gpt3ClkRoot*** GPT3 Clock control name.  
***kCLOCK\_Gpt4ClkRoot*** GPT4 Clock control name.  
***kCLOCK\_Gpt5ClkRoot*** GPT5 Clock control name.  
***kCLOCK\_Gpt6ClkRoot*** GPT6 Clock control name.  
***kCLOCK\_WdogClkRoot*** WDOG Clock control name.  
***kCLOCK\_PdmClkRoot*** PDM Clock control name.

### 5.5.5 enum \_clock\_rootmux\_m7\_clk\_sel

Enumerator

*kCLOCK\_M7RootmuxOsc24M* ARM Cortex-M7 Clock from OSC 24M.  
*kCLOCK\_M7RootmuxSysPll2Div5* ARM Cortex-M7 Clock from SYSTEM PLL2 divided by 5.  
*kCLOCK\_M7RootmuxSysPll2Div4* ARM Cortex-M7 Clock from SYSTEM PLL2 divided by 4.  
*kCLOCK\_M7RootmuxSysVpuPll* ARM Cortex-M7 Clock from VPU PLL.  
*kCLOCK\_M7RootmuxSysPll1* ARM Cortex-M7 Clock from SYSTEM PLL1.  
*kCLOCK\_M7RootmuxAudioPll1* ARM Cortex-M7 Clock from AUDIO PLL1.  
*kCLOCK\_M7RootmuxVideoPll1* ARM Cortex-M7 Clock from VIDEO PLL1.  
*kCLOCK\_M7RootmuxSysPll3* ARM Cortex-M7 Clock from SYSTEM PLL3.

### 5.5.6 enum \_clock\_rootmux\_axi\_clk\_sel

Enumerator

*kCLOCK\_AxiRootmuxOsc24M* ARM MAIN AXI Clock from OSC 24M.  
*kCLOCK\_AxiRootmuxSysPll2Div3* ARM MAIN AXI Clock from SYSTEM PLL2 divided by 3.  
*kCLOCK\_AxiRootmuxSysPll1* ARM MAIN AXI Clock from SYSTEM PLL1.  
*kCLOCK\_AxiRootmuxSysPll2Div4* ARM MAIN AXI Clock from SYSTEM PLL2 divided by 4.  
*kCLOCK\_AxiRootmuxSysPll2* ARM MAIN AXI Clock from SYSTEM PLL2.  
*kCLOCK\_AxiRootmuxAudioPll1* ARM MAIN AXI Clock from AUDIO PLL1.  
*kCLOCK\_AxiRootmuxVideoPll1* ARM MAIN AXI Clock from VIDEO PLL1.  
*kCLOCK\_AxiRootmuxSysPll1Div8* ARM MAIN AXI Clock from SYSTEM PLL1 divided by 8.

### 5.5.7 enum \_clock\_rootmux\_ahb\_clk\_sel

Enumerator

*kCLOCK\_AhbRootmuxOsc24M* ARM AHB Clock from OSC 24M.  
*kCLOCK\_AhbRootmuxSysPll1Div6* ARM AHB Clock from SYSTEM PLL1 divided by 6.  
*kCLOCK\_AhbRootmuxSysPll1* ARM AHB Clock from SYSTEM PLL1.  
*kCLOCK\_AhbRootmuxSysPll1Div2* ARM AHB Clock from SYSTEM PLL1 divided by 2.  
*kCLOCK\_AhbRootmuxSysPll2Div8* ARM AHB Clock from SYSTEM PLL2 divided by 8.  
*kCLOCK\_AhbRootmuxSysPll3* ARM AHB Clock from SYSTEM PLL3.  
*kCLOCK\_AhbRootmuxAudioPll1* ARM AHB Clock from AUDIO PLL1.  
*kCLOCK\_AhbRootmuxVideoPll1* ARM AHB Clock from VIDEO PLL1.

### 5.5.8 enum \_clock\_rootmux\_audio\_ahb\_clk\_sel

Enumerator

*kCLOCK\_AudioAhbRootmuxOsc24M* ARM Audio AHB Clock from OSC 24M.

*kCLOCK\_AudioAhbRootmuxSysPll2Div2* ARM Audio AHB Clock from SYSTEM PLL2 divided by 2.

*kCLOCK\_AudioAhbRootmuxSysPll1* ARM Audio AHB Clock from SYSTEM PLL1.

*kCLOCK\_AudioAhbRootmuxSysPll2* ARM Audio AHB Clock from SYSTEM PLL2.

*kCLOCK\_AudioAhbRootmuxSysPll2Div6* ARM Audio AHB Clock from SYSTEM PLL2 divided by 6.

*kCLOCK\_AudioAhbRootmuxSysPll3* ARM Audio AHB Clock from SYSTEM PLL3.

*kCLOCK\_AudioAhbRootmuxAudioPll1* ARM Audio AHB Clock from AUDIO PLL1.

*kCLOCK\_AudioAhbRootmuxVideoPll1* ARM Audio AHB Clock from VIDEO PLL1.

### 5.5.9 enum \_clock\_rootmux\_qspi\_clk\_sel

Enumerator

*kCLOCK\_QspiRootmuxOsc24M* ARM QSPI Clock from OSC 24M.

*kCLOCK\_QspiRootmuxSysPll1Div2* ARM QSPI Clock from SYSTEM PLL1 divided by 2.

*kCLOCK\_QspiRootmuxSysPll2Div3* ARM QSPI Clock from SYSTEM PLL2 divided by 3.

*kCLOCK\_QspiRootmuxSysPll2Div2* ARM QSPI Clock from SYSTEM PLL2 divided by 2.

*kCLOCK\_QspiRootmuxAudioPll2* ARM QSPI Clock from AUDIO PLL2.

*kCLOCK\_QspiRootmuxSysPll1Div3* ARM QSPI Clock from SYSTEM PLL1 divided by 3.

*kCLOCK\_QspiRootmuxSysPll3* ARM QSPI Clock from SYSTEM PLL3.

*kCLOCK\_QspiRootmuxSysPll1Div8* ARM QSPI Clock from SYSTEM PLL1 divided by 8.

### 5.5.10 enum \_clock\_rootmux\_ecspi\_clk\_sel

Enumerator

*kCLOCK\_EcspiRootmuxOsc24M* ECSPI Clock from OSC 24M.

*kCLOCK\_EcspiRootmuxSysPll2Div5* ECSPI Clock from SYSTEM PLL2 divided by 5.

*kCLOCK\_EcspiRootmuxSysPll1Div20* ECSPI Clock from SYSTEM PLL1 divided by 20.

*kCLOCK\_EcspiRootmuxSysPll1Div5* ECSPI Clock from SYSTEM PLL1 divided by 5.

*kCLOCK\_EcspiRootmuxSysPll1* ECSPI Clock from SYSTEM PLL1.

*kCLOCK\_EcspiRootmuxSysPll3* ECSPI Clock from SYSTEM PLL3.

*kCLOCK\_EcspiRootmuxSysPll2Div4* ECSPI Clock from SYSTEM PLL2 divided by 4.

*kCLOCK\_EcspiRootmuxAudioPll2* ECSPI Clock from AUDIO PLL2.

### 5.5.11 enum \_clock\_rootmux\_enet\_axi\_clk\_sel

Enumerator

*kCLOCK\_EnetAxiRootmuxOsc24M* ENET AXI Clock from OSC 24M.  
*kCLOCK\_EnetAxiRootmuxSysPll1Div3* ENET AXI Clock from SYSTEM PLL1 divided by 3.  
*kCLOCK\_EnetAxiRootmuxSysPll1* ENET AXI Clock from SYSTEM PLL1.  
*kCLOCK\_EnetAxiRootmuxSysPll2Div4* ENET AXI Clock from SYSTEM PLL2 divided by 4.  
*kCLOCK\_EnetAxiRootmuxSysPll2Div5* ENET AXI Clock from SYSTEM PLL2 divided by 5.  
*kCLOCK\_EnetAxiRootmuxAudioPll1* ENET AXI Clock from AUDIO PLL1.  
*kCLOCK\_EnetAxiRootmuxVideoPll1* ENET AXI Clock from VIDEO PLL1.  
*kCLOCK\_EnetAxiRootmuxSysPll3* ENET AXI Clock from SYSTEM PLL3.

### 5.5.12 enum \_clock\_rootmux\_enet\_qos\_clk\_sel

Enumerator

*kCLOCK\_EnetQosRootmuxOsc24M* ENET QOS Clock from OSC 24M.  
*kCLOCK\_EnetQosRootmuxSysPll2Div8* ENET QOS Clock from SYSTEM PLL2 divided by 8.  
*kCLOCK\_EnetQosRootmuxSysPll2Div20* ENET QOS Clock from SYSTEM PLL2 divided by 20.  
*kCLOCK\_EnetQosRootmuxSysPll2Div10* ENET QOS Clock from SYSTEM PLL2 divided by 10.  
*kCLOCK\_EnetQosRootmuxSysPll1Div5* ENET QOS Clock from SYSTEM PLL1 divided by 5.  
*kCLOCK\_EnetQosRootmuxAudioPll1* ENET QOS Clock from AUDIO PLL1.  
*kCLOCK\_EnetQosRootmuxVideoPll1* ENET QOS Clock from VIDEO PLL1.  
*kCLOCK\_EnetQosRootmuxExtClk4* ENET QOS Clock from External Clock 4.

### 5.5.13 enum \_clock\_rootmux\_enet\_ref\_clk\_sel

Enumerator

*kCLOCK\_EnetRefRootmuxOsc24M* ENET REF Clock from OSC 24M.  
*kCLOCK\_EnetRefRootmuxSysPll2Div8* ENET REF Clock from SYSTEM PLL2 divided by 8.  
*kCLOCK\_EnetRefRootmuxSysPll2Div20* ENET REF Clock from SYSTEM PLL2 divided by 20.  
*kCLOCK\_EnetRefRootmuxSysPll2Div10* ENET REF Clock from SYSTEM PLL2 divided by 10.  
*kCLOCK\_EnetRefRootmuxSysPll1Div5* ENET REF Clock from SYSTEM PLL1 divided by 5.  
*kCLOCK\_EnetRefRootmuxAudioPll1* ENET REF Clock from AUDIO PLL1.  
*kCLOCK\_EnetRefRootmuxVideoPll1* ENET REF Clock from VIDEO PLL1.  
*kCLOCK\_EnetRefRootmuxExtClk4* ENET REF Clock from External Clock 4.

### 5.5.14 enum \_clock\_rootmux\_enet\_qos\_timer\_clk\_sel

Enumerator

*kCLOCK\_EnetQosTimerRootmuxOsc24M* ENET QOS TIMER Clock from OSC 24M.  
*kCLOCK\_EnetQosTimerRootmuxSysPll2Div10* ENET QOS TIMER Clock from SYSTEM PLL2 divided by 10.  
*kCLOCK\_EnetQosTimerRootmuxAudioPll1* ENET QOS TIMER Clock from AUDIO PLL1.  
*kCLOCK\_EnetQosTimerRootmuxExtClk1* ENET QOS TIMER Clock from External Clock 1.  
*kCLOCK\_EnetQosTimerRootmuxExtClk2* ENET QOS TIMER Clock External Clock 2.  
*kCLOCK\_EnetQosTimerRootmuxExtClk3* ENET QOS TIMER Clock from External Clock 3.  
*kCLOCK\_EnetQosTimerRootmuxExtClk4* ENET QOS TIMER Clock from External Clock 4.  
*kCLOCK\_EnetQosTimerRootmuxVideoPll1* ENET QOS TIMER Clock from VIDEO PLL1.

### 5.5.15 enum \_clock\_rootmux\_enet\_timer\_clk\_sel

Enumerator

*kCLOCK\_EnetTimerRootmuxOsc24M* ENET TIMER Clock from OSC 24M.  
*kCLOCK\_EnetTimerRootmuxSysPll2Div10* ENET TIMER Clock from SYSTEM PLL2 divided by 10.  
*kCLOCK\_EnetTimerRootmuxAudioPll1* ENET TIMER Clock from AUDIO PLL1.  
*kCLOCK\_EnetTimerRootmuxExtClk1* ENET TIMER Clock from External Clock 1.  
*kCLOCK\_EnetTimerRootmuxExtClk2* ENET TIMER Clock External Clock 2.  
*kCLOCK\_EnetTimerRootmuxExtClk3* ENET TIMER Clock from External Clock 3.  
*kCLOCK\_EnetTimerRootmuxExtClk4* ENET TIMER Clock from External Clock 4.  
*kCLOCK\_EnetTimerRootmuxVideoPll1* ENET TIMER Clock from VIDEO PLL1.

### 5.5.16 enum \_clock\_rootmux\_enet\_phy\_clk\_sel

Enumerator

*kCLOCK\_EnetPhyRootmuxOsc24M* ENET PHY Clock from OSC 24M.  
*kCLOCK\_EnetPhyRootmuxSysPll2Div20* ENET PHY Clock from SYSTEM PLL2 divided by 20.  
*kCLOCK\_EnetPhyRootmuxSysPll2Div8* ENET PHY Clock from SYSTEM PLL2 divided by 8.  
*kCLOCK\_EnetPhyRootmuxSysPll2Div5* ENET PHY Clock from SYSTEM PLL2 divided by 5.  
*kCLOCK\_EnetPhyRootmuxSysPll2Div2* ENET PHY Clock from SYSTEM PLL2 divided by 2.  
*kCLOCK\_EnetPhyRootmuxAudioPll1* ENET PHY Clock from AUDIO PLL1.  
*kCLOCK\_EnetPhyRootmuxVideoPll1* ENET PHY Clock from VIDEO PLL1.  
*kCLOCK\_EnetPhyRootmuxAudioPll2* ENET PHY Clock from AUDIO PLL2.

### 5.5.17 enum \_clock\_rootmux\_flexcan\_clk\_sel

Enumerator

*kCLOCK\_FlexCanRootmuxOsc24M* FLEXCAN Clock from OSC 24M.  
*kCLOCK\_FlexCanRootmuxSysPll2Div5* FLEXCAN Clock from SYSTEM PLL2 divided by 5.  
*kCLOCK\_FlexCanRootmuxSysPll1Div20* FLEXCAN Clock from SYSTEM PLL1 divided by 20.  
*kCLOCK\_FlexCanRootmuxSysPll1Div5* FLEXCAN Clock from SYSTEM PLL1 divided by 5.  
*kCLOCK\_FlexCanRootmuxSysPll1* FLEXCAN Clock from SYSTEM PLL1.  
*kCLOCK\_FlexCanRootmuxSysPll3* FLEXCAN Clock from SYSTEM PLL3.  
*kCLOCK\_FlexCanRootmuxSysPll2Div4* FLEXCAN Clock from SYSTEM PLL2 divided by 4.  
*kCLOCK\_FlexCanRootmuxAudioPll2* FLEXCAN Clock from AUDIO PLL2.

### 5.5.18 enum \_clock\_rootmux\_i2c\_clk\_sel

Enumerator

*kCLOCK\_I2cRootmuxOsc24M* I2C Clock from OSC 24M.  
*kCLOCK\_I2cRootmuxSysPll1Div5* I2C Clock from SYSTEM PLL1 divided by 5.  
*kCLOCK\_I2cRootmuxSysPll2Div20* I2C Clock from SYSTEM PLL2 divided by 20.  
*kCLOCK\_I2cRootmuxSysPll3* I2C Clock from SYSTEM PLL3 .  
*kCLOCK\_I2cRootmuxAudioPll1* I2C Clock from AUDIO PLL1.  
*kCLOCK\_I2cRootmuxVideoPll1* I2C Clock from VIDEO PLL1.  
*kCLOCK\_I2cRootmuxAudioPll2* I2C Clock from AUDIO PLL2.  
*kCLOCK\_I2cRootmuxSysPll1Div6* I2C Clock from SYSTEM PLL1 divided by 6.

### 5.5.19 enum \_clock\_rootmux\_uart\_clk\_sel

Enumerator

*kCLOCK\_UartRootmuxOsc24M* UART Clock from OSC 24M.  
*kCLOCK\_UartRootmuxSysPll1Div10* UART Clock from SYSTEM PLL1 divided by 10.  
*kCLOCK\_UartRootmuxSysPll2Div5* UART Clock from SYSTEM PLL2 divided by 5.  
*kCLOCK\_UartRootmuxSysPll2Div10* UART Clock from SYSTEM PLL2 divided by 10.  
*kCLOCK\_UartRootmuxSysPll3* UART Clock from SYSTEM PLL3.  
*kCLOCK\_UartRootmuxExtClk2* UART Clock from External Clock 2.  
*kCLOCK\_UartRootmuxExtClk34* UART Clock from External Clock 3, External Clock 4.  
*kCLOCK\_UartRootmuxAudioPll2* UART Clock from Audio PLL2.

### 5.5.20 enum \_clock\_rootmux\_gpt

Enumerator

*kCLOCK\_GptRootmuxOsc24M* GPT Clock from OSC 24M.  
*kCLOCK\_GptRootmuxSystemPll2Div10* GPT Clock from SYSTEM PLL2 divided by 10.  
*kCLOCK\_GptRootmuxSysPll1Div2* GPT Clock from SYSTEM PLL1 divided by 2.  
*kCLOCK\_GptRootmuxSysPll1Div20* GPT Clock from SYSTEM PLL1 divided by 20.  
*kCLOCK\_GptRootmuxVideoPll1* GPT Clock from VIDEO PLL1.  
*kCLOCK\_GptRootmuxSystemPll1Div10* GPT Clock from SYSTEM PLL1 divided by 10.  
*kCLOCK\_GptRootmuxAudioPll1* GPT Clock from AUDIO PLL1.  
*kCLOCK\_GptRootmuxExtClk123* GPT Clock from External Clock1, External Clock2, External Clock3.

### 5.5.21 enum \_clock\_rootmux\_wdog\_clk\_sel

Enumerator

*kCLOCK\_WdogRootmuxOsc24M* WDOG Clock from OSC 24M.  
*kCLOCK\_WdogRootmuxSysPll1Div6* WDOG Clock from SYSTEM PLL1 divided by 6.  
*kCLOCK\_WdogRootmuxSysPll1Div5* WDOG Clock from SYSTEM PLL1 divided by 5.  
*kCLOCK\_WdogRootmuxVpuPll* WDOG Clock from VPU DLL.  
*kCLOCK\_WdogRootmuxSystemPll2Div8* WDOG Clock from SYSTEM PLL2 divided by 8.  
*kCLOCK\_WdogRootmuxSystemPll3* WDOG Clock from SYSTEM PLL3.  
*kCLOCK\_WdogRootmuxSystemPll1Div10* WDOG Clock from SYSTEM PLL1 divided by 10.  
*kCLOCK\_WdogRootmuxSystemPll2Div6* WDOG Clock from SYSTEM PLL2 divided by 6.

### 5.5.22 enum \_clock\_rootmux\_pwm\_clk\_sel

Enumerator

*kCLOCK\_PwmRootmuxOsc24M* PWM Clock from OSC 24M.  
*kCLOCK\_PwmRootmuxSysPll2Div10* PWM Clock from SYSTEM PLL2 divided by 10.  
*kCLOCK\_PwmRootmuxSysPll1Div5* PWM Clock from SYSTEM PLL1 divided by 5.  
*kCLOCK\_PwmRootmuxSysPll1Div20* PWM Clock from SYSTEM PLL1 divided by 20.  
*kCLOCK\_PwmRootmuxSystemPll3* PWM Clock from SYSTEM PLL3.  
*kCLOCK\_PwmRootmuxExtClk12* PWM Clock from External Clock1, External Clock2.  
*kCLOCK\_PwmRootmuxSystemPll1Div10* PWM Clock from SYSTEM PLL1 divided by 10.  
*kCLOCK\_PwmRootmuxVideoPll1* PWM Clock from VIDEO PLL1.

### 5.5.23 enum \_clock\_rootmux\_sai\_clk\_sel

Enumerator

- kCLOCK\_SaiRootmuxOsc24M*** SAI Clock from OSC 24M.
- kCLOCK\_SaiRootmuxAudioPll1*** SAI Clock from AUDIO PLL1.
- kCLOCK\_SaiRootmuxAudioPll2*** SAI Clock from AUDIO PLL2.
- kCLOCK\_SaiRootmuxVideoPll1*** SAI Clock from VIDEO PLL1.
- kCLOCK\_SaiRootmuxSysPll1Div6*** SAI Clock from SYSTEM PLL1 divided by 6.
- kCLOCK\_SaiRootmuxOsc26m*** SAI Clock from OSC HDMI 26M.
- kCLOCK\_SaiRootmuxExtClk1*** SAI Clock from External Clock1, External Clock2, External Clock3.
- kCLOCK\_SaiRootmuxExtClk2*** SAI Clock from External Clock2, External Clock3, External Clock4.

### 5.5.24 enum \_clock\_rootmux\_pdm\_clk\_sel

Enumerator

- kCLOCK\_PdmRootmuxOsc24M*** PDM Clock from OSC 24M.
- kCLOCK\_PdmRootmuxSysPll2Div10*** PDM Clock from SYSTEM PLL2 divided by 10.
- kCLOCK\_PdmRootmuxAudioPll1*** PDM Clock from AUDIO PLL1.
- kCLOCK\_PdmRootmuxSysPll1*** PDM Clock from SYSTEM PLL1.
- kCLOCK\_PdmRootmuxSysPll2*** PDM Clock from SYSTEM PLL2.
- kCLOCK\_PdmRootmuxSysPll3*** PDM Clock from SYSTEM PLL3.
- kCLOCK\_PdmRootmuxExtClk3*** PDM Clock from External Clock3.
- kCLOCK\_PdmRootmuxAudioPll2*** PDM Clock from AUDIO PLL2.

### 5.5.25 enum \_clock\_rootmux\_noc\_clk\_sel

Enumerator

- kCLOCK\_NocRootmuxOsc24M*** NOC Clock from OSC 24M.
- kCLOCK\_NocRootmuxSysPll1*** NOC Clock from SYSTEM PLL1.
- kCLOCK\_NocRootmuxSysPll3*** NOC Clock from SYSTEM PLL3.
- kCLOCK\_NocRootmuxSysPll2*** NOC Clock from SYSTEM PLL2.
- kCLOCK\_NocRootmuxSysPll2Div2*** NOC Clock from SYSTEM PLL2 divided by 2.
- kCLOCK\_NocRootmuxAudioPll1*** NOC Clock from AUDIO PLL1.
- kCLOCK\_NocRootmuxVideoPll1*** NOC Clock from VIDEO PLL1.
- kCLOCK\_NocRootmuxAudioPll2*** NOC Clock from AUDIO PLL2.

### 5.5.26 enum \_clock\_pll\_gate

Enumerator

*kCLOCK\_ArmPllGate* ARM PLL Gate.  
*kCLOCK\_GpuPllGate* GPU PLL Gate.  
*kCLOCK\_VpuPllGate* VPU PLL Gate.  
*kCLOCK\_DramPllGate* DRAM PLL1 Gate.  
*kCLOCK\_SysPll1Gate* SYSTEM PLL1 Gate.  
*kCLOCK\_SysPll1Div2Gate* SYSTEM PLL1 Div2 Gate.  
*kCLOCK\_SysPll1Div3Gate* SYSTEM PLL1 Div3 Gate.  
*kCLOCK\_SysPll1Div4Gate* SYSTEM PLL1 Div4 Gate.  
*kCLOCK\_SysPll1Div5Gate* SYSTEM PLL1 Div5 Gate.  
*kCLOCK\_SysPll1Div6Gate* SYSTEM PLL1 Div6 Gate.  
*kCLOCK\_SysPll1Div8Gate* SYSTEM PLL1 Div8 Gate.  
*kCLOCK\_SysPll1Div10Gate* SYSTEM PLL1 Div10 Gate.  
*kCLOCK\_SysPll1Div20Gate* SYSTEM PLL1 Div20 Gate.  
*kCLOCK\_SysPll2Gate* SYSTEM PLL2 Gate.  
*kCLOCK\_SysPll2Div2Gate* SYSTEM PLL2 Div2 Gate.  
*kCLOCK\_SysPll2Div3Gate* SYSTEM PLL2 Div3 Gate.  
*kCLOCK\_SysPll2Div4Gate* SYSTEM PLL2 Div4 Gate.  
*kCLOCK\_SysPll2Div5Gate* SYSTEM PLL2 Div5 Gate.  
*kCLOCK\_SysPll2Div6Gate* SYSTEM PLL2 Div6 Gate.  
*kCLOCK\_SysPll2Div8Gate* SYSTEM PLL2 Div8 Gate.  
*kCLOCK\_SysPll2Div10Gate* SYSTEM PLL2 Div10 Gate.  
*kCLOCK\_SysPll2Div20Gate* SYSTEM PLL2 Div20 Gate.  
*kCLOCK\_SysPll3Gate* SYSTEM PLL3 Gate.  
*kCLOCK\_AudioPll1Gate* AUDIO PLL1 Gate.  
*kCLOCK\_AudioPll2Gate* AUDIO PLL2 Gate.  
*kCLOCK\_VideoPll1Gate* VIDEO PLL1 Gate.  
*kCLOCK\_VideoPll2Gate* VIDEO PLL2 Gate.

### 5.5.27 enum \_clock\_gate\_value

Enumerator

*kCLOCK\_ClockNotNeeded* Clock always disabled.  
*kCLOCK\_ClockNeededRun* Clock enabled when CPU is running.  
*kCLOCK\_ClockNeededRunWait* Clock enabled when CPU is running or in WAIT mode.  
*kCLOCK\_ClockNeededAll* Clock always enabled.

### 5.5.28 enum \_clock\_pll\_bypass\_ctrl

These constants define the PLL control names for PLL bypass.

- 0:15: REG offset to CCM\_ANALOG\_BASE in bytes.
- 16:20: bypass bit shift.

Enumerator

*kCLOCK\_AudioPll1BypassCtrl* CCM Audio PLL1 bypass Control.  
*kCLOCK\_AudioPll2BypassCtrl* CCM Audio PLL2 bypass Control.  
*kCLOCK\_VideoPll1BypassCtrl* CCM Video Pll1 bypass Control.  
*kCLOCK\_DramPllInternalPll1BypassCtrl* CCM DRAM PLL bypass Control.  
*kCLOCK\_ArmPllPwrBypassCtrl* CCM Arm PLL bypass Control.  
*kCLOCK\_SysPll1InternalPll1BypassCtrl* CCM System PLL1 bypass Control.  
*kCLOCK\_SysPll2InternalPll1BypassCtrl* CCM System PLL2 bypass Control.  
*kCLOCK\_SysPll3InternalPll1BypassCtrl* CCM System PLL3 bypass Control.

### 5.5.29 enum \_ccm\_analog\_pll\_clke

These constants define the PLL clock names for PLL clock enable/disable operations.

- 0:15: REG offset to CCM\_ANALOG\_BASE in bytes.
- 16:20: Clock enable bit shift.

Enumerator

*kCLOCK\_AudioPll1Clke* Audio pll1 clke.  
*kCLOCK\_AudioPll2Clke* Audio pll2 clke.  
*kCLOCK\_VideoPll1Clke* Video pll1 clke.  
*kCLOCK\_DramPllClke* Dram pll clke.  
*kCLOCK\_ArmPllClke* Arm pll clke.  
*kCLOCK\_SystemPll1Clke* System pll1 clke.  
*kCLOCK\_SystemPll1Div2Clke* System pll1 Div2 clke.  
*kCLOCK\_SystemPll1Div3Clke* System pll1 Div3 clke.  
*kCLOCK\_SystemPll1Div4Clke* System pll1 Div4 clke.  
*kCLOCK\_SystemPll1Div5Clke* System pll1 Div5 clke.  
*kCLOCK\_SystemPll1Div6Clke* System pll1 Div6 clke.  
*kCLOCK\_SystemPll1Div8Clke* System pll1 Div8 clke.  
*kCLOCK\_SystemPll1Div10Clke* System pll1 Div10 clke.  
*kCLOCK\_SystemPll1Div20Clke* System pll1 Div20 clke.  
*kCLOCK\_SystemPll2Clke* System pll2 clke.  
*kCLOCK\_SystemPll2Div2Clke* System pll2 Div2 clke.  
*kCLOCK\_SystemPll2Div3Clke* System pll2 Div3 clke.  
*kCLOCK\_SystemPll2Div4Clke* System pll2 Div4 clke.

***kCLOCK\_SystemPll2Div5Clke*** System pll2 Div5 clke.  
***kCLOCK\_SystemPll2Div6Clke*** System pll2 Div6 clke.  
***kCLOCK\_SystemPll2Div8Clke*** System pll2 Div8 clke.  
***kCLOCK\_SystemPll2Div10Clke*** System pll2 Div10 clke.  
***kCLOCK\_SystemPll2Div20Clke*** System pll2 Div20 clke.  
***kCLOCK\_SystemPll3Clke*** System pll3 clke.

### 5.5.30 anonymous enum

Enumerator

***kANALOG\_PllRefOsc24M*** reference OSC 24M  
***kANALOG\_PllPadClk*** reference PAD CLK

## 5.6 Function Documentation

### 5.6.1 static void CLOCK\_SetRootMux ( *clock\_root\_control\_t rootClk*, *uint32\_t mux* ) [inline], [static]

User maybe need to set more than one mux ROOT according to the clock tree description in the reference manual.

Parameters

|                |                                                                            |
|----------------|----------------------------------------------------------------------------|
| <i>rootClk</i> | Root clock control (see <a href="#">clock_root_control_t</a> enumeration). |
| <i>mux</i>     | Root mux value (see <a href="#">_ccm_rootmux_xxx</a> enumeration).         |

### 5.6.2 static uint32\_t CLOCK\_GetRootMux ( *clock\_root\_control\_t rootClk* ) [inline], [static]

In order to get the clock source of root, user maybe need to get more than one ROOT's mux value to obtain the final clock source of root.

Parameters

|                |                                                                            |
|----------------|----------------------------------------------------------------------------|
| <i>rootClk</i> | Root clock control (see <a href="#">clock_root_control_t</a> enumeration). |
|----------------|----------------------------------------------------------------------------|

Returns

Root mux value (see [\\_ccm\\_rootmux\\_xxx](#) enumeration).

### 5.6.3 static void CLOCK\_EnableRoot ( *clock\_root\_control\_t rootClk* ) [inline], [static]

Parameters

|                |                                                                           |
|----------------|---------------------------------------------------------------------------|
| <i>rootClk</i> | Root clock control (see <a href="#">clock_root_control_t</a> enumeration) |
|----------------|---------------------------------------------------------------------------|

#### 5.6.4 static void CLOCK\_DisableRoot( [clock\\_root\\_control\\_t](#) *rootClk* ) [inline], [static]

Parameters

|                |                                                                     |
|----------------|---------------------------------------------------------------------|
| <i>rootClk</i> | Root control (see <a href="#">clock_root_control_t</a> enumeration) |
|----------------|---------------------------------------------------------------------|

#### 5.6.5 static bool CLOCK\_IsRootEnabled( [clock\\_root\\_control\\_t](#) *rootClk* ) [inline], [static]

Parameters

|                |                                                                     |
|----------------|---------------------------------------------------------------------|
| <i>rootClk</i> | Root control (see <a href="#">clock_root_control_t</a> enumeration) |
|----------------|---------------------------------------------------------------------|

Returns

CCM root enabled or not.

- true: Clock root is enabled.
- false: Clock root is disabled.

#### 5.6.6 void CLOCK\_UpdateRoot( [clock\\_root\\_control\\_t](#) *ccmRootClk*, [uint32\\_t](#) *mux*, [uint32\\_t](#) *pre*, [uint32\\_t](#) *post* )

Parameters

|                   |                                                                     |
|-------------------|---------------------------------------------------------------------|
| <i>ccmRootClk</i> | Root control (see <a href="#">clock_root_control_t</a> enumeration) |
| <i>mux</i>        | mux value (see <a href="#">_ccm_rootmux_xxx</a> enumeration)        |
| <i>pre</i>        | Pre divider value (0-7, divider=n+1)                                |

|             |                                        |
|-------------|----------------------------------------|
| <i>post</i> | Post divider value (0-63, divider=n+1) |
|-------------|----------------------------------------|

### 5.6.7 void CLOCK\_SetRootDivider ( *clock\_root\_control\_t ccmRootClk*, *uint32\_t pre*, *uint32\_t post* )

Parameters

|                   |                                                                     |
|-------------------|---------------------------------------------------------------------|
| <i>ccmRootClk</i> | Root control (see <a href="#">clock_root_control_t</a> enumeration) |
| <i>pre</i>        | Pre divider value (1-8)                                             |
| <i>post</i>       | Post divider value (1-64)                                           |

### 5.6.8 static uint32\_t CLOCK\_GetRootPreDivider ( *clock\_root\_control\_t rootClk* ) [[inline](#)], [[static](#)]

In order to get the clock source of root, user maybe need to get more than one ROOT's mux value to obtain the final clock source of root.

Parameters

|                |                                                                         |
|----------------|-------------------------------------------------------------------------|
| <i>rootClk</i> | Root clock name (see <a href="#">clock_root_control_t</a> enumeration). |
|----------------|-------------------------------------------------------------------------|

Returns

Root Pre divider value.

### 5.6.9 static uint32\_t CLOCK\_GetRootPostDivider ( *clock\_root\_control\_t rootClk* ) [[inline](#)], [[static](#)]

In order to get the clock source of root, user maybe need to get more than one ROOT's mux value to obtain the final clock source of root.

Parameters

|                |                                                                         |
|----------------|-------------------------------------------------------------------------|
| <i>rootClk</i> | Root clock name (see <a href="#">clock_root_control_t</a> enumeration). |
|----------------|-------------------------------------------------------------------------|

Returns

Root Post divider value.

### 5.6.10 static void CLOCK\_ControlGate ( *uintptr\_t ccmGate*, *clock\_gate\_value\_t control* ) [inline], [static]

Parameters

|                |                                                                                                     |
|----------------|-----------------------------------------------------------------------------------------------------|
| <i>ccmGate</i> | Gate control (see <a href="#">clock_pll_gate_t</a> and <a href="#">clock_ip_name_t</a> enumeration) |
| <i>control</i> | Gate control value (see <a href="#">clock_gate_value_t</a> )                                        |

### 5.6.11 void CLOCK\_EnableClock ( *clock\_ip\_name\_t ccmGate* )

Take care of that one module may need to set more than one clock gate.

Parameters

|                |                                                                                 |
|----------------|---------------------------------------------------------------------------------|
| <i>ccmGate</i> | Gate control for each module (see <a href="#">clock_ip_name_t</a> enumeration). |
|----------------|---------------------------------------------------------------------------------|

### 5.6.12 void CLOCK\_DisableClock ( *clock\_ip\_name\_t ccmGate* )

Take care of that one module may need to set more than one clock gate.

Parameters

|                |                                                                                 |
|----------------|---------------------------------------------------------------------------------|
| <i>ccmGate</i> | Gate control for each module (see <a href="#">clock_ip_name_t</a> enumeration). |
|----------------|---------------------------------------------------------------------------------|

### 5.6.13 static void CLOCK\_PowerUpPII ( *CCM\_ANALOG\_Type \* base*, *clock\_pll\_ctrl\_t pliControl* ) [inline], [static]

Parameters

|                   |                                                                     |
|-------------------|---------------------------------------------------------------------|
| <i>base</i>       | CCM_ANALOG base pointer.                                            |
| <i>pllControl</i> | PLL control name (see <a href="#">clock_pll_ctrl_t</a> enumeration) |

#### 5.6.14 static void CLOCK\_PowerDownPll ( CCM\_ANALOG\_Type \* *base*, clock\_pll\_ctrl\_t *pllControl* ) [inline], [static]

Parameters

|                   |                                                                     |
|-------------------|---------------------------------------------------------------------|
| <i>base</i>       | CCM_ANALOG base pointer.                                            |
| <i>pllControl</i> | PLL control name (see <a href="#">clock_pll_ctrl_t</a> enumeration) |

#### 5.6.15 static void CLOCK\_SetPllBypass ( CCM\_ANALOG\_Type \* *base*, clock\_pll\_bypass\_ctrl\_t *pllControl*, bool *bypass* ) [inline], [static]

Parameters

|                   |                                                                                                                                 |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>       | CCM_ANALOG base pointer.                                                                                                        |
| <i>pllControl</i> | PLL control name (see <a href="#">clock_pll_bypass_ctrl_t</a> enumeration)                                                      |
| <i>bypass</i>     | Bypass the PLL. <ul style="list-style-type: none"><li>• true: Bypass the PLL.</li><li>• false: Do not bypass the PLL.</li></ul> |

#### 5.6.16 static bool CLOCK\_IsPllBypassed ( CCM\_ANALOG\_Type \* *base*, clock\_pll\_bypass\_ctrl\_t *pllControl* ) [inline], [static]

Parameters

|                   |                                                                            |
|-------------------|----------------------------------------------------------------------------|
| <i>base</i>       | CCM_ANALOG base pointer.                                                   |
| <i>pllControl</i> | PLL control name (see <a href="#">clock_pll_bypass_ctrl_t</a> enumeration) |

Returns

- PLL bypass status.
- true: The PLL is bypassed.

- false: The PLL is not bypassed.

### 5.6.17 static bool CLOCK\_IsPllLocked ( CCM\_ANALOG\_Type \* *base*, clock\_pll\_ctrl\_t *pllControl* ) [inline], [static]

Parameters

|                   |                                                                     |
|-------------------|---------------------------------------------------------------------|
| <i>base</i>       | CCM_ANALOG base pointer.                                            |
| <i>pllControl</i> | PLL control name (see <a href="#">clock_pll_ctrl_t</a> enumeration) |

Returns

PLL lock status.

- true: The PLL clock is locked.
- false: The PLL clock is not locked.

### 5.6.18 static void CLOCK\_EnableAnalogClock ( CCM\_ANALOG\_Type \* *base*, clock\_pll\_clke\_t *pllClock* ) [inline], [static]

Parameters

|                 |                                                                   |
|-----------------|-------------------------------------------------------------------|
| <i>base</i>     | CCM_ANALOG base pointer.                                          |
| <i>pllClock</i> | PLL clock name (see <a href="#">clock_pll_clke_t</a> enumeration) |

### 5.6.19 static void CLOCK\_DisableAnalogClock ( CCM\_ANALOG\_Type \* *base*, clock\_pll\_clke\_t *pllClock* ) [inline], [static]

Parameters

|                 |                                                                   |
|-----------------|-------------------------------------------------------------------|
| <i>base</i>     | CCM_ANALOG base pointer.                                          |
| <i>pllClock</i> | PLL clock name (see <a href="#">clock_pll_clke_t</a> enumeration) |

### 5.6.20 static void CLOCK\_OverridePllClke ( CCM\_ANALOG\_Type \* *base*, clock\_pll\_clke\_t *ovClock*, bool *override* ) [inline], [static]

Parameters

|                 |                                                                                                                                                                        |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>     | CCM_ANALOG base pointer.                                                                                                                                               |
| <i>ovClock</i>  | PLL clock name (see <a href="#">clock_pll_clke_t</a> enumeration)                                                                                                      |
| <i>override</i> | Override the PLL. <ul style="list-style-type: none"> <li>• true: Override the PLL clke, CCM will handle it.</li> <li>• false: Do not override the PLL clke.</li> </ul> |

### 5.6.21 static void CLOCK\_OverridePIIPd ( CCM\_ANALOG\_Type \* *base*, clock\_pll\_ctrl\_t *pdClock*, bool *override* ) [inline], [static]

Parameters

|                 |                                                                                                                                                                        |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>     | CCM_ANALOG base pointer.                                                                                                                                               |
| <i>pdClock</i>  | PLL clock name (see <a href="#">clock_pll_ctrl_t</a> enumeration)                                                                                                      |
| <i>override</i> | Override the PLL. <ul style="list-style-type: none"> <li>• true: Override the PLL clke, CCM will handle it.</li> <li>• false: Do not override the PLL clke.</li> </ul> |

### 5.6.22 void CLOCK\_InitArmPll ( const ccm\_analog\_integer\_pll\_config\_t \* *config* )

Parameters

|               |                                                                                                          |
|---------------|----------------------------------------------------------------------------------------------------------|
| <i>config</i> | Pointer to the configuration structure(see <a href="#">ccm_analog_integer_pll_config_t</a> enumeration). |
|---------------|----------------------------------------------------------------------------------------------------------|

Note

This function can't detect whether the Arm PLL has been enabled and used by some IPs.

### 5.6.23 void CLOCK\_InitSysPll1 ( const ccm\_analog\_integer\_pll\_config\_t \* *config* )

Parameters

|               |                                                                                                          |
|---------------|----------------------------------------------------------------------------------------------------------|
| <i>config</i> | Pointer to the configuration structure(see <a href="#">ccm_analog_integer_pll_config_t</a> enumeration). |
|---------------|----------------------------------------------------------------------------------------------------------|

Note

This function can't detect whether the SYS PLL has been enabled and used by some IPs.

#### **5.6.24 void CLOCK\_InitSysPLL2 ( const ccm\_analog\_integer\_pll\_config\_t \* *config* )**

Parameters

|               |                                                                                                          |
|---------------|----------------------------------------------------------------------------------------------------------|
| <i>config</i> | Pointer to the configuration structure(see <a href="#">ccm_analog_integer_pll_config_t</a> enumeration). |
|---------------|----------------------------------------------------------------------------------------------------------|

Note

This function can't detect whether the SYS PLL has been enabled and used by some IPs.

#### **5.6.25 void CLOCK\_InitSysPLL3 ( const ccm\_analog\_integer\_pll\_config\_t \* *config* )**

Parameters

|               |                                                                                                          |
|---------------|----------------------------------------------------------------------------------------------------------|
| <i>config</i> | Pointer to the configuration structure(see <a href="#">ccm_analog_integer_pll_config_t</a> enumeration). |
|---------------|----------------------------------------------------------------------------------------------------------|

Note

This function can't detect whether the SYS PLL has been enabled and used by some IPs.

#### **5.6.26 void CLOCK\_InitAudioPLL1 ( const ccm\_analog\_frac\_pll\_config\_t \* *config* )**

Parameters

|               |                                                                                                       |
|---------------|-------------------------------------------------------------------------------------------------------|
| <i>config</i> | Pointer to the configuration structure(see <a href="#">ccm_analog_frac_pll_config_t</a> enumeration). |
|---------------|-------------------------------------------------------------------------------------------------------|

Note

This function can't detect whether the AUDIO PLL has been enabled and used by some IPs.

### 5.6.27 void CLOCK\_InitAudioPII2 ( const ccm\_analog\_frac\_pll\_config\_t \* *config* )

Parameters

|               |                                                                                                       |
|---------------|-------------------------------------------------------------------------------------------------------|
| <i>config</i> | Pointer to the configuration structure(see <a href="#">ccm_analog_frac_pll_config_t</a> enumeration). |
|---------------|-------------------------------------------------------------------------------------------------------|

Note

This function can't detect whether the AUDIO PLL has been enabled and used by some IPs.

### 5.6.28 void CLOCK\_InitVideoPII1 ( const ccm\_analog\_frac\_pll\_config\_t \* *config* )

Parameters

|               |                                                                                                       |
|---------------|-------------------------------------------------------------------------------------------------------|
| <i>config</i> | Pointer to the configuration structure(see <a href="#">ccm_analog_frac_pll_config_t</a> enumeration). |
|---------------|-------------------------------------------------------------------------------------------------------|

### 5.6.29 void CLOCK\_InitIntegerPII ( CCM\_ANALOG\_Type \* *base*, const ccm\_analog\_integer\_pll\_config\_t \* *config*, clock\_pll\_ctrl\_t *type* )

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | CCM ANALOG base address |
|-------------|-------------------------|

|               |                                                                                                          |
|---------------|----------------------------------------------------------------------------------------------------------|
| <i>config</i> | Pointer to the configuration structure(see <a href="#">ccm_analog_integer_pll_config_t</a> enumeration). |
| <i>type</i>   | integer pll type                                                                                         |

**5.6.30 `uint32_t CLOCK_GetIntegerPllFreq ( CCM_ANALOG_Type * base, clock_pll_ctrl_t type, uint32_t refClkFreq, bool pll1Bypass )`**

Parameters

|                   |                            |
|-------------------|----------------------------|
| <i>base</i>       | CCM ANALOG base address.   |
| <i>type</i>       | integer pll type           |
| <i>refClkFreq</i> | Reference clock frequency. |
| <i>pll1Bypass</i> | pll1 bypass flag           |

Returns

Clock frequency

**5.6.31 `void CLOCK_InitFracPll ( CCM_ANALOG_Type * base, const ccm_analog_frac_pll_config_t * config, clock_pll_ctrl_t type )`**

Parameters

|               |                                                                                                       |
|---------------|-------------------------------------------------------------------------------------------------------|
| <i>base</i>   | CCM ANALOG base address.                                                                              |
| <i>config</i> | Pointer to the configuration structure(see <a href="#">ccm_analog_frac_pll_config_t</a> enumeration). |
| <i>type</i>   | fractional pll type.                                                                                  |

**5.6.32 `uint32_t CLOCK_GetFracPllFreq ( CCM_ANALOG_Type * base, clock_pll_ctrl_t type, uint32_t refClkFreq )`**

Parameters

|                   |                            |
|-------------------|----------------------------|
| <i>base</i>       | CCM_ANALOG base pointer.   |
| <i>type</i>       | fractional pll type.       |
| <i>refClkFreq</i> | Reference clock frequency. |

Returns

Clock frequency

### 5.6.33 uint32\_t CLOCK\_GetPIIFreq ( *clock\_pll\_ctrl\_t pIIf* )

Parameters

|             |                      |
|-------------|----------------------|
| <i>pIIf</i> | fractional pll type. |
|-------------|----------------------|

Returns

Clock frequency

### 5.6.34 uint32\_t CLOCK\_GetPIIRefClkFreq ( *clock\_pll\_ctrl\_t ctrl* )

Parameters

|             |                      |
|-------------|----------------------|
| <i>ctrl</i> | fractional pll type. |
|-------------|----------------------|

Returns

Clock frequency

### 5.6.35 uint32\_t CLOCK\_GetFreq ( *clock\_name\_t clockName* )

This function checks the current clock configurations and then calculates the clock frequency for a specific clock name defined in *clock\_name\_t*.

Parameters

|                  |                                                  |
|------------------|--------------------------------------------------|
| <i>clockName</i> | Clock names defined in <code>clock_name_t</code> |
|------------------|--------------------------------------------------|

Returns

Clock frequency value in hertz

### **5.6.36 `uint32_t CLOCK_GetClockRootFreq ( clock_root_t clockRoot )`**

Parameters

|                  |                                                                                          |
|------------------|------------------------------------------------------------------------------------------|
| <i>clockRoot</i> | The clock root used to get the frequency, please refer to <a href="#">clock_root_t</a> . |
|------------------|------------------------------------------------------------------------------------------|

Returns

The frequency of selected clock root.

### **5.6.37 `uint32_t CLOCK_GetCoreM7Freq ( void )`**

Returns

Clock frequency; If the clock is invalid, returns 0.

### **5.6.38 `uint32_t CLOCK_GetAxiFreq ( void )`**

Returns

Clock frequency; If the clock is invalid, returns 0.

### **5.6.39 `uint32_t CLOCK_GetAhbFreq ( void )`**

Returns

Clock frequency; If the clock is invalid, returns 0.

### **5.6.40 `uint32_t CLOCK_GetEnetAxiFreq ( void )`**

return Clock frequency; If the clock is invalid, returns 0.

# Chapter 6

## IOMUXC: IOMUX Controller

### 6.1 Overview

IOMUXC driver provides APIs for pin configuration. It also supports the miscellaneous functions integrated in IOMUXC.

### Files

- file [fsl\\_iomuxc.h](#)

### Driver version

- #define [FSL\\_IOMUXC\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 0, 4))  
*IOMUXC driver version 2.0.4.*

### Pin function ID

The pin function ID is a tuple of <muxRegister muxMode inputRegister inputDaisy configRegister>

- #define **IOMUXC\_BOOT\_MODE0\_SRC\_BOOT\_MODE0** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330250
- #define **IOMUXC\_BOOT\_MODE1\_SRC\_BOOT\_MODE1** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330254
- #define **IOMUXC\_BOOT\_MODE2\_SRC\_BOOT\_MODE2** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330258
- #define **IOMUXC\_BOOT\_MODE3\_SRC\_BOOT\_MODE3** 0x00000000, 0x0, 0x00000000, 0x0, 0x3033025C
- #define **IOMUXC\_JTAG\_MOD\_JTAG\_MODE** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330260
- #define **IOMUXC\_JTAG\_TDI\_JTAG\_TDI** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330264
- #define **IOMUXC\_JTAG\_TMS\_JTAG\_TMS** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330268
- #define **IOMUXC\_JTAG\_TCK\_JTAG\_TCK** 0x00000000, 0x0, 0x00000000, 0x0, 0x3033026C
- #define **IOMUXC\_JTAG\_TDO\_JTAG\_TDO** 0x00000000, 0x0, 0x00000000, 0x0, 0x30330270
- #define **IOMUXC\_RTC\_XTAL1\_SNVS\_RTC** 0x00000000, 0x0, 0x00000000, 0x0, 0x00000000
- #define **IOMUXC\_PMIC\_STBY\_REQ\_CCM\_PMIC\_STBY\_REQ** 0x00000000, 0x0, 0x00000000, 0x0, 0x00000000
- #define **IOMUXC\_PMIC\_ON\_REQ\_SNVS\_PMIC\_ON\_REQ** 0x00000000, 0x0, 0x00000000, 0x0, 0x00000000
- #define **IOMUXC\_ONOFF\_SNVS\_ONOFF** 0x00000000, 0x0, 0x00000000, 0x0, 0x00000000
- #define **IOMUXC POR\_B\_SNVS\_POR\_B** 0x00000000, 0x0, 0x00000000, 0x0, 0x00000000
- #define **IOMUXC\_GPIO1\_IO00\_GPIO1\_IO00** 0x30330014, 0x0, 0x00000000, 0x0, 0x30330274
- #define **IOMUXC\_GPIO1\_IO00\_CCM\_ENET\_PHY\_REF\_CLK\_ROOT** 0x30330014, 0x1, 0x00000000, 0x0, 0x30330274
- #define **IOMUXC\_GPIO1\_IO00\_ISP\_FL\_TRIG\_0** 0x30330014, 0x3, 0x303305D4, 0x0, 0x30330274
- #define **IOMUXC\_GPIO1\_IO00\_ANAMIX\_REF\_CLK\_32K** 0x30330014, 0x5, 0x00000000, 0x0, 0x30330274

- #define **IOMUXC\_GPIO1\_IO00\_CCM\_EXT\_CLK1** 0x30330014, 0x6, 0x00000000, 0x0, 0x30330274
- #define **IOMUXC\_GPIO1\_IO01\_GPIO1\_IO01** 0x30330018, 0x0, 0x00000000, 0x0, 0x30330278
- #define **IOMUXC\_GPIO1\_IO01\_PWM1\_OUT** 0x30330018, 0x1, 0x00000000, 0x0, 0x30330278
- #define **IOMUXC\_GPIO1\_IO01\_ISP\_SHUTTER\_TRIG\_0** 0x30330018, 0x3, 0x303305DC, 0x0, 0x30330278
- #define **IOMUXC\_GPIO1\_IO01\_ANAMIX\_REF\_CLK\_24M** 0x30330018, 0x5, 0x00000000, 0x0, 0x30330278
- #define **IOMUXC\_GPIO1\_IO01\_CCM\_EXT\_CLK2** 0x30330018, 0x6, 0x00000000, 0x0, 0x30330278
- #define **IOMUXC\_GPIO1\_IO02\_GPIO1\_IO02** 0x3033001C, 0x0, 0x00000000, 0x0, 0x3033027C
- #define **IOMUXC\_GPIO1\_IO02\_WDOG1\_WDOG\_B** 0x3033001C, 0x1, 0x00000000, 0x0, 0x3033027C
- #define **IOMUXC\_GPIO1\_IO02\_ISP\_FLASH\_TRIG\_0** 0x3033001C, 0x3, 0x00000000, 0x0, 0x3033027C
- #define **IOMUXC\_GPIO1\_IO02\_WDOG1\_WDOG\_ANY** 0x3033001C, 0x5, 0x00000000, 0x0, 0x3033027C
- #define **IOMUXC\_GPIO1\_IO02\_SJC\_DE\_B** 0x3033001C, 0x7, 0x00000000, 0x0, 0x3033027C
- #define **IOMUXC\_GPIO1\_IO03\_GPIO1\_IO03** 0x30330020, 0x0, 0x00000000, 0x0, 0x30330280
- #define **IOMUXC\_GPIO1\_IO03\_USDHC1\_VSELECT** 0x30330020, 0x1, 0x00000000, 0x0, 0x30330280
- #define **IOMUXC\_GPIO1\_IO03\_ISP\_PRELIGHT\_TRIG\_0** 0x30330020, 0x3, 0x00000000, 0x0, 0x30330280
- #define **IOMUXC\_GPIO1\_IO03\_SDMA1\_EXT\_EVENT0** 0x30330020, 0x5, 0x00000000, 0x0, 0x30330280
- #define **IOMUXC\_GPIO1\_IO04\_GPIO1\_IO04** 0x30330024, 0x0, 0x00000000, 0x0, 0x30330284
- #define **IOMUXC\_GPIO1\_IO04\_USDHC2\_VSELECT** 0x30330024, 0x1, 0x00000000, 0x0, 0x30330284
- #define **IOMUXC\_GPIO1\_IO04\_ISP\_SHUTTER\_OPEN\_0** 0x30330024, 0x3, 0x00000000, 0x0, 0x30330284
- #define **IOMUXC\_GPIO1\_IO04\_SDMA1\_EXT\_EVENT1** 0x30330024, 0x5, 0x00000000, 0x0, 0x30330284
- #define **IOMUXC\_GPIO1\_IO05\_GPIO1\_IO05** 0x30330028, 0x0, 0x00000000, 0x0, 0x30330288
- #define **IOMUXC\_GPIO1\_IO05\_M7\_NMI** 0x30330028, 0x1, 0x00000000, 0x0, 0x30330288
- #define **IOMUXC\_GPIO1\_IO05\_ISP\_FL\_TRIG\_1** 0x30330028, 0x3, 0x303305D8, 0x0, 0x30330288
- #define **IOMUXC\_GPIO1\_IO05\_CCM\_PMIC\_READY** 0x30330028, 0x5, 0x30330554, 0x0, 0x30330288
- #define **IOMUXC\_GPIO1\_IO06\_GPIO1\_IO06** 0x3033002C, 0x0, 0x00000000, 0x0, 0x3033028C
- #define **IOMUXC\_GPIO1\_IO06\_ENET\_QOS\_MDC** 0x3033002C, 0x1, 0x00000000, 0x0, 0x3033028C
- #define **IOMUXC\_GPIO1\_IO06\_ISP\_SHUTTER\_TRIG\_1** 0x3033002C, 0x3, 0x303305E0, 0x0, 0x3033028C
- #define **IOMUXC\_GPIO1\_IO06\_USDHC1\_CD\_B** 0x3033002C, 0x5, 0x00000000, 0x0, 0x3033028C
- #define **IOMUXC\_GPIO1\_IO06\_CCM\_EXT\_CLK3** 0x3033002C, 0x6, 0x00000000, 0x0, 0x3033028C
- #define **IOMUXC\_GPIO1\_IO07\_GPIO1\_IO07** 0x30330030, 0x0, 0x00000000, 0x0, 0x30330290
- #define **IOMUXC\_GPIO1\_IO07\_ENET\_QOS\_MDIO** 0x30330030, 0x1, 0x30330590, 0x0,

- #define **IOMUXC\_GPIO1\_IO07\_ISP\_FLASH\_TRIG\_1** 0x30330030, 0x3, 0x00000000, 0x0, 0x30330290
- #define **IOMUXC\_GPIO1\_IO07\_USDHC1\_WP** 0x30330030, 0x5, 0x00000000, 0x0, 0x30330290
- #define **IOMUXC\_GPIO1\_IO07\_CCM\_EXT\_CLK4** 0x30330030, 0x6, 0x00000000, 0x0, 0x30330290
- #define **IOMUXC\_GPIO1\_IO08\_GPIO1\_IO08** 0x30330034, 0x0, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC\_GPIO1\_IO08\_ENET\_QOS\_1588\_EVENT0\_IN** 0x30330034, 0x1, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC\_GPIO1\_IO08\_PWM1\_OUT** 0x30330034, 0x2, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC\_GPIO1\_IO08\_ISP\_PRELIGHT\_TRIG\_1** 0x30330034, 0x3, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC\_GPIO1\_IO08\_ENET\_QOS\_1588\_EVENT0\_AUX\_IN** 0x30330034, 0x4, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC\_GPIO1\_IO08\_USDHC2\_RESET\_B** 0x30330034, 0x5, 0x00000000, 0x0, 0x30330294
- #define **IOMUXC\_GPIO1\_IO09\_GPIO1\_IO09** 0x30330038, 0x0, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC\_GPIO1\_IO09\_ENET\_QOS\_1588\_EVENT0\_OUT** 0x30330038, 0x1, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC\_GPIO1\_IO09\_PWM2\_OUT** 0x30330038, 0x2, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC\_GPIO1\_IO09\_ISP\_SHUTTER\_OPEN\_1** 0x30330038, 0x3, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC\_GPIO1\_IO09\_USDHC3\_RESET\_B** 0x30330038, 0x4, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC\_GPIO1\_IO09\_SDMA2\_EXT\_EVENT0** 0x30330038, 0x5, 0x00000000, 0x0, 0x30330298
- #define **IOMUXC\_GPIO1\_IO10\_GPIO1\_IO10** 0x3033003C, 0x0, 0x00000000, 0x0, 0x3033029C
- #define **IOMUXC\_GPIO1\_IO10\_USB1\_ID** 0x3033003C, 0x1, 0x00000000, 0x0, 0x3033029C
- #define **IOMUXC\_GPIO1\_IO10\_PWM3\_OUT** 0x3033003C, 0x2, 0x00000000, 0x0, 0x3033029C
- #define **IOMUXC\_GPIO1\_IO11\_GPIO1\_IO11** 0x30330040, 0x0, 0x00000000, 0x0, 0x303302A0
- #define **IOMUXC\_GPIO1\_IO11\_USB2\_ID** 0x30330040, 0x1, 0x00000000, 0x0, 0x303302A0
- #define **IOMUXC\_GPIO1\_IO11\_PWM2\_OUT** 0x30330040, 0x2, 0x00000000, 0x0, 0x303302A0
- #define **IOMUXC\_GPIO1\_IO11\_USDHC3\_VSELECT** 0x30330040, 0x4, 0x00000000, 0x0, 0x303302A0
- #define **IOMUXC\_GPIO1\_IO11\_CCM\_PMIC\_READY** 0x30330040, 0x5, 0x30330554, 0x1, 0x303302A0
- #define **IOMUXC\_GPIO1\_IO12\_GPIO1\_IO12** 0x30330044, 0x0, 0x00000000, 0x0, 0x303302A4
- #define **IOMUXC\_GPIO1\_IO12\_USB1\_PWR** 0x30330044, 0x1, 0x00000000, 0x0, 0x303302A4
- #define **IOMUXC\_GPIO1\_IO12\_SDMA2\_EXT\_EVENT1** 0x30330044, 0x5, 0x00000000, 0x0, 0x303302A4
- #define **IOMUXC\_GPIO1\_IO13\_GPIO1\_IO13** 0x30330048, 0x0, 0x00000000, 0x0, 0x303302A8
- #define **IOMUXC\_GPIO1\_IO13\_USB1\_OC** 0x30330048, 0x1, 0x00000000, 0x0, 0x303302A8
- #define **IOMUXC\_GPIO1\_IO13\_PWM2\_OUT** 0x30330048, 0x5, 0x00000000, 0x0, 0x303302A8
- #define **IOMUXC\_GPIO1\_IO14\_GPIO1\_IO14** 0x3033004C, 0x0, 0x00000000, 0x0, 0x303302A8

- AC
- #define **IOMUXC\_GPIO1\_IO14\_USB2\_PWR** 0x3033004C, 0x1, 0x00000000, 0x0, 0x303302-AC
- #define **IOMUXC\_GPIO1\_IO14\_USDHC3\_CD\_B** 0x3033004C, 0x4, 0x30330608, 0x0, 0x303302AC
- #define **IOMUXC\_GPIO1\_IO14\_PWM3\_OUT** 0x3033004C, 0x5, 0x00000000, 0x0, 0x303302-AC
- #define **IOMUXC\_GPIO1\_IO14\_CCM\_CLKO1** 0x3033004C, 0x6, 0x00000000, 0x0, 0x303302AC
- #define **IOMUXC\_GPIO1\_IO15\_GPIO1\_IO15** 0x30330050, 0x0, 0x00000000, 0x0, 0x303302-B0
- #define **IOMUXC\_GPIO1\_IO15\_USB2\_OC** 0x30330050, 0x1, 0x00000000, 0x0, 0x303302B0
- #define **IOMUXC\_GPIO1\_IO15\_USDHC3\_WP** 0x30330050, 0x4, 0x30330634, 0x0, 0x303302-B0
- #define **IOMUXC\_GPIO1\_IO15\_PWM4\_OUT** 0x30330050, 0x5, 0x00000000, 0x0, 0x303302-B0
- #define **IOMUXC\_GPIO1\_IO15\_CCM\_CLKO2** 0x30330050, 0x6, 0x00000000, 0x0, 0x303302-B0
- #define **IOMUXC\_ENET\_MDC\_ENET\_QOS\_MDC** 0x30330054, 0x0, 0x00000000, 0x0, 0x303302B4
- #define **IOMUXC\_ENET\_MDC\_AUDIOMIX\_SAI6\_TX\_DATA0** 0x30330054, 0x2, 0x00000000, 0x0, 0x303302B4
- #define **IOMUXC\_ENET\_MDC\_GPIO1\_IO16** 0x30330054, 0x5, 0x00000000, 0x0, 0x303302-B4
- #define **IOMUXC\_ENET\_MDC\_USDHC3\_STROBE** 0x30330054, 0x6, 0x30330630, 0x0, 0x303302B4
- #define **IOMUXC\_ENET\_MDIO\_ENET\_QOS\_MDIO** 0x30330058, 0x0, 0x30330590, 0x1, 0x303302B8
- #define **IOMUXC\_ENET\_MDIO\_AUDIOMIX\_SAI6\_TX\_SYNC** 0x30330058, 0x2, 0x30330528, 0x0, 0x303302B8
- #define **IOMUXC\_ENET\_MDIO\_AUDIOMIX\_PDM\_BIT\_STREAM3** 0x30330058, 0x3, 0x303304CC, 0x0, 0x303302B8
- #define **IOMUXC\_ENET\_MDIO\_GPIO1\_IO17** 0x30330058, 0x5, 0x00000000, 0x0, 0x303302-B8
- #define **IOMUXC\_ENET\_MDIO\_USDHC3\_DATA5** 0x30330058, 0x6, 0x30330624, 0x0, 0x303302B8
- #define **IOMUXC\_ENET\_TD3\_ENET\_QOS\_RGMII\_TD3** 0x3033005C, 0x0, 0x00000000, 0x0, 0x303302BC
- #define **IOMUXC\_ENET\_TD3\_AUDIOMIX\_SAI6\_TX\_BCLK** 0x3033005C, 0x2, 0x30330524, 0x0, 0x303302BC
- #define **IOMUXC\_ENET\_TD3\_AUDIOMIX\_PDM\_BIT\_STREAM2** 0x3033005C, 0x3, 0x303304C8, 0x0, 0x303302BC
- #define **IOMUXC\_ENET\_TD3\_GPIO1\_IO18** 0x3033005C, 0x5, 0x00000000, 0x0, 0x303302B-C
- #define **IOMUXC\_ENET\_TD3\_USDHC3\_DATA6** 0x3033005C, 0x6, 0x30330628, 0x0, 0x303302BC
- #define **IOMUXC\_ENET\_TD2\_ENET\_QOS\_RGMII\_TD2** 0x30330060, 0x0, 0x00000000, 0x0, 0x303302C0
- #define **IOMUXC\_ENET\_TD2\_CCM\_ENET\_QOS\_CLOCK\_GENERATE\_REF\_CLK** 0x30330060, 0x1, 0x00000000, 0x0, 0x303302C0

- #define **IOMUXC\_ENET\_TD2\_AUDIOMIX\_SAI6\_RX\_DATA0** 0x30330060, 0x2, 0x3033051-C, 0x0, 0x303302C0
- #define **IOMUXC\_ENET\_TD2\_AUDIOMIX\_PDM\_BIT\_STREAM1** 0x30330060, 0x3, 0x303304C4, 0x0, 0x303302C0
- #define **IOMUXC\_ENET\_TD2\_GPIO1\_IO19** 0x30330060, 0x5, 0x00000000, 0x0, 0x303302C0
- #define **IOMUXC\_ENET\_TD2\_USDHC3\_DATA7** 0x30330060, 0x6, 0x3033062C, 0x0, 0x303302C0
- #define **IOMUXC\_ENET\_TD1\_ENET\_QOS\_RGMII\_TD1** 0x30330064, 0x0, 0x00000000, 0x0, 0x303302C4
- #define **IOMUXC\_ENET\_TD1\_AUDIOMIX\_SAI6\_RX\_SYNC** 0x30330064, 0x2, 0x30330520, 0x0, 0x303302C4
- #define **IOMUXC\_ENET\_TD1\_AUDIOMIX\_PDM\_BIT\_STREAM0** 0x30330064, 0x3, 0x303304C0, 0x0, 0x303302C4
- #define **IOMUXC\_ENET\_TD1\_GPIO1\_IO20** 0x30330064, 0x5, 0x00000000, 0x0, 0x303302C4
- #define **IOMUXC\_ENET\_TD1\_USDHC3\_CD\_B** 0x30330064, 0x6, 0x30330608, 0x1, 0x303302C4
- #define **IOMUXC\_ENET\_TD0\_ENET\_QOS\_RGMII\_TD0** 0x30330068, 0x0, 0x00000000, 0x0, 0x303302C8
- #define **IOMUXC\_ENET\_TD0\_AUDIOMIX\_SAI6\_RX\_BCLK** 0x30330068, 0x2, 0x30330518, 0x0, 0x303302C8
- #define **IOMUXC\_ENET\_TD0\_AUDIOMIX\_PDM\_CLK** 0x30330068, 0x3, 0x00000000, 0x0, 0x303302C8
- #define **IOMUXC\_ENET\_TD0\_GPIO1\_IO21** 0x30330068, 0x5, 0x00000000, 0x0, 0x303302C8
- #define **IOMUXC\_ENET\_TD0\_USDHC3\_WP** 0x30330068, 0x6, 0x30330634, 0x1, 0x303302C8
- #define **IOMUXC\_ENET\_TX\_CTL\_ENET\_QOS\_RGMII\_TX\_CTL** 0x3033006C, 0x0, 0x00000000, 0x0, 0x303302CC
- #define **IOMUXC\_ENET\_TX\_CTL\_AUDIOMIX\_SAI6\_MCLK** 0x3033006C, 0x2, 0x30330514, 0x0, 0x303302CC
- #define **IOMUXC\_ENET\_TX\_CTL\_AUDIOMIX\_SPDIF1\_OUT** 0x3033006C, 0x3, 0x00000000, 0x0, 0x303302CC
- #define **IOMUXC\_ENET\_TX\_CTL\_GPIO1\_IO22** 0x3033006C, 0x5, 0x00000000, 0x0, 0x303302CC
- #define **IOMUXC\_ENET\_TX\_CTL\_USDHC3\_DATA0** 0x3033006C, 0x6, 0x30330610, 0x0, 0x303302CC
- #define **IOMUXC\_ENET\_TXC\_CCM\_ENET\_QOS\_CLOCK\_GENERATE\_TX\_CLK** 0x30330070, 0x0, 0x00000000, 0x0, 0x303302D0
- #define **IOMUXC\_ENET\_TXC\_ENET\_QOS\_TX\_ER** 0x30330070, 0x1, 0x00000000, 0x0, 0x303302D0
- #define **IOMUXC\_ENET\_TXC\_AUDIOMIX\_SAI7\_TX\_DATA0** 0x30330070, 0x2, 0x00000000, 0x0, 0x303302D0
- #define **IOMUXC\_ENET\_TXC\_GPIO1\_IO23** 0x30330070, 0x5, 0x00000000, 0x0, 0x303302D0
- #define **IOMUXC\_ENET\_TXC\_USDHC3\_DATA1** 0x30330070, 0x6, 0x30330614, 0x0, 0x303302D0
- #define **IOMUXC\_ENET\_RX\_CTL\_ENET\_QOS\_RGMII\_RX\_CTL** 0x30330074, 0x0, 0x00000000, 0x0, 0x303302D4
- #define **IOMUXC\_ENET\_RX\_CTL\_AUDIOMIX\_SAI7\_TX\_SYNC** 0x30330074, 0x2, 0x30330540, 0x0, 0x303302D4
- #define **IOMUXC\_ENET\_RX\_CTL\_AUDIOMIX\_PDM\_BIT\_STREAM3** 0x30330074, 0x3, 0x303304CC, 0x1, 0x303302D4

- #define **IOMUXC\_ENET\_RX\_CTL\_GPIO1\_IO24** 0x30330074, 0x5, 0x00000000, 0x0, 0x303302D4
- #define **IOMUXC\_ENET\_RX\_CTL\_USDHC3\_DATA2** 0x30330074, 0x6, 0x30330618, 0x0, 0x303302D4
- #define **IOMUXC\_ENET\_RXC\_CCM\_ENET\_QOS\_CLOCK\_GENERATE\_RX\_CLK** 0x30330078, 0x0, 0x00000000, 0x0, 0x303302D8
- #define **IOMUXC\_ENET\_RXC\_ENET\_QOS\_RX\_ER** 0x30330078, 0x1, 0x00000000, 0x0, 0x303302D8
- #define **IOMUXC\_ENET\_RXC\_AUDIOMIX\_SAI7\_TX\_BCLK** 0x30330078, 0x2, 0x3033053-C, 0x0, 0x303302D8
- #define **IOMUXC\_ENET\_RXC\_AUDIOMIX\_PDM\_BIT\_STREAM2** 0x30330078, 0x3, 0x303304C8, 0x1, 0x303302D8
- #define **IOMUXC\_ENET\_RXC\_GPIO1\_IO25** 0x30330078, 0x5, 0x00000000, 0x0, 0x303302-D8
- #define **IOMUXC\_ENET\_RXC\_USDHC3\_DATA3** 0x30330078, 0x6, 0x3033061C, 0x0, 0x303302D8
- #define **IOMUXC\_ENET\_RD0\_ENET\_QOS\_RGMII\_RD0** 0x3033007C, 0x0, 0x00000000, 0x0, 0x303302DC
- #define **IOMUXC\_ENET\_RD0\_AUDIOMIX\_SAI7\_RX\_DATA0** 0x3033007C, 0x2, 0x30330534, 0x0, 0x303302DC
- #define **IOMUXC\_ENET\_RD0\_AUDIOMIX\_PDM\_BIT\_STREAM1** 0x3033007C, 0x3, 0x303304C4, 0x1, 0x303302DC
- #define **IOMUXC\_ENET\_RD0\_GPIO1\_IO26** 0x3033007C, 0x5, 0x00000000, 0x0, 0x303302D-C
- #define **IOMUXC\_ENET\_RD0\_USDHC3\_DATA4** 0x3033007C, 0x6, 0x30330620, 0x0, 0x303302DC
- #define **IOMUXC\_ENET\_RD1\_ENET\_QOS\_RGMII\_RD1** 0x30330080, 0x0, 0x00000000, 0x0, 0x303302E0
- #define **IOMUXC\_ENET\_RD1\_AUDIOMIX\_SAI7\_RX\_SYNC** 0x30330080, 0x2, 0x30330538, 0x0, 0x303302E0
- #define **IOMUXC\_ENET\_RD1\_AUDIOMIX\_PDM\_BIT\_STREAM0** 0x30330080, 0x3, 0x303304C0, 0x1, 0x303302E0
- #define **IOMUXC\_ENET\_RD1\_GPIO1\_IO27** 0x30330080, 0x5, 0x00000000, 0x0, 0x303302E0
- #define **IOMUXC\_ENET\_RD1\_USDHC3\_RESET\_B** 0x30330080, 0x6, 0x00000000, 0x0, 0x303302E0
- #define **IOMUXC\_ENET\_RD2\_ENET\_QOS\_RGMII\_RD2** 0x30330084, 0x0, 0x00000000, 0x0, 0x303302E4
- #define **IOMUXC\_ENET\_RD2\_AUDIOMIX\_SAI7\_RX\_BCLK** 0x30330084, 0x2, 0x30330530, 0x0, 0x303302E4
- #define **IOMUXC\_ENET\_RD2\_AUDIOMIX\_PDM\_CLK** 0x30330084, 0x3, 0x00000000, 0x0, 0x303302E4
- #define **IOMUXC\_ENET\_RD2\_GPIO1\_IO28** 0x30330084, 0x5, 0x00000000, 0x0, 0x303302E4
- #define **IOMUXC\_ENET\_RD2\_USDHC3\_CLK** 0x30330084, 0x6, 0x30330604, 0x0, 0x303302-E4
- #define **IOMUXC\_ENET\_RD3\_ENET\_QOS\_RGMII\_RD3** 0x30330088, 0x0, 0x00000000, 0x0, 0x303302E8
- #define **IOMUXC\_ENET\_RD3\_AUDIOMIX\_SAI7\_MCLK** 0x30330088, 0x2, 0x3033052C, 0x0, 0x303302E8
- #define **IOMUXC\_ENET\_RD3\_AUDIOMIX\_SPDIF1\_IN** 0x30330088, 0x3, 0x30330544, 0x0, 0x303302E8

- #define **IOMUXC\_ENET\_RD3\_GPIO1\_IO29** 0x30330088, 0x5, 0x00000000, 0x0, 0x303302E8
- #define **IOMUXC\_ENET\_RD3\_USDHC3\_CMD** 0x30330088, 0x6, 0x3033060C, 0x0, 0x303302E8
- #define **IOMUXC\_SD1\_CLK\_USDHC1\_CLK** 0x3033008C, 0x0, 0x00000000, 0x0, 0x303302-EC
- #define **IOMUXC\_SD1\_CLK\_ENET1\_MDC** 0x3033008C, 0x1, 0x00000000, 0x0, 0x303302EC
- #define **IOMUXC\_SD1\_CLK\_I2C5\_SCL** 0x3033008C, 0x3, 0x303305C4, 0x0, 0x303302EC
- #define **IOMUXC\_SD1\_CLK\_UART1\_TX** 0x3033008C, 0x4, 0x00000000, 0x0, 0x303302EC
- #define **IOMUXC\_SD1\_CLK\_UART1\_RX** 0x3033008C, 0x4, 0x303305E8, 0x0, 0x303302EC
- #define **IOMUXC\_SD1\_CLK\_GPIO2\_IO00** 0x3033008C, 0x5, 0x00000000, 0x0, 0x303302EC
- #define **IOMUXC\_SD1\_CMD\_USDHC1\_CMD** 0x30330090, 0x0, 0x00000000, 0x0, 0x303302-F0
- #define **IOMUXC\_SD1\_CMD\_ENET1\_MDIO** 0x30330090, 0x1, 0x3033057C, 0x0, 0x303302-F0
- #define **IOMUXC\_SD1\_CMD\_I2C5\_SDA** 0x30330090, 0x3, 0x303305C8, 0x0, 0x303302F0
- #define **IOMUXC\_SD1\_CMD\_UART1\_RX** 0x30330090, 0x4, 0x303305E8, 0x1, 0x303302F0
- #define **IOMUXC\_SD1\_CMD\_UART1\_TX** 0x30330090, 0x4, 0x00000000, 0x0, 0x303302F0
- #define **IOMUXC\_SD1\_CMD\_GPIO2\_IO01** 0x30330090, 0x5, 0x00000000, 0x0, 0x303302F0
- #define **IOMUXC\_SD1\_DATA0\_USDHC1\_DATA0** 0x30330094, 0x0, 0x00000000, 0x0, 0x303302F4
- #define **IOMUXC\_SD1\_DATA0\_ENET1\_RGMII\_TD1** 0x30330094, 0x1, 0x00000000, 0x0, 0x303302F4
- #define **IOMUXC\_SD1\_DATA0\_I2C6\_SCL** 0x30330094, 0x3, 0x303305CC, 0x0, 0x303302F4
- #define **IOMUXC\_SD1\_DATA0\_UART1\_RTS\_B** 0x30330094, 0x4, 0x303305E4, 0x0, 0x303302F4
- #define **IOMUXC\_SD1\_DATA0\_UART1\_CTS\_B** 0x30330094, 0x4, 0x00000000, 0x0, 0x303302F4
- #define **IOMUXC\_SD1\_DATA0\_GPIO2\_IO02** 0x30330094, 0x5, 0x00000000, 0x0, 0x303302-F4
- #define **IOMUXC\_SD1\_DATA1\_USDHC1\_DATA1** 0x30330098, 0x0, 0x00000000, 0x0, 0x303302F8
- #define **IOMUXC\_SD1\_DATA1\_ENET1\_RGMII\_TD0** 0x30330098, 0x1, 0x00000000, 0x0, 0x303302F8
- #define **IOMUXC\_SD1\_DATA1\_I2C6\_SDA** 0x30330098, 0x3, 0x303305D0, 0x0, 0x303302F8
- #define **IOMUXC\_SD1\_DATA1\_UART1\_CTS\_B** 0x30330098, 0x4, 0x00000000, 0x0, 0x303302F8
- #define **IOMUXC\_SD1\_DATA1\_UART1\_RTS\_B** 0x30330098, 0x4, 0x303305E4, 0x1, 0x303302F8
- #define **IOMUXC\_SD1\_DATA1\_GPIO2\_IO03** 0x30330098, 0x5, 0x00000000, 0x0, 0x303302-F8
- #define **IOMUXC\_SD1\_DATA2\_USDHC1\_DATA2** 0x3033009C, 0x0, 0x00000000, 0x0, 0x303302FC
- #define **IOMUXC\_SD1\_DATA2\_ENET1\_RGMII\_RD0** 0x3033009C, 0x1, 0x30330580, 0x0, 0x303302FC
- #define **IOMUXC\_SD1\_DATA2\_I2C4\_SCL** 0x3033009C, 0x3, 0x303305BC, 0x0, 0x303302FC
- #define **IOMUXC\_SD1\_DATA2\_UART2\_TX** 0x3033009C, 0x4, 0x00000000, 0x0, 0x303302FC
- #define **IOMUXC\_SD1\_DATA2\_UART2\_RX** 0x3033009C, 0x4, 0x303305F0, 0x0, 0x303302F-C
- #define **IOMUXC\_SD1\_DATA2\_GPIO2\_IO04** 0x3033009C, 0x5, 0x00000000, 0x0, 0x303302-FC
- #define **IOMUXC\_SD1\_DATA3\_USDHC1\_DATA3** 0x303300A0, 0x0, 0x00000000, 0x0,

- 0x30330300
- #define **IOMUXC\_SD1\_DATA3\_ENET1\_RGMII\_RD1** 0x303300A0, 0x1, 0x30330584, 0x0, 0x30330300
- #define **IOMUXC\_SD1\_DATA3\_I2C4\_SDA** 0x303300A0, 0x3, 0x303305C0, 0x0, 0x30330300
- #define **IOMUXC\_SD1\_DATA3\_UART2\_RX** 0x303300A0, 0x4, 0x303305F0, 0x1, 0x30330300
- #define **IOMUXC\_SD1\_DATA3\_UART2\_TX** 0x303300A0, 0x4, 0x00000000, 0x0, 0x30330300
- #define **IOMUXC\_SD1\_DATA3\_GPIO2\_IO05** 0x303300A0, 0x5, 0x00000000, 0x0, 0x30330300
- #define **IOMUXC\_SD1\_DATA4\_USDHC1\_DATA4** 0x303300A4, 0x0, 0x00000000, 0x0, 0x30330304
- #define **IOMUXC\_SD1\_DATA4\_ENET1\_RGMII\_TX\_CTL** 0x303300A4, 0x1, 0x00000000, 0x0, 0x30330304
- #define **IOMUXC\_SD1\_DATA4\_I2C1\_SCL** 0x303300A4, 0x3, 0x303305A4, 0x0, 0x30330304
- #define **IOMUXC\_SD1\_DATA4\_UART2\_RTS\_B** 0x303300A4, 0x4, 0x303305EC, 0x0, 0x30330304
- #define **IOMUXC\_SD1\_DATA4\_UART2\_CTS\_B** 0x303300A4, 0x4, 0x00000000, 0x0, 0x30330304
- #define **IOMUXC\_SD1\_DATA4\_GPIO2\_IO06** 0x303300A4, 0x5, 0x00000000, 0x0, 0x30330304
- #define **IOMUXC\_SD1\_DATA5\_USDHC1\_DATA5** 0x303300A8, 0x0, 0x00000000, 0x0, 0x30330308
- #define **IOMUXC\_SD1\_DATA5\_ENET1\_TX\_ER** 0x303300A8, 0x1, 0x00000000, 0x0, 0x30330308
- #define **IOMUXC\_SD1\_DATA5\_I2C1\_SDA** 0x303300A8, 0x3, 0x303305A8, 0x0, 0x30330308
- #define **IOMUXC\_SD1\_DATA5\_UART2\_CTS\_B** 0x303300A8, 0x4, 0x00000000, 0x0, 0x30330308
- #define **IOMUXC\_SD1\_DATA5\_UART2\_RTS\_B** 0x303300A8, 0x4, 0x303305EC, 0x1, 0x30330308
- #define **IOMUXC\_SD1\_DATA5\_GPIO2\_IO07** 0x303300A8, 0x5, 0x00000000, 0x0, 0x30330308
- #define **IOMUXC\_SD1\_DATA6\_USDHC1\_DATA6** 0x303300AC, 0x0, 0x00000000, 0x0, 0x3033030C
- #define **IOMUXC\_SD1\_DATA6\_ENET1\_RGMII\_RX\_CTL** 0x303300AC, 0x1, 0x30330588, 0x0, 0x3033030C
- #define **IOMUXC\_SD1\_DATA6\_I2C2\_SCL** 0x303300AC, 0x3, 0x303305AC, 0x0, 0x3033030C
- #define **IOMUXC\_SD1\_DATA6\_UART3\_TX** 0x303300AC, 0x4, 0x00000000, 0x0, 0x3033030C
- #define **IOMUXC\_SD1\_DATA6\_UART3\_RX** 0x303300AC, 0x4, 0x303305F8, 0x0, 0x3033030C
- #define **IOMUXC\_SD1\_DATA6\_GPIO2\_IO08** 0x303300AC, 0x5, 0x00000000, 0x0, 0x3033030C
- #define **IOMUXC\_SD1\_DATA7\_USDHC1\_DATA7** 0x303300B0, 0x0, 0x00000000, 0x0, 0x30330310
- #define **IOMUXC\_SD1\_DATA7\_ENET1\_RX\_ER** 0x303300B0, 0x1, 0x3033058C, 0x0, 0x30330310
- #define **IOMUXC\_SD1\_DATA7\_I2C2\_SDA** 0x303300B0, 0x3, 0x303305B0, 0x0, 0x30330310
- #define **IOMUXC\_SD1\_DATA7\_UART3\_RX** 0x303300B0, 0x4, 0x303305F8, 0x1, 0x30330310
- #define **IOMUXC\_SD1\_DATA7\_UART3\_TX** 0x303300B0, 0x4, 0x00000000, 0x0, 0x30330310
- #define **IOMUXC\_SD1\_DATA7\_GPIO2\_IO09** 0x303300B0, 0x5, 0x00000000, 0x0, 0x30330310
- #define **IOMUXC\_SD1\_RESET\_B\_USDHC1\_RESET\_B** 0x303300B4, 0x0, 0x00000000, 0x0, 0x30330314
- #define **IOMUXC\_SD1\_RESET\_B\_ENET1\_TX\_CLK** 0x303300B4, 0x1, 0x30330578, 0x0, 0x30330314
- #define **IOMUXC\_SD1\_RESET\_B\_I2C3\_SCL** 0x303300B4, 0x3, 0x303305B4, 0x0, 0x30330314

- #define **IOMUXC\_SD1\_RESET\_B\_UART3\_RTS\_B** 0x303300B4, 0x4, 0x303305F4, 0x0, 0x30330314
- #define **IOMUXC\_SD1\_RESET\_B\_UART3\_CTS\_B** 0x303300B4, 0x4, 0x00000000, 0x0, 0x30330314
- #define **IOMUXC\_SD1\_RESET\_B\_GPIO2\_IO10** 0x303300B4, 0x5, 0x00000000, 0x0, 0x30330314
- #define **IOMUXC\_SD1\_STROBE\_USDHC1\_STROBE** 0x303300B8, 0x0, 0x00000000, 0x0, 0x30330318
- #define **IOMUXC\_SD1\_STROBE\_I2C3\_SDA** 0x303300B8, 0x3, 0x303305B8, 0x0, 0x30330318
- #define **IOMUXC\_SD1\_STROBE\_UART3\_CTS\_B** 0x303300B8, 0x4, 0x00000000, 0x0, 0x30330318
- #define **IOMUXC\_SD1\_STROBE\_UART3\_RTS\_B** 0x303300B8, 0x4, 0x303305F4, 0x1, 0x30330318
- #define **IOMUXC\_SD1\_STROBE\_GPIO2\_IO11** 0x303300B8, 0x5, 0x00000000, 0x0, 0x30330318
- #define **IOMUXC\_SD2\_CD\_B\_USDHC2\_CD\_B** 0x303300BC, 0x0, 0x00000000, 0x0, 0x3033031C
- #define **IOMUXC\_SD2\_CD\_B\_GPIO2\_IO12** 0x303300BC, 0x5, 0x00000000, 0x0, 0x3033031C
- #define **IOMUXC\_SD2\_CLK\_USDHC2\_CLK** 0x303300C0, 0x0, 0x00000000, 0x0, 0x30330320
- #define **IOMUXC\_SD2\_CLK\_ECSPI2\_SCLK** 0x303300C0, 0x2, 0x30330568, 0x0, 0x30330320
- #define **IOMUXC\_SD2\_CLK\_UART4\_RX** 0x303300C0, 0x3, 0x30330600, 0x0, 0x30330320
- #define **IOMUXC\_SD2\_CLK\_UART4\_TX** 0x303300C0, 0x3, 0x00000000, 0x0, 0x30330320
- #define **IOMUXC\_SD2\_CLK\_GPIO2\_IO13** 0x303300C0, 0x5, 0x00000000, 0x0, 0x30330320
- #define **IOMUXC\_SD2\_CMD\_USDHC2\_CMD** 0x303300C4, 0x0, 0x00000000, 0x0, 0x30330324
- #define **IOMUXC\_SD2\_CMD\_ECSPI2\_MOSI** 0x303300C4, 0x2, 0x30330570, 0x0, 0x30330324
- #define **IOMUXC\_SD2\_CMD\_UART4\_TX** 0x303300C4, 0x3, 0x00000000, 0x0, 0x30330324
- #define **IOMUXC\_SD2\_CMD\_UART4\_RX** 0x303300C4, 0x3, 0x30330600, 0x1, 0x30330324
- #define **IOMUXC\_SD2\_CMD\_AUDIOMIX\_PDM\_CLK** 0x303300C4, 0x4, 0x00000000, 0x0, 0x30330324
- #define **IOMUXC\_SD2\_CMD\_GPIO2\_IO14** 0x303300C4, 0x5, 0x00000000, 0x0, 0x30330324
- #define **IOMUXC\_SD2\_DATA0\_USDHC2\_DATA0** 0x303300C8, 0x0, 0x00000000, 0x0, 0x30330328
- #define **IOMUXC\_SD2\_DATA0\_I2C4\_SDA** 0x303300C8, 0x2, 0x303305C0, 0x1, 0x30330328
- #define **IOMUXC\_SD2\_DATA0\_UART2\_RX** 0x303300C8, 0x3, 0x303305F0, 0x2, 0x30330328
- #define **IOMUXC\_SD2\_DATA0\_UART2\_TX** 0x303300C8, 0x3, 0x00000000, 0x0, 0x30330328
- #define **IOMUXC\_SD2\_DATA0\_AUDIOMIX\_PDM\_BIT\_STREAM0** 0x303300C8, 0x4, 0x303304C0, 0x2, 0x30330328
- #define **IOMUXC\_SD2\_DATA0\_GPIO2\_IO15** 0x303300C8, 0x5, 0x00000000, 0x0, 0x30330328
- #define **IOMUXC\_SD2\_DATA1\_USDHC2\_DATA1** 0x303300CC, 0x0, 0x00000000, 0x0, 0x3033032C
- #define **IOMUXC\_SD2\_DATA1\_I2C4\_SCL** 0x303300CC, 0x2, 0x303305BC, 0x1, 0x3033032C
- #define **IOMUXC\_SD2\_DATA1\_UART2\_TX** 0x303300CC, 0x3, 0x00000000, 0x0, 0x3033032C
- #define **IOMUXC\_SD2\_DATA1\_UART2\_RX** 0x303300CC, 0x3, 0x303305F0, 0x3, 0x3033032C
- #define **IOMUXC\_SD2\_DATA1\_AUDIOMIX\_PDM\_BIT\_STREAM1** 0x303300CC, 0x4, 0x303304C4, 0x2, 0x3033032C
- #define **IOMUXC\_SD2\_DATA1\_GPIO2\_IO16** 0x303300CC, 0x5, 0x00000000, 0x0, 0x3033032C
- #define **IOMUXC\_SD2\_DATA2\_USDHC2\_DATA2** 0x303300D0, 0x0, 0x00000000, 0x0, 0x30330330
- #define **IOMUXC\_SD2\_DATA2\_ECSPI2\_SS0** 0x303300D0, 0x2, 0x30330574, 0x0, 0x30330330

- #define **IOMUXC\_SD2\_DATA2\_AUDIOMIX\_SPDIF1\_OUT** 0x303300D0, 0x3, 0x00000000, 0x0, 0x30330330
- #define **IOMUXC\_SD2\_DATA2\_AUDIOMIX\_PDM\_BIT\_STREAM2** 0x303300D0, 0x4, 0x303304C8, 0x2, 0x30330330
- #define **IOMUXC\_SD2\_DATA2\_GPIO2\_IO17** 0x303300D0, 0x5, 0x00000000, 0x0, 0x30330330
- #define **IOMUXC\_SD2\_DATA3\_USDHC2\_DATA3** 0x303300D4, 0x0, 0x00000000, 0x0, 0x30330334
- #define **IOMUXC\_SD2\_DATA3\_ECSPI2\_MISO** 0x303300D4, 0x2, 0x3033056C, 0x0, 0x30330334
- #define **IOMUXC\_SD2\_DATA3\_AUDIOMIX\_SPDIF1\_IN** 0x303300D4, 0x3, 0x30330544, 0x1, 0x30330334
- #define **IOMUXC\_SD2\_DATA3\_AUDIOMIX\_PDM\_BIT\_STREAM3** 0x303300D4, 0x4, 0x303304CC, 0x2, 0x30330334
- #define **IOMUXC\_SD2\_DATA3\_GPIO2\_IO18** 0x303300D4, 0x5, 0x00000000, 0x0, 0x30330334
- #define **IOMUXC\_SD2\_RESET\_B\_USDHC2\_RESET\_B** 0x303300D8, 0x0, 0x00000000, 0x0, 0x30330338
- #define **IOMUXC\_SD2\_RESET\_B\_GPIO2\_IO19** 0x303300D8, 0x5, 0x00000000, 0x0, 0x30330338
- #define **IOMUXC\_SD2\_WP\_USDHC2\_WP** 0x303300DC, 0x0, 0x00000000, 0x0, 0x3033033C
- #define **IOMUXC\_SD2\_WP\_GPIO2\_IO20** 0x303300DC, 0x5, 0x00000000, 0x0, 0x3033033C
- #define **IOMUXC\_SD2\_WP\_CORESIGHT\_EVENTI** 0x303300DC, 0x6, 0x00000000, 0x0, 0x3033033C
- #define **IOMUXC\_NAND\_ALE\_NAND\_ALE** 0x303300E0, 0x0, 0x00000000, 0x0, 0x30330340
- #define **IOMUXC\_NAND\_ALE\_FLEXSPI\_A\_SCLK** 0x303300E0, 0x1, 0x00000000, 0x0, 0x30330340
- #define **IOMUXC\_NAND\_ALE\_AUDIOMIX\_SAI3\_TX\_BCLK** 0x303300E0, 0x2, 0x303304-E8, 0x0, 0x30330340
- #define **IOMUXC\_NAND\_ALE\_ISP\_FL\_TRIG\_0** 0x303300E0, 0x3, 0x303305D4, 0x1, 0x30330340
- #define **IOMUXC\_NAND\_ALE\_UART3\_RX** 0x303300E0, 0x4, 0x303305F8, 0x2, 0x30330340
- #define **IOMUXC\_NAND\_ALE\_UART3\_TX** 0x303300E0, 0x4, 0x00000000, 0x0, 0x30330340
- #define **IOMUXC\_NAND\_ALE\_GPIO3\_IO00** 0x303300E0, 0x5, 0x00000000, 0x0, 0x30330340
- #define **IOMUXC\_NAND\_ALE\_CORESIGHT\_TRACE\_CLK** 0x303300E0, 0x6, 0x00000000, 0x0, 0x30330340
- #define **IOMUXC\_NAND\_CE0\_B\_NAND\_CE0\_B** 0x303300E4, 0x0, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC\_NAND\_CE0\_B\_FLEXSPI\_A\_SS0\_B** 0x303300E4, 0x1, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC\_NAND\_CE0\_B\_AUDIOMIX\_SAI3\_TX\_DATA0** 0x303300E4, 0x2, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC\_NAND\_CE0\_B\_ISP\_SHUTTER\_TRIG\_0** 0x303300E4, 0x3, 0x303305DC, 0x1, 0x30330344
- #define **IOMUXC\_NAND\_CE0\_B\_UART3\_TX** 0x303300E4, 0x4, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC\_NAND\_CE0\_B\_UART3\_RX** 0x303300E4, 0x4, 0x303305F8, 0x3, 0x30330344
- #define **IOMUXC\_NAND\_CE0\_B\_GPIO3\_IO01** 0x303300E4, 0x5, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC\_NAND\_CE0\_B\_CORESIGHT\_TRACE\_CTL** 0x303300E4, 0x6, 0x00000000, 0x0, 0x30330344
- #define **IOMUXC\_NAND\_CE1\_B\_NAND\_CE1\_B** 0x303300E8, 0x0, 0x00000000, 0x0, 0x30330348
- #define **IOMUXC\_NAND\_CE1\_B\_FLEXSPI\_A\_SS1\_B** 0x303300E8, 0x1, 0x00000000, 0x0,

- 0x30330348
- #define **IOMUXC\_NAND\_CE1\_B\_USDHC3\_STROBE** 0x303300E8, 0x2, 0x30330630, 0x1, 0x30330348
  - #define **IOMUXC\_NAND\_CE1\_B\_I2C4\_SCL** 0x303300E8, 0x4, 0x303305BC, 0x2, 0x30330348
  - #define **IOMUXC\_NAND\_CE1\_B\_GPIO3\_IO02** 0x303300E8, 0x5, 0x00000000, 0x0, 0x30330348
  - #define **IOMUXC\_NAND\_CE1\_B\_CORESIGHT\_TRACE00** 0x303300E8, 0x6, 0x00000000, 0x0, 0x30330348
  - #define **IOMUXC\_NAND\_CE2\_B\_NAND\_CE2\_B** 0x303300EC, 0x0, 0x00000000, 0x0, 0x3033034C
  - #define **IOMUXC\_NAND\_CE2\_B\_FLEXSPI\_B\_SS0\_B** 0x303300EC, 0x1, 0x00000000, 0x0, 0x3033034C
  - #define **IOMUXC\_NAND\_CE2\_B\_USDHC3\_DATA5** 0x303300EC, 0x2, 0x30330624, 0x1, 0x3033034C
  - #define **IOMUXC\_NAND\_CE2\_B\_I2C4\_SDA** 0x303300EC, 0x4, 0x303305C0, 0x2, 0x3033034C
  - #define **IOMUXC\_NAND\_CE2\_B\_GPIO3\_IO03** 0x303300EC, 0x5, 0x00000000, 0x0, 0x3033034C
  - #define **IOMUXC\_NAND\_CE2\_B\_CORESIGHT\_TRACE01** 0x303300EC, 0x6, 0x00000000, 0x0, 0x3033034C
  - #define **IOMUXC\_NAND\_CE3\_B\_NAND\_CE3\_B** 0x303300F0, 0x0, 0x00000000, 0x0, 0x30330350
  - #define **IOMUXC\_NAND\_CE3\_B\_FLEXSPI\_B\_SS1\_B** 0x303300F0, 0x1, 0x00000000, 0x0, 0x30330350
  - #define **IOMUXC\_NAND\_CE3\_B\_USDHC3\_DATA6** 0x303300F0, 0x2, 0x30330628, 0x1, 0x30330350
  - #define **IOMUXC\_NAND\_CE3\_B\_I2C3\_SDA** 0x303300F0, 0x4, 0x303305B8, 0x1, 0x30330350
  - #define **IOMUXC\_NAND\_CE3\_B\_GPIO3\_IO04** 0x303300F0, 0x5, 0x00000000, 0x0, 0x30330350
  - #define **IOMUXC\_NAND\_CE3\_B\_CORESIGHT\_TRACE02** 0x303300F0, 0x6, 0x00000000, 0x0, 0x30330350
  - #define **IOMUXC\_NAND\_CLE\_NAND\_CLE** 0x303300F4, 0x0, 0x00000000, 0x0, 0x30330354
  - #define **IOMUXC\_NAND\_CLE\_FLEXSPI\_B\_SCLK** 0x303300F4, 0x1, 0x00000000, 0x0, 0x30330354
  - #define **IOMUXC\_NAND\_CLE\_USDHC3\_DATA7** 0x303300F4, 0x2, 0x3033062C, 0x1, 0x30330354
  - #define **IOMUXC\_NAND\_CLE\_UART4\_RX** 0x303300F4, 0x4, 0x30330600, 0x2, 0x30330354
  - #define **IOMUXC\_NAND\_CLE\_UART4\_TX** 0x303300F4, 0x4, 0x00000000, 0x0, 0x30330354
  - #define **IOMUXC\_NAND\_CLE\_GPIO3\_IO05** 0x303300F4, 0x5, 0x00000000, 0x0, 0x30330354
  - #define **IOMUXC\_NAND\_CLE\_CORESIGHT\_TRACE03** 0x303300F4, 0x6, 0x00000000, 0x0, 0x30330354
  - #define **IOMUXC\_NAND\_DATA00\_NAND\_DATA00** 0x303300F8, 0x0, 0x00000000, 0x0, 0x30330358
  - #define **IOMUXC\_NAND\_DATA00\_FLEXSPI\_A\_DATA0** 0x303300F8, 0x1, 0x00000000, 0x0, 0x30330358
  - #define **IOMUXC\_NAND\_DATA00\_AUDIOMIX\_SAI3\_RX\_DATA0** 0x303300F8, 0x2, 0x303304E4, 0x0, 0x30330358
  - #define **IOMUXC\_NAND\_DATA00\_ISP\_FLASH\_TRIG\_0** 0x303300F8, 0x3, 0x00000000, 0x0, 0x30330358
  - #define **IOMUXC\_NAND\_DATA00\_UART4\_RX** 0x303300F8, 0x4, 0x30330600, 0x3,

- 0x30330358
- #define **IOMUXC\_NAND\_DATA00\_UART4\_TX** 0x303300F8, 0x4, 0x00000000, 0x0,
- 0x30330358
- #define **IOMUXC\_NAND\_DATA00\_GPIO3\_IO06** 0x303300F8, 0x5, 0x00000000, 0x0,
- 0x30330358
- #define **IOMUXC\_NAND\_DATA00\_CORESIGHT\_TRACE04** 0x303300F8, 0x6, 0x00000000,
- 0x0, 0x30330358
- #define **IOMUXC\_NAND\_DATA01\_NAND\_DATA01** 0x303300FC, 0x0, 0x00000000, 0x0,
- 0x3033035C
- #define **IOMUXC\_NAND\_DATA01\_FLEXSPI\_A\_DATA1** 0x303300FC, 0x1, 0x00000000,
- 0x0, 0x3033035C
- #define **IOMUXC\_NAND\_DATA01\_AUDIOMIX\_SAI3\_TX\_SYNC** 0x303300FC, 0x2,
- 0x303304EC, 0x0, 0x3033035C
- #define **IOMUXC\_NAND\_DATA01\_ISP\_PRELIGHT\_TRIG\_0** 0x303300FC, 0x3, 0x00000000,
- 0x0, 0x3033035C
- #define **IOMUXC\_NAND\_DATA01\_UART4\_TX** 0x303300FC, 0x4, 0x00000000, 0x0,
- 0x3033035C
- #define **IOMUXC\_NAND\_DATA01\_UART4\_RX** 0x303300FC, 0x4, 0x30330600, 0x4,
- 0x3033035C
- #define **IOMUXC\_NAND\_DATA01\_GPIO3\_IO07** 0x303300FC, 0x5, 0x00000000, 0x0,
- 0x3033035C
- #define **IOMUXC\_NAND\_DATA01\_CORESIGHT\_TRACE05** 0x303300FC, 0x6, 0x00000000,
- 0x0, 0x3033035C
- #define **IOMUXC\_NAND\_DATA02\_NAND\_DATA02** 0x30330100, 0x0, 0x00000000, 0x0,
- 0x30330360
- #define **IOMUXC\_NAND\_DATA02\_FLEXSPI\_A\_DATA2** 0x30330100, 0x1, 0x00000000, 0x0,
- 0x30330360
- #define **IOMUXC\_NAND\_DATA02\_USDHC3\_CD\_B** 0x30330100, 0x2, 0x30330608, 0x2,
- 0x30330360
- #define **IOMUXC\_NAND\_DATA02\_UART4\_CTS\_B** 0x30330100, 0x3, 0x00000000, 0x0,
- 0x30330360
- #define **IOMUXC\_NAND\_DATA02\_UART4\_RTS\_B** 0x30330100, 0x3, 0x303305FC, 0x0,
- 0x30330360
- #define **IOMUXC\_NAND\_DATA02\_I2C4\_SDA** 0x30330100, 0x4, 0x303305C0, 0x3, 0x30330360
- #define **IOMUXC\_NAND\_DATA02\_GPIO3\_IO08** 0x30330100, 0x5, 0x00000000, 0x0,
- 0x30330360
- #define **IOMUXC\_NAND\_DATA02\_CORESIGHT\_TRACE06** 0x30330100, 0x6, 0x00000000,
- 0x0, 0x30330360
- #define **IOMUXC\_NAND\_DATA03\_NAND\_DATA03** 0x30330104, 0x0, 0x00000000, 0x0,
- 0x30330364
- #define **IOMUXC\_NAND\_DATA03\_FLEXSPI\_A\_DATA3** 0x30330104, 0x1, 0x00000000, 0x0,
- 0x30330364
- #define **IOMUXC\_NAND\_DATA03\_USDHC3\_WP** 0x30330104, 0x2, 0x30330634, 0x2,
- 0x30330364
- #define **IOMUXC\_NAND\_DATA03\_UART4\_RTS\_B** 0x30330104, 0x3, 0x303305FC, 0x1,
- 0x30330364
- #define **IOMUXC\_NAND\_DATA03\_UART4\_CTS\_B** 0x30330104, 0x3, 0x00000000, 0x0,
- 0x30330364
- #define **IOMUXC\_NAND\_DATA03\_ISP\_FL\_TRIG\_1** 0x30330104, 0x4, 0x303305D8, 0x1,
- 0x30330364

- #define **IOMUXC\_NAND\_DATA03\_GPIO3\_IO09** 0x30330104, 0x5, 0x00000000, 0x0, 0x30330364
- #define **IOMUXC\_NAND\_DATA03\_CORESIGHT\_TRACE07** 0x30330104, 0x6, 0x00000000, 0x0, 0x30330364
- #define **IOMUXC\_NAND\_DATA04\_NAND\_DATA04** 0x30330108, 0x0, 0x00000000, 0x0, 0x30330368
- #define **IOMUXC\_NAND\_DATA04\_FLEXSPI\_B\_DATA0** 0x30330108, 0x1, 0x00000000, 0x0, 0x30330368
- #define **IOMUXC\_NAND\_DATA04\_USDHC3\_DATA0** 0x30330108, 0x2, 0x30330610, 0x1, 0x30330368
- #define **IOMUXC\_NAND\_DATA04\_FLEXSPI\_A\_DATA4** 0x30330108, 0x3, 0x00000000, 0x0, 0x30330368
- #define **IOMUXC\_NAND\_DATA04\_ISP\_SHUTTER\_TRIG\_1** 0x30330108, 0x4, 0x303305E0, 0x1, 0x30330368
- #define **IOMUXC\_NAND\_DATA04\_GPIO3\_IO10** 0x30330108, 0x5, 0x00000000, 0x0, 0x30330368
- #define **IOMUXC\_NAND\_DATA04\_CORESIGHT\_TRACE08** 0x30330108, 0x6, 0x00000000, 0x0, 0x30330368
- #define **IOMUXC\_NAND\_DATA05\_NAND\_DATA05** 0x3033010C, 0x0, 0x00000000, 0x0, 0x3033036C
- #define **IOMUXC\_NAND\_DATA05\_FLEXSPI\_B\_DATA1** 0x3033010C, 0x1, 0x00000000, 0x0, 0x3033036C
- #define **IOMUXC\_NAND\_DATA05\_USDHC3\_DATA1** 0x3033010C, 0x2, 0x30330614, 0x1, 0x3033036C
- #define **IOMUXC\_NAND\_DATA05\_FLEXSPI\_A\_DATA5** 0x3033010C, 0x3, 0x00000000, 0x0, 0x3033036C
- #define **IOMUXC\_NAND\_DATA05\_ISP\_FLASH\_TRIG\_1** 0x3033010C, 0x4, 0x00000000, 0x0, 0x3033036C
- #define **IOMUXC\_NAND\_DATA05\_GPIO3\_IO11** 0x3033010C, 0x5, 0x00000000, 0x0, 0x3033036C
- #define **IOMUXC\_NAND\_DATA05\_CORESIGHT\_TRACE09** 0x3033010C, 0x6, 0x00000000, 0x0, 0x3033036C
- #define **IOMUXC\_NAND\_DATA06\_NAND\_DATA06** 0x30330110, 0x0, 0x00000000, 0x0, 0x30330370
- #define **IOMUXC\_NAND\_DATA06\_FLEXSPI\_B\_DATA2** 0x30330110, 0x1, 0x00000000, 0x0, 0x30330370
- #define **IOMUXC\_NAND\_DATA06\_USDHC3\_DATA2** 0x30330110, 0x2, 0x30330618, 0x1, 0x30330370
- #define **IOMUXC\_NAND\_DATA06\_FLEXSPI\_A\_DATA6** 0x30330110, 0x3, 0x00000000, 0x0, 0x30330370
- #define **IOMUXC\_NAND\_DATA06\_ISP\_PRELIGHT\_TRIG\_1** 0x30330110, 0x4, 0x00000000, 0x0, 0x30330370
- #define **IOMUXC\_NAND\_DATA06\_GPIO3\_IO12** 0x30330110, 0x5, 0x00000000, 0x0, 0x30330370
- #define **IOMUXC\_NAND\_DATA06\_CORESIGHT\_TRACE10** 0x30330110, 0x6, 0x00000000, 0x0, 0x30330370
- #define **IOMUXC\_NAND\_DATA07\_NAND\_DATA07** 0x30330114, 0x0, 0x00000000, 0x0, 0x30330374
- #define **IOMUXC\_NAND\_DATA07\_FLEXSPI\_B\_DATA3** 0x30330114, 0x1, 0x00000000, 0x0,

- 0x30330374
- #define **IOMUXC\_NAND\_DATA07\_USDHC3\_DATA3** 0x30330114, 0x2, 0x3033061C, 0x1, 0x30330374
- #define **IOMUXC\_NAND\_DATA07\_FLEXSPI\_A\_DATA7** 0x30330114, 0x3, 0x00000000, 0x0, 0x30330374
- #define **IOMUXC\_NAND\_DATA07\_ISP\_SHUTTER\_OPEN\_1** 0x30330114, 0x4, 0x00000000, 0x0, 0x30330374
- #define **IOMUXC\_NAND\_DATA07\_GPIO3\_IO13** 0x30330114, 0x5, 0x00000000, 0x0, 0x30330374
- #define **IOMUXC\_NAND\_DATA07\_CORESIGHT\_TRACE11** 0x30330114, 0x6, 0x00000000, 0x0, 0x30330374
- #define **IOMUXC\_NAND\_DQS\_NAND\_DQS** 0x30330118, 0x0, 0x00000000, 0x0, 0x30330378
- #define **IOMUXC\_NAND\_DQS\_FLEXSPI\_A\_DQS** 0x30330118, 0x1, 0x00000000, 0x0, 0x30330378
- #define **IOMUXC\_NAND\_DQS\_AUDIOMIX\_SAI3\_MCLK** 0x30330118, 0x2, 0x303304E0, 0x0, 0x30330378
- #define **IOMUXC\_NAND\_DQS\_ISP\_SHUTTER\_OPEN\_0** 0x30330118, 0x3, 0x00000000, 0x0, 0x30330378
- #define **IOMUXC\_NAND\_DQS\_I2C3\_SCL** 0x30330118, 0x4, 0x303305B4, 0x1, 0x30330378
- #define **IOMUXC\_NAND\_DQS\_GPIO3\_IO14** 0x30330118, 0x5, 0x00000000, 0x0, 0x30330378
- #define **IOMUXC\_NAND\_DQS\_CORESIGHT\_TRACE12** 0x30330118, 0x6, 0x00000000, 0x0, 0x30330378
- #define **IOMUXC\_NAND\_RE\_B\_NAND\_RE\_B** 0x3033011C, 0x0, 0x00000000, 0x0, 0x3033037-C
- #define **IOMUXC\_NAND\_RE\_B\_FLEXSPI\_B\_DQS** 0x3033011C, 0x1, 0x00000000, 0x0, 0x3033037C
- #define **IOMUXC\_NAND\_RE\_B\_USDHC3\_DATA4** 0x3033011C, 0x2, 0x30330620, 0x1, 0x3033037C
- #define **IOMUXC\_NAND\_RE\_B\_UART4\_TX** 0x3033011C, 0x4, 0x00000000, 0x0, 0x3033037-C
- #define **IOMUXC\_NAND\_RE\_B\_UART4\_RX** 0x3033011C, 0x4, 0x30330600, 0x5, 0x3033037-C
- #define **IOMUXC\_NAND\_RE\_B\_GPIO3\_IO15** 0x3033011C, 0x5, 0x00000000, 0x0, 0x3033037-C
- #define **IOMUXC\_NAND\_RE\_B\_CORESIGHT\_TRACE13** 0x3033011C, 0x6, 0x00000000, 0x0, 0x3033037C
- #define **IOMUXC\_NAND\_READY\_B\_NAND\_READY\_B** 0x30330120, 0x0, 0x00000000, 0x0, 0x30330380
- #define **IOMUXC\_NAND\_READY\_B\_USDHC3\_RESET\_B** 0x30330120, 0x2, 0x00000000, 0x0, 0x30330380
- #define **IOMUXC\_NAND\_READY\_B\_I2C3\_SCL** 0x30330120, 0x4, 0x303305B4, 0x2, 0x30330380
- #define **IOMUXC\_NAND\_READY\_B\_GPIO3\_IO16** 0x30330120, 0x5, 0x00000000, 0x0, 0x30330380
- #define **IOMUXC\_NAND\_READY\_B\_CORESIGHT\_TRACE14** 0x30330120, 0x6, 0x00000000, 0x0, 0x30330380
- #define **IOMUXC\_NAND\_WE\_B\_NAND\_WE\_B** 0x30330124, 0x0, 0x00000000, 0x0, 0x30330384
- #define **IOMUXC\_NAND\_WE\_B\_USDHC3\_CLK** 0x30330124, 0x2, 0x30330604, 0x1, 0x30330384

- #define **IOMUXC\_NAND\_WE\_B\_I2C3\_SDA** 0x30330124, 0x4, 0x303305B8, 0x2, 0x30330384
- #define **IOMUXC\_NAND\_WE\_B\_GPIO3\_IO17** 0x30330124, 0x5, 0x00000000, 0x0, 0x30330384
- #define **IOMUXC\_NAND\_WE\_B\_CORESIGHT\_TRACE15** 0x30330124, 0x6, 0x00000000, 0x0, 0x30330384
- #define **IOMUXC\_NAND\_WP\_B\_NAND\_WP\_B** 0x30330128, 0x0, 0x00000000, 0x0, 0x30330388
- #define **IOMUXC\_NAND\_WP\_B\_USDHC3\_CMD** 0x30330128, 0x2, 0x3033060C, 0x1, 0x30330388
- #define **IOMUXC\_NAND\_WP\_B\_I2C4\_SCL** 0x30330128, 0x4, 0x303305BC, 0x3, 0x30330388
- #define **IOMUXC\_NAND\_WP\_B\_GPIO3\_IO18** 0x30330128, 0x5, 0x00000000, 0x0, 0x30330388
- #define **IOMUXC\_NAND\_WP\_B\_CORESIGHT\_EVENTO** 0x30330128, 0x6, 0x00000000, 0x0, 0x30330388
- #define **IOMUXC\_SAI5\_RXFS\_AUDIOMIX\_SAI5\_RX\_SYNC** 0x3033012C, 0x0, 0x30330508, 0x0, 0x3033038C
- #define **IOMUXC\_SAI5\_RXFS\_AUDIOMIX\_SAI1\_TX\_DATA0** 0x3033012C, 0x1, 0x00000000, 0x0, 0x3033038C
- #define **IOMUXC\_SAI5\_RXFS\_PWM4\_OUT** 0x3033012C, 0x2, 0x00000000, 0x0, 0x3033038C
- #define **IOMUXC\_SAI5\_RXFS\_I2C6\_SCL** 0x3033012C, 0x3, 0x303305CC, 0x1, 0x3033038C
- #define **IOMUXC\_SAI5\_RXFS\_GPIO3\_IO19** 0x3033012C, 0x5, 0x00000000, 0x0, 0x3033038C
- #define **IOMUXC\_SAI5\_RXC\_AUDIOMIX\_SAI5\_RX\_BCLK** 0x30330130, 0x0, 0x303304F4, 0x0, 0x30330390
- #define **IOMUXC\_SAI5\_RXC\_AUDIOMIX\_SAI1\_TX\_DATA1** 0x30330130, 0x1, 0x00000000, 0x0, 0x30330390
- #define **IOMUXC\_SAI5\_RXC\_PWM3\_OUT** 0x30330130, 0x2, 0x00000000, 0x0, 0x30330390
- #define **IOMUXC\_SAI5\_RXC\_I2C6\_SDA** 0x30330130, 0x3, 0x303305D0, 0x1, 0x30330390
- #define **IOMUXC\_SAI5\_RXC\_AUDIOMIX\_PDM\_CLK** 0x30330130, 0x4, 0x00000000, 0x0, 0x30330390
- #define **IOMUXC\_SAI5\_RXC\_GPIO3\_IO20** 0x30330130, 0x5, 0x00000000, 0x0, 0x30330390
- #define **IOMUXC\_SAI5\_RXD0\_AUDIOMIX\_SAI5\_RX\_DATA0** 0x30330134, 0x0, 0x303304F8, 0x0, 0x30330394
- #define **IOMUXC\_SAI5\_RXD0\_AUDIOMIX\_SAI1\_TX\_DATA2** 0x30330134, 0x1, 0x00000000, 0x0, 0x30330394
- #define **IOMUXC\_SAI5\_RXD0\_PWM2\_OUT** 0x30330134, 0x2, 0x00000000, 0x0, 0x30330394
- #define **IOMUXC\_SAI5\_RXD0\_I2C5\_SCL** 0x30330134, 0x3, 0x303305C4, 0x1, 0x30330394
- #define **IOMUXC\_SAI5\_RXD0\_AUDIOMIX\_PDM\_BIT\_STREAM0** 0x30330134, 0x4, 0x303304C0, 0x3, 0x30330394
- #define **IOMUXC\_SAI5\_RXD0\_GPIO3\_IO21** 0x30330134, 0x5, 0x00000000, 0x0, 0x30330394
- #define **IOMUXC\_SAI5\_RXD1\_AUDIOMIX\_SAI5\_RX\_DATA1** 0x30330138, 0x0, 0x303304FC, 0x0, 0x30330398
- #define **IOMUXC\_SAI5\_RXD1\_AUDIOMIX\_SAI1\_TX\_DATA3** 0x30330138, 0x1, 0x00000000, 0x0, 0x30330398
- #define **IOMUXC\_SAI5\_RXD1\_AUDIOMIX\_SAI1\_TX\_SYNC** 0x30330138, 0x2, 0x303304D8, 0x0, 0x30330398
- #define **IOMUXC\_SAI5\_RXD1\_AUDIOMIX\_SAI5\_TX\_SYNC** 0x30330138, 0x3, 0x30330510, 0x0, 0x30330398
- #define **IOMUXC\_SAI5\_RXD1\_AUDIOMIX\_PDM\_BIT\_STREAM1** 0x30330138, 0x4, 0x303304C4, 0x3, 0x30330398
- #define **IOMUXC\_SAI5\_RXD1\_GPIO3\_IO22** 0x30330138, 0x5, 0x00000000, 0x0, 0x30330398
- #define **IOMUXC\_SAI5\_RXD1\_CAN1\_TX** 0x30330138, 0x6, 0x00000000, 0x0, 0x30330398

- #define **IOMUXC\_SAI5\_RXD2\_AUDIOMIX\_SAI5\_RX\_DATA2** 0x3033013C, 0x0, 0x30330500, 0x0, 0x3033039C
- #define **IOMUXC\_SAI5\_RXD2\_AUDIOMIX\_SAI1\_TX\_DATA4** 0x3033013C, 0x1, 0x00000000, 0x0, 0x3033039C
- #define **IOMUXC\_SAI5\_RXD2\_AUDIOMIX\_SAI1\_TX\_SYNC** 0x3033013C, 0x2, 0x303304-D8, 0x1, 0x3033039C
- #define **IOMUXC\_SAI5\_RXD2\_AUDIOMIX\_SAI5\_TX\_BCLK** 0x3033013C, 0x3, 0x3033050-C, 0x0, 0x3033039C
- #define **IOMUXC\_SAI5\_RXD2\_AUDIOMIX\_PDM\_BIT\_STREAM2** 0x3033013C, 0x4, 0x303304C8, 0x3, 0x3033039C
- #define **IOMUXC\_SAI5\_RXD2\_GPIO3\_IO23** 0x3033013C, 0x5, 0x00000000, 0x0, 0x3033039-C
- #define **IOMUXC\_SAI5\_RXD2\_CAN1\_RX** 0x3033013C, 0x6, 0x3033054C, 0x0, 0x3033039C
- #define **IOMUXC\_SAI5\_RXD3\_AUDIOMIX\_SAI5\_RX\_DATA3** 0x30330140, 0x0, 0x30330504, 0x0, 0x303303A0
- #define **IOMUXC\_SAI5\_RXD3\_AUDIOMIX\_SAI1\_TX\_DATA5** 0x30330140, 0x1, 0x00000000, 0x0, 0x303303A0
- #define **IOMUXC\_SAI5\_RXD3\_AUDIOMIX\_SAI1\_TX\_SYNC** 0x30330140, 0x2, 0x303304-D8, 0x2, 0x303303A0
- #define **IOMUXC\_SAI5\_RXD3\_AUDIOMIX\_SAI5\_TX\_DATA0** 0x30330140, 0x3, 0x00000000, 0x0, 0x303303A0
- #define **IOMUXC\_SAI5\_RXD3\_AUDIOMIX\_PDM\_BIT\_STREAM3** 0x30330140, 0x4, 0x303304CC, 0x3, 0x303303A0
- #define **IOMUXC\_SAI5\_RXD3\_GPIO3\_IO24** 0x30330140, 0x5, 0x00000000, 0x0, 0x303303A0
- #define **IOMUXC\_SAI5\_RXD3\_CAN2\_TX** 0x30330140, 0x6, 0x00000000, 0x0, 0x303303A0
- #define **IOMUXC\_SAI5\_MCLK\_AUDIOMIX\_SAI5\_MCLK** 0x30330144, 0x0, 0x303304F0, 0x0, 0x303303A4
- #define **IOMUXC\_SAI5\_MCLK\_AUDIOMIX\_SAI1\_TX\_BCLK** 0x30330144, 0x1, 0x303304-D4, 0x0, 0x303303A4
- #define **IOMUXC\_SAI5\_MCLK\_PWM1\_OUT** 0x30330144, 0x2, 0x00000000, 0x0, 0x303303-A4
- #define **IOMUXC\_SAI5\_MCLK\_I2C5\_SDA** 0x30330144, 0x3, 0x303305C8, 0x1, 0x303303A4
- #define **IOMUXC\_SAI5\_MCLK\_GPIO3\_IO25** 0x30330144, 0x5, 0x00000000, 0x0, 0x303303-A4
- #define **IOMUXC\_SAI5\_MCLK\_CAN2\_RX** 0x30330144, 0x6, 0x30330550, 0x0, 0x303303A4
- #define **IOMUXC\_SAI1\_RXFS\_AUDIOMIX\_SAI1\_RX\_SYNC** 0x30330148, 0x0, 0x303304-D0, 0x0, 0x303303A8
- #define **IOMUXC\_SAI1\_RXFS\_ENET1\_1588\_EVENT0\_IN** 0x30330148, 0x4, 0x00000000, 0x0, 0x303303A8
- #define **IOMUXC\_SAI1\_RXFS\_GPIO4\_IO00** 0x30330148, 0x5, 0x00000000, 0x0, 0x303303A8
- #define **IOMUXC\_SAI1\_RXC\_AUDIOMIX\_SAI1\_RX\_BCLK** 0x3033014C, 0x0, 0x00000000, 0x0, 0x303303AC
- #define **IOMUXC\_SAI1\_RXC\_AUDIOMIX\_PDM\_CLK** 0x3033014C, 0x3, 0x00000000, 0x0, 0x303303AC
- #define **IOMUXC\_SAI1\_RXC\_ENET1\_1588\_EVENT0\_OUT** 0x3033014C, 0x4, 0x00000000, 0x0, 0x303303AC
- #define **IOMUXC\_SAI1\_RXC\_GPIO4\_IO01** 0x3033014C, 0x5, 0x00000000, 0x0, 0x303303AC
- #define **IOMUXC\_SAI1\_RXD0\_AUDIOMIX\_SAI1\_RX\_DATA0** 0x30330150, 0x0, 0x00000000, 0x0, 0x303303B0
- #define **IOMUXC\_SAI1\_RXD0\_AUDIOMIX\_SAI1\_TX\_DATA1** 0x30330150, 0x2, 0x00000000,

- 0x0, 0x303303B0
- #define **IOMUXC\_SAI1\_RXD0\_AUDIO MIX\_PDM\_BIT\_STREAM0** 0x30330150, 0x3, 0x303304C0, 0x4, 0x303303B0
  - #define **IOMUXC\_SAI1\_RXD0\_ENET1\_1588\_EVENT1\_IN** 0x30330150, 0x4, 0x00000000, 0x0, 0x303303B0
  - #define **IOMUXC\_SAI1\_RXD0\_GPIO4\_IO02** 0x30330150, 0x5, 0x00000000, 0x0, 0x303303B0
  - #define **IOMUXC\_SAI1\_RXD1\_AUDIO MIX\_SAI1\_RX\_DATA1** 0x30330154, 0x0, 0x00000000, 0x0, 0x303303B4
  - #define **IOMUXC\_SAI1\_RXD1\_AUDIO MIX\_PDM\_BIT\_STREAM1** 0x30330154, 0x3, 0x303304C4, 0x4, 0x303303B4
  - #define **IOMUXC\_SAI1\_RXD1\_ENET1\_1588\_EVENT1\_OUT** 0x30330154, 0x4, 0x00000000, 0x0, 0x303303B4
  - #define **IOMUXC\_SAI1\_RXD1\_GPIO4\_IO03** 0x30330154, 0x5, 0x00000000, 0x0, 0x303303B4
  - #define **IOMUXC\_SAI1\_RXD2\_AUDIO MIX\_SAI1\_RX\_DATA2** 0x30330158, 0x0, 0x00000000, 0x0, 0x303303B8
  - #define **IOMUXC\_SAI1\_RXD2\_AUDIO MIX\_PDM\_BIT\_STREAM2** 0x30330158, 0x3, 0x303304C8, 0x4, 0x303303B8
  - #define **IOMUXC\_SAI1\_RXD2\_ENET1\_MDC** 0x30330158, 0x4, 0x00000000, 0x0, 0x303303-B8
  - #define **IOMUXC\_SAI1\_RXD2\_GPIO4\_IO04** 0x30330158, 0x5, 0x00000000, 0x0, 0x303303B8
  - #define **IOMUXC\_SAI1\_RXD3\_AUDIO MIX\_SAI1\_RX\_DATA3** 0x3033015C, 0x0, 0x00000000, 0x0, 0x303303BC
  - #define **IOMUXC\_SAI1\_RXD3\_AUDIO MIX\_PDM\_BIT\_STREAM3** 0x3033015C, 0x3, 0x303304CC, 0x4, 0x303303BC
  - #define **IOMUXC\_SAI1\_RXD3\_ENET1\_MDIO** 0x3033015C, 0x4, 0x3033057C, 0x1, 0x303303-BC
  - #define **IOMUXC\_SAI1\_RXD3\_GPIO4\_IO05** 0x3033015C, 0x5, 0x00000000, 0x0, 0x303303-BC
  - #define **IOMUXC\_SAI1\_RXD4\_AUDIO MIX\_SAI1\_RX\_DATA4** 0x30330160, 0x0, 0x00000000, 0x0, 0x303303C0
  - #define **IOMUXC\_SAI1\_RXD4\_AUDIO MIX\_SAI6\_TX\_BCLK** 0x30330160, 0x1, 0x30330524, 0x1, 0x303303C0
  - #define **IOMUXC\_SAI1\_RXD4\_AUDIO MIX\_SAI6\_RX\_BCLK** 0x30330160, 0x2, 0x30330518, 0x1, 0x303303C0
  - #define **IOMUXC\_SAI1\_RXD4\_ENET1\_RGMII\_RD0** 0x30330160, 0x4, 0x30330580, 0x1, 0x303303C0
  - #define **IOMUXC\_SAI1\_RXD4\_GPIO4\_IO06** 0x30330160, 0x5, 0x00000000, 0x0, 0x303303C0
  - #define **IOMUXC\_SAI1\_RXD5\_AUDIO MIX\_SAI1\_RX\_DATA5** 0x30330164, 0x0, 0x00000000, 0x0, 0x303303C4
  - #define **IOMUXC\_SAI1\_RXD5\_AUDIO MIX\_SAI6\_TX\_DATA0** 0x30330164, 0x1, 0x00000000, 0x0, 0x303303C4
  - #define **IOMUXC\_SAI1\_RXD5\_AUDIO MIX\_SAI6\_RX\_DATA0** 0x30330164, 0x2, 0x3033051-C, 0x1, 0x303303C4
  - #define **IOMUXC\_SAI1\_RXD5\_AUDIO MIX\_SAI1\_RX\_SYNC** 0x30330164, 0x3, 0x303304-D0, 0x1, 0x303303C4
  - #define **IOMUXC\_SAI1\_RXD5\_ENET1\_RGMII\_RD1** 0x30330164, 0x4, 0x30330584, 0x1, 0x303303C4
  - #define **IOMUXC\_SAI1\_RXD5\_GPIO4\_IO07** 0x30330164, 0x5, 0x00000000, 0x0, 0x303303C4
  - #define **IOMUXC\_SAI1\_RXD6\_AUDIO MIX\_SAI1\_RX\_DATA6** 0x30330168, 0x0, 0x00000000, 0x0, 0x303303C8

- #define **IOMUXC\_SAI1\_RXD6\_AUDIOMIX\_SAI1\_TX\_SYNC** 0x30330168, 0x1, 0x30330528, 0x1, 0x303303C8
- #define **IOMUXC\_SAI1\_RXD6\_AUDIOMIX\_SAI1\_RX\_SYNC** 0x30330168, 0x2, 0x30330520, 0x1, 0x303303C8
- #define **IOMUXC\_SAI1\_RXD6\_ENET1\_RGMII\_RD2** 0x30330168, 0x4, 0x00000000, 0x0, 0x303303C8
- #define **IOMUXC\_SAI1\_RXD6\_GPIO4\_IO08** 0x30330168, 0x5, 0x00000000, 0x0, 0x303303C8
- #define **IOMUXC\_SAI1\_RXD7\_AUDIOMIX\_SAI1\_RX\_DATA7** 0x3033016C, 0x0, 0x00000000, 0x0, 0x303303CC
- #define **IOMUXC\_SAI1\_RXD7\_AUDIOMIX\_SAI1\_MCLK** 0x3033016C, 0x1, 0x30330514, 0x1, 0x303303CC
- #define **IOMUXC\_SAI1\_RXD7\_AUDIOMIX\_SAI1\_TX\_SYNC** 0x3033016C, 0x2, 0x303304-D8, 0x3, 0x303303CC
- #define **IOMUXC\_SAI1\_RXD7\_AUDIOMIX\_SAI1\_TX\_DATA4** 0x3033016C, 0x3, 0x00000000, 0x0, 0x303303CC
- #define **IOMUXC\_SAI1\_RXD7\_ENET1\_RGMII\_RD3** 0x3033016C, 0x4, 0x00000000, 0x0, 0x303303CC
- #define **IOMUXC\_SAI1\_RXD7\_GPIO4\_IO09** 0x3033016C, 0x5, 0x00000000, 0x0, 0x303303-CC
- #define **IOMUXC\_SAI1\_TXFS\_AUDIOMIX\_SAI1\_TX\_SYNC** 0x30330170, 0x0, 0x303304-D8, 0x4, 0x303303D0
- #define **IOMUXC\_SAI1\_TXFS\_ENET1\_RGMII\_RX\_CTL** 0x30330170, 0x4, 0x30330588, 0x1, 0x303303D0
- #define **IOMUXC\_SAI1\_TXFS\_GPIO4\_IO10** 0x30330170, 0x5, 0x00000000, 0x0, 0x303303D0
- #define **IOMUXC\_SAI1\_TXC\_AUDIOMIX\_SAI1\_TX\_BCLK** 0x30330174, 0x0, 0x303304D4, 0x1, 0x303303D4
- #define **IOMUXC\_SAI1\_TXC\_ENET1\_RGMII\_RXC** 0x30330174, 0x4, 0x00000000, 0x0, 0x303303D4
- #define **IOMUXC\_SAI1\_TXC\_GPIO4\_IO11** 0x30330174, 0x5, 0x00000000, 0x0, 0x303303D4
- #define **IOMUXC\_SAI1\_TXD0\_AUDIOMIX\_SAI1\_TX\_DATA0** 0x30330178, 0x0, 0x00000000, 0x0, 0x303303D8
- #define **IOMUXC\_SAI1\_TXD0\_ENET1\_RGMII\_TD0** 0x30330178, 0x4, 0x00000000, 0x0, 0x303303D8
- #define **IOMUXC\_SAI1\_TXD0\_GPIO4\_IO12** 0x30330178, 0x5, 0x00000000, 0x0, 0x303303D8
- #define **IOMUXC\_SAI1\_TXD1\_AUDIOMIX\_SAI1\_TX\_DATA1** 0x3033017C, 0x0, 0x00000000, 0x0, 0x303303DC
- #define **IOMUXC\_SAI1\_TXD1\_ENET1\_RGMII\_TD1** 0x3033017C, 0x4, 0x00000000, 0x0, 0x303303DC
- #define **IOMUXC\_SAI1\_TXD1\_GPIO4\_IO13** 0x3033017C, 0x5, 0x00000000, 0x0, 0x303303-DC
- #define **IOMUXC\_SAI1\_TXD2\_AUDIOMIX\_SAI1\_TX\_DATA2** 0x30330180, 0x0, 0x00000000, 0x0, 0x303303E0
- #define **IOMUXC\_SAI1\_TXD2\_ENET1\_RGMII\_TD2** 0x30330180, 0x4, 0x00000000, 0x0, 0x303303E0
- #define **IOMUXC\_SAI1\_TXD2\_GPIO4\_IO14** 0x30330180, 0x5, 0x00000000, 0x0, 0x303303E0
- #define **IOMUXC\_SAI1\_TXD3\_AUDIOMIX\_SAI1\_TX\_DATA3** 0x30330184, 0x0, 0x00000000, 0x0, 0x303303E4
- #define **IOMUXC\_SAI1\_TXD3\_ENET1\_RGMII\_TD3** 0x30330184, 0x4, 0x00000000, 0x0, 0x303303E4
- #define **IOMUXC\_SAI1\_TXD3\_GPIO4\_IO15** 0x30330184, 0x5, 0x00000000, 0x0, 0x303303E4

- #define **IOMUXC\_SAI1\_TXD4\_AUDIOMIX\_SAI1\_TX\_DATA4** 0x30330188, 0x0, 0x00000000, 0x0, 0x303303E8
- #define **IOMUXC\_SAI1\_TXD4\_AUDIOMIX\_SAI6\_RX\_BCLK** 0x30330188, 0x1, 0x30330518, 0x2, 0x303303E8
- #define **IOMUXC\_SAI1\_TXD4\_AUDIOMIX\_SAI6\_TX\_BCLK** 0x30330188, 0x2, 0x30330524, 0x2, 0x303303E8
- #define **IOMUXC\_SAI1\_TXD4\_ENET1\_RGMII\_TX\_CTL** 0x30330188, 0x4, 0x00000000, 0x0, 0x303303E8
- #define **IOMUXC\_SAI1\_TXD4\_GPIO4\_IO16** 0x30330188, 0x5, 0x00000000, 0x0, 0x303303E8
- #define **IOMUXC\_SAI1\_TXD5\_AUDIOMIX\_SAI1\_TX\_DATA5** 0x3033018C, 0x0, 0x00000000, 0x0, 0x303303EC
- #define **IOMUXC\_SAI1\_TXD5\_AUDIOMIX\_SAI6\_RX\_DATA0** 0x3033018C, 0x1, 0x3033051-C, 0x2, 0x303303EC
- #define **IOMUXC\_SAI1\_TXD5\_AUDIOMIX\_SAI6\_TX\_DATA0** 0x3033018C, 0x2, 0x00000000, 0x0, 0x303303EC
- #define **IOMUXC\_SAI1\_TXD5\_ENET1\_RGMII\_TXC** 0x3033018C, 0x4, 0x00000000, 0x0, 0x303303EC
- #define **IOMUXC\_SAI1\_TXD5\_GPIO4\_IO17** 0x3033018C, 0x5, 0x00000000, 0x0, 0x303303E-C
- #define **IOMUXC\_SAI1\_TXD6\_AUDIOMIX\_SAI1\_TX\_DATA6** 0x30330190, 0x0, 0x00000000, 0x0, 0x303303F0
- #define **IOMUXC\_SAI1\_TXD6\_AUDIOMIX\_SAI6\_RX\_SYNC** 0x30330190, 0x1, 0x30330520, 0x2, 0x303303F0
- #define **IOMUXC\_SAI1\_TXD6\_AUDIOMIX\_SAI6\_TX\_SYNC** 0x30330190, 0x2, 0x30330528, 0x2, 0x303303F0
- #define **IOMUXC\_SAI1\_TXD6\_ENET1\_RX\_ER** 0x30330190, 0x4, 0x3033058C, 0x1, 0x303303F0
- #define **IOMUXC\_SAI1\_TXD6\_GPIO4\_IO18** 0x30330190, 0x5, 0x00000000, 0x0, 0x303303F0
- #define **IOMUXC\_SAI1\_TXD7\_AUDIOMIX\_SAI1\_TX\_DATA7** 0x30330194, 0x0, 0x00000000, 0x0, 0x303303F4
- #define **IOMUXC\_SAI1\_TXD7\_AUDIOMIX\_SAI6\_MCLK** 0x30330194, 0x1, 0x30330514, 0x2, 0x303303F4
- #define **IOMUXC\_SAI1\_TXD7\_AUDIOMIX\_PDM\_CLK** 0x30330194, 0x3, 0x00000000, 0x0, 0x303303F4
- #define **IOMUXC\_SAI1\_TXD7\_ENET1\_TX\_ER** 0x30330194, 0x4, 0x00000000, 0x0, 0x303303F4
- #define **IOMUXC\_SAI1\_TXD7\_GPIO4\_IO19** 0x30330194, 0x5, 0x00000000, 0x0, 0x303303F4
- #define **IOMUXC\_SAI1\_MCLK\_AUDIOMIX\_SAI1\_MCLK** 0x30330198, 0x0, 0x00000000, 0x0, 0x303303F8
- #define **IOMUXC\_SAI1\_MCLK\_AUDIOMIX\_SAI1\_TX\_BCLK** 0x30330198, 0x2, 0x303304-D4, 0x2, 0x303303F8
- #define **IOMUXC\_SAI1\_MCLK\_ENET1\_TX\_CLK** 0x30330198, 0x4, 0x30330578, 0x1, 0x303303F8
- #define **IOMUXC\_SAI1\_MCLK\_GPIO4\_IO20** 0x30330198, 0x5, 0x00000000, 0x0, 0x303303-F8
- #define **IOMUXC\_SAI2\_RXFS\_AUDIOMIX\_SAI2\_RX\_SYNC** 0x3033019C, 0x0, 0x00000000, 0x0, 0x303303FC
- #define **IOMUXC\_SAI2\_RXFS\_AUDIOMIX\_SAI5\_TX\_SYNC** 0x3033019C, 0x1, 0x30330510, 0x2, 0x303303FC
- #define **IOMUXC\_SAI2\_RXFS\_AUDIOMIX\_SAI5\_TX\_DATA1** 0x3033019C, 0x2, 0x00000000,

- 0x0, 0x303303FC
- #define **IOMUXC\_SAI2\_RXFS\_AUDIO MIX\_SAI2\_RX\_DATA1** 0x3033019C, 0x3, 0x303304-DC, 0x0, 0x303303FC
- #define **IOMUXC\_SAI2\_RXFS\_UART1\_TX** 0x3033019C, 0x4, 0x00000000, 0x0, 0x303303FC
- #define **IOMUXC\_SAI2\_RXFS\_UART1\_RX** 0x3033019C, 0x4, 0x303305E8, 0x2, 0x303303FC
- #define **IOMUXC\_SAI2\_RXFS\_GPIO4\_IO21** 0x3033019C, 0x5, 0x00000000, 0x0, 0x303303F-C
- #define **IOMUXC\_SAI2\_RXFS\_AUDIO MIX\_PDM\_BIT\_STREAM2** 0x3033019C, 0x6, 0x303304C8, 0x5, 0x303303FC
- #define **IOMUXC\_SAI2\_RXC\_AUDIO MIX\_SAI2\_RX\_BCLK** 0x303301A0, 0x0, 0x00000000, 0x0, 0x30330400
- #define **IOMUXC\_SAI2\_RXC\_AUDIO MIX\_SAI5\_TX\_BCLK** 0x303301A0, 0x1, 0x3033050-C, 0x2, 0x30330400
- #define **IOMUXC\_SAI2\_RXC\_CAN1\_TX** 0x303301A0, 0x3, 0x00000000, 0x0, 0x30330400
- #define **IOMUXC\_SAI2\_RXC\_UART1\_RX** 0x303301A0, 0x4, 0x303305E8, 0x3, 0x30330400
- #define **IOMUXC\_SAI2\_RXC\_UART1\_TX** 0x303301A0, 0x4, 0x00000000, 0x0, 0x30330400
- #define **IOMUXC\_SAI2\_RXC\_GPIO4\_IO22** 0x303301A0, 0x5, 0x00000000, 0x0, 0x30330400
- #define **IOMUXC\_SAI2\_RXC\_AUDIO MIX\_PDM\_BIT\_STREAM1** 0x303301A0, 0x6, 0x303304C4, 0x5, 0x30330400
- #define **IOMUXC\_SAI2\_RXD0\_AUDIO MIX\_SAI2\_RX\_DATA0** 0x303301A4, 0x0, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC\_SAI2\_RXD0\_AUDIO MIX\_SAI5\_TX\_DATA0** 0x303301A4, 0x1, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC\_SAI2\_RXD0\_ENET\_QOS\_1588\_EVENT2\_OUT** 0x303301A4, 0x2, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC\_SAI2\_RXD0\_AUDIO MIX\_SAI2\_TX\_DATA1** 0x303301A4, 0x3, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC\_SAI2\_RXD0\_UART1\_RTS\_B** 0x303301A4, 0x4, 0x303305E4, 0x2, 0x30330404
- #define **IOMUXC\_SAI2\_RXD0\_UART1\_CTS\_B** 0x303301A4, 0x4, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC\_SAI2\_RXD0\_GPIO4\_IO23** 0x303301A4, 0x5, 0x00000000, 0x0, 0x30330404
- #define **IOMUXC\_SAI2\_RXD0\_AUDIO MIX\_PDM\_BIT\_STREAM3** 0x303301A4, 0x6, 0x303304CC, 0x5, 0x30330404
- #define **IOMUXC\_SAI2\_TXFS\_AUDIO MIX\_SAI2\_TX\_SYNC** 0x303301A8, 0x0, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC\_SAI2\_TXFS\_AUDIO MIX\_SAI5\_TX\_DATA1** 0x303301A8, 0x1, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC\_SAI2\_TXFS\_ENET\_QOS\_1588\_EVENT3\_OUT** 0x303301A8, 0x2, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC\_SAI2\_TXFS\_AUDIO MIX\_SAI2\_TX\_DATA1** 0x303301A8, 0x3, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC\_SAI2\_TXFS\_UART1\_CTS\_B** 0x303301A8, 0x4, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC\_SAI2\_TXFS\_UART1\_RTS\_B** 0x303301A8, 0x4, 0x303305E4, 0x3, 0x30330408
- #define **IOMUXC\_SAI2\_TXFS\_GPIO4\_IO24** 0x303301A8, 0x5, 0x00000000, 0x0, 0x30330408
- #define **IOMUXC\_SAI2\_TXFS\_AUDIO MIX\_PDM\_BIT\_STREAM2** 0x303301A8, 0x6, 0x303304C8, 0x6, 0x30330408
- #define **IOMUXC\_SAI2\_RXC\_AUDIO MIX\_SAI2\_TX\_BCLK** 0x303301AC, 0x0, 0x00000000, 0x0, 0x3033040C

- #define **IOMUXC\_SAI2\_TXC\_AUDIOMIX\_SAI5\_TX\_DATA2** 0x303301AC, 0x1, 0x00000000, 0x0, 0x3033040C
- #define **IOMUXC\_SAI2\_TXC\_CAN1\_RX** 0x303301AC, 0x3, 0x3033054C, 0x1, 0x3033040C
- #define **IOMUXC\_SAI2\_TXC\_GPIO4\_IO25** 0x303301AC, 0x5, 0x00000000, 0x0, 0x3033040C
- #define **IOMUXC\_SAI2\_TXC\_AUDIOMIX\_PDM\_BIT\_STREAM1** 0x303301AC, 0x6, 0x303304C4, 0x6, 0x3033040C
- #define **IOMUXC\_SAI2\_TXD0\_AUDIOMIX\_SAI2\_TX\_DATA0** 0x303301B0, 0x0, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC\_SAI2\_TXD0\_AUDIOMIX\_SAI5\_TX\_DATA3** 0x303301B0, 0x1, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC\_SAI2\_TXD0\_ENET\_QOS\_1588\_EVENT2\_IN** 0x303301B0, 0x2, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC\_SAI2\_TXD0\_CAN2\_TX** 0x303301B0, 0x3, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC\_SAI2\_TXD0\_ENET\_QOS\_1588\_EVENT2\_AUX\_IN** 0x303301B0, 0x4, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC\_SAI2\_TXD0\_GPIO4\_IO26** 0x303301B0, 0x5, 0x00000000, 0x0, 0x30330410
- #define **IOMUXC\_SAI2\_MCLK\_AUDIOMIX\_SAI2\_MCLK** 0x303301B4, 0x0, 0x00000000, 0x0, 0x30330414
- #define **IOMUXC\_SAI2\_MCLK\_AUDIOMIX\_SAI5\_MCLK** 0x303301B4, 0x1, 0x303304F0, 0x2, 0x30330414
- #define **IOMUXC\_SAI2\_MCLK\_ENET\_QOS\_1588\_EVENT3\_IN** 0x303301B4, 0x2, 0x00000000, 0x0, 0x30330414
- #define **IOMUXC\_SAI2\_MCLK\_CAN2\_RX** 0x303301B4, 0x3, 0x30330550, 0x1, 0x30330414
- #define **IOMUXC\_SAI2\_MCLK\_ENET\_QOS\_1588\_EVENT3\_AUX\_IN** 0x303301B4, 0x4, 0x00000000, 0x0, 0x30330414
- #define **IOMUXC\_SAI2\_MCLK\_GPIO4\_IO27** 0x303301B4, 0x5, 0x00000000, 0x0, 0x30330414
- #define **IOMUXC\_SAI2\_MCLK\_AUDIOMIX\_SAI3\_MCLK** 0x303301B4, 0x6, 0x303304E0, 0x1, 0x30330414
- #define **IOMUXC\_SAI3\_RXFS\_AUDIOMIX\_SAI3\_RX\_SYNC** 0x303301B8, 0x0, 0x00000000, 0x0, 0x30330418
- #define **IOMUXC\_SAI3\_RXFS\_AUDIOMIX\_SAI2\_RX\_DATA1** 0x303301B8, 0x1, 0x303304-DC, 0x1, 0x30330418
- #define **IOMUXC\_SAI3\_RXFS\_AUDIOMIX\_SAI5\_RX\_SYNC** 0x303301B8, 0x2, 0x30330508, 0x2, 0x30330418
- #define **IOMUXC\_SAI3\_RXFS\_AUDIOMIX\_SAI3\_RX\_DATA1** 0x303301B8, 0x3, 0x00000000, 0x0, 0x30330418
- #define **IOMUXC\_SAI3\_RXFS\_AUDIOMIX\_SPDIF1\_IN** 0x303301B8, 0x4, 0x30330544, 0x2, 0x30330418
- #define **IOMUXC\_SAI3\_RXFS\_GPIO4\_IO28** 0x303301B8, 0x5, 0x00000000, 0x0, 0x30330418
- #define **IOMUXC\_SAI3\_RXFS\_AUDIOMIX\_PDM\_BIT\_STREAM0** 0x303301B8, 0x6, 0x303304C0, 0x5, 0x30330418
- #define **IOMUXC\_SAI3\_RXC\_AUDIOMIX\_SAI3\_RX\_BCLK** 0x303301BC, 0x0, 0x00000000, 0x0, 0x3033041C
- #define **IOMUXC\_SAI3\_RXC\_AUDIOMIX\_SAI2\_RX\_DATA2** 0x303301BC, 0x1, 0x00000000, 0x0, 0x3033041C
- #define **IOMUXC\_SAI3\_RXC\_AUDIOMIX\_SAI5\_RX\_BCLK** 0x303301BC, 0x2, 0x303304-F4, 0x2, 0x3033041C
- #define **IOMUXC\_SAI3\_RXC\_GPT1\_CLK** 0x303301BC, 0x3, 0x3033059C, 0x0, 0x3033041C
- #define **IOMUXC\_SAI3\_RXC\_UART2\_CTS\_B** 0x303301BC, 0x4, 0x00000000, 0x0, 0x3033041-C
- #define **IOMUXC\_SAI3\_RXC\_UART2\_RTS\_B** 0x303301BC, 0x4, 0x303305EC, 0x2,

- 0x3033041C
- #define **IOMUXC\_SAI3\_RXC\_GPIO4\_IO29** 0x303301BC, 0x5, 0x00000000, 0x0, 0x3033041C
  - #define **IOMUXC\_SAI3\_RXC\_AUDIOMIX\_PDM\_CLK** 0x303301BC, 0x6, 0x00000000, 0x0, 0x3033041C
  - #define **IOMUXC\_SAI3\_RXD\_AUDIOMIX\_SAI3\_RX\_DATA0** 0x303301C0, 0x0, 0x303304-E4, 0x1, 0x30330420
  - #define **IOMUXC\_SAI3\_RXD\_AUDIOMIX\_SAI2\_RX\_DATA3** 0x303301C0, 0x1, 0x00000000, 0x0, 0x30330420
  - #define **IOMUXC\_SAI3\_RXD\_AUDIOMIX\_SAI5\_RX\_DATA0** 0x303301C0, 0x2, 0x303304-F8, 0x2, 0x30330420
  - #define **IOMUXC\_SAI3\_RXD\_UART2\_RTS\_B** 0x303301C0, 0x4, 0x303305EC, 0x3, 0x30330420
  - #define **IOMUXC\_SAI3\_RXD\_UART2\_CTS\_B** 0x303301C0, 0x4, 0x00000000, 0x0, 0x30330420
  - #define **IOMUXC\_SAI3\_RXD\_GPIO4\_IO30** 0x303301C0, 0x5, 0x00000000, 0x0, 0x30330420
  - #define **IOMUXC\_SAI3\_RXD\_AUDIOMIX\_PDM\_BIT\_STREAM1** 0x303301C0, 0x6, 0x303304C4, 0x7, 0x30330420
  - #define **IOMUXC\_SAI3\_TXFS\_AUDIOMIX\_SAI3\_TX\_SYNC** 0x303301C4, 0x0, 0x303304-E-C, 0x1, 0x30330424
  - #define **IOMUXC\_SAI3\_TXFS\_AUDIOMIX\_SAI2\_TX\_DATA1** 0x303301C4, 0x1, 0x00000000, 0x0, 0x30330424
  - #define **IOMUXC\_SAI3\_TXFS\_AUDIOMIX\_SAI5\_RX\_DATA1** 0x303301C4, 0x2, 0x303304-FC, 0x2, 0x30330424
  - #define **IOMUXC\_SAI3\_TXFS\_AUDIOMIX\_SAI3\_TX\_DATA1** 0x303301C4, 0x3, 0x00000000, 0x0, 0x30330424
  - #define **IOMUXC\_SAI3\_TXFS\_UART2\_RX** 0x303301C4, 0x4, 0x303305F0, 0x4, 0x30330424
  - #define **IOMUXC\_SAI3\_TXFS\_UART2\_TX** 0x303301C4, 0x4, 0x00000000, 0x0, 0x30330424
  - #define **IOMUXC\_SAI3\_TXFS\_GPIO4\_IO31** 0x303301C4, 0x5, 0x00000000, 0x0, 0x30330424
  - #define **IOMUXC\_SAI3\_TXFS\_AUDIOMIX\_PDM\_BIT\_STREAM3** 0x303301C4, 0x6, 0x303304CC, 0x6, 0x30330424
  - #define **IOMUXC\_SAI3\_TXC\_AUDIOMIX\_SAI3\_TX\_BCLK** 0x303301C8, 0x0, 0x303304E8, 0x1, 0x30330428
  - #define **IOMUXC\_SAI3\_TXC\_AUDIOMIX\_SAI2\_TX\_DATA2** 0x303301C8, 0x1, 0x00000000, 0x0, 0x30330428
  - #define **IOMUXC\_SAI3\_TXC\_AUDIOMIX\_SAI5\_RX\_DATA2** 0x303301C8, 0x2, 0x30330500, 0x2, 0x30330428
  - #define **IOMUXC\_SAI3\_TXC\_GPT1\_CAPTURE1** 0x303301C8, 0x3, 0x30330594, 0x0, 0x30330428
  - #define **IOMUXC\_SAI3\_TXC\_UART2\_TX** 0x303301C8, 0x4, 0x00000000, 0x0, 0x30330428
  - #define **IOMUXC\_SAI3\_TXC\_UART2\_RX** 0x303301C8, 0x4, 0x303305F0, 0x5, 0x30330428
  - #define **IOMUXC\_SAI3\_TXC\_GPIO5\_IO00** 0x303301C8, 0x5, 0x00000000, 0x0, 0x30330428
  - #define **IOMUXC\_SAI3\_TXC\_AUDIOMIX\_PDM\_BIT\_STREAM2** 0x303301C8, 0x6, 0x303304C8, 0x7, 0x30330428
  - #define **IOMUXC\_SAI3\_TXD\_AUDIOMIX\_SAI3\_TX\_DATA0** 0x303301CC, 0x0, 0x00000000, 0x0, 0x3033042C
  - #define **IOMUXC\_SAI3\_TXD\_AUDIOMIX\_SAI2\_TX\_DATA3** 0x303301CC, 0x1, 0x00000000, 0x0, 0x3033042C
  - #define **IOMUXC\_SAI3\_TXD\_AUDIOMIX\_SAI5\_RX\_DATA3** 0x303301CC, 0x2, 0x30330504, 0x2, 0x3033042C
  - #define **IOMUXC\_SAI3\_TXD\_GPT1\_CAPTURE2** 0x303301CC, 0x3, 0x30330598, 0x0, 0x3033042C
  - #define **IOMUXC\_SAI3\_TXD\_AUDIOMIX\_SPDIF1\_EXT\_CLK** 0x303301CC, 0x4, 0x30330548,

- 0x0, 0x3033042C
- #define **IOMUXC\_SAI3\_TXD\_GPIO5\_IO01** 0x303301CC, 0x5, 0x00000000, 0x0, 0x3033042C
  - #define **IOMUXC\_SAI3\_MCLK\_AUDIOMIX\_SAI3\_MCLK** 0x303301D0, 0x0, 0x303304E0, 0x2, 0x30330430
  - #define **IOMUXC\_SAI3\_MCLK\_PWM4\_OUT** 0x303301D0, 0x1, 0x00000000, 0x0, 0x30330430
  - #define **IOMUXC\_SAI3\_MCLK\_AUDIOMIX\_SAI5\_MCLK** 0x303301D0, 0x2, 0x303304F0, 0x3, 0x30330430
  - #define **IOMUXC\_SAI3\_MCLK\_AUDIOMIX\_SPDIF1\_OUT** 0x303301D0, 0x4, 0x00000000, 0x0, 0x30330430
  - #define **IOMUXC\_SAI3\_MCLK\_GPIO5\_IO02** 0x303301D0, 0x5, 0x00000000, 0x0, 0x30330430
  - #define **IOMUXC\_SAI3\_MCLK\_AUDIOMIX\_SPDIF1\_IN** 0x303301D0, 0x6, 0x30330544, 0x3, 0x30330430
  - #define **IOMUXC\_SPDIF\_TX\_AUDIOMIX\_SPDIF1\_OUT** 0x303301D4, 0x0, 0x00000000, 0x0, 0x30330434
  - #define **IOMUXC\_SPDIF\_TX\_PWM3\_OUT** 0x303301D4, 0x1, 0x00000000, 0x0, 0x30330434
  - #define **IOMUXC\_SPDIF\_TX\_I2C5\_SCL** 0x303301D4, 0x2, 0x303305C4, 0x2, 0x30330434
  - #define **IOMUXC\_SPDIF\_TX\_GPT1\_COMPARE1** 0x303301D4, 0x3, 0x00000000, 0x0, 0x30330434
  - #define **IOMUXC\_SPDIF\_TX\_CAN1\_TX** 0x303301D4, 0x4, 0x00000000, 0x0, 0x30330434
  - #define **IOMUXC\_SPDIF\_RX\_GPIO5\_IO03** 0x303301D4, 0x5, 0x00000000, 0x0, 0x30330434
  - #define **IOMUXC\_SPDIF\_RX\_AUDIOMIX\_SPDIF1\_IN** 0x303301D8, 0x0, 0x30330544, 0x4, 0x30330438
  - #define **IOMUXC\_SPDIF\_RX\_PWM2\_OUT** 0x303301D8, 0x1, 0x00000000, 0x0, 0x30330438
  - #define **IOMUXC\_SPDIF\_RX\_I2C5\_SDA** 0x303301D8, 0x2, 0x303305C8, 0x2, 0x30330438
  - #define **IOMUXC\_SPDIF\_RX\_GPT1\_COMPARE2** 0x303301D8, 0x3, 0x00000000, 0x0, 0x30330438
  - #define **IOMUXC\_SPDIF\_RX\_CAN1\_RX** 0x303301D8, 0x4, 0x3033054C, 0x2, 0x30330438
  - #define **IOMUXC\_SPDIF\_RX\_GPIO5\_IO04** 0x303301D8, 0x5, 0x00000000, 0x0, 0x30330438
  - #define **IOMUXC\_SPDIF\_EXT\_CLK\_AUDIOMIX\_SPDIF1\_EXT\_CLK** 0x303301DC, 0x0, 0x30330548, 0x1, 0x3033043C
  - #define **IOMUXC\_SPDIF\_EXT\_CLK\_PWM1\_OUT** 0x303301DC, 0x1, 0x00000000, 0x0, 0x3033043C
  - #define **IOMUXC\_SPDIF\_EXT\_CLK\_GPT1\_COMPARE3** 0x303301DC, 0x3, 0x00000000, 0x0, 0x3033043C
  - #define **IOMUXC\_SPDIF\_EXT\_CLK\_GPIO5\_IO05** 0x303301DC, 0x5, 0x00000000, 0x0, 0x3033043C
  - #define **IOMUXC\_ECSPI1\_SCLK\_ECSPI1\_SCLK** 0x303301E0, 0x0, 0x30330558, 0x0, 0x30330440
  - #define **IOMUXC\_ECSPI1\_SCLK\_UART3\_RX** 0x303301E0, 0x1, 0x303305F8, 0x4, 0x30330440
  - #define **IOMUXC\_ECSPI1\_SCLK\_UART3\_TX** 0x303301E0, 0x1, 0x00000000, 0x0, 0x30330440
  - #define **IOMUXC\_ECSPI1\_SCLK\_I2C1\_SCL** 0x303301E0, 0x2, 0x303305A4, 0x1, 0x30330440
  - #define **IOMUXC\_ECSPI1\_SCLK\_AUDIOMIX\_SAI7\_RX\_SYNC** 0x303301E0, 0x3, 0x30330538, 0x1, 0x30330440
  - #define **IOMUXC\_ECSPI1\_SCLK\_GPIO5\_IO06** 0x303301E0, 0x5, 0x00000000, 0x0, 0x30330440
  - #define **IOMUXC\_ECSPI1\_MOSI\_ECSPI1\_MOSI** 0x303301E4, 0x0, 0x30330560, 0x0, 0x30330444
  - #define **IOMUXC\_ECSPI1\_MOSI\_UART3\_TX** 0x303301E4, 0x1, 0x00000000, 0x0, 0x30330444
  - #define **IOMUXC\_ECSPI1\_MOSI\_UART3\_RX** 0x303301E4, 0x1, 0x303305F8, 0x5, 0x30330444
  - #define **IOMUXC\_ECSPI1\_MOSI\_I2C1\_SDA** 0x303301E4, 0x2, 0x303305A8, 0x1, 0x30330444
  - #define **IOMUXC\_ECSPI1\_MOSI\_AUDIOMIX\_SAI7\_RX\_BCLK** 0x303301E4, 0x3, 0x30330530,

- 0x1, 0x30330444
- #define **IOMUXC\_ECSP1\_MOSI\_GPIO5\_IO07** 0x303301E4, 0x5, 0x00000000, 0x0,  
0x30330444
- #define **IOMUXC\_ECSP1\_MISO\_ECSP1\_MISO** 0x303301E8, 0x0, 0x3033055C, 0x0,  
0x30330448
- #define **IOMUXC\_ECSP1\_MISO\_UART3\_CTS\_B** 0x303301E8, 0x1, 0x00000000, 0x0,  
0x30330448
- #define **IOMUXC\_ECSP1\_MISO\_UART3\_RTS\_B** 0x303301E8, 0x1, 0x303305F4, 0x2,  
0x30330448
- #define **IOMUXC\_ECSP1\_MISO\_I2C2\_SCL** 0x303301E8, 0x2, 0x303305AC, 0x1, 0x30330448
- #define **IOMUXC\_ECSP1\_MISO\_AUDIOMIX\_SAI7\_RX\_DATA0** 0x303301E8, 0x3,  
0x30330534, 0x1, 0x30330448
- #define **IOMUXC\_ECSP1\_MISO\_GPIO5\_IO08** 0x303301E8, 0x5, 0x00000000, 0x0,  
0x30330448
- #define **IOMUXC\_ECSP1\_SS0\_ECSP1\_SS0** 0x303301EC, 0x0, 0x30330564, 0x0, 0x3033044-  
C
- #define **IOMUXC\_ECSP1\_SS0\_UART3\_RTS\_B** 0x303301EC, 0x1, 0x303305F4, 0x3,  
0x3033044C
- #define **IOMUXC\_ECSP1\_SS0\_UART3\_CTS\_B** 0x303301EC, 0x1, 0x00000000, 0x0,  
0x3033044C
- #define **IOMUXC\_ECSP1\_SS0\_I2C2\_SDA** 0x303301EC, 0x2, 0x303305B0, 0x1, 0x3033044C
- #define **IOMUXC\_ECSP1\_SS0\_AUDIOMIX\_SAI7\_TX\_SYNC** 0x303301EC, 0x3, 0x30330540,  
0x1, 0x3033044C
- #define **IOMUXC\_ECSP1\_SS0\_GPIO5\_IO09** 0x303301EC, 0x5, 0x00000000, 0x0, 0x3033044-  
C
- #define **IOMUXC\_ECSP2\_SCLK\_ECSP2\_SCLK** 0x303301F0, 0x0, 0x30330568, 0x1,  
0x30330450
- #define **IOMUXC\_ECSP2\_SCLK\_UART4\_RX** 0x303301F0, 0x1, 0x30330600, 0x6, 0x30330450
- #define **IOMUXC\_ECSP2\_SCLK\_UART4\_TX** 0x303301F0, 0x1, 0x00000000, 0x0, 0x30330450
- #define **IOMUXC\_ECSP2\_SCLK\_I2C3\_SCL** 0x303301F0, 0x2, 0x303305B4, 0x3, 0x30330450
- #define **IOMUXC\_ECSP2\_SCLK\_AUDIOMIX\_SAI7\_TX\_BCLK** 0x303301F0, 0x3, 0x3033053-  
C, 0x1, 0x30330450
- #define **IOMUXC\_ECSP2\_SCLK\_GPIO5\_IO10** 0x303301F0, 0x5, 0x00000000, 0x0,  
0x30330450
- #define **IOMUXC\_ECSP2\_MOSI\_ECSP2\_MOSI** 0x303301F4, 0x0, 0x30330570, 0x1,  
0x30330454
- #define **IOMUXC\_ECSP2\_MOSI\_UART4\_TX** 0x303301F4, 0x1, 0x00000000, 0x0, 0x30330454
- #define **IOMUXC\_ECSP2\_MOSI\_UART4\_RX** 0x303301F4, 0x1, 0x30330600, 0x7, 0x30330454
- #define **IOMUXC\_ECSP2\_MOSI\_I2C3\_SDA** 0x303301F4, 0x2, 0x303305B8, 0x3, 0x30330454
- #define **IOMUXC\_ECSP2\_MOSI\_AUDIOMIX\_SAI7\_TX\_DATA0** 0x303301F4, 0x3,  
0x00000000, 0x0, 0x30330454
- #define **IOMUXC\_ECSP2\_MOSI\_GPIO5\_IO11** 0x303301F4, 0x5, 0x00000000, 0x0,  
0x30330454
- #define **IOMUXC\_ECSP2\_MISO\_ECSP2\_MISO** 0x303301F8, 0x0, 0x3033056C, 0x1,  
0x30330458
- #define **IOMUXC\_ECSP2\_MISO\_UART4\_CTS\_B** 0x303301F8, 0x1, 0x00000000, 0x0,  
0x30330458
- #define **IOMUXC\_ECSP2\_MISO\_UART4\_RTS\_B** 0x303301F8, 0x1, 0x303305FC, 0x2,  
0x30330458
- #define **IOMUXC\_ECSP2\_MISO\_I2C4\_SCL** 0x303301F8, 0x2, 0x303305BC, 0x4, 0x30330458
- #define **IOMUXC\_ECSP2\_MISO\_AUDIOMIX\_SAI7\_MCLK** 0x303301F8, 0x3, 0x3033052-

- C, 0x1, 0x30330458
- #define **IOMUXC\_ECSPI2\_MISO\_CCM\_CLKO1** 0x303301F8, 0x4, 0x00000000, 0x0,  
0x30330458
- #define **IOMUXC\_ECSPI2\_MISO\_GPIO5\_IO12** 0x303301F8, 0x5, 0x00000000, 0x0,  
0x30330458
- #define **IOMUXC\_ECSPI2\_SS0\_ECSPI2\_SS0** 0x303301FC, 0x0, 0x30330574, 0x1, 0x3033045-  
C
- #define **IOMUXC\_ECSPI2\_SS0\_UART4\_RTS\_B** 0x303301FC, 0x1, 0x303305FC, 0x3,  
0x3033045C
- #define **IOMUXC\_ECSPI2\_SS0\_UART4\_CTS\_B** 0x303301FC, 0x1, 0x00000000, 0x0,  
0x3033045C
- #define **IOMUXC\_ECSPI2\_SS0\_I2C4\_SDA** 0x303301FC, 0x2, 0x303305C0, 0x4, 0x3033045C
- #define **IOMUXC\_ECSPI2\_SS0\_CCM\_CLKO2** 0x303301FC, 0x4, 0x00000000, 0x0, 0x3033045-  
C
- #define **IOMUXC\_ECSPI2\_SS0\_GPIO5\_IO13** 0x303301FC, 0x5, 0x00000000, 0x0, 0x3033045-  
C
- #define **IOMUXC\_I2C1\_SCL\_I2C1\_SCL** 0x30330200, 0x0, 0x303305A4, 0x2, 0x30330460
- #define **IOMUXC\_I2C1\_SCL\_ENET\_QOS\_MDC** 0x30330200, 0x1, 0x00000000, 0x0,  
0x30330460
- #define **IOMUXC\_I2C1\_SCL\_ECSPI1\_SCLK** 0x30330200, 0x3, 0x30330558, 0x1, 0x30330460
- #define **IOMUXC\_I2C1\_SCL\_GPIO5\_IO14** 0x30330200, 0x5, 0x00000000, 0x0, 0x30330460
- #define **IOMUXC\_I2C1\_SDA\_I2C1\_SDA** 0x30330204, 0x0, 0x303305A8, 0x2, 0x30330464
- #define **IOMUXC\_I2C1\_SDA\_ENET\_QOS\_MDIO** 0x30330204, 0x1, 0x30330590, 0x2,  
0x30330464
- #define **IOMUXC\_I2C1\_SDA\_ECSPI1\_MOSI** 0x30330204, 0x3, 0x30330560, 0x1, 0x30330464
- #define **IOMUXC\_I2C1\_SDA\_GPIO5\_IO15** 0x30330204, 0x5, 0x00000000, 0x0, 0x30330464
- #define **IOMUXC\_I2C2\_SCL\_I2C2\_SCL** 0x30330208, 0x0, 0x303305AC, 0x2, 0x30330468
- #define **IOMUXC\_I2C2\_SCL\_ENET\_QOS\_1588\_EVENT1\_IN** 0x30330208, 0x1, 0x00000000,  
0x0, 0x30330468
- #define **IOMUXC\_I2C2\_SCL\_USDHC3\_CD\_B** 0x30330208, 0x2, 0x30330608, 0x3, 0x30330468
- #define **IOMUXC\_I2C2\_SCL\_ECSPI1\_MISO** 0x30330208, 0x3, 0x3033055C, 0x1, 0x30330468
- #define **IOMUXC\_I2C2\_SCL\_ENET\_QOS\_1588\_EVENT1\_AUX\_IN** 0x30330208, 0x4,  
0x00000000, 0x0, 0x30330468
- #define **IOMUXC\_I2C2\_SCL\_GPIO5\_IO16** 0x30330208, 0x5, 0x00000000, 0x0, 0x30330468
- #define **IOMUXC\_I2C2\_SDA\_I2C2\_SDA** 0x3033020C, 0x0, 0x303305B0, 0x2, 0x3033046C
- #define **IOMUXC\_I2C2\_SDA\_ENET\_QOS\_1588\_EVENT1\_OUT** 0x3033020C, 0x1, 0x00000000,  
0x0, 0x3033046C
- #define **IOMUXC\_I2C2\_SDA\_USDHC3\_WP** 0x3033020C, 0x2, 0x30330634, 0x3, 0x3033046C
- #define **IOMUXC\_I2C2\_SDA\_ECSPI1\_SS0** 0x3033020C, 0x3, 0x30330564, 0x1, 0x3033046C
- #define **IOMUXC\_I2C2\_SDA\_GPIO5\_IO17** 0x3033020C, 0x5, 0x00000000, 0x0, 0x3033046C
- #define **IOMUXC\_I2C3\_SCL\_I2C3\_SCL** 0x30330210, 0x0, 0x303305B4, 0x4, 0x30330470
- #define **IOMUXC\_I2C3\_SCL\_PWM4\_OUT** 0x30330210, 0x1, 0x00000000, 0x0, 0x30330470
- #define **IOMUXC\_I2C3\_SCL\_GPT2\_CLK** 0x30330210, 0x2, 0x00000000, 0x0, 0x30330470
- #define **IOMUXC\_I2C3\_SCL\_ECSPI2\_SCLK** 0x30330210, 0x3, 0x30330568, 0x2, 0x30330470
- #define **IOMUXC\_I2C3\_SCL\_GPIO5\_IO18** 0x30330210, 0x5, 0x00000000, 0x0, 0x30330470
- #define **IOMUXC\_I2C3\_SDA\_I2C3\_SDA** 0x30330214, 0x0, 0x303305B8, 0x4, 0x30330474
- #define **IOMUXC\_I2C3\_SDA\_PWM3\_OUT** 0x30330214, 0x1, 0x00000000, 0x0, 0x30330474
- #define **IOMUXC\_I2C3\_SDA\_GPT3\_CLK** 0x30330214, 0x2, 0x00000000, 0x0, 0x30330474
- #define **IOMUXC\_I2C3\_SDA\_ECSPI2\_MOSI** 0x30330214, 0x3, 0x30330570, 0x2, 0x30330474
- #define **IOMUXC\_I2C3\_SDA\_GPIO5\_IO19** 0x30330214, 0x5, 0x00000000, 0x0, 0x30330474
- #define **IOMUXC\_I2C4\_SCL\_I2C4\_SCL** 0x30330218, 0x0, 0x303305BC, 0x5, 0x30330478
- #define **IOMUXC\_I2C4\_SCL\_PWM2\_OUT** 0x30330218, 0x1, 0x00000000, 0x0, 0x30330478
- #define **IOMUXC\_I2C4\_SCL\_CLKREQ\_B** 0x30330218, 0x2, 0x303305A0, 0x0,

0x30330478

- #define **IOMUXC\_I2C4\_SCL\_ECSPI2\_MISO** 0x30330218, 0x3, 0x3033056C, 0x2, 0x30330478
- #define **IOMUXC\_I2C4\_SCL\_GPIO5\_IO20** 0x30330218, 0x5, 0x00000000, 0x0, 0x30330478
- #define **IOMUXC\_I2C4\_SDA\_I2C4\_SDA** 0x3033021C, 0x0, 0x303305C0, 0x5, 0x3033047C
- #define **IOMUXC\_I2C4\_SDA\_PWM1\_OUT** 0x3033021C, 0x1, 0x00000000, 0x0, 0x3033047C
- #define **IOMUXC\_I2C4\_SDA\_ECSPI2\_SS0** 0x3033021C, 0x3, 0x30330574, 0x2, 0x3033047C
- #define **IOMUXC\_I2C4\_SDA\_GPIO5\_IO21** 0x3033021C, 0x5, 0x00000000, 0x0, 0x3033047C
- #define **IOMUXC\_UART1\_RXD\_UART1\_RX** 0x30330220, 0x0, 0x303305E8, 0x4, 0x30330480
- #define **IOMUXC\_UART1\_RXD\_UART1\_TX** 0x30330220, 0x0, 0x00000000, 0x0, 0x30330480
- #define **IOMUXC\_UART1\_RXD\_ECSPI3\_SCLK** 0x30330220, 0x1, 0x00000000, 0x0, 0x30330480
- #define **IOMUXC\_UART1\_RXD\_GPIO5\_IO22** 0x30330220, 0x5, 0x00000000, 0x0, 0x30330480
- #define **IOMUXC\_UART1\_TXD\_UART1\_TX** 0x30330224, 0x0, 0x00000000, 0x0, 0x30330484
- #define **IOMUXC\_UART1\_TXD\_UART1\_RX** 0x30330224, 0x0, 0x303305E8, 0x5, 0x30330484
- #define **IOMUXC\_UART1\_TXD\_ECSPI3\_MOSI** 0x30330224, 0x1, 0x00000000, 0x0, 0x30330484
- #define **IOMUXC\_UART1\_TXD\_GPIO5\_IO23** 0x30330224, 0x5, 0x00000000, 0x0, 0x30330484
- #define **IOMUXC\_UART2\_RXD\_UART2\_RX** 0x30330228, 0x0, 0x303305F0, 0x6, 0x30330488
- #define **IOMUXC\_UART2\_RXD\_UART2\_TX** 0x30330228, 0x0, 0x00000000, 0x0, 0x30330488
- #define **IOMUXC\_UART2\_RXD\_ECSPI3\_MISO** 0x30330228, 0x1, 0x00000000, 0x0, 0x30330488
- #define **IOMUXC\_UART2\_RXD\_GPT1\_COMPARE3** 0x30330228, 0x3, 0x00000000, 0x0, 0x30330488
- #define **IOMUXC\_UART2\_RXD\_GPIO5\_IO24** 0x30330228, 0x5, 0x00000000, 0x0, 0x30330488
- #define **IOMUXC\_UART2\_TXD\_UART2\_TX** 0x3033022C, 0x0, 0x00000000, 0x0, 0x3033048-C
- #define **IOMUXC\_UART2\_TXD\_UART2\_RX** 0x3033022C, 0x0, 0x303305F0, 0x7, 0x3033048-C
- #define **IOMUXC\_UART2\_TXD\_ECSPI3\_SS0** 0x3033022C, 0x1, 0x00000000, 0x0, 0x3033048-C
- #define **IOMUXC\_UART2\_TXD\_GPT1\_COMPARE2** 0x3033022C, 0x3, 0x00000000, 0x0, 0x3033048-C
- #define **IOMUXC\_UART2\_TXD\_GPIO5\_IO25** 0x3033022C, 0x5, 0x00000000, 0x0, 0x3033048-C
- #define **IOMUXC\_UART3\_RXD\_UART3\_RX** 0x30330230, 0x0, 0x303305F8, 0x6, 0x30330490
- #define **IOMUXC\_UART3\_RXD\_UART3\_TX** 0x30330230, 0x0, 0x00000000, 0x0, 0x30330490
- #define **IOMUXC\_UART3\_RXD\_UART1\_CTS\_B** 0x30330230, 0x1, 0x00000000, 0x0, 0x30330490
- #define **IOMUXC\_UART3\_RXD\_UART1\_RTS\_B** 0x30330230, 0x1, 0x303305E4, 0x4, 0x30330490
- #define **IOMUXC\_UART3\_RXD\_USDHC3\_RESET\_B** 0x30330230, 0x2, 0x00000000, 0x0, 0x30330490
- #define **IOMUXC\_UART3\_RXD\_GPT1\_CAPTURE2** 0x30330230, 0x3, 0x30330598, 0x1, 0x30330490
- #define **IOMUXC\_UART3\_RXD\_CAN2\_TX** 0x30330230, 0x4, 0x00000000, 0x0, 0x30330490
- #define **IOMUXC\_UART3\_RXD\_GPIO5\_IO26** 0x30330230, 0x5, 0x00000000, 0x0, 0x30330490
- #define **IOMUXC\_UART3\_TXD\_UART3\_TX** 0x30330234, 0x0, 0x00000000, 0x0, 0x30330494
- #define **IOMUXC\_UART3\_TXD\_UART3\_RX** 0x30330234, 0x0, 0x303305F8, 0x7, 0x30330494
- #define **IOMUXC\_UART3\_TXD\_UART1\_RTS\_B** 0x30330234, 0x1, 0x303305E4, 0x5, 0x30330494
- #define **IOMUXC\_UART3\_TXD\_UART1\_CTS\_B** 0x30330234, 0x1, 0x00000000, 0x0, 0x30330494

- #define **IOMUXC\_UART3\_TXD\_USDHC3\_VSELECT** 0x30330234, 0x2, 0x00000000, 0x0, 0x30330494
- #define **IOMUXC\_UART3\_TXD\_GPT1\_CLK** 0x30330234, 0x3, 0x3033059C, 0x1, 0x30330494
- #define **IOMUXC\_UART3\_TXD\_CAN2\_RX** 0x30330234, 0x4, 0x30330550, 0x2, 0x30330494
- #define **IOMUXC\_UART3\_TXD\_GPIO5\_IO27** 0x30330234, 0x5, 0x00000000, 0x0, 0x30330494
- #define **IOMUXC\_UART4\_RXD\_UART4\_RX** 0x30330238, 0x0, 0x30330600, 0x8, 0x30330498
- #define **IOMUXC\_UART4\_RXD\_UART4\_TX** 0x30330238, 0x0, 0x00000000, 0x0, 0x30330498
- #define **IOMUXC\_UART4\_RXD\_UART2\_CTS\_B** 0x30330238, 0x1, 0x00000000, 0x0, 0x30330498
- #define **IOMUXC\_UART4\_RXD\_UART2\_RTS\_B** 0x30330238, 0x1, 0x303305EC, 0x4, 0x30330498
- #define **IOMUXC\_UART4\_RXD\_PCIE\_CLKREQ\_B** 0x30330238, 0x2, 0x303305A0, 0x1, 0x30330498
- #define **IOMUXC\_UART4\_RXD\_GPT1\_COMPARE1** 0x30330238, 0x3, 0x00000000, 0x0, 0x30330498
- #define **IOMUXC\_UART4\_RXD\_I2C6\_SCL** 0x30330238, 0x4, 0x303305CC, 0x2, 0x30330498
- #define **IOMUXC\_UART4\_RXD\_GPIO5\_IO28** 0x30330238, 0x5, 0x00000000, 0x0, 0x30330498
- #define **IOMUXC\_UART4\_TXD\_UART4\_TX** 0x3033023C, 0x0, 0x00000000, 0x0, 0x3033049-C
- #define **IOMUXC\_UART4\_TXD\_UART4\_RX** 0x3033023C, 0x0, 0x30330600, 0x9, 0x3033049-C
- #define **IOMUXC\_UART4\_TXD\_UART2\_RTS\_B** 0x3033023C, 0x1, 0x303305EC, 0x5, 0x3033049C
- #define **IOMUXC\_UART4\_TXD\_UART2\_CTS\_B** 0x3033023C, 0x1, 0x00000000, 0x0, 0x3033049C
- #define **IOMUXC\_UART4\_TXD\_GPT1\_CAPTURE1** 0x3033023C, 0x3, 0x30330594, 0x1, 0x3033049C
- #define **IOMUXC\_UART4\_TXD\_I2C6\_SDA** 0x3033023C, 0x4, 0x303305D0, 0x2, 0x3033049C
- #define **IOMUXC\_UART4\_TXD\_GPIO5\_IO29** 0x3033023C, 0x5, 0x00000000, 0x0, 0x3033049-C
- #define **IOMUXC\_HDMI\_DDC\_SCL\_HDMIMIX\_HDMI\_SCL** 0x30330240, 0x0, 0x00000000, 0x0, 0x303304A0
- #define **IOMUXC\_HDMI\_DDC\_SCL\_I2C5\_SCL** 0x30330240, 0x3, 0x303305C4, 0x3, 0x303304A0
- #define **IOMUXC\_HDMI\_DDC\_SCL\_CAN1\_TX** 0x30330240, 0x4, 0x00000000, 0x0, 0x303304A0
- #define **IOMUXC\_HDMI\_DDC\_SCL\_GPIO3\_IO26** 0x30330240, 0x5, 0x00000000, 0x0, 0x303304A0
- #define **IOMUXC\_HDMI\_DDC\_SCL\_EARC\_TEST\_OUT0** 0x30330240, 0x6, 0x00000000, 0x0, 0x303304A0
- #define **IOMUXC\_HDMI\_DDC\_SDA\_HDMIMIX\_HDMI\_SDA** 0x30330244, 0x0, 0x00000000, 0x0, 0x303304A4
- #define **IOMUXC\_HDMI\_DDC\_SDA\_I2C5\_SDA** 0x30330244, 0x3, 0x303305C8, 0x3, 0x303304A4
- #define **IOMUXC\_HDMI\_DDC\_SDA\_CAN1\_RX** 0x30330244, 0x4, 0x3033054C, 0x3, 0x303304A4
- #define **IOMUXC\_HDMI\_DDC\_SDA\_GPIO3\_IO27** 0x30330244, 0x5, 0x00000000, 0x0, 0x303304A4
- #define **IOMUXC\_HDMI\_DDC\_SDA\_EARC\_TEST\_OUT1** 0x30330244, 0x6, 0x00000000, 0x0, 0x303304A4
- #define **IOMUXC\_HDMI\_CEC\_HDMIMIX\_HDMI\_CEC** 0x30330248, 0x0, 0x00000000, 0x0,

0x303304A8

- #define **IOMUXC\_HDMI\_CEC\_I2C6\_SCL** 0x30330248, 0x3, 0x303305CC, 0x3, 0x303304A8
- #define **IOMUXC\_HDMI\_CEC\_CAN2\_TX** 0x30330248, 0x4, 0x00000000, 0x0, 0x303304A8
- #define **IOMUXC\_HDMI\_CEC\_GPIO3\_IO28** 0x30330248, 0x5, 0x00000000, 0x0, 0x303304A8
- #define **IOMUXC\_HDMI\_HPD\_HDMIMIX\_HDMI\_HPD** 0x3033024C, 0x0, 0x00000000, 0x0, 0x303304AC
- #define **IOMUXC\_HDMI\_HPD\_AUDIOMIX\_HDMI\_HPD\_O** 0x3033024C, 0x1, 0x00000000, 0x0, 0x303304AC
- #define **IOMUXC\_HDMI\_HPD\_I2C6\_SDA** 0x3033024C, 0x3, 0x303305D0, 0x3, 0x303304AC
- #define **IOMUXC\_HDMI\_HPD\_CAN2\_RX** 0x3033024C, 0x4, 0x30330550, 0x3, 0x303304AC
- #define **IOMUXC\_HDMI\_HPD\_GPIO3\_IO29** 0x3033024C, 0x5, 0x00000000, 0x0, 0x303304AC

## Configuration

- static void **IOMUXC\_SetPinMux** (uintptr\_t muxRegister, uint32\_t muxMode, uintptr\_t inputRegister, uint32\_t inputDaisy, uintptr\_t configRegister, uint32\_t inputOnfield)
 

*Sets the IOMUXC pin mux mode.*
- static void **IOMUXC\_SetPinConfig** (uintptr\_t muxRegister, uint32\_t muxMode, uintptr\_t inputRegister, uint32\_t inputDaisy, uintptr\_t configRegister, uint32\_t configValue)
 

*Sets the IOMUXC pin configuration.*

## 6.2 Macro Definition Documentation

### 6.2.1 #define FSL\_IOMUXC\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 4))

## 6.3 Function Documentation

### 6.3.1 static void IOMUXC\_SetPinMux ( *uintptr\_t muxRegister*, *uint32\_t muxMode*, *uintptr\_t inputRegister*, *uint32\_t inputDaisy*, *uintptr\_t configRegister*, *uint32\_t inputOnfield* ) [inline], [static]

Note

The first five parameters can be filled with the pin function ID macros.

This is an example to set the I2C4\_SDA as the pwm1\_OUT:

```
* IOMUXC_SetPinMux(IOMUXC_I2C4_SDA_PWM1_OUT, 0);
*
```

Parameters

|                       |                                  |
|-----------------------|----------------------------------|
| <i>muxRegister</i>    | The pin mux register_            |
| <i>muxMode</i>        | The pin mux mode_                |
| <i>inputRegister</i>  | The select input register_       |
| <i>inputDaisy</i>     | The input daisy_                 |
| <i>configRegister</i> | The config register_             |
| <i>inputOnfield</i>   | The pad->module input inversion_ |

### 6.3.2 static void IOMUXC\_SetPinConfig ( *uintptr\_t muxRegister*, *uint32\_t muxMode*, *uintptr\_t inputRegister*, *uint32\_t inputDaisy*, *uintptr\_t configRegister*, *uint32\_t configValue* ) [inline], [static]

Note

The previous five parameters can be filled with the pin function ID macros.

This is an example to set pin configuration for IOMUXC\_I2C4\_SDA\_PWM1\_OUT:

```
* IOMUXC_SetPinConfig(IOMUXC_I2C4_SDA_PWM1_OUT, IOMUXC_SW_PAD_CTL_PAD_ODE_MASK |
 IOMUXC0_SW_PAD_CTL_PAD_DSE(2U))
*
```

Parameters

|                       |                            |
|-----------------------|----------------------------|
| <i>muxRegister</i>    | The pin mux register_      |
| <i>muxMode</i>        | The pin mux mode_          |
| <i>inputRegister</i>  | The select input register_ |
| <i>inputDaisy</i>     | The input daisy_           |
| <i>configRegister</i> | The config register_       |
| <i>configValue</i>    | The pin config value_      |

# Chapter 7

## CACHE: ARMV7-M7 CACHE Memory Controller

### 7.1 Overview

The MCUXpresso SDK provides a peripheral driver for the CACHE Controller of MCUXpresso SDK devices.

The CACHE driver is created to help the user more easily operate the cache memory. The APIs for basic operations are including the following three levels:

1L. The L1 cache driver API. This level provides the level 1 caches controller drivers. The L1 caches are mainly integrated in the Core memory system, Cortex-M7 L1 caches, etc. For our Cortex-M4 series platforms, the L1 cache is the local memory controller (LMEM) which is not integrated in the Cortex-M4 processor memory system.

2L. The L2 cache driver API. This level provides the level 2 cache controller drivers. The L2 cache could be integrated in the CORE memory system or an external L2 cache memory, PL310, etc.

3L. The combined cache driver API. This level provides many APIs for combined L1 and L2 cache maintain operations. This is provided for MCUXpresso SDK drivers (DMA, ENET, USDHC, etc) which should do the cache maintenance in their transactional APIs.

### 7.2 Function groups

#### 7.2.1 L1 CACHE Operation

The L1 CACHE has both code cache and data cache. This function group provides independent two groups API for both code cache and data cache. There are Enable/Disable APIs for code cache and data cache control and cache maintenance operations as Invalidate/Clean/CleanInvalidate by all and by address range.

#### 7.2.2 L2 CACHE Operation

The L2 CACHE does not divide the cache to data and code. Instead, this function group provides one group cache maintenance operations as Enable/Disable/Invalidate/Clean/CleanInvalidate by all and by address range. Except the maintenance operation APIs, the L2 CACHE has its initialization/configure API. The user can use the default configure parameter by calling L2CACHE\_GetDefaultConfig() or changing the parameters as they wish. Then, call L2CACHE\_Init to do the L2 CACHE initialization. After initialization, the L2 cache can then be enabled.

Note: For the core external l2 Cache, the SoC usually has the control bit to select the SRAM to use as L2 Cache or normal SRAM. Make sure this selection is right when you use the L2 CACHE feature.

## Driver version

- #define **FSL\_CACHE\_DRIVER\_VERSION** (**MAKE\_VERSION**(2, 0, 4))  
*cache driver version 2.0.4.*

## Control for cortex-m7 L1 cache

- static void **L1CACHE\_EnableICache** (void)  
*Enables cortex-m7 L1 instruction cache.*
- static void **L1CACHE\_DisableICache** (void)  
*Disables cortex-m7 L1 instruction cache.*
- static void **L1CACHE\_InvalidateICache** (void)  
*Invalidate cortex-m7 L1 instruction cache.*
- void **L1CACHE\_InvalidateICacheByRange** (uint32\_t address, uint32\_t size\_byte)  
*Invalidate cortex-m7 L1 instruction cache by range.*
- static void **L1CACHE\_EnableDCache** (void)  
*Enables cortex-m7 L1 data cache.*
- static void **L1CACHE\_DisableDCache** (void)  
*Disables cortex-m7 L1 data cache.*
- static void **L1CACHE\_InvalidateDCache** (void)  
*Invalidates cortex-m7 L1 data cache.*
- static void **L1CACHE\_CleanDCache** (void)  
*Cleans cortex-m7 L1 data cache.*
- static void **L1CACHE\_CleanInvalidateDCache** (void)  
*Cleans and Invalidates cortex-m7 L1 data cache.*
- static void **L1CACHE\_InvalidateDCacheByRange** (uint32\_t address, uint32\_t size\_byte)  
*Invalidates cortex-m7 L1 data cache by range.*
- static void **L1CACHE\_CleanDCacheByRange** (uint32\_t address, uint32\_t size\_byte)  
*Cleans cortex-m7 L1 data cache by range.*
- static void **L1CACHE\_CleanInvalidateDCacheByRange** (uint32\_t address, uint32\_t size\_byte)  
*Cleans and Invalidates cortex-m7 L1 data cache by range.*

## Unified Cache Control for all caches (cortex-m7 L1 cache + I2 pI310)

Mainly used for many drivers for easy cache operation.

- void **ICACHE\_InvalidateByRange** (uint32\_t address, uint32\_t size\_byte)  
*Invalidates all instruction caches by range.*
- void **DCACHE\_InvalidateByRange** (uint32\_t address, uint32\_t size\_byte)  
*Invalidates all data caches by range.*
- void **DCACHE\_CleanByRange** (uint32\_t address, uint32\_t size\_byte)  
*Cleans all data caches by range.*
- void **DCACHE\_CleanInvalidateByRange** (uint32\_t address, uint32\_t size\_byte)  
*Cleans and Invalidates all data caches by range.*

## 7.3 Macro Definition Documentation

### 7.3.1 #define FSL\_CACHE\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 4))

## 7.4 Function Documentation

7.4.1 **void L1CACHE\_InvalidateCacheByRange ( *uint32\_t address*, *uint32\_t size\_byte* )**

## Parameters

|                  |                                                    |
|------------------|----------------------------------------------------|
| <i>address</i>   | The start address of the memory to be invalidated. |
| <i>size_byte</i> | The memory size.                                   |

## Note

The start address and size\_byte should be 32-byte(FSL\_FEATURE\_L1ICACHE\_LINESIZE\_BYTE) aligned. The startAddr here will be forced to align to L1 I-cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

#### 7.4.2 static void L1CACHE\_InvalidateDCacheByRange ( uint32\_t *address*, uint32\_t *size\_byte* ) [inline], [static]

## Parameters

|                  |                                                    |
|------------------|----------------------------------------------------|
| <i>address</i>   | The start address of the memory to be invalidated. |
| <i>size_byte</i> | The memory size.                                   |

## Note

The start address and size\_byte should be 32-byte(FSL\_FEATURE\_L1DCACHE\_LINESIZE\_BYTE) aligned. The startAddr here will be forced to align to L1 D-cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

#### 7.4.3 static void L1CACHE\_CleanDCacheByRange ( uint32\_t *address*, uint32\_t *size\_byte* ) [inline], [static]

## Parameters

|                  |                                                |
|------------------|------------------------------------------------|
| <i>address</i>   | The start address of the memory to be cleaned. |
| <i>size_byte</i> | The memory size.                               |

## Note

The start address and size\_byte should be 32-byte(FSL\_FEATURE\_L1DCACHE\_LINESIZE\_BYTE) aligned. The startAddr here will be forced to align to L1 D-cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

7.4.4 **static void L1CACHE\_CleanInvalidateDCacheByRange ( uint32\_t *address*,  
              uint32\_t *size\_byte* ) [inline], [static]**

Parameters

|                  |                                                              |
|------------------|--------------------------------------------------------------|
| <i>address</i>   | The start address of the memory to be clean and invalidated. |
| <i>size_byte</i> | The memory size.                                             |

Note

The start address and *size\_byte* should be 32-byte(FSL\_FEATURE\_L1DCACHE\_LINESIZE\_BYTE) aligned. The startAddr here will be forced to align to L1 D-cache line size if startAddr is not aligned. For the *size\_byte*, application should make sure the alignment or make sure the right operation order if the *size\_byte* is not aligned.

#### 7.4.5 void ICACHE\_InvalidateByRange ( **uint32\_t address, uint32\_t size\_byte** )

Both cortex-m7 L1 cache line and L2 PL310 cache line length is 32-byte.

Parameters

|                  |                                       |
|------------------|---------------------------------------|
| <i>address</i>   | The physical address.                 |
| <i>size_byte</i> | size of the memory to be invalidated. |

Note

*address* and *size* should be aligned to cache line size 32-Byte due to the cache operation unit is one cache line. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the *size\_byte*, application should make sure the alignment or make sure the right operation order if the *size\_byte* is not aligned.

#### 7.4.6 void DCACHE\_InvalidateByRange ( **uint32\_t address, uint32\_t size\_byte** )

Both cortex-m7 L1 cache line and L2 PL310 cache line length is 32-byte.

Parameters

|                |                       |
|----------------|-----------------------|
| <i>address</i> | The physical address. |
|----------------|-----------------------|

|                  |                                       |
|------------------|---------------------------------------|
| <i>size_byte</i> | size of the memory to be invalidated. |
|------------------|---------------------------------------|

## Note

address and size should be aligned to cache line size 32-Byte due to the cache operation unit is one cache line. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

**7.4.7 void DCACHE\_CleanByRange ( uint32\_t *address*, uint32\_t *size\_byte* )**

Both cortex-m7 L1 cache line and L2 PL310 cache line length is 32-byte.

## Parameters

|                  |                                   |
|------------------|-----------------------------------|
| <i>address</i>   | The physical address.             |
| <i>size_byte</i> | size of the memory to be cleaned. |

## Note

address and size should be aligned to cache line size 32-Byte due to the cache operation unit is one cache line. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

**7.4.8 void DCACHE\_CleanInvalidateByRange ( uint32\_t *address*, uint32\_t *size\_byte* )**

Both cortex-m7 L1 cache line and L2 PL310 cache line length is 32-byte.

## Parameters

|                  |                                                   |
|------------------|---------------------------------------------------|
| <i>address</i>   | The physical address.                             |
| <i>size_byte</i> | size of the memory to be cleaned and invalidated. |

## Note

address and size should be aligned to cache line size 32-Byte due to the cache operation unit is one cache line. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

# Chapter 8

## Common Driver

### 8.1 Overview

The MCUXpresso SDK provides a driver for the common module of MCUXpresso SDK devices.

#### Macros

- `#define FSL_DRIVER_TRANSFER_DOUBLE_WEAK_IRQ 1`  
*Macro to use the default weak IRQ handler in drivers.*
- `#define MAKE_STATUS(group, code) (((group)*100L) + (code))`  
*Construct a status code value from a group and code number.*
- `#define MAKE_VERSION(major, minor, bugfix) (((major)*65536L) + ((minor)*256L) + (bugfix))`  
*Construct the version number for drivers.*
- `#define ARRAY_SIZE(x) (sizeof(x) / sizeof((x)[0]))`  
*Computes the number of elements in an array.*
- `#define SUPPRESS_FALL_THROUGH_WARNING()`  
*For switch case code block, if case section ends without "break;" statement, there will be fallthrough warning with compiler flag -Wextra or -Wimplicit-fallthrough=n when using armgcc.*

#### Typedefs

- `typedef int32_t status_t`  
*Type used for all status and error return values.*

## Enumerations

- enum `_status_groups` {  
    `kStatusGroup_Generic` = 0,  
    `kStatusGroup_FLASH` = 1,  
    `kStatusGroup_LP SPI` = 4,  
    `kStatusGroup_FLEXIO_SPI` = 5,  
    `kStatusGroup_DSPI` = 6,  
    `kStatusGroup_FLEXIO_UART` = 7,  
    `kStatusGroup_FLEXIO_I2C` = 8,  
    `kStatusGroup_LPI2C` = 9,  
    `kStatusGroup_UART` = 10,  
    `kStatusGroup_I2C` = 11,  
    `kStatusGroup_LPSCI` = 12,  
    `kStatusGroup_LPUART` = 13,  
    `kStatusGroup_SPI` = 14,  
    `kStatusGroup_XRDC` = 15,  
    `kStatusGroup_SEMA42` = 16,  
    `kStatusGroup_SDHC` = 17,  
    `kStatusGroup_SDMMC` = 18,  
    `kStatusGroup_SAI` = 19,  
    `kStatusGroup_MCG` = 20,  
    `kStatusGroup_SCG` = 21,  
    `kStatusGroup_SD SPI` = 22,  
    `kStatusGroup_FLEXIO_I2S` = 23,  
    `kStatusGroup_FLEXIO_MCULCD` = 24,  
    `kStatusGroup_FLASHIAP` = 25,  
    `kStatusGroup_FLEXCOMM_I2C` = 26,  
    `kStatusGroup_I2S` = 27,  
    `kStatusGroup_IUART` = 28,  
    `kStatusGroup_CSI` = 29,  
    `kStatusGroup_MIPI_DSI` = 30,  
    `kStatusGroup_SDRAMC` = 35,  
    `kStatusGroup_POWER` = 39,  
    `kStatusGroup_ENET` = 40,  
    `kStatusGroup_PHY` = 41,  
    `kStatusGroup_TRGMUX` = 42,  
    `kStatusGroup_SMARTCARD` = 43,  
    `kStatusGroup_LMEM` = 44,  
    `kStatusGroup_QSPI` = 45,  
    `kStatusGroup_DMA` = 50,  
    `kStatusGroup_EDMA` = 51,  
    `kStatusGroup_DMAMGR` = 52,  
    `kStatusGroup_FLEXCAN` = 53,  
    `kStatusGroup_LTC` = 54,  
    `kStatusGroup_FLEXIO_CAMERA` = 55,  
    `kStatusGroup_LPC_SPI` = 56,  
    `kStatusGroup_EPC_USAR` = 57,  
    `kStatusGroup_DMIC` = 58,  
    `kStatusGroup_SDIF` = 59,  
}

```

kStatusGroup_ELE = 167 }
 Status group numbers.
• enum {
 kStatus_Success = MAKE_STATUS(kStatusGroup_Generic, 0),
 kStatus_Fail = MAKE_STATUS(kStatusGroup_Generic, 1),
 kStatus_ReadOnly = MAKE_STATUS(kStatusGroup_Generic, 2),
 kStatus_OutOfRange = MAKE_STATUS(kStatusGroup_Generic, 3),
 kStatus_InvalidArgument = MAKE_STATUS(kStatusGroup_Generic, 4),
 kStatus_Timeout = MAKE_STATUS(kStatusGroup_Generic, 5),
 kStatus_NoTransferInProgress,
 kStatus_Busy = MAKE_STATUS(kStatusGroup_Generic, 7),
 kStatus_NoData }
 Generic status return codes.

```

## Functions

- void \* **SDK\_Malloc** (size\_t size, size\_t alignbytes)
 *Allocate memory with given alignment and aligned size.*
- void **SDK\_Free** (void \*ptr)
 *Free memory.*
- void **SDK\_DelayAtLeastUs** (uint32\_t delayTime\_us, uint32\_t coreClock\_Hz)
 *Delay at least for some time.*
- static **status\_t EnableIRQ** (IRQn\_Type interrupt)
 *Enable specific interrupt.*
- static **status\_t DisableIRQ** (IRQn\_Type interrupt)
 *Disable specific interrupt.*
- static **status\_t EnableIRQWithPriority** (IRQn\_Type interrupt, uint8\_t priNum)
 *Enable the IRQ, and also set the interrupt priority.*
- static **status\_t IRQ\_SetPriority** (IRQn\_Type interrupt, uint8\_t priNum)
 *Set the IRQ priority.*
- static **status\_t IRQ\_ClearPendingIRQ** (IRQn\_Type interrupt)
 *Clear the pending IRQ flag.*
- static uint32\_t **DisableGlobalIRQ** (void)
 *Disable the global IRQ.*
- static void **EnableGlobalIRQ** (uint32\_t primask)
 *Enable the global IRQ.*

## Driver version

- #define **FSL\_COMMON\_DRIVER\_VERSION** (MAKE\_VERSION(2, 4, 0))
 *common driver version.*

## Debug console type definition.

- #define **DEBUG\_CONSOLE\_DEVICE\_TYPE\_NONE** 0U
 *No debug console.*
- #define **DEBUG\_CONSOLE\_DEVICE\_TYPE\_UART** 1U
 *Debug console based on UART.*
- #define **DEBUG\_CONSOLE\_DEVICE\_TYPE\_LPUART** 2U

- `#define DEBUG_CONSOLE_DEVICE_TYPE_LPSCI 3U`  
*Debug console based on LPSCI.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_USBCDC 4U`  
*Debug console based on USBCDC.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_FLEXCOMM 5U`  
*Debug console based on FLEXCOMM.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_IUART 6U`  
*Debug console based on i.MX UART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_VUSART 7U`  
*Debug console based on LPC\_VUSART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_MINI_USART 8U`  
*Debug console based on LPC\_USART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_SWO 9U`  
*Debug console based on SWO.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_QSCI 10U`  
*Debug console based on QSCI.*

## Min/max macros

- `#define MIN(a, b) (((a) < (b)) ? (a) : (b))`  
*Computes the minimum of a and b.*
- `#define MAX(a, b) (((a) > (b)) ? (a) : (b))`  
*Computes the maximum of a and b.*

## UINT16\_MAX(UINT32\_MAX value

- `#define UINT16_MAX ((uint16_t)-1)`  
*Max value of uint16\_t type.*
- `#define UINT32_MAX ((uint32_t)-1)`  
*Max value of uint32\_t type.*

## Atomic modification

These macros are used for atomic access, such as read-modify-write to the peripheral registers.

Take `SDK_ATOMIC_LOCAL_CLEAR_AND_SET` as an example: the parameter `addr` means the address of the peripheral register or variable you want to modify atomically, the parameter `clearBits` is the bits to clear, the parameter `setBits` is the bits to set. For example, to set a 32-bit register bit1:bit0 to 0b10, use like this:

```
volatile uint32_t * reg = (volatile uint32_t *)REG_ADDR;
SDK_ATOMIC_LOCAL_CLEAR_AND_SET(reg, 0x03, 0x02);
```

In this example, the register bit1:bit0 are cleared and bit1 is set, as a result, register bit1:bit0 = 0b10.

## Note

For the platforms don't support exclusive load and store, these macros disable the global interrupt to protect the modification.

These macros only guarantee the local processor atomic operations. For the multi-processor devices, use hardware semaphore such as SEMA42 to guarantee exclusive access if necessary.

- `#define SDK_ATOMIC_LOCAL_ADD(addr, val)`  
*Add value val from the variable at address address.*
- `#define SDK_ATOMIC_LOCAL_SUB(addr, val)`  
*Subtract value val to the variable at address address.*
- `#define SDK_ATOMIC_LOCAL_SET(addr, bits)`  
*Set the bits specified by bits to the variable at address address.*
- `#define SDK_ATOMIC_LOCAL_CLEAR(addr, bits)`  
*Clear the bits specified by bits to the variable at address address.*
- `#define SDK_ATOMIC_LOCAL_TOGGLE(addr, bits)`  
*Toggle the bits specified by bits to the variable at address address.*
- `#define SDK_ATOMIC_LOCAL_CLEAR_AND_SET(addr, clearBits, setBits)`  
*For the variable at address address, clear the bits specified by clearBits and set the bits specified by setBits.*

## Timer utilities

- `#define USEC_TO_COUNT(us, clockFreqInHz) (uint64_t)((uint64_t)(us) * (clockFreqInHz)) / 1000000U)`  
*Macro to convert a microsecond period to raw count value.*
- `#define COUNT_TO_USEC(count, clockFreqInHz) (uint64_t)((uint64_t)(count)*1000000U / (clockFreqInHz))`  
*Macro to convert a raw count value to microsecond.*
- `#define MSEC_TO_COUNT(ms, clockFreqInHz) (uint64_t)((uint64_t)(ms) * (clockFreqInHz) / 1000U)`  
*Macro to convert a millisecond period to raw count value.*
- `#define COUNT_TO_MSEC(count, clockFreqInHz) (uint64_t)((uint64_t)(count)*1000U / (clockFreqInHz))`  
*Macro to convert a raw count value to millisecond.*

## Alignment variable definition macros

- `#define SDK_ALIGN(var, alignbytes) var __attribute__((aligned(alignbytes)))`  
*Macro to define a variable with alignbytes alignment.*
- `#define SDK_L1DCACHE_ALIGN(var) SDK_ALIGN(var, FSL_FEATURE_L1DCACHE_LINESIZE_BYTEx)`  
*Macro to define a variable with L1 d-cache line size alignment.*
- `#define SDK_SIZEALIGN(var, alignbytes) ((unsigned int)((var) + ((alignbytes)-1U)) & (unsigned int)(~(unsigned int)((alignbytes)-1U)))`  
*Macro to define a variable with L2 cache line size alignment.*

## Non-cacheable region definition macros

For initialized non-zero non-cacheable variables, please use "AT\_NONCACHEABLE\_SECTION\_INIT(var) ={xx};" or "AT\_NONCACHEABLE\_SECTION\_ALIGN\_INIT(var) ={xx};" in your projects to

define them.

For zero-init non-cacheable variables, please use "AT\_NONCACHEABLE\_SECTION(var);" or "-AT\_NONCACHEABLE\_SECTION\_ALIGN(var);" to define them, these zero-initied variables will be initialized to zero in system startup.

#### Note

For GCC, when the non-cacheable section is required, please define "\_\_STARTUP\_INITIALIZE\_NONCACHEDATA" in your projects to make sure the non-cacheable section variables will be initialized in system startup.

- #define `AT_NONCACHEABLE_SECTION(var) __attribute__((section("NonCacheable,\"aw\",%nobits @)))` var  
*Define a variable var, and place it in non-cacheable section.*
- #define `AT_NONCACHEABLE_SECTION_ALIGN(var, alignbytes) __attribute__((section("NonCacheable,\"aw\",%nobits @)))` var \_\_attribute\_\_((aligned(alignbytes)))  
*Define a variable var, and place it in non-cacheable section, the start address of the variable is aligned to alignbytes.*
- #define `AT_NONCACHEABLE_SECTION_INIT(var) __attribute__((section("NonCacheable.-init")))` var  
*Define a variable var with initial value, and place it in non-cacheable section.*
- #define `AT_NONCACHEABLE_SECTION_ALIGN_INIT(var, alignbytes) __attribute__((section("NonCacheable.init")))` var \_\_attribute\_\_((aligned(alignbytes)))  
*Define a variable var with initial value, and place it in non-cacheable section, the start address of the variable is aligned to alignbytes.*

## Time sensitive region

- #define `AT_QUICKACCESS_SECTION_CODE(func) __attribute__((section("CodeQuickAccess"), __noinline__))` func  
*Place function in a section which can be accessed quickly by core.*
- #define `AT_QUICKACCESS_SECTION_DATA(var) __attribute__((section("DataQuickAccess")))` var  
*Place data in a section which can be accessed quickly by core.*
- #define `AT_QUICKACCESS_SECTION_DATA_ALIGN(var, alignbytes) __attribute__((section("DataQuickAccess")))` var \_\_attribute\_\_((aligned(alignbytes)))  
*Place data in a section which can be accessed quickly by core, and the variable address is set to align with alignbytes.*

## Ram Function

- #define `RAMFUNCTION_SECTION_CODE(func) __attribute__((section("RamFunction")))` func  
*Place function in ram.*

## 8.2 Macro Definition Documentation

8.2.1 `#define FSL_DRIVER_TRANSFER_DOUBLE_WEAK_IRQ 1`

8.2.2 `#define MAKE_STATUS( group, code ) (((group)*100L) + (code))`

8.2.3 `#define MAKE_VERSION( major, minor, bugfix ) (((major)*65536L) + ((minor)*256L) + (bugfix))`

The driver version is a 32-bit number, for both 32-bit platforms(such as Cortex M) and 16-bit platforms(such as DSC).

|        |  |               |  |               |  |         |  |   |
|--------|--|---------------|--|---------------|--|---------|--|---|
| Unused |  | Major Version |  | Minor Version |  | Bug Fix |  |   |
| 31     |  | 25 24         |  | 17 16         |  | 9 8     |  | 0 |

- 8.2.4 `#define FSL_COMMON_DRIVER_VERSION (MAKE_VERSION(2, 4, 0))`
- 8.2.5 `#define DEBUG_CONSOLE_DEVICE_TYPE_NONE 0U`
- 8.2.6 `#define DEBUG_CONSOLE_DEVICE_TYPE_UART 1U`
- 8.2.7 `#define DEBUG_CONSOLE_DEVICE_TYPE_LPUART 2U`
- 8.2.8 `#define DEBUG_CONSOLE_DEVICE_TYPE_LPSCI 3U`
- 8.2.9 `#define DEBUG_CONSOLE_DEVICE_TYPE_USBCDC 4U`
- 8.2.10 `#define DEBUG_CONSOLE_DEVICE_TYPE_FLEXCOMM 5U`
- 8.2.11 `#define DEBUG_CONSOLE_DEVICE_TYPE_IUART 6U`
- 8.2.12 `#define DEBUG_CONSOLE_DEVICE_TYPE_VUSART 7U`
- 8.2.13 `#define DEBUG_CONSOLE_DEVICE_TYPE_MINI_USART 8U`
- 8.2.14 `#define DEBUG_CONSOLE_DEVICE_TYPE_SWO 9U`
- 8.2.15 `#define DEBUG_CONSOLE_DEVICE_TYPE_QSCI 10U`
- 8.2.16 `#define MIN( a, b ) (((a) < (b)) ? (a) : (b))`
- 8.2.17 `#define MAX( a, b ) (((a) > (b)) ? (a) : (b))`
- 8.2.18 `#define ARRAY_SIZE( x ) (sizeof(x) / sizeof((x)[0]))`
- 8.2.19 `#define UINT16_MAX ((uint16_t)-1)`
- 8.2.20 `#define UINT32_MAX ((uint32_t)-1)`
- 8.2.21 `#define SUPPRESS_FALL_THROUGH_WARNING( )`

To suppress this warning, "SUPPRESS\_FALL\_THROUGH\_WARNING();" need to be added at the end of each case section which misses "break;" statement.

```
8.2.22 #define SDK_SIZEALIGN(var, alignbytes) ((unsigned int)((var) + ((alignbytes)-1U)) & (unsigned int)(~(unsigned int)((alignbytes)-1U)))
```

Macro to change a value to a given size aligned value

## 8.3 Typedef Documentation

### 8.3.1 `typedef int32_t status_t`

## 8.4 Enumeration Type Documentation

### 8.4.1 `enum _status_groups`

Enumerator

`kStatusGroup_Generic` Group number for generic status codes.

`kStatusGroup_FLASH` Group number for FLASH status codes.

`kStatusGroup_LP SPI` Group number for LP SPI status codes.

`kStatusGroup_FLEXIO_SPI` Group number for FLEXIO SPI status codes.

`kStatusGroup_DSPI` Group number for DSPI status codes.

`kStatusGroup_FLEXIO_UART` Group number for FLEXIO UART status codes.

`kStatusGroup_FLEXIO_I2C` Group number for FLEXIO I2C status codes.

`kStatusGroup_LPI2C` Group number for LPI2C status codes.

`kStatusGroup_UART` Group number for UART status codes.

`kStatusGroup_I2C` Group number for I2C status codes.

`kStatusGroup_LPSCI` Group number for LPSCI status codes.

`kStatusGroup_LPUART` Group number for LPUART status codes.

`kStatusGroup_SPI` Group number for SPI status code.

`kStatusGroup_XRDC` Group number for XRDC status code.

`kStatusGroup_SEMA42` Group number for SEMA42 status code.

`kStatusGroup_SDHC` Group number for SDHC status code.

`kStatusGroup_SDMMC` Group number for SDMMC status code.

`kStatusGroup_SAI` Group number for SAI status code.

`kStatusGroup_MCG` Group number for MCG status codes.

`kStatusGroup_SCG` Group number for SCG status codes.

`kStatusGroup_SD SPI` Group number for SD SPI status codes.

`kStatusGroup_FLEXIO_I2S` Group number for FLEXIO I2S status codes.

`kStatusGroup_FLEXIO_MCULCD` Group number for FLEXIO LCD status codes.

`kStatusGroup_FLASHIAP` Group number for FLASHIAP status codes.

`kStatusGroup_FLEXCOMM_I2C` Group number for FLEXCOMM I2C status codes.

`kStatusGroup_I2S` Group number for I2S status codes.

`kStatusGroup_IUART` Group number for IUART status codes.

`kStatusGroup_CSI` Group number for CSI status codes.

`kStatusGroup_MIPI_DSI` Group number for MIPI DSI status codes.

`kStatusGroup_SDRAMC` Group number for SDRAMC status codes.

*kStatusGroup\_POWER* Group number for POWER status codes.  
*kStatusGroup\_ENET* Group number for ENET status codes.  
*kStatusGroup\_PHY* Group number for PHY status codes.  
*kStatusGroup\_TRGMUX* Group number for TRGMUX status codes.  
*kStatusGroup\_SMARTCARD* Group number for SMARTCARD status codes.  
*kStatusGroup\_LMEM* Group number for LMEM status codes.  
*kStatusGroup\_QSPI* Group number for QSPI status codes.  
*kStatusGroup\_DMA* Group number for DMA status codes.  
*kStatusGroup\_EDMA* Group number for EDMA status codes.  
*kStatusGroup\_DMAMGR* Group number for DMAMGR status codes.  
*kStatusGroup\_FLEXCAN* Group number for FlexCAN status codes.  
*kStatusGroup\_LTC* Group number for LTC status codes.  
*kStatusGroup\_FLEXIO\_CAMERA* Group number for FLEXIO CAMERA status codes.  
*kStatusGroup\_LPC\_SPI* Group number for LPC\_SPI status codes.  
*kStatusGroup\_LPC\_USART* Group number for LPC\_USART status codes.  
*kStatusGroup\_DMIC* Group number for DMIC status codes.  
*kStatusGroup\_SDIF* Group number for SDIF status codes.  
*kStatusGroup\_SPIFI* Group number for SPIFI status codes.  
*kStatusGroup OTP* Group number for OTP status codes.  
*kStatusGroup\_MCAN* Group number for MCAN status codes.  
*kStatusGroup\_CAAM* Group number for CAAM status codes.  
*kStatusGroup\_ECSPI* Group number for ECSPI status codes.  
*kStatusGroup\_USDHC* Group number for USDHC status codes.  
*kStatusGroup\_LPC\_I2C* Group number for LPC\_I2C status codes.  
*kStatusGroup\_DCP* Group number for DCP status codes.  
*kStatusGroup\_MSCAN* Group number for MSCAN status codes.  
*kStatusGroup\_ESAI* Group number for ESAI status codes.  
*kStatusGroup\_FLEXSPI* Group number for FLEXSPI status codes.  
*kStatusGroup\_MMDC* Group number for MMDC status codes.  
*kStatusGroup\_PDM* Group number for MIC status codes.  
*kStatusGroup\_SDMA* Group number for SDMA status codes.  
*kStatusGroup\_ICS* Group number for ICS status codes.  
*kStatusGroup\_SPDIF* Group number for SPDIF status codes.  
*kStatusGroup\_LPC\_MINISPI* Group number for LPC\_MINISPI status codes.  
*kStatusGroup\_HASHCRYPT* Group number for Hashcrypt status codes.  
*kStatusGroup\_LPC\_SPI\_SSP* Group number for LPC\_SPI\_SSP status codes.  
*kStatusGroup\_I3C* Group number for I3C status codes.  
*kStatusGroup\_LPC\_I2C\_1* Group number for LPC\_I2C\_1 status codes.  
*kStatusGroup\_NOTIFIER* Group number for NOTIFIER status codes.  
*kStatusGroup\_DebugConsole* Group number for debug console status codes.  
*kStatusGroup\_SEMC* Group number for SEMC status codes.  
*kStatusGroup\_ApplicationRangeStart* Starting number for application groups.  
*kStatusGroup\_IAP* Group number for IAP status codes.  
*kStatusGroup\_SFA* Group number for SFA status codes.  
*kStatusGroup\_SPC* Group number for SPC status codes.

*kStatusGroup\_PUF* Group number for PUF status codes.  
*kStatusGroup\_TOUCH\_PANEL* Group number for touch panel status codes.  
*kStatusGroup\_VBAT* Group number for VBAT status codes.  
*kStatusGroup\_HAL\_GPIO* Group number for HAL GPIO status codes.  
*kStatusGroup\_HAL\_UART* Group number for HAL UART status codes.  
*kStatusGroup\_HAL\_TIMER* Group number for HAL TIMER status codes.  
*kStatusGroup\_HAL\_SPI* Group number for HAL SPI status codes.  
*kStatusGroup\_HAL\_I2C* Group number for HAL I2C status codes.  
*kStatusGroup\_HAL\_FLASH* Group number for HAL FLASH status codes.  
*kStatusGroup\_HAL\_PWM* Group number for HAL PWM status codes.  
*kStatusGroup\_HAL\_RNG* Group number for HAL RNG status codes.  
*kStatusGroup\_HAL\_I2S* Group number for HAL I2S status codes.  
*kStatusGroup\_HAL\_ADC\_SENSOR* Group number for HAL ADC SENSOR status codes.  
*kStatusGroup\_TIMERMANAGER* Group number for TiMER MANAGER status codes.  
*kStatusGroup\_SERIALMANAGER* Group number for SERIAL MANAGER status codes.  
*kStatusGroup\_LED* Group number for LED status codes.  
*kStatusGroup\_BUTTON* Group number for BUTTON status codes.  
*kStatusGroup\_EXTERN\_EEPROM* Group number for EXTERN EEPROM status codes.  
*kStatusGroup\_SHELL* Group number for SHELL status codes.  
*kStatusGroup\_MEM\_MANAGER* Group number for MEM MANAGER status codes.  
*kStatusGroup\_LIST* Group number for List status codes.  
*kStatusGroup\_OSA* Group number for OSA status codes.  
*kStatusGroup\_COMMON\_TASK* Group number for Common task status codes.  
*kStatusGroup\_MSG* Group number for messaging status codes.  
*kStatusGroup\_SDK\_OCOTP* Group number for OCOTP status codes.  
*kStatusGroup\_SDK\_FLEXSPINOR* Group number for FLEXSPINOR status codes.  
*kStatusGroup\_CODEC* Group number for codec status codes.  
*kStatusGroup\_ASRC* Group number for codec status ASRC.  
*kStatusGroup\_OTFAD* Group number for codec status codes.  
*kStatusGroup\_SDIOSLV* Group number for SDIOSLV status codes.  
*kStatusGroup\_MECC* Group number for MECC status codes.  
*kStatusGroup\_ENET\_QOS* Group number for ENET\_QOS status codes.  
*kStatusGroup\_LOG* Group number for LOG status codes.  
*kStatusGroup\_I3CBUS* Group number for I3CBUS status codes.  
*kStatusGroup\_QSCI* Group number for QSCI status codes.  
*kStatusGroup\_ELEMU* Group number for ELEMU status codes.  
*kStatusGroup\_QUEUEDSPI* Group number for QSPI status codes.  
*kStatusGroup\_POWER\_MANAGER* Group number for POWER\_MANAGER status codes.  
*kStatusGroup\_IPED* Group number for IPED status codes.  
*kStatusGroup\_ELS\_PKC* Group number for ELS PKC status codes.  
*kStatusGroup\_CSS\_PKC* Group number for CSS PKC status codes.  
*kStatusGroup\_HOSTIF* Group number for HOSTIF status codes.  
*kStatusGroup\_CLIF* Group number for CLIF status codes.  
*kStatusGroup\_BMA* Group number for BMA status codes.  
*kStatusGroup\_NETC* Group number for NETC status codes.

***kStatusGroup\_ELE*** Group number for ELE status codes.

### 8.4.2 anonymous enum

Enumerator

***kStatus\_Success*** Generic status for Success.

***kStatus\_Fail*** Generic status for Fail.

***kStatus\_ReadOnly*** Generic status for read only failure.

***kStatus\_OutOfRange*** Generic status for out of range access.

***kStatus\_InvalidArgument*** Generic status for invalid argument check.

***kStatus\_Timeout*** Generic status for timeout.

***kStatus\_NoTransferInProgress*** Generic status for no transfer in progress.

***kStatus\_Busy*** Generic status for module is busy.

***kStatus\_NoData*** Generic status for no data is found for the operation.

## 8.5 Function Documentation

### 8.5.1 **void\* SDK\_Malloc ( size\_t size, size\_t alignbytes )**

This is provided to support the dynamically allocated memory used in cache-able region.

Parameters

|                   |                                |
|-------------------|--------------------------------|
| <i>size</i>       | The length required to malloc. |
| <i>alignbytes</i> | The alignment size.            |

Return values

|            |                   |
|------------|-------------------|
| <i>The</i> | allocated memory. |
|------------|-------------------|

### 8.5.2 **void SDK\_Free ( void \*ptr )**

Parameters

|            |                           |
|------------|---------------------------|
| <i>ptr</i> | The memory to be release. |
|------------|---------------------------|

### 8.5.3 **void SDK\_DelayAtLeastUs ( uint32\_t delayTime\_us, uint32\_t coreClock\_Hz )**

Please note that, this API uses while loop for delay, different run-time environments make the time not precise, if precise delay count was needed, please implement a new delay function with hardware timer.

Parameters

|                     |                                    |
|---------------------|------------------------------------|
| <i>delayTime_us</i> | Delay time in unit of microsecond. |
| <i>coreClock_Hz</i> | Core clock frequency with Hz.      |

#### 8.5.4 static status\_t EnableIRQ ( IRQn\_Type *interrupt* ) [inline], [static]

Enable LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only enables the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1 INT VECTORS.

Parameters

|                  |                 |
|------------------|-----------------|
| <i>interrupt</i> | The IRQ number. |
|------------------|-----------------|

Return values

|                        |                                |
|------------------------|--------------------------------|
| <i>kStatus_Success</i> | Interrupt enabled successfully |
| <i>kStatus_Fail</i>    | Failed to enable the interrupt |

#### 8.5.5 static status\_t DisableIRQ ( IRQn\_Type *interrupt* ) [inline], [static]

Disable LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only disables the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1 INT VECTORS.

Parameters

|                  |                 |
|------------------|-----------------|
| <i>interrupt</i> | The IRQ number. |
|------------------|-----------------|

Return values

|                        |                                 |
|------------------------|---------------------------------|
| <i>kStatus_Success</i> | Interrupt disabled successfully |
| <i>kStatus_Fail</i>    | Failed to disable the interrupt |

### 8.5.6 static status\_t EnableIRQWithPriority ( IRQn\_Type *interrupt*, uint8\_t *priNum* ) [inline], [static]

Only handle LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only handles the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1 INT VECTORS.

Parameters

|                  |                                                       |
|------------------|-------------------------------------------------------|
| <i>interrupt</i> | The IRQ to Enable.                                    |
| <i>priNum</i>    | Priority number set to interrupt controller register. |

Return values

|                        |                                       |
|------------------------|---------------------------------------|
| <i>kStatus_Success</i> | Interrupt priority set successfully   |
| <i>kStatus_Fail</i>    | Failed to set the interrupt priority. |

### 8.5.7 static status\_t IRQ\_SetPriority ( IRQn\_Type *interrupt*, uint8\_t *priNum* ) [inline], [static]

Only handle LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only handles the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1 INT VECTORS.

Parameters

|                  |                                                       |
|------------------|-------------------------------------------------------|
| <i>interrupt</i> | The IRQ to set.                                       |
| <i>priNum</i>    | Priority number set to interrupt controller register. |

Return values

|                        |                                       |
|------------------------|---------------------------------------|
| <i>kStatus_Success</i> | Interrupt priority set successfully   |
| <i>kStatus_Fail</i>    | Failed to set the interrupt priority. |

### 8.5.8 static status\_t IRQ\_ClearPendingIRQ ( IRQn\_Type *interrupt* ) [inline], [static]

Only handle LEVEL1 interrupt. For some devices, there might be multiple interrupt levels. For example, there are NVIC and intmux. Here the interrupts connected to NVIC are the LEVEL1 interrupts, because they are routed to the core directly. The interrupts connected to intmux are the LEVEL2 interrupts, they are routed to NVIC first then routed to core.

This function only handles the LEVEL1 interrupts. The number of LEVEL1 interrupts is indicated by the feature macro FSL FEATURE NUMBER OF LEVEL1 INT VECTORS.

Parameters

|                  |                              |
|------------------|------------------------------|
| <i>interrupt</i> | The flag which IRQ to clear. |
|------------------|------------------------------|

Return values

|                        |                                       |
|------------------------|---------------------------------------|
| <i>kStatus_Success</i> | Interrupt priority set successfully   |
| <i>kStatus_Fail</i>    | Failed to set the interrupt priority. |

### 8.5.9 static uint32\_t DisableGlobalIRQ ( void ) [inline], [static]

Disable the global interrupt and return the current primask register. User is required to provided the primask register for the [EnableGlobalIRQ\(\)](#).

Returns

Current primask value.

### 8.5.10 static void EnableGlobalIRQ ( uint32\_t *primask* ) [inline], [static]

Set the primask register with the provided primask value but not just enable the primask. The idea is for the convenience of integration of RTOS. some RTOS get its own management mechanism of primask. User is required to use the [EnableGlobalIRQ\(\)](#) and [DisableGlobalIRQ\(\)](#) in pair.

Parameters

|                |                                                                                                                                    |
|----------------|------------------------------------------------------------------------------------------------------------------------------------|
| <i>primask</i> | value of primask register to be restored. The primask value is supposed to be provided by the <a href="#">DisableGlobalIRQ()</a> . |
|----------------|------------------------------------------------------------------------------------------------------------------------------------|

# Chapter 9

## ASRC: Asynchronous sample rate converter

### 9.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Asynchronous sample rate converter module of MCUXpresso SDK devices.

The Asynchronous sample rate converter support convert between sample rate: kASRC\_SampleRate\_8000 = 8000, /\*!< 8K sample rate

### Modules

- [ASRC Driver](#)
- [ASRC SDMA Driver](#)

## 9.2 ASRC Driver

### 9.2.1 Overview

#### Data Structures

- `struct _asrc_data_format`  
`asrc context data format` [More...](#)
- `struct _asrc_access_ctrl`  
`asrc context access control` The ASRC provides interleaving support in hardware to ensure that a variety of sample source can be internally combined tp config with this format. [More...](#)
- `struct _asrc_context_input_config`  
`asrc context input configuration` [More...](#)
- `struct _asrc_context_output_config`  
`asrc context output configuration` [More...](#)
- `struct _asrc_context_prefilter_config`  
`asrc context prefilter configuration` [More...](#)
- `struct _asrc_context_resampler_config`  
`asrc context resampler configuration` [More...](#)
- `struct _asrc_context_config`  
`asrc context configuration` [More...](#)
- `struct _asrc_transfer`  
`ASRC transfer.` [More...](#)

#### Macros

- `#define FSL_ASRC_INPUT_FIFO_DEPTH (128U)`  
`ASRC fifo depth.`
- `#define ASRC_SUPPORT_MAXIMUM_CONTEXT_PROCESSOR_NUMBER 4U`  
`ASRC support maximum channel number of context.`

#### Typedefs

- `typedef enum _asrc_context asrc_context_t`  
`asrc context id`
- `typedef enum _asrc_data_endianness asrc_data_endianness_t`  
`asrc data endianness`
- `typedef enum _asrc_data_width asrc_data_width_t`  
`data width`
- `typedef enum _asrc_data_type asrc_data_type_t`  
`data type`
- `typedef enum _asrc_data_sign asrc_data_sign_t`  
`sign extension`
- `typedef enum _asrc_sampleBuffer_init_mode asrc_sampleBuffer_init_mode_t`  
`asrc prefilter and resampler sample buffer init mode`
- `typedef enum _asrc_sampleBuffer_stop_mode asrc_sampleBuffer_stop_mode_t`

- *asrc prefiler and resampler sample buffer stop mode*
- **typedef enum**  
`_asrc_prefilter_stage1_result asrc_prefilter_stage1_result_t`  
*ASRC prefiler stage1 result format.*
- **typedef enum** `_asrc_resampler_taps` `asrc_resampler_taps_t`  
*ASRC resampler taps.*
- **typedef struct** `_asrc_data_format` `asrc_data_format_t`  
*asrc context data format*
- **typedef struct** `_asrc_access_ctrl` `asrc_access_ctrl_t`  
*asrc context access control The ASRC provides interleaving support in hardware to ensure that a variety of sample source can be internally combined tp confir with this format.*
- **typedef struct**  
`_asrc_context_input_config` `asrc_context_input_config_t`  
*asrc context input configuration*
- **typedef struct**  
`_asrc_context_output_config` `asrc_context_output_config_t`  
*asrc context output configuration*
- **typedef struct**  
`_asrc_context_prefilter_config` `asrc_context_prefilter_config_t`  
*asrc context prefiler configuration*
- **typedef struct**  
`_asrc_context_resampler_config` `asrc_context_resampler_config_t`  
*asrc context resampler configuration*
- **typedef struct** `_asrc_context_config` `asrc_context_config_t`  
*asrc context configuration*
- **typedef struct** `_asrc_transfer` `asrc_transfer_t`  
*ASRC transfer.*

## Enumerations

- **enum** {  
`kStatus_ASRCIdle` = MAKE\_STATUS(kStatusGroup\_ASRC, 0),  
`kStatus_ASRCBusy` = MAKE\_STATUS(kStatusGroup\_ASRC, 1),  
`kStatus_ASRCInvalidArgument` = MAKE\_STATUS(kStatusGroup\_ASRC, 2),  
`kStatus_ASRCConfigureFailed` = MAKE\_STATUS(kStatusGroup\_ASRC, 3),  
`kStatus_ASRCConvertError` = MAKE\_STATUS(kStatusGroup\_ASRC, 4),  
`kStatus_ASRCNotSupport` = MAKE\_STATUS(kStatusGroup\_ASRC, 5),  
`kStatus_ASRCQueueFull` = MAKE\_STATUS(kStatusGroup\_ASRC, 6),  
`kStatus_ASRCQueueIdle` = MAKE\_STATUS(kStatusGroup\_ASRC, 7),  
`kStatus_ASRCLoadFirmwareFailed` = MAKE\_STATUS(kStatusGroup\_ASRC, 8),  
`kStatus_ASRCResamplerConfigureFailed` = MAKE\_STATUS(kStatusGroup\_ASRC, 9),  
`kStatus_ASRPCPrefilterConfigureFailed` = MAKE\_STATUS(kStatusGroup\_ASRC, 10) }  
*ASRC return status, \_asrc\_status.*
- **enum** `_asrc_context` {  
`kASRC_Context0` = 0,  
`kASRC_Context1` = 1,  
`kASRC_Context2` = 2,

```

kASRC_Context3 = 3 }

 asrc context id

• enum {
 kASRC_Context0InputFifoOverflow = 1U,
 kASRC_Context1InputFifoOverflow = 1U << 1U,
 kASRC_Context2InputFifoOverflow = 1U << 2U,
 kASRC_Context3InputFifoOverflow = 1U << 3U,
 kASRC_Context0OutFifoReadEmpty = 1U << 4U,
 kASRC_Context1OutFifoReadEmpty = 1U << 5U,
 kASRC_Context2OutFifoReadEmpty = 1U << 6U,
 kASRC_Context3OutFifoReadEmpty = 1U << 7U,
 kASRC_Context0RunStopDone = 1U << 8U,
 kASRC_Context1RunStopDone = 1U << 9U,
 kASRC_Context2RunStopDone = 1U << 10U,
 kASRC_Context3RunStopDone = 1U << 11U,
 kASRC_ContextAllInterruptStatus = 0xFFFFU }

```

*The ASRC interrupt enable flag, \_asrc\_interrupt\_mask.*

- enum {
 kASRC\_FifoStatusInputFifoWatermarkFlag,
 kASRC\_FifoStatusOutputFifoWatermarkFlag }
- ASRC fifo status, \_asrc\_fifo\_status.*
- enum *\_asrc\_data\_endianness* {
 kASRC\_DataEndianLittle = 0U,
 kASRC\_DataEndianBig = 1U }
- asrc data endianness*
- enum *\_asrc\_data\_width* {
 kASRC\_DataWidth32Bit = 3U,
 kASRC\_DataWidth24Bit = 2U,
 kASRC\_DataWidth20Bit = 1U,
 kASRC\_DataWidth16Bit = 0U }
- data width*
- enum *\_asrc\_data\_type* {
 kASRC\_DataTypeInteger = 0U,
 kASRC\_DataTypeFloat = 1U }
- data type*
- enum *\_asrc\_data\_sign* {
 kASRC\_DataSigned = 0U,
 kASRC\_DataUnsigned = 1U }
- sign extension*
- enum *\_asrc\_sampleBuffer\_init\_mode* {
 kASRC\_SampleBufferNoPreFillOnInit = 0U,
 kASRC\_SampleBufferFillFirstSampleOnInit,
 kASRC\_SampleBufferFillZeroOnInit = 2U }
- asrc prefilter and resampler sample buffer init mode*
- enum *\_asrc\_sampleBuffer\_stop\_mode* {
 kASRC\_SampleBufferFillLastSampleOnStop,
 kASRC\_SampleBufferFillZeroOnStop = 1U }

- *asrc prefILTER and resampler sample buffer stop mode.*
- enum `_asrc_prefilter_stage1_result` {
   
  `kASRC_PrefilterStage1ResultInt` = 0U,  
`kASRC_PrefilterStage1ResultFloat` = 1U }
   
*ASRC prefILTER stage1 result format.*
- enum `_asrc_resampler_taps` {
   
  `kASRC_ResamplerTaps_32` = 32U,  
`kASRC_ResamplerTaps_64` = 64U,  
`kASRC_ResamplerTaps_128` = 128U }
   
*ASRC resampler taps.*
- enum {
   
  `kASRC_SampleRate_8000` = 8000,  
`kASRC_SampleRate_11025` = 11025,  
`kASRC_SampleRate_12000` = 12000,  
`kASRC_SampleRate_16000` = 16000,  
`kASRC_SampleRate_22050` = 22050,  
`kASRC_SampleRate_24000` = 24000,  
`kASRC_SampleRate_32000` = 32000,  
`kASRC_SampleRate_44100` = 44100,  
`kASRC_SampleRate_48000` = 48000,  
`kASRC_SampleRate_64000` = 64000,  
`kASRC_SampleRate_88200` = 88200,  
`kASRC_SampleRate_96000` = 96000,  
`kASRC_SampleRate_128000` = 128000,  
`kASRC_SampleRate_176400` = 176400,  
`kASRC_SampleRate_192000` = 192000,  
`kASRC_SampleRate_256000` = 256000,  
`kASRC_SampleRate_352800` = 352800,  
`kASRC_SampleRate_384000` = 384000,  
`kASRC_SampleRate_768000` = 768000 }
   
*ASRC support sample rate, \_asrc\_sample\_rate.*

## Driver version

- #define `FSL_ASRC_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 6)`)
   
*Version 2.0.6.*

## Initialization and deinitialization

- `uint32_t ASRC_GetInstance (ASRC_Type *base)`
  
*Get instance number of the ASRC peripheral.*
- `void ASRC_Init (ASRC_Type *base)`
  
*brief Initializes the asrc peripheral.*
- `void ASRC_Deinit (ASRC_Type *base)`
  
*De-initializes the ASRC peripheral.*

- void [ASRC\\_GetContextDefaultConfig](#) ([asrc\\_context\\_config\\_t](#) \*config, [uint32\\_t](#) channels, [uint32\\_t](#) inSampleRate, [uint32\\_t](#) outSampleRate)  
*ASRC get context default configuration.*
- [status\\_t ASRC\\_SetContextConfig](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context, [asrc\\_context\\_config\\_t](#) \*config)  
*ASRC configure context.*
- [status\\_t ASRC\\_SetContextOutputConfig](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context, [asrc\\_context\\_output\\_config\\_t](#) \*config)  
*ASRC configure context output.*
- [status\\_t ASRC\\_SetContextInputConfig](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context, [asrc\\_context\\_input\\_config\\_t](#) \*config)  
*ASRC configure context input.*
- static void [ASRC\\_EnableContextRun](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context, bool enable)  
*ASRC context enable run.*
- static void [ASRC\\_EnableContextRunStop](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context, bool enable)  
*ASRC context enable run stop.*
- static void [ASRC\\_EnableContextInDMA](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context, bool enable)  
*ASRC context input DMA request enable.*
- static void [ASRC\\_EnableContextOutDMA](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context, bool enable)  
*ASRC context output DMA request enable.*
- static void [ASRC\\_EnablePreFilterBypass](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context, bool bypass)  
*ASRC prefilter bypass mode This function enable or disable the ASRC prefilter bypass mode.*
- static void [ASRC\\_EnableResamplerBypass](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context, bool bypass)  
*ASRC resampler bypass mode This function enable or disable the ASRC resampler bypass mode.*
- static void [ASRC\\_SetContextChannelNumber](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context, [uint32\\_t](#) channels)  
*ASRC set context channel number.*
- [uint32\\_t ASRC\\_GetContextOutSampleSize](#) ([uint32\\_t](#) inSampleRate, [uint32\\_t](#) inSamplesSize, [uint32\\_t](#) inWidth, [uint32\\_t](#) outSampleRate, [uint32\\_t](#) outWidth)  
*ASRC get output sample count.*

## Interrupts

- static void [ASRC\\_EnableInterrupt](#) ([ASRC\\_Type](#) \*base, [uint32\\_t](#) mask)  
*ASRC interrupt enable This function enable the ASRC interrupt with the provided mask.*
- static void [ASRC\\_DisableInterrupt](#) ([ASRC\\_Type](#) \*base, [uint32\\_t](#) mask)  
*ASRC interrupt disable This function disable the ASRC interrupt with the provided mask.*

## Status

- static [uint32\\_t ASRC\\_GetInterruptStatus](#) ([ASRC\\_Type](#) \*base)  
*Gets the ASRC interrupt status flag state.*
- static void [ASRC\\_ClearInterruptStatus](#) ([ASRC\\_Type](#) \*base, [uint32\\_t](#) status)  
*clear the ASRC interrupt status flag state.*
- static [uint32\\_t ASRC\\_GetFifoStatus](#) ([ASRC\\_Type](#) \*base, [asrc\\_context\\_t](#) context)

*Gets the ASRC fifo status flag.*

## fifo Operations

- static void [ASRC\\_WriteContextFifo](#) (ASRC\_Type \*base, [asrc\\_context\\_t](#) context, uint32\_t data)  
*write the ASRC context fifo.*
- static uint32\_t [ASRC\\_ReadContextFifo](#) (ASRC\_Type \*base, [asrc\\_context\\_t](#) context)  
*read the ASRC context fifo.*
- static uint32\_t [ASRC\\_GetWriteContextFifoAddr](#) (ASRC\_Type \*base, [asrc\\_context\\_t](#) context)  
*Get ASRC write fifo address.*
- static uint32\_t [ASRC\\_GetReadContextFifoAddr](#) (ASRC\_Type \*base, [asrc\\_context\\_t](#) context)  
*Get the ASRC read context fifo address.*
- uint32\_t [ASRC\\_ReadFIFORemainedSample](#) (ASRC\_Type \*base, [asrc\\_context\\_t](#) context, uint32\_t \*outAddr, uint32\_t outWidth, uint32\_t sampleCount)  
*Get the ASRC read fifo remained samples.*

## Transactional

- [status\\_t ASRC\\_TransferBlocking](#) (ASRC\_Type \*base, [asrc\\_context\\_t](#) context, [asrc\\_transfer\\_t](#) \*xfer)  
*ASRC blocking convert audio sample rate.*

### 9.2.2 Data Structure Documentation

#### 9.2.2.1 struct \_asrc\_data\_format

##### Data Fields

- uint8\_t [dataPosition](#)  
*context input data sample position*
- [asrc\\_data\\_endianness\\_t](#) [dataEndianness](#)  
*context input data endianness*
- [asrc\\_data\\_width\\_t](#) [dataWidth](#)  
*context input data width*
- [asrc\\_data\\_type\\_t](#) [dataType](#)  
*context input data type*
- [asrc\\_data\\_sign\\_t](#) [dataSign](#)  
*context input data signed or unsigned*

#### 9.2.2.2 struct \_asrc\_access\_ctrl

The interleave patter is controlled using 3 register fields: GROUP\_LENGTH, ACCESS\_LENGTH, ITERATIONIS. This is intended to support hardware configurations which distribute a single context across samples from multiple audio sources. Take a example as below: accessGroupLen = 6, the sample group

length is 6 samples accessIterations = 2, the 2 sequential ACCESS\_LENGTH read from single source accessLen = 2, the 2 samples fetch from one source.

## Data Fields

- `uint8_t accessIterations`  
*number of sequential fetches per source*
- `uint8_t accessGroupLen`  
*number of channels in a context*
- `uint8_t accessLen`  
*number of channels per source1*

### 9.2.2.3 struct \_asrc\_context\_input\_config

## Data Fields

- `uint32_t sampleRate`  
*input audio data sample rate*
- `uint8_t watermark`  
*input water mark per samples*
- `asrc_access_ctrl_t accessCtrl`  
*input access control*
- `asrc_data_format_t dataFormat`  
*input data format*

### 9.2.2.4 struct \_asrc\_context\_output\_config

## Data Fields

- `uint32_t sampleRate`  
*output audio data sample rate*
- `uint8_t watermark`  
*output water mark per samples*
- `asrc_access_ctrl_t accessCtrl`  
*output access control*
- `asrc_data_format_t dataFormat`  
*output data format*
- `bool enableDither`  
*output path contains a TPDF dither function.*
- `bool enableIEC60958`  
*output IEC60958 bit field insertion enable*

## Field Documentation

### (1) `bool _asrc_context_output_config::enableDither`

The dither function support all fixed output modes(16, 20, 24, 32bits) dither is not supported in 32bit floating point output mode

### 9.2.2.5 struct \_asrc\_context\_prefilter\_config

#### Data Fields

- `asrc_sampleBuffer_init_mode_t initMode`  
*prefilter initial mode*
- `asrc_sampleBuffer_stop_mode_t stopMode`  
*prefilter stop mode*
- `asrc_prefilter_stage1_result_t stage1Result`  
*stage1 data store format*
- `uint32_t filterSt1Taps`  
*prefilter stage1 taps*
- `uint32_t filterSt2Taps`  
*prefilter stage2 taps*
- `uint32_t filterSt1Exp`  
*prefilter stage1 expansion factor*
- `const uint32_t * filterCoeffAddress`  
*prefilter coeff address*

### 9.2.2.6 struct \_asrc\_context\_resampler\_config

#### Data Fields

- `asrc_sampleBuffer_init_mode_t initMode`  
*initial mode*
- `asrc_sampleBuffer_stop_mode_t stopMode`  
*resampler stop mode*
- `asrc_resampler_taps_t tap`  
*resampleer taps*
- `uint32_t filterPhases`  
*interpolation phases*
- `uint64_t filterCenterTap`  
*interpolation center tap*
- `const uint32_t * filterCoeffAddress`  
*interpolation coeff address*

### 9.2.2.7 struct \_asrc\_context\_config

#### Data Fields

- `uint8_t contextChannelNums`  
*context channel numbers*
- `asrc_context_input_config_t contextInput`  
*context input configuration*
- `asrc_context_output_config_t contextOutput`  
*context output configuration*
- `asrc_context_prefilter_config_t contextPrefilter`  
*context pre filter configuration*
- `asrc_context_resampler_config_t contextResampler`

*context resampler configuration*

### 9.2.2.8 struct \_asrc\_transfer

#### Data Fields

- `uint32_t * inDataAddr`  
*address of audio data to be converted*
- `uint32_t inDataSize`  
*size of the audio data*
- `uint32_t * outDataAddr`  
*address of audio data that is been converted*
- `uint32_t outDataSize`  
*size of the audio data*

### 9.2.3 Typedef Documentation

#### 9.2.3.1 `typedef struct _asrc_access_ctrl asrc_access_ctrl_t`

The interleave pattern is controlled using 3 register fields: GROUP\_LENGTH, ACCESS\_LENGTH, ITERATIONIS. This is intended to support hardware configurations which distribute a single context across samples from multiple audio sources. Take an example as below: accessGroupLen = 6, the sample group length is 6 samples accessIterations = 2, the 2 sequential ACCESS\_LENGTH read from single source accessLen = 2, the 2 samples fetch from one source.

### 9.2.4 Enumeration Type Documentation

#### 9.2.4.1 `anonymous enum`

Enumerator

`kStatus_ASRCIdle` ASRC is idle.

`kStatus_ASRCBusy` ASRC is busy.

`kStatus_ASRCInvalidArgument` ASRC invalid argument.

`kStatus_ASRCConfigureFailed` ASRC configure failed.

`kStatus_ASRCConvertError` ASRC convert error failed.

`kStatus_ASRCNotSupport` ASRC not support.

`kStatus_ASRCQueueFull` ASRC queue full.

`kStatus_ASRCQueueIdle` ASRC queue idle.

`kStatus_ASRCLoadFirmwareFailed` ASRC load firmware failed.

`kStatus_ASRCResamplerConfigureFailed` ASRC resampler configured failed.

`kStatus_ASRCPrefilterConfigureFailed` ASRC prefilter configured failed.

#### 9.2.4.2 enum \_asrc\_context

Enumerator

*kASRC\_Context0* Context 0 value.  
*kASRC\_Context1* Context 1 value.  
*kASRC\_Context2* Context 2 value.  
*kASRC\_Context3* Context 3 value.

#### 9.2.4.3 anonymous enum

Enumerator

*kASRC\_Context0InputFifoOverflow* context 0 input fifo overflow  
*kASRC\_Context1InputFifoOverflow* context 1 input fifo overflow  
*kASRC\_Context2InputFifoOverflow* context 2 input fifo overflow  
*kASRC\_Context3InputFifoOverflow* context 3 input fifo overflow  
*kASRC\_Context0OutFifoReadEmpty* context 0 out fifo read empty  
*kASRC\_Context1OutFifoReadEmpty* context 1 out fifo read empty  
*kASRC\_Context2OutFifoReadEmpty* context 2 out fifo read empty  
*kASRC\_Context3OutFifoReadEmpty* context 3 out fifo read empty  
*kASRC\_Context0RunStopDone* context 0 run stop done interrupt  
*kASRC\_Context1RunStopDone* context 1 run stop done interrupt  
*kASRC\_Context2RunStopDone* context 2 run stop done interrupt  
*kASRC\_Context3RunStopDone* context 3 run stop done interrupt  
*kASRC\_ContextAllInterruptStatus* all the context interrupt status

#### 9.2.4.4 anonymous enum

Enumerator

*kASRC\_FifoStatusInputFifoWatermarkFlag* input water mark flag raised  
*kASRC\_FifoStatusOutputFifoWatermarkFlag* output water mark flag raised

#### 9.2.4.5 enum \_asrc\_data\_endianness

Enumerator

*kASRC\_DataEndianLittle* context data little endian  
*kASRC\_DataEndianBig* context data big endian

#### 9.2.4.6 enum \_asrc\_data\_width

Enumerator

*kASRC\_DataWidth32Bit* data width 32bit

*kASRC\_DataWidth24Bit* data width 24bit  
*kASRC\_DataWidth20Bit* data width 20bit  
*kASRC\_DataWidth16Bit* data width 16bit

#### 9.2.4.7 enum \_asrc\_data\_type

Enumerator

*kASRC\_DataTypeInteger* data type int  
*kASRC\_DataTypeFloat* data type float, single precision floating point format

#### 9.2.4.8 enum \_asrc\_data\_sign

Enumerator

*kASRC\_DataSigned* input data is signed  
*kASRC\_DataUnsigned* input data is unsinged

#### 9.2.4.9 enum \_asrc\_sampleBuffer\_init\_mode

Enumerator

*kASRC\_SampleBufferNoPreFillOnInit* do not pre-fill  
*kASRC\_SampleBufferFillFirstSampleOnInit* replicate the first sample to fill the right half of the sample buffer  
*kASRC\_SampleBufferFillZeroOnInit* zero fill the right half og the sample buffer

#### 9.2.4.10 enum \_asrc\_sampleBuffer\_stop\_mode

Enumerator

*kASRC\_SampleBufferFillLastSampleOnStop* replicate the last sample to fill the left half of the sample buffer  
*kASRC\_SampleBufferFillZeroOnStop* zero fill the left half of the sample buffer

#### 9.2.4.11 enum \_asrc\_prefilter\_stage1\_result

Enumerator

*kASRC\_PrefilterStage1ResultInt* prefilter stage1 results are stored in 32 bit int format  
*kASRC\_PrefilterStage1ResultFloat* prefilter stage1 results are stored in 32 bit float format

#### 9.2.4.12 enum \_asrc\_resampler\_taps

Enumerator

*kASRC\_ResamplerTaps\_32* resampler taps 32  
*kASRC\_ResamplerTaps\_64* resampler taps 64  
*kASRC\_ResamplerTaps\_128* resampler taps 128

#### 9.2.4.13 anonymous enum

Enumerator

*kASRC\_SampleRate\_8000* 8K sample rate  
*kASRC\_SampleRate\_11025* 11025 sample rate  
*kASRC\_SampleRate\_12000* 12K sample rate  
*kASRC\_SampleRate\_16000* 16K sample rate  
*kASRC\_SampleRate\_22050* 22.05K sample rate  
*kASRC\_SampleRate\_24000* 24K sample rate  
*kASRC\_SampleRate\_32000* 32K sample rate  
*kASRC\_SampleRate\_44100* 44.1K sample rate  
*kASRC\_SampleRate\_48000* 48K sample rate  
*kASRC\_SampleRate\_64000* 64K sample rate  
*kASRC\_SampleRate\_88200* 88.2K sample rate  
*kASRC\_SampleRate\_96000* 96K sample rate  
*kASRC\_SampleRate\_128000* 128K sample rate  
*kASRC\_SampleRate\_176400* 176K sample rate  
*kASRC\_SampleRate\_192000* 256K sample rate  
*kASRC\_SampleRate\_256000* 256K sample rate  
*kASRC\_SampleRate\_352800* 352.8K sample rate  
*kASRC\_SampleRate\_384000* 384K sample rate  
*kASRC\_SampleRate\_768000* 768K sample rate

### 9.2.5 Function Documentation

#### 9.2.5.1 uint32\_t ASRC\_GetInstance ( ASRC\_Type \* *base* )

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | ASRC base pointer. |
|-------------|--------------------|

### 9.2.5.2 void ASRC\_Init ( ASRC\_Type \* *base* )

This API gates the asrc clock. The asrc module can't operate unless ASRC\_Init is called to enable the clock.

param base asrc base pointer.

### 9.2.5.3 void ASRC\_Deinit ( ASRC\_Type \* *base* )

This API gates the ASRC clock and disable ASRC module. The ASRC module can't operate unless ASRC\_Init

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | ASRC base pointer. |
|-------------|--------------------|

### 9.2.5.4 void ASRC\_GetContextDefaultConfig ( asrc\_context\_config\_t \* *config*, uint32\_t *channels*, uint32\_t *inSampleRate*, uint32\_t *outSampleRate* )

Parameters

|                      |                                     |
|----------------------|-------------------------------------|
| <i>config</i>        | ASRC context configuration pointer. |
| <i>channels</i>      | input audio data channel numbers.   |
| <i>inSampleRate</i>  | input sample rate.                  |
| <i>outSampleRate</i> | output sample rate.                 |

### 9.2.5.5 status\_t ASRC\_SetContextConfig ( ASRC\_Type \* *base*, asrc\_context\_t *context*, asrc\_context\_config\_t \* *config* )

Parameters

|                |                                                  |
|----------------|--------------------------------------------------|
| <i>base</i>    | ASRC base pointer.                               |
| <i>context</i> | index of asrc context, reference asrc_context_t. |
| <i>config</i>  | ASRC context configuration pointer.              |

Return values

|                                |                                                                                                                      |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------|
| <i>kStatus_InvalidArgument</i> | invalid parameters. kStatus_ASRCConfigureFailed context configure failed. kStatus_Success context configure success. |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------|

### 9.2.5.6 status\_t ASRC\_SetContextOutputConfig ( ASRC\_Type \* *base*, asrc\_context\_t *context*, asrc\_context\_output\_config\_t \* *config* )

Parameters

|                |                                                  |
|----------------|--------------------------------------------------|
| <i>base</i>    | ASRC base pointer.                               |
| <i>context</i> | index of asrc context, reference asrc_context_t. |
| <i>config</i>  | ASRC context output configuration pointer.       |

### 9.2.5.7 status\_t ASRC\_SetContextInputConfig ( ASRC\_Type \* *base*, asrc\_context\_t *context*, asrc\_context\_input\_config\_t \* *config* )

Parameters

|                |                                                  |
|----------------|--------------------------------------------------|
| <i>base</i>    | ASRC base pointer.                               |
| <i>context</i> | index of asrc context, reference asrc_context_t. |
| <i>config</i>  | ASRC context input configuration pointer.        |

### 9.2.5.8 static void ASRC\_EnableContextRun ( ASRC\_Type \* *base*, asrc\_context\_t *context*, bool *enable* ) [inline], [static]

All control fields associated with a context must be stable prior to setting context run enable.

Parameters

|                |                                                                                                                                            |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | ASRC base pointer.                                                                                                                         |
| <i>context</i> | ASRC context index.                                                                                                                        |
| <i>enable</i>  | true is enable, inform the datapath begin processing sample data for the context. false is disable, data processing will halt immediately. |

### 9.2.5.9 static void ASRC\_EnableContextRunStop ( ASRC\_Type \* *base*, asrc\_context\_t *context*, bool *enable* ) [inline], [static]

This function used to flush the ASRC pipeline and completely end processing for a context.

Parameters

|                |                                   |
|----------------|-----------------------------------|
| <i>base</i>    | ASRC base pointer.                |
| <i>context</i> | ASRC context index.               |
| <i>enable</i>  | true is enable, false is disable. |

#### 9.2.5.10 static void ASRC\_EnableContextInDMA ( ASRC\_Type \* *base*, asrc\_context\_t *context*, bool *enable* ) [inline], [static]

Parameters

|                |                                   |
|----------------|-----------------------------------|
| <i>base</i>    | ASRC base pointer.                |
| <i>context</i> | ASRC context index.               |
| <i>enable</i>  | true is enable, false is disable. |

#### 9.2.5.11 static void ASRC\_EnableContextOutDMA ( ASRC\_Type \* *base*, asrc\_context\_t *context*, bool *enable* ) [inline], [static]

Parameters

|                |                                   |
|----------------|-----------------------------------|
| <i>base</i>    | ASRC base pointer.                |
| <i>context</i> | ASRC context index.               |
| <i>enable</i>  | true is enable, false is disable. |

#### 9.2.5.12 static void ASRC\_EnablePreFilterBypass ( ASRC\_Type \* *base*, asrc\_context\_t *context*, bool *bypass* ) [inline], [static]

Parameters

|                |                                       |
|----------------|---------------------------------------|
| <i>base</i>    | ASRC peripheral base address.         |
| <i>context</i> | context processor number.             |
| <i>bypass</i>  | true is bypass, false is normal mode. |

#### 9.2.5.13 static void ASRC\_EnableResamplerBypass ( ASRC\_Type \* *base*, asrc\_context\_t *context*, bool *bypass* ) [inline], [static]

Parameters

|                |                                       |
|----------------|---------------------------------------|
| <i>base</i>    | ASRC peripheral base address.         |
| <i>context</i> | context processor number.             |
| <i>bypass</i>  | true is bypass, false is normal mode. |

#### 9.2.5.14 static void ASRC\_SetContextChannelNumber ( ASRC\_Type \* *base*, asrc\_context\_t *context*, uint32\_t *channels* ) [inline], [static]

Note: The maximum channel number in one context can not exceed 32.

Parameters

|                 |                               |
|-----------------|-------------------------------|
| <i>base</i>     | ASRC peripheral base address. |
| <i>context</i>  | context number.               |
| <i>channels</i> | channel number, should <= 32. |

#### 9.2.5.15 uint32\_t ASRC\_GetContextOutSampleSize ( uint32\_t *inSampleRate*, uint32\_t *inSamplesSize*, uint32\_t *inWidth*, uint32\_t *outSampleRate*, uint32\_t *outWidth* )

Parameters

|                      |                                                                                          |
|----------------------|------------------------------------------------------------------------------------------|
| <i>inSampleRate</i>  | output sample rate.                                                                      |
| <i>inSamplesSize</i> | input sample rate.                                                                       |
| <i>inWidth</i>       | input samples buffer size, the size of buffer should be converted to align with 4 byte . |
| <i>outSampleRate</i> | input sample width.                                                                      |
| <i>outWidth</i>      | Output width.                                                                            |

Return values

|               |               |
|---------------|---------------|
| <i>output</i> | samples size. |
|---------------|---------------|

#### 9.2.5.16 static void ASRC\_EnableInterrupt ( ASRC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                                               |
|-------------|---------------------------------------------------------------|
| <i>base</i> | ASRC peripheral base address.                                 |
| <i>mask</i> | The interrupts to enable. Logical OR of _asrc_interrupt_mask. |

#### 9.2.5.17 static void ASRC\_DisableInterrupt ( ASRC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | ASRC peripheral base address.                                  |
| <i>mask</i> | The interrupts to disable. Logical OR of _asrc_interrupt_mask. |

#### 9.2.5.18 static uint32\_t ASRC\_GetInterruptStatus ( ASRC\_Type \* *base* ) [inline], [static]

Parameters

|             |                   |
|-------------|-------------------|
| <i>base</i> | ASRC base pointer |
|-------------|-------------------|

Returns

ASRC Tx status flag value. Use the Status Mask to get the status value needed.

#### 9.2.5.19 static void ASRC\_ClearInterruptStatus ( ASRC\_Type \* *base*, uint32\_t *status* ) [inline], [static]

Parameters

|               |                            |
|---------------|----------------------------|
| <i>base</i>   | ASRC base pointer          |
| <i>status</i> | status flag to be cleared. |

#### 9.2.5.20 static uint32\_t ASRC\_GetFifoStatus ( ASRC\_Type \* *base*, asrc\_context\_t *context* ) [inline], [static]

Parameters

|                |                   |
|----------------|-------------------|
| <i>base</i>    | ASRC base pointer |
| <i>context</i> | context id        |

#### 9.2.5.21 static void ASRC\_WriteContextFifo ( ASRC\_Type \* *base*, asrc\_context\_t *context*, uint32\_t *data* ) [inline], [static]

Parameters

|                |                    |
|----------------|--------------------|
| <i>base</i>    | ASRC base pointer. |
| <i>context</i> | context id.        |
| <i>data</i>    | data to write.     |

#### 9.2.5.22 static uint32\_t ASRC\_ReadContextFifo ( ASRC\_Type \* *base*, asrc\_context\_t *context* ) [inline], [static]

Parameters

|                |                    |
|----------------|--------------------|
| <i>base</i>    | ASRC base pointer. |
| <i>context</i> | context id.        |

Return values

|             |       |
|-------------|-------|
| <i>read</i> | data. |
|-------------|-------|

#### 9.2.5.23 static uint32\_t ASRC\_GetWriteContextFifoAddr ( ASRC\_Type \* *base*, asrc\_context\_t *context* ) [inline], [static]

Parameters

|                |                    |
|----------------|--------------------|
| <i>base</i>    | ASRC base pointer. |
| <i>context</i> | context id.        |

Return values

|              |               |
|--------------|---------------|
| <i>write</i> | fifo address. |
|--------------|---------------|

#### 9.2.5.24 static uint32\_t ASRC\_GetReadContextFifoAddr ( ASRC\_Type \* *base*, asrc\_context\_t *context* ) [inline], [static]

Parameters

|                |                    |
|----------------|--------------------|
| <i>base</i>    | ASRC base pointer. |
| <i>context</i> | context id.        |

Return values

|             |               |
|-------------|---------------|
| <i>read</i> | fifo address. |
|-------------|---------------|

#### 9.2.5.25 uint32\_t ASRC\_ReadFIFORemainedSample ( ASRC\_Type \* *base*, asrc\_context\_t *context*, uint32\_t \* *outAddr*, uint32\_t *outWidth*, uint32\_t *sampleCount* )

Since the DMA request will be triggered only when the sample group in read fifo is bigger than the watermark, so when the data size cannot be divisible by the (watermark + 1), then part of sample will left in read fifo, application should call this api to get the left samples.

Parameters

|                    |                                                  |
|--------------------|--------------------------------------------------|
| <i>base</i>        | ASRC base pointer.                               |
| <i>context</i>     | context id.                                      |
| <i>outAddr</i>     | address to receive remained sample in read fifo. |
| <i>outWidth</i>    | output data width.                               |
| <i>sampleCount</i> | specify the read sample count.                   |

Return values

|               |                                      |
|---------------|--------------------------------------|
| <i>sample</i> | counts actual read from output fifo. |
|---------------|--------------------------------------|

#### 9.2.5.26 status\_t ASRC\_TransferBlocking ( ASRC\_Type \* *base*, asrc\_context\_t *context*, asrc\_transfer\_t \* *xfer* )

This function depends on the configuration of input and output, so it should be called after the ASRC\_SetContextConfig. The data format it supports: 1.16bit 16bit per sample in input buffer, input buffer

size should be calculate as: samples 2U output buffer size can be calculated by call function ASRC\_GetContextOutSampleSize, the parameter outWidth should be 2 2.20bit 24bit per sample in input buffer, input buffer size should be calculate as: samples 3U output buffer size can be calculated by call function ASRC\_GetContextOutSampleSize, the outWidth should be 3. 3.24bit 24bit per sample in input buffer, input buffer size should be calculate as: samples \* 3U output buffer size can be calculated by call function ASRC\_GetContextOutSampleSize, the outWidth should be 3. 4.32bit 32bit per sample in input buffer, input buffer size should be calculate as: samples \* 4U output buffer size can be calculated by call function ASRC\_GetContextOutSampleSize, the outWidth should be 4.

#### Parameters

|                |                      |
|----------------|----------------------|
| <i>base</i>    | ASRC base pointer.   |
| <i>context</i> | context id.          |
| <i>xfer</i>    | .xfer configuration. |

#### Return values

|                         |
|-------------------------|
| <i>kStatus_Success.</i> |
|-------------------------|

## 9.3 ASRC SDMA Driver

### 9.3.1 Overview

#### Data Structures

- struct `_asrc_p2p_sdma_config`  
*destination peripheral configuration [More...](#)*
- struct `_asrc_sdma_in_handle`  
*ASRC sdma in handle. [More...](#)*
- struct `_asrc_sdma_out_handle`  
*ASRC sdma out handle. [More...](#)*
- struct `_asrc_sdma_handle`  
*ASRC DMA transfer handle, users should not touch the content of the handle. [More...](#)*

#### Macros

- `#define ASRC_XFER_IN_QUEUE_SIZE 4U`  
*ASRC xfer queue size.*

#### Typedefs

- `typedef struct _asrc_sdma_handle asrc_sdma_handle_t`  
*ASRC sdma handle prototype.*
- `typedef void(* asrc_sdma_callback_t )(ASRC_Type *base, asrc_sdma_handle_t *handle, status_t status, void *userData)`  
*ASRC SDMA transfer callback function for finish and error.*
- `typedef void(* asrc_start_peripheral_t )(bool start)`  
*ASRC trigger peripheral function pointer.*
- `typedef struct _asrc_p2p_sdma_config asrc_p2p_sdma_config_t`  
*destination peripheral configuration*
- `typedef struct _asrc_sdma_in_handle asrc_sdma_in_handle_t`  
*ASRC sdma in handle.*
- `typedef struct _asrc_sdma_out_handle asrc_sdma_out_handle_t`  
*ASRC sdma out handle.*

#### Driver version

- `#define FSL_ASRC_SDMA_DRIVER_VERSION (MAKE_VERSION(2, 0, 3))`  
*Version 2.0.3.*

## ASRC SDMA Transactional

- void [ASRC\\_TransferInCreateHandleSDMA](#) (ASRC\_Type \*base, [asrc\\_sdma\\_handle\\_t](#) \*handle, [asrc\\_sdma\\_callback\\_t](#) callback, [sdma\\_handle\\_t](#) \*dmaHandle, uint32\_t eventSource, [asrc\\_context\\_t](#) context, const [asrc\\_p2p\\_sdma\\_config\\_t](#) \*periphConfig, void \*userData)
   
*Initializes the ASRC input SDMA handle.*
- void [ASRC\\_TransferOutCreateHandleSDMA](#) (ASRC\_Type \*base, [asrc\\_sdma\\_handle\\_t](#) \*handle, [asrc\\_sdma\\_callback\\_t](#) callback, [sdma\\_handle\\_t](#) \*dmaHandle, uint32\_t eventSource, [asrc\\_context\\_t](#) context, const [asrc\\_p2p\\_sdma\\_config\\_t](#) \*periphConfig, void \*userData)
   
*Initializes the ASRC output SDMA handle.*
- status\_t [ASRC\\_TransferSetContextConfigSDMA](#) (ASRC\_Type \*base, [asrc\\_sdma\\_handle\\_t](#) \*handle, [asrc\\_context\\_config\\_t](#) \*asrcConfig)
   
*Configures the ASRC context.*
- status\_t [ASRC\\_TransferSDMA](#) (ASRC\_Type \*base, [asrc\\_sdma\\_handle\\_t](#) \*handle, [asrc\\_transfer\\_t](#) \*xfer)
   
*Performs a non-blocking ASRC transfer using DMA.*
- void [ASRC\\_TransferAbortInSDMA](#) (ASRC\_Type \*base, [asrc\\_sdma\\_handle\\_t](#) \*handle)
   
*Aborts a ASRC in transfer using SDMA.*
- void [ASRC\\_TransferAbortOutSDMA](#) (ASRC\_Type \*base, [asrc\\_sdma\\_handle\\_t](#) \*handle)
   
*brief Aborts a ASRC out transfer using SDMA.*

### 9.3.2 Data Structure Documentation

#### 9.3.2.1 struct \_asrc\_p2p\_sdma\_config

##### Data Fields

- uint32\_t [eventSource](#)
  
*peripheral event source*
- uint8\_t [watermark](#)
  
*peripheral watermark*
- uint8\_t [channel](#)
  
*peripheral channel number*
- uint8\_t [fifoWidth](#)
  
*peripheral fifo width*
- bool [enableContinuous](#)
  
*true is the amount of samples to be transferred is unknown and script will keep on transferring as long as both events are detected and script must be stopped by application, false is The amount of samples to be transferred is equal to the count field of mode word*
- [asrc\\_start\\_peripheral\\_t](#) [startPeripheral](#)
  
*trigger peripheral start*

#### 9.3.2.2 struct \_asrc\_sdma\_in\_handle

##### Data Fields

- [sdma\\_handle\\_t](#) \* [sdmaHandle](#)

- **DMA handler for ASRC.**
- **uint32\_t eventSource**  
ASRC event source number.
- **asrc\_sdma\_callback\_t callback**  
Callback for users while transfer finish or error occurs.
- **void \*userData**  
User callback parameter.
- **sdma\_buffer\_descriptor\_t bdPool [ASRC\_XFER\_IN\_QUEUE\_SIZE]**  
BD pool for SDMA transfer.
- **uint8\_t asrcInWatermark**  
The transfer data count in a DMA request.
- **uint8\_t bytesPerSample**  
Bytes in a sample.
- **uint32\_t \* asrcQueue [ASRC\_XFER\_IN\_QUEUE\_SIZE]**  
Transfer queue storing queued transfer.
- **size\_t sdmaTransferSize [ASRC\_XFER\_IN\_QUEUE\_SIZE]**  
Data bytes need to transfer.
- **volatile uint8\_t queueUser**  
Index for user to queue transfer.
- **volatile uint8\_t queueDriver**  
Index for driver to get the transfer data and size.
- **const asrc\_p2p\_sdma\_config\_t \* peripheralConfig**  
peripheral configuration
- **uint32\_t state**  
Internal state for ASRC SDMA transfer.

## Field Documentation

- (1) **sdma\_buffer\_descriptor\_t \_asrc\_sdma\_in\_handle::bdPool[ASRC\_XFER\_IN\_QUEUE\_SIZE]**
- (2) **uint32\_t\* \_asrc\_sdma\_in\_handle::asrcQueue[ASRC\_XFER\_IN\_QUEUE\_SIZE]**
- (3) **volatile uint8\_t \_asrc\_sdma\_in\_handle::queueUser**

### 9.3.2.3 struct \_asrc\_sdma\_out\_handle

#### Data Fields

- **sdma\_handle\_t \* sdmaHandle**  
DMA handler for ASRC.
- **void \*userData**  
User callback parameter.
- **uint32\_t state**  
Internal state for ASRC SDMA transfer.
- **uint8\_t bytesPerSample**  
Bytes in a sample.
- **uint32\_t eventSource**  
ASRC event source number.
- **asrc\_sdma\_callback\_t callback**  
Callback for users while transfer finish or error occurs.
- **uint8\_t asrcOutWatermark**

- *The transfer data count in a DMA request.*
- **sdma\_buffer\_descriptor\_t bdPool** [ASRC\_XFER\_OUT\_QUEUE\_SIZE]
  - BD pool for SDMA transfer.*
- **uint32\_t \* asrcQueue** [ASRC\_XFER\_OUT\_QUEUE\_SIZE]
  - Transfer queue storing queued transfer.*
- **size\_t sdmaTransferSize** [ASRC\_XFER\_OUT\_QUEUE\_SIZE]
  - Data bytes need to transfer.*
- **volatile uint8\_t queueUser**
  - Index for user to queue transfer.*
- **volatile uint8\_t queueDriver**
  - Index for driver to get the transfer data and size.*
- **const asrc\_p2p\_sdma\_config\_t \* peripheralConfig**
  - peripheral configuration*
- **uint32\_t nonAlignSize**
  - non align size*
- **void \* nonAlignAddr**
  - non align address*

## Field Documentation

- (1) **sdma\_buffer\_descriptor\_t \_asrc\_sdma\_out\_handle::bdPool[ASRC\_XFER\_OUT\_QUEUE\_SIZE]**
- (2) **uint32\_t\* \_asrc\_sdma\_out\_handle::asrcQueue[ASRC\_XFER\_OUT\_QUEUE\_SIZE]**
- (3) **volatile uint8\_t \_asrc\_sdma\_out\_handle::queueUser**

### 9.3.2.4 struct \_asrc\_sdma\_handle

#### Data Fields

- **asrc\_sdma\_in\_handle\_t inDMAHandle**
  - input dma handle*
- **asrc\_sdma\_out\_handle\_t outDMAHandle**
  - output dma handle*
- **asrc\_context\_t context**
  - ASRC context number.*
- **uint8\_t dataChannels**
  - ASRC process data channel number.*

### 9.3.3 Function Documentation

#### 9.3.3.1 void ASRC\_TransferInCreateHandleSDMA ( ASRC\_Type \* base,                   asrc\_sdma\_handle\_t \* handle, asrc\_sdma\_callback\_t callback, sdma\_handle\_t                   \* dmaHandle, uint32\_t eventSource, asrc\_context\_t context, const                   asrc\_p2p\_sdma\_config\_t \* periphConfig, void \* userData )

This function initializes the ASRC input DMA handle, which can be used for other ASRC transactional APIs. Usually, for a specified ASRC context, call this API once to get the initialized handle.

Parameters

|                     |                                                                      |
|---------------------|----------------------------------------------------------------------|
| <i>base</i>         | ASRC base pointer.                                                   |
| <i>handle</i>       | ASRC SDMA handle pointer.                                            |
| <i>base</i>         | ASRC peripheral base address.                                        |
| <i>callback</i>     | Pointer to user callback function.                                   |
| <i>dmaHandle</i>    | SDMA handle pointer, this handle shall be static allocated by users. |
| <i>eventSource</i>  | ASRC input sdma event source.                                        |
| <i>context</i>      | ASRC context number.                                                 |
| <i>periphConfig</i> | peripheral configurations, used for case.                            |
| <i>userData</i>     | User parameter passed to the callback function.                      |

**9.3.3.2 void ASRC\_TransferOutCreateHandleSDMA ( ASRC\_Type \* *base*,  
 asrc\_sdma\_handle\_t \* *handle*, asrc\_sdma\_callback\_t *callback*, sdma\_handle\_t  
 \* *dmaHandle*, uint32\_t *eventSource*, asrc\_context\_t *context*, const  
 asrc\_p2p\_sdma\_config\_t \* *periphConfig*, void \* *userData* )**

This function initializes the ASRC out DMA handle, which can be used for other ASRC transactional APIs. Usually, for a specified ASRC context, call this API once to get the initialized handle.

Parameters

|                     |                                                                      |
|---------------------|----------------------------------------------------------------------|
| <i>base</i>         | ASRC base pointer.                                                   |
| <i>handle</i>       | ASRC SDMA handle pointer.                                            |
| <i>callback</i>     | ASRC outcallback.                                                    |
| <i>dmaHandle</i>    | SDMA handle pointer, this handle shall be static allocated by users. |
| <i>eventSource</i>  | ASRC output event source.                                            |
| <i>context</i>      | ASRC context number.                                                 |
| <i>periphConfig</i> | peripheral configurations, used for case.                            |
| <i>userData</i>     | User parameter passed to the callback function.                      |

**9.3.3.3 status\_t ASRC\_TransferSetContextConfigSDMA ( ASRC\_Type \* *base*,  
 asrc\_sdma\_handle\_t \* *handle*, asrc\_context\_config\_t \* *asrcConfig* )**

Parameters

|                   |                              |
|-------------------|------------------------------|
| <i>base</i>       | ASRC base pointer.           |
| <i>handle</i>     | ASRC SDMA handle pointer.    |
| <i>asrcConfig</i> | asrc context configurations. |

#### 9.3.3.4 status\_t ASRC\_TransferSDMA ( ASRC\_Type \* *base*, asrc\_sdma\_handle\_t \* *handle*, asrc\_transfer\_t \* *xfer* )

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | ASRC base pointer.                |
| <i>handle</i> | ASRC SDMA handle pointer.         |
| <i>xfer</i>   | ASRC xfer configurations pointer. |

Return values

|                                |                                      |
|--------------------------------|--------------------------------------|
| <i>kStatus_Success</i>         | Start a ASRC SDMA send successfully. |
| <i>kStatus_InvalidArgument</i> | The input argument is invalid.       |
| <i>kStatus_TxBusy</i>          | ASRC is busy sending data.           |

#### 9.3.3.5 void ASRC\_TransferAbortInSDMA ( ASRC\_Type \* *base*, asrc\_sdma\_handle\_t \* *handle* )

Parameters

|               |                           |
|---------------|---------------------------|
| <i>base</i>   | ASRC base pointer.        |
| <i>handle</i> | ASRC SDMA handle pointer. |

#### 9.3.3.6 void ASRC\_TransferAbortOutSDMA ( ASRC\_Type \* *base*, asrc\_sdma\_handle\_t \* *handle* )

param base ASRC base pointer. param handle ASRC SDMA handle pointer.

# Chapter 10

## ECSPI: Enhanced Configurable Serial Peripheral Interface Driver

### 10.1 Overview

#### Modules

- [ECSPI CMSIS Driver](#)
- [ECSPI Driver](#)
- [ECSPI FreeRTOS Driver](#)
- [ECSPI SDMA Driver](#)

## 10.2 ECSPI Driver

### 10.2.1 Overview

ECSPI driver includes functional APIs and transactional APIs.

Functional APIs are feature/property target low level APIs. Functional APIs can be used for ECSPI initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the SPI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. ECSPI functional operation groups provide the functional API set.

Transactional APIs are transaction target high level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. All transactional APIs use the spi\_handle\_t as the first parameter. Initialize the handle by calling the SPI\_MasterTransferCreateHandle() or SPI\_SlaveTransferCreateHandle() API.

Transactional APIs support asynchronous transfer. This means that the functions SPI\_MasterTransferNonBlocking() and SPI\_SlaveTransferNonBlocking() set up the interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the kStatus\_SPI\_Idle status.

### 10.2.2 Typical use case

#### 10.2.2.1 SPI master transfer using polling method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ecspi

#### 10.2.2.2 SPI master transfer using an interrupt method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ecspi

## Data Structures

- struct [\\_ecspi\\_channel\\_config](#)  
*ECSPI user channel configure structure. [More...](#)*
- struct [\\_ecspi\\_master\\_config](#)  
*ECSPI master configure structure. [More...](#)*
- struct [\\_ecspi\\_slave\\_config](#)  
*ECSPI slave configure structure. [More...](#)*
- struct [\\_ecspi\\_transfer](#)  
*ECSPI transfer structure. [More...](#)*
- struct [\\_ecspi\\_master\\_handle](#)  
*ECSPI master handle structure. [More...](#)*

## Macros

- #define `ECSPI_DUMMYDATA` (0x00U)  
*ECSPI dummy transfer data, the data is sent while txBuff is NULL.*
- #define `SPI_RETRY_TIMES` 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/  
*Retry times for waiting flag.*

## TypeDefs

- typedef enum `_ecspi_clock_polarity` `ecspi_clock_polarity_t`  
*ECSPI clock polarity configuration.*
- typedef enum `_ecspi_clock_phase` `ecspi_clock_phase_t`  
*ECSPI clock phase configuration.*
- typedef enum `_ecspi_data_ready` `ecspi_Data_ready_t`  
*ECSPI SPI\_RDY signal configuration.*
- typedef enum `_ecspi_channel_source` `ecspi_channel_source_t`  
*ECSPI channel select source.*
- typedef enum `_ecspi_master_slave_mode` `ecspi_master_slave_mode_t`  
*ECSPI master or slave mode configuration.*
- typedef enum `_ecspi_data_line_inactive_state_t` `ecspi_data_line_inactive_state_t`  
*ECSPI data line inactive state configuration.*
- typedef enum `_ecspi_clock_inactive_state_t` `ecspi_clock_inactive_state_t`  
*ECSPI clock inactive state configuration.*
- typedef enum `_ecspi_chip_select_active_state_t` `ecspi_chip_select_active_state_t`  
*ECSPI active state configuration.*
- typedef enum `_ecspi_sample_period_clock_source` `ecspi_sample_period_clock_source_t`  
*ECSPI sample period clock configuration.*
- typedef struct `_ecspi_channel_config` `ecspi_channel_config_t`  
*ECSPI user channel configure structure.*
- typedef struct `_ecspi_master_config` `ecspi_master_config_t`  
*ECSPI master configure structure.*
- typedef struct `_ecspi_slave_config` `ecspi_slave_config_t`  
*ECSPI slave configure structure.*
- typedef struct `_ecspi_transfer` `ecspi_transfer_t`  
*ECSPI transfer structure.*
- typedef `ecspi_master_handle_t` `ecspi_slave_handle_t`  
*Slave handle is the same with master handle.*
- typedef void(\* `ecspi_master_callback_t`)`(ECSPI_Type *base, ecspi_master_handle_t *handle, status_t status, void *userData)`  
*ECSPI master callback for finished transmit.*
- typedef void(\* `ecspi_slave_callback_t`)`(ECSPI_Type *base, ecspi_slave_handle_t *handle, status_t`

status, void \*userData)  
*ECSPI slave callback for finished transmit.*

## Enumerations

- enum {
   
**kStatus\_ECSPI\_Busy** = MAKE\_STATUS(kStatusGroup\_ECSPI, 0),
   
**kStatus\_ECSPI\_Idle** = MAKE\_STATUS(kStatusGroup\_ECSPI, 1),
   
**kStatus\_ECSPI\_Error** = MAKE\_STATUS(kStatusGroup\_ECSPI, 2),
   
**kStatus\_ECSPI\_HardwareOverFlow** = MAKE\_STATUS(kStatusGroup\_ECSPI, 3),
   
**kStatus\_ECSPI\_Timeout** = MAKE\_STATUS(kStatusGroup\_ECSPI, 4) }
   
*Return status for the ECSPI driver.*
- enum **\_ecspi\_clock\_polarity** {
   
**kECSPI\_PolarityActiveHigh** = 0x0U,
   
**kECSPI\_PolarityActiveLow** }
   
*ECSPI clock polarity configuration.*
- enum **\_ecspi\_clock\_phase** {
   
**kECSPI\_ClockPhaseFirstEdge**,
   
**kECSPI\_ClockPhaseSecondEdge** }
   
*ECSPI clock phase configuration.*
- enum {
   
**kECSPI\_Tx fifoEmptyInterruptEnable** = ECSPI\_INTREG\_TEEN\_MASK,
   
**kECSPI\_TxFifoDataRequestInterruptEnable** = ECSPI\_INTREG\_TDREN\_MASK,
   
**kECSPI\_TxFifoFullInterruptEnable** = ECSPI\_INTREG\_TFEN\_MASK,
   
**kECSPI\_RxFifoReadyInterruptEnable** = ECSPI\_INTREG\_RREN\_MASK,
   
**kECSPI\_RxFifoDataRequestInterruptEnable** = ECSPI\_INTREG\_RDREN\_MASK,
   
**kECSPI\_RxFifoFullInterruptEnable** = ECSPI\_INTREG\_RFEN\_MASK,
   
**kECSPI\_RxFifoOverflowInterruptEnable** = ECSPI\_INTREG\_ROEN\_MASK,
   
**kECSPI\_TransferCompleteInterruptEnable** = ECSPI\_INTREG\_TCEN\_MASK,
   
**kECSPI\_AllInterruptEnable** }
   
*ECSPI interrupt sources.*
- enum {
   
**kECSPI\_Tx fifoEmptyFlag** = ECSPI\_STATREG\_TE\_MASK,
   
**kECSPI\_TxFifoDataRequestFlag** = ECSPI\_STATREG\_TDR\_MASK,
   
**kECSPI\_TxFifoFullFlag** = ECSPI\_STATREG\_TF\_MASK,
   
**kECSPI\_RxFifoReadyFlag** = ECSPI\_STATREG\_RR\_MASK,
   
**kECSPI\_RxFifoDataRequestFlag** = ECSPI\_STATREG\_RDR\_MASK,
   
**kECSPI\_RxFifoFullFlag** = ECSPI\_STATREG\_RF\_MASK,
   
**kECSPI\_RxFifoOverflowFlag** = ECSPI\_STATREG\_RO\_MASK,
   
**kECSPI\_TransferCompleteFlag** = ECSPI\_STATREG\_TC\_MASK }
   
*ECSPI status flags.*
- enum {
   
**kECSPI\_TxDmaEnable** = ECSPI\_DMAREG\_TEDEN\_MASK,
   
**kECSPI\_RxDmaEnable** = ECSPI\_DMAREG\_RXDEN\_MASK,
   
**kECSPI\_DmaAllEnable** = (ECSPI\_DMAREG\_TEDEN\_MASK | ECSPI\_DMAREG\_RXDEN\_M-

- ASK) }
- ECSPI DMA enable.*
- enum \_ecspi\_data\_ready {
 kECSPI\_DataReadyIgnore = 0x0U,
 kECSPI\_DataReadyFallingEdge,
 kECSPI\_DataReadyLowLevel }
- ECSPI SPI\_RDY signal configuration.*
- enum \_ecspi\_channel\_source {
 kECSPI\_Channel0 = 0x0U,
 kECSPI\_Channel1,
 kECSPI\_Channel2,
 kECSPI\_Channel3 }
- ECSPI channel select source.*
- enum \_ecspi\_master\_slave\_mode {
 kECSPI\_Slave = 0U,
 kECSPI\_Master }
- ECSPI master or slave mode configuration.*
- enum \_ecspi\_data\_line\_inactive\_state\_t {
 kECSPI\_DataLineInactiveStateHigh = 0x0U,
 kECSPI\_DataLineInactiveStateLow }
- ECSPI data line inactive state configuration.*
- enum \_ecspi\_clock\_inactive\_state\_t {
 kECSPI\_ClockInactiveStateLow = 0x0U,
 kECSPI\_ClockInactiveStateHigh }
- ECSPI clock inactive state configuration.*
- enum \_ecspi\_chip\_select\_active\_state\_t {
 kECSPI\_ChipSelectActiveStateLow = 0x0U,
 kECSPI\_ChipSelectActiveStateHigh }
- ECSPI active state configuration.*
- enum \_ecspi\_sample\_period\_clock\_source {
 kECSPI\_spiClock = 0x0U,
 kECSPI\_lowFreqClock }
- ECSPI sample period clock configuration.*

## Functions

- uint32\_t **ECSPI\_GetInstance** (ECSPI\_Type \*base)
 

*Get the instance for ECSPI module.*

## Driver version

- #define **FSL\_ECSPI\_DRIVER\_VERSION** (MAKE\_VERSION(2, 3, 2))
 

*ECSPI driver version.*

## Initialization and deinitialization

- void [ECSPI\\_MasterGetDefaultConfig](#) (`ecspi_master_config_t` \*config)  
*Sets the ECSPI configuration structure to default values.*
- void [ECSPI\\_MasterInit](#) (`ECSPI_Type` \*base, const `ecspi_master_config_t` \*config, `uint32_t` src-Clock\_Hz)  
*Initializes the ECSPI with configuration.*
- void [ECSPI\\_SlaveGetDefaultConfig](#) (`ecspi_slave_config_t` \*config)  
*Sets the ECSPI configuration structure to default values.*
- void [ECSPI\\_SlaveInit](#) (`ECSPI_Type` \*base, const `ecspi_slave_config_t` \*config)  
*Initializes the ECSPI with configuration.*
- void [ECSPI\\_Deinit](#) (`ECSPI_Type` \*base)  
*De-initializes the ECSPI.*
- static void [ECSPI\\_Enable](#) (`ECSPI_Type` \*base, bool enable)  
*Enables or disables the ECSPI.*

## Status

- static `uint32_t` [ECSPI\\_GetStatusFlags](#) (`ECSPI_Type` \*base)  
*Gets the status flag.*
- static void [ECSPI\\_ClearStatusFlags](#) (`ECSPI_Type` \*base, `uint32_t` mask)  
*Clear the status flag.*

## Interrupts

- static void [ECSPI\\_EnableInterrupts](#) (`ECSPI_Type` \*base, `uint32_t` mask)  
*Enables the interrupt for the ECSPI.*
- static void [ECSPI\\_DisableInterrupts](#) (`ECSPI_Type` \*base, `uint32_t` mask)  
*Disables the interrupt for the ECSPI.*

## Software Reset

- static void [ECSPI\\_SoftwareReset](#) (`ECSPI_Type` \*base)  
*Software reset.*

## Channel mode check

- static bool [ECSPI\\_IsMaster](#) (`ECSPI_Type` \*base, `ecspi_channel_source_t` channel)  
*Mode check.*

## DMA Control

- static void [ECSPI\\_EnableDMA](#) (`ECSPI_Type` \*base, `uint32_t` mask, bool enable)  
*Enables the DMA source for ECSPI.*

## FIFO Operation

- static uint8\_t **ECSPI\_GetTxFifoCount** (ECSPI\_Type \*base)  
*Get the Tx FIFO data count.*
- static uint8\_t **ECSPI\_GetRxFifoCount** (ECSPI\_Type \*base)  
*Get the Rx FIFO data count.*

## Bus Operations

- static void **ECSPI\_SetChannelSelect** (ECSPI\_Type \*base, **ecspi\_channel\_source\_t** channel)  
*Set channel select for transfer.*
- void **ECSPI\_SetChannelConfig** (ECSPI\_Type \*base, **ecspi\_channel\_source\_t** channel, const **ecspi\_channel\_config\_t** \*config)  
*Set channel select configuration for transfer.*
- void **ECSPI\_SetBaudRate** (ECSPI\_Type \*base, uint32\_t baudRate\_Bps, uint32\_t srcClock\_Hz)  
*Sets the baud rate for ECSPI transfer.*
- **status\_t ECSPI\_WriteBlocking** (ECSPI\_Type \*base, uint32\_t \*buffer, size\_t size)  
*Sends a buffer of data bytes using a blocking method.*
- static void **ECSPI\_WriteData** (ECSPI\_Type \*base, uint32\_t data)  
*Writes a data into the ECSPI data register.*
- static uint32\_t **ECSPI\_ReadData** (ECSPI\_Type \*base)  
*Gets a data from the ECSPI data register.*

## Transactional

- void **ECSPI\_MasterTransferCreateHandle** (ECSPI\_Type \*base, **ecspi\_master\_handle\_t** \*handle, **ecspi\_master\_callback\_t** callback, void \*userData)  
*Initializes the ECSPI master handle.*
- **status\_t ECSPI\_MasterTransferBlocking** (ECSPI\_Type \*base, **ecspi\_transfer\_t** \*xfer)  
*Transfers a block of data using a polling method.*
- **status\_t ECSPI\_MasterTransferNonBlocking** (ECSPI\_Type \*base, **ecspi\_master\_handle\_t** \*handle, **ecspi\_transfer\_t** \*xfer)  
*Performs a non-blocking ECSPI interrupt transfer.*
- **status\_t ECSPI\_MasterTransferGetCount** (ECSPI\_Type \*base, **ecspi\_master\_handle\_t** \*handle, size\_t \*count)  
*Gets the bytes of the ECSPI interrupt transferred.*
- void **ECSPI\_MasterTransferAbort** (ECSPI\_Type \*base, **ecspi\_master\_handle\_t** \*handle)  
*Aborts an ECSPI transfer using interrupt.*
- void **ECSPI\_MasterTransferHandleIRQ** (ECSPI\_Type \*base, **ecspi\_master\_handle\_t** \*handle)  
*Interrupts the handler for the ECSPI.*
- void **ECSPI\_SlaveTransferCreateHandle** (ECSPI\_Type \*base, **ecspi\_slave\_handle\_t** \*handle, **ecspi\_slave\_callback\_t** callback, void \*userData)  
*Initializes the ECSPI slave handle.*
- static **status\_t ECSPI\_SlaveTransferNonBlocking** (ECSPI\_Type \*base, **ecspi\_slave\_handle\_t** \*handle, **ecspi\_transfer\_t** \*xfer)  
*Performs a non-blocking ECSPI slave interrupt transfer.*

- static `status_t ECSPI_SlaveTransferGetCount` (`ECSPi_Type *base`, `ecspi_slave_handle_t *handle`, `size_t *count`)  
*Gets the bytes of the ECSPi interrupt transferred.*
- static void `ECSPI_SlaveTransferAbort` (`ECSPi_Type *base`, `ecspi_slave_handle_t *handle`)  
*Aborts an ECSPi slave transfer using interrupt.*
- void `ECSPI_SlaveTransferHandleIRQ` (`ECSPi_Type *base`, `ecspi_slave_handle_t *handle`)  
*Interrupts a handler for the ECSPi slave.*

## 10.2.3 Data Structure Documentation

### 10.2.3.1 struct \_ecspi\_channel\_config

#### Data Fields

- `ecspi_master_slave_mode_t channelMode`  
*Channel mode.*
- `ecspi_clock_inactive_state_t clockInactiveState`  
*Clock line (SCLK) inactive state.*
- `ecspi_data_line_inactive_state_t dataLineInactiveState`  
*Data line (MOSI&MISO) inactive state.*
- `ecspi_chip_select_active_state_t chipSelectActiveState`  
*Chip select(SS) line active state.*
- `ecspi_clock_polarity_t polarity`  
*Clock polarity.*
- `ecspi_clock_phase_t phase`  
*Clock phase.*

### 10.2.3.2 struct \_ecspi\_master\_config

#### Data Fields

- `ecspi_channel_source_t channel`  
*Channel number.*
- `ecspi_channel_config_t channelConfig`  
*Channel configuration.*
- `ecspi_sample_period_clock_source_t samplePeriodClock`  
*Sample period clock source.*
- `uint16_t burstLength`  
*Burst length.*
- `uint8_t chipSelectDelay`  
*SS delay time.*
- `uint16_t samplePeriod`  
*Sample period.*
- `uint8_t txFifoThreshold`  
*TX Threshold.*
- `uint8_t rxFifoThreshold`  
*RX Threshold.*
- `uint32_t baudRate_Bps`

- *ECSPI baud rate for master mode.*
- `bool enableLoopback`  
*Enable the ECSPI loopback test.*

## Field Documentation

### (1) `uint16_t _ecspi_master_config::burstLength`

The length shall be less than 4096 bits

### (2) `bool _ecspi_master_config::enableLoopback`

## 10.2.3.3 `struct _ecspi_slave_config`

### Data Fields

- `uint16_t burstLength`  
*Burst length.*
- `uint8_t txFifoThreshold`  
*TX Threshold.*
- `uint8_t rxFifoThreshold`  
*RX Threshold.*
- `ecspi_channel_config_t channelConfig`  
*Channel configuration.*

## Field Documentation

### (1) `uint16_t _ecspi_slave_config::burstLength`

The length shall be less than 4096 bits

## 10.2.3.4 `struct _ecspi_transfer`

### Data Fields

- `uint32_t * txData`  
*Send buffer.*
- `uint32_t * rxData`  
*Receive buffer.*
- `size_t dataSize`  
*Transfer bytes.*
- `ecspi_channel_source_t channel`  
*ECSPI channel select.*

## 10.2.3.5 `struct _ecspi_master_handle`

### Data Fields

- `ecspi_channel_source_t channel`

- *Channel number.*  
• `uint32_t *volatile txData`  
    *Transfer buffer.*
- `uint32_t *volatile rxData`  
    *Receive buffer.*
- `volatile size_t txRemainingBytes`  
    *Send data remaining in bytes.*
- `volatile size_t rxRemainingBytes`  
    *Receive data remaining in bytes.*
- `volatile uint32_t state`  
    *ECSPI internal state.*
- `size_t transferSize`  
    *Bytes to be transferred.*
- `ecspi_master_callback_t callback`  
    *ECSPI callback.*
- `void *userData`  
    *Callback parameter.*

## 10.2.4 Macro Definition Documentation

10.2.4.1 `#define FSL_ECSPI_DRIVER_VERSION (MAKE_VERSION(2, 3, 2))`

10.2.4.2 `#define ECSPI_DUMMYDATA (0x00U)`

10.2.4.3 `#define SPI_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */`

## 10.2.5 Typedef Documentation

10.2.5.1 `typedef enum _ecspi_clock_polarity ecspi_clock_polarity_t`

10.2.5.2 `typedef enum _ecspi_clock_phase ecspi_clock_phase_t`

10.2.5.3 `typedef enum _ecspi_data_ready ecspi_Data_ready_t`

10.2.5.4 `typedef enum _ecspi_channel_source ecspi_channel_source_t`

10.2.5.5 `typedef enum _ecspi_master_slave_mode ecspi_master_slave_mode_t`

10.2.5.6 `typedef enum _ecspi_data_line_inactive_state_t ecspi_data_line_inactive_state_t`

10.2.5.7 `typedef enum _ecspi_clock_inactive_state_t ecspi_clock_inactive_state_t`

10.2.5.8 `typedef enum _ecspi_chip_select_active_state_t ecspi_chip_select_active_state_t`

10.2.5.9 `typedef enum _ecspi_sample_period_clock_source ecspi_sample_period_clock_source_t`

10.2.5.10 `typedef struct _ecspi_channel_config ecspi_channel_config_t`

10.2.5.11 `typedef struct _ecspi_master_config ecspi_master_config_t`

10.2.5.12 `typedef struct _ecspi_slave_config ecspi_slave_config_t`

## 10.2.6 Enumeration Type Documentation

### 10.2.6.1 anonymous enum

Enumerator

`kStatus_ECSPI_Busy` ECSPI bus is busy.

`kStatus_ECSPI_Idle` ECSPI is idle.

*kStatus\_ECSPI\_Error* ECSPI error.  
*kStatus\_ECSPI\_HardwareOverflow* ECSPI hardware overflow.  
*kStatus\_ECSPI\_Timeout* ECSPI timeout polling status flags.

#### 10.2.6.2 enum \_ecspi\_clock\_polarity

Enumerator

*kECSPI\_PolarityActiveHigh* Active-high ECSPI polarity high (idles low).  
*kECSPI\_PolarityActiveLow* Active-low ECSPI polarity low (idles high).

#### 10.2.6.3 enum \_ecspi\_clock\_phase

Enumerator

*kECSPI\_ClockPhaseFirstEdge* First edge on SPSCK occurs at the middle of the first cycle of a data transfer.  
*kECSPI\_ClockPhaseSecondEdge* First edge on SPSCK occurs at the start of the first cycle of a data transfer.

#### 10.2.6.4 anonymous enum

Enumerator

*kECSPI\_TxfifoEmptyInterruptEnable* Transmit FIFO buffer empty interrupt.  
*kECSPI\_TxFifoDataRequestInterruptEnable* Transmit FIFO data request interrupt.  
*kECSPI\_TxFifoFullInterruptEnable* Transmit FIFO full interrupt.  
*kECSPI\_RxFifoReadyInterruptEnable* Receiver FIFO ready interrupt.  
*kECSPI\_RxFifoDataRequestInterruptEnable* Receiver FIFO data request interrupt.  
*kECSPI\_RxFifoFullInterruptEnable* Receiver FIFO full interrupt.  
*kECSPI\_RxFifoOverflowInterruptEnable* Receiver FIFO buffer overflow interrupt.  
*kECSPI\_TransferCompleteInterruptEnable* Transfer complete interrupt.  
*kECSPI\_AllInterruptEnable* All interrupt.

#### 10.2.6.5 anonymous enum

Enumerator

*kECSPI\_Tx fifoEmptyFlag* Transmit FIFO buffer empty flag.  
*kECSPI\_TxFifoDataRequestFlag* Transmit FIFO data request flag.  
*kECSPI\_TxFifoFullFlag* Transmit FIFO full flag.  
*kECSPI\_RxFifoReadyFlag* Receiver FIFO ready flag.  
*kECSPI\_RxFifoDataRequestFlag* Receiver FIFO data request flag.  
*kECSPI\_RxFifoFullFlag* Receiver FIFO full flag.

*kECSPI\_RxFifoOverFlowFlag* Receiver FIFO buffer overflow flag.

*kECSPI\_TransferCompleteFlag* Transfer complete flag.

### 10.2.6.6 anonymous enum

Enumerator

*kECSPI\_TxDmaEnable* Tx DMA request source.

*kECSPI\_RxDmaEnable* Rx DMA request source.

*kECSPI\_DmaAllEnable* All DMA request source.

### 10.2.6.7 enum \_ecspi\_data\_ready

Enumerator

*kECSPI\_DataReadyIgnore* SPI\_RDY signal is ignored.

*kECSPI\_DataReadyFallingEdge* SPI\_RDY signal will be triggered by the falling edge.

*kECSPI\_DataReadyLowLevel* SPI\_RDY signal will be triggered by a low level.

### 10.2.6.8 enum \_ecspi\_channel\_source

Enumerator

*kECSPI\_Channel0* Channel 0 is selected.

*kECSPI\_Channel1* Channel 1 is selected.

*kECSPI\_Channel2* Channel 2 is selected.

*kECSPI\_Channel3* Channel 3 is selected.

### 10.2.6.9 enum \_ecspi\_master\_slave\_mode

Enumerator

*kECSPI\_Slave* ECSPI peripheral operates in slave mode.

*kECSPI\_Master* ECSPI peripheral operates in master mode.

### 10.2.6.10 enum \_ecspi\_data\_line\_inactive\_state\_t

Enumerator

*kECSPI\_DataLineInactiveStateHigh* The data line inactive state stays high.

*kECSPI\_DataLineInactiveStateLow* The data line inactive state stays low.

### 10.2.6.11 enum \_ecspi\_clock\_inactive\_state\_t

Enumerator

*kECSPI\_ClockInactiveStateLow* The SCLK inactive state stays low.

*kECSPI\_ClockInactiveStateHigh* The SCLK inactive state stays high.

### 10.2.6.12 enum \_ecspi\_chip\_select\_active\_state\_t

Enumerator

*kECSPI\_ChipSelectActiveStateLow* The SS signal line active stays low.

*kECSPI\_ChipSelectActiveStateHigh* The SS signal line active stays high.

### 10.2.6.13 enum \_ecspi\_sample\_period\_clock\_source

Enumerator

*kECSPI\_spiClock* The sample period clock source is SCLK.

*kECSPI\_lowFreqClock* The sample seriod clock source is low\_frequency reference clock(32.768 kHz).

## 10.2.7 Function Documentation

### 10.2.7.1 uint32\_t ECSPI\_GetInstance ( **ECSPI\_Type** \* *base* )

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | ECSPI base address |
|-------------|--------------------|

### 10.2.7.2 void ECSPI\_MasterGetDefaultConfig ( **ecspi\_master\_config\_t** \* *config* )

The purpose of this API is to get the configuration structure initialized for use in [ECSPI\\_MasterInit\(\)](#). User may use the initialized structure unchanged in ECSPI\_MasterInit, or modify some fields of the structure before calling ECSPI\_MasterInit. After calling this API, the master is ready to transfer. Example:

```
ecspi_master_config_t config;
ECSPI_MasterGetDefaultConfig(&config);
```

## Parameters

|               |                             |
|---------------|-----------------------------|
| <i>config</i> | pointer to config structure |
|---------------|-----------------------------|

**10.2.7.3 void ECSPI\_MasterInit ( **ECSPI\_Type** \* *base*, **const ecspi\_master\_config\_t** \* *config*, **uint32\_t** *srcClock\_Hz* )**

The configuration structure can be filled by user from scratch, or be set with default values by [ECSPI-MasterGetDefaultConfig\(\)](#). After calling this API, the slave is ready to transfer. Example

```
ecspi_master_config_t config = {
 .baudRate_Bps = 400000,
 ...
};
ECSPI_MasterInit(ECSP10, &config);
```

## Parameters

|                    |                                           |
|--------------------|-------------------------------------------|
| <i>base</i>        | ECSPI base pointer                        |
| <i>config</i>      | pointer to master configuration structure |
| <i>srcClock_Hz</i> | Source clock frequency.                   |

**10.2.7.4 void ECSPI\_SlaveGetDefaultConfig ( **ecspi\_slave\_config\_t** \* *config* )**

The purpose of this API is to get the configuration structure initialized for use in [ECSPI\\_SlaveInit\(\)](#). User may use the initialized structure unchanged in [ECSPI\\_SlaveInit\(\)](#), or modify some fields of the structure before calling [ECSPI\\_SlaveInit\(\)](#). After calling this API, the master is ready to transfer. Example:

```
ecspi_Slaveconfig_t config;
ECSPI_SlaveGetDefaultConfig(&config);
```

## Parameters

|               |                             |
|---------------|-----------------------------|
| <i>config</i> | pointer to config structure |
|---------------|-----------------------------|

**10.2.7.5 void ECSPI\_SlaveInit ( **ECSPI\_Type** \* *base*, **const ecspi\_slave\_config\_t** \* *config* )**

The configuration structure can be filled by user from scratch, or be set with default values by [ECSPI-SlaveGetDefaultConfig\(\)](#). After calling this API, the slave is ready to transfer. Example

```
ecspi_Slaveconfig_t config = {
 .baudRate_Bps = 400000,
 ...
};
ECSPI_SlaveInit(ECSP11, &config);
```

Parameters

|               |                                           |
|---------------|-------------------------------------------|
| <i>base</i>   | ECSPI base pointer                        |
| <i>config</i> | pointer to master configuration structure |

#### 10.2.7.6 void ECSPI\_Deinit ( **ECSPI\_Type** \* *base* )

Calling this API resets the ECSPI module, gates the ECSPI clock. The ECSPI module can't work unless calling the ECSPI\_MasterInit/ECSPI\_SlaveInit to initialize module.

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | ECSPI base pointer |
|-------------|--------------------|

#### 10.2.7.7 static void ECSPI\_Enable ( **ECSPI\_Type** \* *base*, **bool** *enable* ) [inline], [static]

Parameters

|               |                                                     |
|---------------|-----------------------------------------------------|
| <i>base</i>   | ECSPI base pointer                                  |
| <i>enable</i> | pass true to enable module, false to disable module |

#### 10.2.7.8 static uint32\_t ECSPI\_GetStatusFlags ( **ECSPI\_Type** \* *base* ) [inline], [static]

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | ECSPI base pointer |
|-------------|--------------------|

Returns

ECSPI Status, use status flag to AND \_ecspi\_flags could get the related status.

#### 10.2.7.9 static void ECSPI\_ClearStatusFlags ( **ECSPI\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

|             |                                                                                 |
|-------------|---------------------------------------------------------------------------------|
| <i>base</i> | ECSPI base pointer                                                              |
| <i>mask</i> | ECSPI Status, use status flag to AND _ecspi_flags could get the related status. |

**10.2.7.10 static void ECSPI\_EnableInterrupts ( **ECSPI\_Type** \* *base*, **uint32\_t** *mask* )  
[**inline**], [**static**]**

Parameters

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | ECSPI base pointer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <i>mask</i> | <p>ECSPI interrupt source. The parameter can be any combination of the following values:</p> <ul style="list-style-type: none"> <li>• kECSPI_Tx_fifoEmptyInterruptEnable</li> <li>• kECSPI_Tx_FifoDataReqestInterruptEnable</li> <li>• kECSPI_Tx_FifoFullInterruptEnable</li> <li>• kECSPI_Rx_FifoReadyInterruptEnable</li> <li>• kECSPI_Rx_FifoDataReqestInterruptEnable</li> <li>• kECSPI_Rx_FifoFullInterruptEnable</li> <li>• kECSPI_Rx_FifoOverFlowInterruptEnable</li> <li>• kECSPI_TransferCompleteInterruptEnable</li> <li>• kECSPI_AllInterruptEnable</li> </ul> |

**10.2.7.11 static void ECSPI\_DisableInterrupts ( *ECSPI\_Type* \* *base*, *uint32\_t* *mask* )  
[inline], [static]**

Parameters

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | ECSPI base pointer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| <i>mask</i> | <p>ECSPI interrupt source. The parameter can be any combination of the following values:</p> <ul style="list-style-type: none"> <li>• kECSPI_Tx_fifoEmptyInterruptEnable</li> <li>• kECSPI_Tx_FifoDataRequestInterruptEnable</li> <li>• kECSPI_Tx_FifoFullInterruptEnable</li> <li>• kECSPI_Rx_FifoReadyInterruptEnable</li> <li>• kECSPI_Rx_FifoDataRequestInterruptEnable</li> <li>• kECSPI_Rx_FifoFullInterruptEnable</li> <li>• kECSPI_Rx_FifoOverFlowInterruptEnable</li> <li>• kECSPI_TransferCompleteInterruptEnable</li> <li>• kECSPI_AllInterruptEnable</li> </ul> |

**10.2.7.12 static void ECSPI\_SoftwareReset ( *ECSPI\_Type* \* *base* ) [inline], [static]**

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | ECSPI base pointer |
|-------------|--------------------|

**10.2.7.13 static bool ECSPI\_IsMaster ( *ECSPI\_Type* \* *base*, *ecspi\_channel\_source\_t* *channel* ) [inline], [static]**

Parameters

|                |                      |
|----------------|----------------------|
| <i>base</i>    | ECSPI base pointer   |
| <i>channel</i> | ECSPI channel source |

Returns

mode of channel

**10.2.7.14 static void ECSPI\_EnableDMA ( *ECSPI\_Type* \* *base*, *uint32\_t* *mask*, *bool enable* ) [inline], [static]**

Parameters

|               |                                                                                                                                                                                                     |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | ECSPI base pointer                                                                                                                                                                                  |
| <i>mask</i>   | ECSPI DMA source. The parameter can be any of the following values: <ul style="list-style-type: none"><li>• kECSPI_TxDmaEnable</li><li>• kECSPI_RxDmaEnable</li><li>• kECSPI_DmaAllEnable</li></ul> |
| <i>enable</i> | True means enable DMA, false means disable DMA                                                                                                                                                      |

#### **10.2.7.15 static uint8\_t ECSPI\_GetTxFifoCount ( ECSPI\_Type \* *base* ) [inline], [static]**

Parameters

|             |                     |
|-------------|---------------------|
| <i>base</i> | ECSPI base pointer. |
|-------------|---------------------|

Returns

the number of words in Tx FIFO buffer.

#### **10.2.7.16 static uint8\_t ECSPI\_GetRxFifoCount ( ECSPI\_Type \* *base* ) [inline], [static]**

Parameters

|             |                     |
|-------------|---------------------|
| <i>base</i> | ECSPI base pointer. |
|-------------|---------------------|

Returns

the number of words in Rx FIFO buffer.

#### **10.2.7.17 static void ECSPI\_SetChannelSelect ( ECSPI\_Type \* *base*, ecspi\_channel\_source\_t *channel* ) [inline], [static]**

Parameters

|                |                    |
|----------------|--------------------|
| <i>base</i>    | ECSPI base pointer |
| <i>channel</i> | Channel source.    |

#### 10.2.7.18 void ECSPI\_SetChannelConfig ( **ECSPI\_Type** \* *base*, **ecspi\_channel\_source\_t** *channel*, **const ecspi\_channel\_config\_t** \* *config* )

The purpose of this API is to set the channel will be use to transfer. User may use this API after instance has been initialized or before transfer start. The configuration structure *ecspi\_channel\_config* can be filled by user from scratch. After calling this API, user can select this channel as transfer channel.

Parameters

|                |                                 |
|----------------|---------------------------------|
| <i>base</i>    | ECSPI base pointer              |
| <i>channel</i> | Channel source.                 |
| <i>config</i>  | Configuration struct of channel |

#### 10.2.7.19 void ECSPI\_SetBaudRate ( **ECSPI\_Type** \* *base*, **uint32\_t** *baudRate\_Bps*, **uint32\_t** *srcClock\_Hz* )

This is only used in master.

Parameters

|                     |                                     |
|---------------------|-------------------------------------|
| <i>base</i>         | ECSPI base pointer                  |
| <i>baudRate_Bps</i> | baud rate needed in Hz.             |
| <i>srcClock_Hz</i>  | ECSPI source clock frequency in Hz. |

#### 10.2.7.20 **status\_t** ECSPI\_WriteBlocking ( **ECSPI\_Type** \* *base*, **uint32\_t** \* *buffer*, **size\_t** *size* )

Note

This function blocks via polling until all bytes have been sent.

Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | ECSPI base pointer               |
| <i>buffer</i> | The data bytes to send           |
| <i>size</i>   | The number of data bytes to send |

Return values

|                              |                                         |
|------------------------------|-----------------------------------------|
| <i>kStatus_Success</i>       | Successfully start a transfer.          |
| <i>kStatus_ECSPI_Timeout</i> | The transfer timed out and was aborted. |

#### 10.2.7.21 static void ECSPI\_WriteData ( **ECSPI\_Type** \* *base*, **uint32\_t** *data* ) [inline], [static]

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | ECSPI base pointer      |
| <i>data</i> | Data needs to be write. |

#### 10.2.7.22 static uint32\_t ECSPI\_ReadData ( **ECSPI\_Type** \* *base* ) [inline], [static]

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | ECSPI base pointer |
|-------------|--------------------|

Returns

Data in the register.

#### 10.2.7.23 void ECSPI\_MasterTransferCreateHandle ( **ECSPI\_Type** \* *base*, **ecspi\_master\_handle\_t** \* *handle*, **ecspi\_master\_callback\_t** *callback*, **void** \* *userData* )

This function initializes the ECSPI master handle which can be used for other ECSPI master transactional APIs. Usually, for a specified ECSPI instance, call this API once to get the initialized handle.

Parameters

|                 |                                |
|-----------------|--------------------------------|
| <i>base</i>     | ECSPI peripheral base address. |
| <i>handle</i>   | ECSPI handle pointer.          |
| <i>callback</i> | Callback function.             |
| <i>userData</i> | User data.                     |

#### 10.2.7.24 status\_t ECSPI\_MasterTransferBlocking ( **ECSPI\_Type** \* *base*, **ecspi\_transfer\_t** \* *xfer* )

Parameters

|             |                                        |
|-------------|----------------------------------------|
| <i>base</i> | SPI base pointer                       |
| <i>xfer</i> | pointer to spi_xfer_config_t structure |

Return values

|                                |                                         |
|--------------------------------|-----------------------------------------|
| <i>kStatus_Success</i>         | Successfully start a transfer.          |
| <i>kStatus_InvalidArgument</i> | Input argument is invalid.              |
| <i>kStatus_ECSPI_Timeout</i>   | The transfer timed out and was aborted. |

#### 10.2.7.25 status\_t ECSPI\_MasterTransferNonBlocking ( **ECSPI\_Type** \* *base*, **ecspi\_master\_handle\_t** \* *handle*, **ecspi\_transfer\_t** \* *xfer* )

Note

The API immediately returns after transfer initialization is finished.

If ECSPI transfer data frame size is 16 bits, the transfer size cannot be an odd number.

Parameters

|               |                                                                            |
|---------------|----------------------------------------------------------------------------|
| <i>base</i>   | ECSPI peripheral base address.                                             |
| <i>handle</i> | pointer to ecspi_master_handle_t structure which stores the transfer state |
| <i>xfer</i>   | pointer to ecspi_transfer_t structure                                      |

Return values

|                                |                                                 |
|--------------------------------|-------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully start a transfer.                  |
| <i>kStatus_InvalidArgument</i> | Input argument is invalid.                      |
| <i>kStatus_ECSPI_Busy</i>      | ECSPI is not idle, is running another transfer. |

#### 10.2.7.26 status\_t **ECSPI\_MasterTransferGetCount** ( **ECSPI\_Type** \* *base*, **ecspi\_master\_handle\_t** \* *handle*, **size\_t** \* *count* )

Parameters

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | ECSPI peripheral base address.                                      |
| <i>handle</i> | Pointer to ECSPI transfer handle, this should be a static variable. |
| <i>count</i>  | Transferred bytes of ECSPI master.                                  |

Return values

|                                     |                                                                |
|-------------------------------------|----------------------------------------------------------------|
| <i>kStatus_ECSPI_Success</i>        | Succeed get the transfer count.                                |
| <i>kStatus_NoTransferInProgress</i> | There is not a non-blocking transaction currently in progress. |

#### 10.2.7.27 void **ECSPI\_MasterTransferAbort** ( **ECSPI\_Type** \* *base*, **ecspi\_master\_handle\_t** \* *handle* )

Parameters

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | ECSPI peripheral base address.                                      |
| <i>handle</i> | Pointer to ECSPI transfer handle, this should be a static variable. |

#### 10.2.7.28 void **ECSPI\_MasterTransferHandleIRQ** ( **ECSPI\_Type** \* *base*, **ecspi\_master\_handle\_t** \* *handle* )

Parameters

|               |                                                                                          |
|---------------|------------------------------------------------------------------------------------------|
| <i>base</i>   | ECSPI peripheral base address.                                                           |
| <i>handle</i> | pointer to <code>ecspi_master_handle_t</code> structure which stores the transfer state. |

**10.2.7.29 void ECSPI\_SlaveTransferCreateHandle ( `ECSPI_Type * base,`  
`ecspi_slave_handle_t * handle, ecspi_slave_callback_t callback, void * userData`  
`)`**

This function initializes the ECSPI slave handle which can be used for other ECSPI slave transactional APIs. Usually, for a specified ECSPI instance, call this API once to get the initialized handle.

Parameters

|                 |                                |
|-----------------|--------------------------------|
| <i>base</i>     | ECSPI peripheral base address. |
| <i>handle</i>   | ECSPI handle pointer.          |
| <i>callback</i> | Callback function.             |
| <i>userData</i> | User data.                     |

**10.2.7.30 static status\_t ECSPI\_SlaveTransferNonBlocking ( `ECSPI_Type * base,`  
`ecspi_slave_handle_t * handle, ecspi_transfer_t * xfer ) [inline],`  
`[static]`**

Note

The API returns immediately after the transfer initialization is finished.

Parameters

|               |                                                                                         |
|---------------|-----------------------------------------------------------------------------------------|
| <i>base</i>   | ECSPI peripheral base address.                                                          |
| <i>handle</i> | pointer to <code>ecspi_master_handle_t</code> structure which stores the transfer state |
| <i>xfer</i>   | pointer to <code>ecspi_transfer_t</code> structure                                      |

Return values

|                                |                                                 |
|--------------------------------|-------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully start a transfer.                  |
| <i>kStatus_InvalidArgument</i> | Input argument is invalid.                      |
| <i>kStatus_ECSPI_Busy</i>      | ECSPI is not idle, is running another transfer. |

**10.2.7.31 static status\_t ECSPI\_SlaveTransferGetCount ( `ECSPI_Type * base,`  
`ecspi_slave_handle_t * handle, size_t * count ) [inline], [static]`**

Parameters

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | ECSPI peripheral base address.                                      |
| <i>handle</i> | Pointer to ECSPI transfer handle, this should be a static variable. |
| <i>count</i>  | Transferred bytes of ECSPI slave.                                   |

Return values

|                                      |                                                                |
|--------------------------------------|----------------------------------------------------------------|
| <i>kStatus_ECSPI_Success</i>         | Succeed get the transfer count.                                |
| <i>kStatus_NoTransferIn-Progress</i> | There is not a non-blocking transaction currently in progress. |

#### 10.2.7.32 **static void ECSPI\_SlaveTransferAbort ( ECSPI\_Type \* *base*, ecspi\_slave\_handle\_t \* *handle* ) [inline], [static]**

Parameters

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | ECSPI peripheral base address.                                      |
| <i>handle</i> | Pointer to ECSPI transfer handle, this should be a static variable. |

#### 10.2.7.33 **void ECSPI\_SlaveTransferHandleIRQ ( ECSPI\_Type \* *base*, ecspi\_slave\_handle\_t \* *handle* )**

Parameters

|               |                                                                           |
|---------------|---------------------------------------------------------------------------|
| <i>base</i>   | ECSPI peripheral base address.                                            |
| <i>handle</i> | pointer to ecspi_slave_handle_t structure which stores the transfer state |

## 10.3 ECSPI FreeRTOS Driver

### 10.3.1 Overview

#### Driver version

- #define `FSL_ECSPI_FREERTOS_DRIVER_VERSION` (`MAKE_VERSION(2, 2, 0)`)  
*ECSPI FreeRTOS driver version.*

#### ECSPI RTOS Operation

- `status_t ECSPI_RTOS_Init` (`ecspi_rtos_handle_t *handle`, `ECSPI_Type *base`, const `ecspi_master_config_t *masterConfig`, `uint32_t srcClock_Hz`)  
*Initializes ECSPI.*
- `status_t ECSPI_RTOS_Deinit` (`ecspi_rtos_handle_t *handle`)  
*Deinitializes the ECSPI.*
- `status_t ECSPI_RTOS_Transfer` (`ecspi_rtos_handle_t *handle`, `ecspi_transfer_t *transfer`)  
*Performs ECSPI transfer.*

### 10.3.2 Macro Definition Documentation

#### 10.3.2.1 #define FSL\_ECSPI\_FREERTOS\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 0))

### 10.3.3 Function Documentation

#### 10.3.3.1 `status_t ECSPI_RTOS_Init ( ecspi_rtos_handle_t * handle, ECSPI_Type * base, const ecspi_master_config_t * masterConfig, uint32_t srcClock_Hz )`

This function initializes the ECSPI module and related RTOS context.

Parameters

|                           |                                                                            |
|---------------------------|----------------------------------------------------------------------------|
| <code>handle</code>       | The RTOS ECSPI handle, the pointer to an allocated space for RTOS context. |
| <code>base</code>         | The pointer base address of the ECSPI instance to initialize.              |
| <code>masterConfig</code> | Configuration structure to set-up ECSPI in master mode.                    |
| <code>srcClock_Hz</code>  | Frequency of input clock of the ECSPI module.                              |

Returns

status of the operation.

### 10.3.3.2 status\_t ECSPI\_RTOS\_Deinit ( *ecspi\_rtos\_handle\_t \* handle* )

This function deinitializes the ECSPI module and related RTOS context.

Parameters

|               |                        |
|---------------|------------------------|
| <i>handle</i> | The RTOS ECSPI handle. |
|---------------|------------------------|

### **10.3.3.3 status\_t ECSPI\_RTOS\_Transfer ( *ecspi\_rtos\_handle\_t* \* *handle*, *ecspi\_transfer\_t* \* *transfer* )**

This function performs an ECSPI transfer according to data given in the transfer structure.

Parameters

|                 |                                               |
|-----------------|-----------------------------------------------|
| <i>handle</i>   | The RTOS ECSPI handle.                        |
| <i>transfer</i> | Structure specifying the transfer parameters. |

Returns

status of the operation.

## 10.4 ECSPI SDMA Driver

### 10.4.1 Overview

#### Data Structures

- struct `_ecspi_sdma_handle`

*ECSPI SDMA transfer handle, users should not touch the content of the handle. [More...](#)*

#### Typedefs

- `typedef void(* ecspi_sdma_callback_t )(ECSPI_Type *base, _ecspi_sdma_handle_t *handle, status_t status, void *userData)`  
*ECSPI SDMA callback called at the end of transfer.*

#### Driver version

- `#define FSL_ECSPI_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 2, 0))`  
*ECSPI FreeRTOS driver version.*

#### DMA Transactional

- `void ECSPI_MasterTransferCreateHandleSDMA (ECSPI_Type *base, _ecspi_sdma_handle_t *handle, _ecspi_sdma_callback_t callback, void *userData, _sdma_handle_t *txHandle, _sdma_handle_t *rxHandle, uint32_t eventSourceTx, uint32_t eventSourceRx, uint32_t TxChannel, uint32_t RxChannel)`  
*Initialize the ECSPI master SDMA handle.*
- `void ECSPI_SlaveTransferCreateHandleSDMA (ECSPI_Type *base, _ecspi_sdma_handle_t *handle, _ecspi_sdma_callback_t callback, void *userData, _sdma_handle_t *txHandle, _sdma_handle_t *rxHandle, uint32_t eventSourceTx, uint32_t eventSourceRx, uint32_t TxChannel, uint32_t RxChannel)`  
*Initialize the ECSPI Slave SDMA handle.*
- `status_t ECSPI_MasterTransferSDMA (ECSPI_Type *base, _ecspi_sdma_handle_t *handle, _ecspi_transfer_t *xfer)`  
*Perform a non-blocking ECSPI master transfer using SDMA.*
- `status_t ECSPI_SlaveTransferSDMA (ECSPI_Type *base, _ecspi_sdma_handle_t *handle, _ecspi_transfer_t *xfer)`  
*Perform a non-blocking ECSPI slave transfer using SDMA.*
- `void ECSPI_MasterTransferAbortSDMA (ECSPI_Type *base, _ecspi_sdma_handle_t *handle)`  
*Abort a ECSPI master transfer using SDMA.*
- `void ECSPI_SlaveTransferAbortSDMA (ECSPI_Type *base, _ecspi_sdma_handle_t *handle)`  
*Abort a ECSPI slave transfer using SDMA.*

## 10.4.2 Data Structure Documentation

### 10.4.2.1 struct \_ecspi\_sdma\_handle

#### Data Fields

- bool `txInProgress`  
*Send transfer finished.*
- bool `rxInProgress`  
*Receive transfer finished.*
- `sdma_handle_t * txSdmaHandle`  
*DMA handler for ECSPI send.*
- `sdma_handle_t * rxSdmaHandle`  
*DMA handler for ECSPI receive.*
- `ecspi_sdma_callback_t callback`  
*Callback for ECSPI SDMA transfer.*
- void \* `userData`  
*User Data for ECSPI SDMA callback.*
- uint32\_t `state`  
*Internal state of ECSPI SDMA transfer.*
- uint32\_t `ChannelTx`  
*Channel for send handle.*
- uint32\_t `ChannelRx`  
*Channel for receive handler.*

## 10.4.3 Macro Definition Documentation

### 10.4.3.1 #define FSL\_ECSPI\_FREERTOS\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 0))

## 10.4.4 Typedef Documentation

### 10.4.4.1 `typedef void(* ecspi_sdma_callback_t)(ECSPI_Type *base, ecspi_sdma_handle_t *handle, status_t status, void *userData)`

## 10.4.5 Function Documentation

### 10.4.5.1 `void ECSPI_MasterTransferCreateHandleSDMA ( ECSPI_Type * base, ecspi_sdma_handle_t * handle, ecspi_sdma_callback_t callback, void * userData, sdma_handle_t * txHandle, sdma_handle_t * rxHandle, uint32_t eventSourceTx, uint32_t eventSourceRx, uint32_t TxChannel, uint32_t RxChannel )`

This function initializes the ECSPI master SDMA handle which can be used for other SPI master transactional APIs. Usually, for a specified ECSPI instance, user need only call this API once to get the initialized handle.

## Parameters

|                      |                                                                                  |
|----------------------|----------------------------------------------------------------------------------|
| <i>base</i>          | ECSPI peripheral base address.                                                   |
| <i>handle</i>        | ECSPI handle pointer.                                                            |
| <i>callback</i>      | User callback function called at the end of a transfer.                          |
| <i>userData</i>      | User data for callback.                                                          |
| <i>txHandle</i>      | SDMA handle pointer for ECSPI Tx, the handle shall be static allocated by users. |
| <i>rxHandle</i>      | SDMA handle pointer for ECSPI Rx, the handle shall be static allocated by users. |
| <i>eventSourceTx</i> | event source for ECSPI send, which can be found in SDMA mapping.                 |
| <i>eventSourceRx</i> | event source for ECSPI receive, which can be found in SDMA mapping.              |
| <i>TxChannel</i>     | SDMA channel for ECSPI send.                                                     |
| <i>RxChannel</i>     | SDMA channel for ECSPI receive.                                                  |

```
10.4.5.2 void ECSPI_SlaveTransferCreateHandleSDMA (ECSPI_Type * base,

 ecspi_sdma_handle_t * handle, ecspi_sdma_callback_t callback, void *

 userData, sdma_handle_t * txHandle, sdma_handle_t * rxHandle, uint32_t

 eventSourceTx, uint32_t eventSourceRx, uint32_t TxChannel, uint32_t

 RxChannel)
```

This function initializes the ECSPI Slave SDMA handle which can be used for other SPI Slave transactional APIs. Usually, for a specified ECSPI instance, user need only call this API once to get the initialized handle.

## Parameters

|                      |                                                                                  |
|----------------------|----------------------------------------------------------------------------------|
| <i>base</i>          | ECSPI peripheral base address.                                                   |
| <i>handle</i>        | ECSPI handle pointer.                                                            |
| <i>callback</i>      | User callback function called at the end of a transfer.                          |
| <i>userData</i>      | User data for callback.                                                          |
| <i>txHandle</i>      | SDMA handle pointer for ECSPI Tx, the handle shall be static allocated by users. |
| <i>rxHandle</i>      | SDMA handle pointer for ECSPI Rx, the handle shall be static allocated by users. |
| <i>eventSourceTx</i> | event source for ECSPI send, which can be found in SDMA mapping.                 |

|                      |                                                                     |
|----------------------|---------------------------------------------------------------------|
| <i>eventSourceRx</i> | event source for ECSPI receive, which can be found in SDMA mapping. |
| <i>TxChannel</i>     | SDMA channel for ECSPI send.                                        |
| <i>RxChannel</i>     | SDMA channel for ECSPI receive.                                     |

#### 10.4.5.3 status\_t **ECSPI\_MasterTransferSDMA** ( **ECSPI\_Type \* base, ecspi\_sdma\_handle\_t \* handle, ecspi\_transfer\_t \* xfer** )

Note

This interface returned immediately after transfer initiates.

Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>base</i>   | ECSPI peripheral base address.      |
| <i>handle</i> | ECSPI SDMA handle pointer.          |
| <i>xfer</i>   | Pointer to sdma transfer structure. |

Return values

|                                |                                                 |
|--------------------------------|-------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully start a transfer.                  |
| <i>kStatus_InvalidArgument</i> | Input argument is invalid.                      |
| <i>kStatus_ECSPI_Busy</i>      | ECSPI is not idle, is running another transfer. |

#### 10.4.5.4 status\_t **ECSPI\_SlaveTransferSDMA** ( **ECSPI\_Type \* base, ecspi\_sdma\_handle\_t \* handle, ecspi\_transfer\_t \* xfer** )

Note

This interface returned immediately after transfer initiates.

Parameters

|               |                                |
|---------------|--------------------------------|
| <i>base</i>   | ECSPI peripheral base address. |
| <i>handle</i> | ECSPI SDMA handle pointer.     |

|             |                                     |
|-------------|-------------------------------------|
| <i>xfer</i> | Pointer to sdma transfer structure. |
|-------------|-------------------------------------|

Return values

|                                |                                                 |
|--------------------------------|-------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully start a transfer.                  |
| <i>kStatus_InvalidArgument</i> | Input argument is invalid.                      |
| <i>kStatus_ECSPI_Busy</i>      | ECSPI is not idle, is running another transfer. |

#### 10.4.5.5 void ECSPI\_MasterTransferAbortSDMA ( **ECSPI\_Type** \* *base*, **ecspi\_sdma\_handle\_t** \* *handle* )

Parameters

|               |                                |
|---------------|--------------------------------|
| <i>base</i>   | ECSPI peripheral base address. |
| <i>handle</i> | ECSPI SDMA handle pointer.     |

#### 10.4.5.6 void ECSPI\_SlaveTransferAbortSDMA ( **ECSPI\_Type** \* *base*, **ecspi\_sdma\_handle\_t** \* *handle* )

Parameters

|               |                                |
|---------------|--------------------------------|
| <i>base</i>   | ECSPI peripheral base address. |
| <i>handle</i> | ECSPI SDMA handle pointer.     |

## 10.5 ECSPi CMSIS Driver

This section describes the programming interface of the ecspi Cortex Microcontroller Software Interface Standard (CMSIS) driver. And this driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method please refer to <http://www.-keil.com/pack/doc/cmsis/Driver/html/index.html>.

### 10.5.1 Function groups

#### 10.5.1.1 ECSPi CMSIS GetVersion Operation

This function group will return the ECSPi CMSIS Driver version to user.

#### 10.5.1.2 ECSPi CMSIS GetCapabilities Operation

This function group will return the capabilities of this driver.

#### 10.5.1.3 ECSPi CMSIS Initialize and Uninitialize Operation

This function will initialize and uninitialized the instance in master mode or slave mode. And this API must be called before you configure an instance or after you Deinit an instance. The right steps to start an instance is that you must initialize the instance which been selected firstly, then you can power on the instance. After these all have been done, you can configure the instance by using control operation. If you want to Uninitialize the instance, you must power off the instance first.

#### 10.5.1.4 ECSPi CMSIS Transfer Operation

This function group controls the transfer, master send/receive data, and slave send/receive data.

#### 10.5.1.5 ECSPi CMSIS Status Operation

This function group gets the ecspi transfer status.

#### 10.5.1.6 ECSPi CMSIS Control Operation

This function can select instance as master mode or slave mode, set baudrate for master mode transfer, get current baudrate of master mode transfer, set transfer data bits and set other control command.

## 10.5.2 Typical use case

### 10.5.2.1 Master Operation

```
/* Variables */
uint8_t masterRxData[TRANSFER_SIZE] = {0U};
uint8_t masterTxData[TRANSFER_SIZE] = {0U};

/*ECSPI master init*/
Driver_SPI0.Initialize(ECSPI_MasterSignalEvent_t);
Driver_SPI0.PowerControl(ARM_POWER_FULL);
Driver_SPI0.Control(ARM_SPI_MODE_MASTER, TRANSFER_BAUDRATE);

/* Start master transfer */
Driver_SPI0.Transfer(masterTxData, masterRxData, TRANSFER_SIZE);

/* Master power off */
Driver_SPI0.PowerControl(ARM_POWER_OFF);

/* Master uninitialize */
Driver_SPI0.Uninitialize();
```

### 10.5.2.2 Slave Operation

```
/* Variables */
uint8_t slaveRxData[TRANSFER_SIZE] = {0U};
uint8_t slaveTxData[TRANSFER_SIZE] = {0U};

/*DSPI slave init*/
Driver_SPI2.Initialize(ECSPI_SlaveSignalEvent_t);
Driver_SPI2.PowerControl(ARM_POWER_FULL);
Driver_SPI2.Control(ARM_SPI_MODE_SLAVE, false);

/* Start slave transfer */
Driver_SPI2.Transfer(slaveTxData, slaveRxData, TRANSFER_SIZE);

/* slave power off */
Driver_SPI2.PowerControl(ARM_POWER_OFF);

/* slave uninitialize */
Driver_SPI2.Uninitialize();
```

# Chapter 11

## ENET: Ethernet MAC Driver

### 11.1 Overview

The MCUXpresso SDK provides a peripheral driver for the 10/100 Mbps Ethernet MAC (ENET) module of MCUXpresso SDK devices.

#### ENET: Ethernet MAC Driver {EthernetMACDriver}

### 11.2 Operations of Ethernet MAC Driver

#### 11.2.1 MII interface Operation

The MII interface is the interface connected with MAC and PHY. the Serial management interface - MII management interface should be set before any access to the external PHY chip register. Call [ENET\\_SetSMI\(\)](#) to initialize the MII management interface. Use [ENET\\_StartSMIRead\(\)](#), [ENET\\_StartSMIWrite\(\)](#), and [ENET\\_ReadSMIData\(\)](#) to read/write to PHY registers. This function group sets up the MII and serial management SMI interface, gets data from the SMI interface, and starts the SMI read and write command. Use [ENET\\_SetMII\(\)](#) to configure the MII before successfully getting data from the external PHY.

#### 11.2.2 MAC address filter

This group sets/gets the ENET mac address and the multicast group address filter. [ENET\\_AddMulticastGroup\(\)](#) should be called to add the ENET MAC to the multicast group. The IEEE 1588 feature requires receiving the PTP message.

#### 11.2.3 Other Basic control Operations

This group has the receive active API [ENET\\_ActiveRead\(\)](#) for single and multiple rings. The [ENET\\_AVBConfigure\(\)](#) is provided to configure the AVB features to support the AVB frames transmission. Note that due to the AVB frames transmission scheme being a credit-based TX scheme, it is only supported with the Enhanced buffer descriptors. Because of this, the AVB configuration should only be done with the Enhanced buffer descriptor. When the AVB feature is required, make sure the the "ENET\_ENHANCEDBUFFERDESCRIPTOR\_MODE" is defined before using this feature.

#### 11.2.4 Transactional Operation

For ENET receive, the [ENET\\_GetRxFrameSize\(\)](#) function needs to be called to get the received data size. Then, call the [ENET\\_ReadFrame\(\)](#) function to get the received data. If the received error occurs, call the

`ENET_GetRxErrBeforeReadFrame()` function after `ENET_GetRxFrameSize()` and before `ENET_ReadFrame()` functions to get the detailed error information.

For ENET transmit, call the `ENET_SendFrame()` function to send the data out. The transmit data error information is only accessible for the IEEE 1588 enhanced buffer descriptor mode. When the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` is defined, the `ENET_GetTxErrAfterSendFrame()` can be used to get the detail transmit error information. The transmit error information can only be updated by uDMA after the data is transmitted. The `ENET_GetTxErrAfterSendFrame()` function is recommended to be called on the transmit interrupt handler.

If send/read frame with zero-copy mechanism is needed, there're special APIs like `ENET_GetRxFrame()` and `ENET_StartTxFrame()`. The send frame zero-copy APIs can't be used mixed with `ENET_SendFrame()` for the same ENET peripheral, same as read frame zero-copy APIs.

## 11.2.5 PTP IEEE 1588 Feature Operation

This function group configures the PTP IEEE 1588 feature, starts/stops/gets/sets/adjusts the PTP IEEE 1588 timer, gets the receive/transmit frame timestamp, and PTP IEEE 1588 timer channel feature setting.

The `ENET_Ptp1588Configure()` function needs to be called when the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` is defined and the IEEE 1588 feature is required.

## 11.3 Typical use case

### 11.3.1 ENET Initialization, receive, and transmit operations

For the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` undefined use case, use the legacy type buffer descriptor transmit/receive the frame as follows. Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/enet`. For the `ENET_ENHANCEDBUFFERDESCRIPTOR_MODE` defined use case, add the PTP IEEE 1588 configuration to enable the PTP IEEE 1588 feature. The initialization occurs as follows. Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/enet`

## Data Structures

- struct `_enet_rx_bd_struct`  
*Defines the receive buffer descriptor structure for the little endian system. [More...](#)*
- struct `_enet_tx_bd_struct`  
*Defines the enhanced transmit buffer descriptor structure for the little endian system. [More...](#)*
- struct `_enet_data_error_stats`  
*Defines the ENET data error statistics structure. [More...](#)*
- struct `_enet_rx_frame_error`  
*Defines the Rx frame error structure. [More...](#)*
- struct `_enet_transfer_stats`  
*Defines the ENET transfer statistics structure. [More...](#)*
- struct `enet_frame_info`  
*Defines the frame info structure. [More...](#)*

- struct `_enet_tx_dirty_ring`  
*Defines the ENET transmit dirty addresses ring/queue structure.* [More...](#)
- struct `_enet_buffer_config`  
*Defines the receive buffer descriptor configuration structure.* [More...](#)
- struct `_enet_intcoalesce_config`  
*Defines the interrupt coalescing configure structure.* [More...](#)
- struct `_enet_avb_config`  
*Defines the ENET AVB Configure structure.* [More...](#)
- struct `_enet_config`  
*Defines the basic configuration structure for the ENET device.* [More...](#)
- struct `_enet_tx_bd_ring`  
*Defines the ENET transmit buffer descriptor ring/queue structure.* [More...](#)
- struct `_enet_rx_bd_ring`  
*Defines the ENET receive buffer descriptor ring/queue structure.* [More...](#)
- struct `_enet_handle`  
*Defines the ENET handler structure.* [More...](#)

## Macros

- #define `ENET_BUFFDESCRIPTOR_RX_ERR_MASK`  
*Defines the receive error status flag mask.*

## Typedefs

- typedef enum `_enet_mii_mode` `enet_mii_mode_t`  
*Defines the MII/RMII/RGMII mode for data interface between the MAC and the PHY.*
- typedef enum `_enet_mii_speed` `enet_mii_speed_t`  
*Defines the 10/100/1000 Mbps speed for the MII data interface.*
- typedef enum `_enet_mii_duplex` `enet_mii_duplex_t`  
*Defines the half or full duplex for the MII data interface.*
- typedef enum `_enet_mii_write` `enet_mii_write_t`  
*Define the MII opcode for normal MDIO\_CLAUSES\_22 Frame.*
- typedef enum `_enet_mii_read` `enet_mii_read_t`  
*Defines the read operation for the MII management frame.*
- typedef enum  
`_enet_mii_extend_opcode` `enet_mii_extend_opcode`  
*Define the MII opcode for extended MDIO\_CLAUSES\_45 Frame.*
- typedef enum  
`_enet_special_control_flag` `enet_special_control_flag_t`  
*Defines a special configuration for ENET MAC controller.*
- typedef enum `_enet_interrupt_enable` `enet_interrupt_enable_t`  
*List of interrupts supported by the peripheral.*
- typedef enum `_enet_event` `enet_event_t`  
*Defines the common interrupt event for callback use.*
- typedef enum `_enet_idle_slope` `enet_idle_slope_t`  
*Defines certain idle slope for bandwidth fraction.*
- typedef enum `_enet_tx_accelerator` `enet_tx_accelerator_t`  
*Defines the transmit accelerator configuration.*
- typedef enum `_enet_rx_accelerator` `enet_rx_accelerator_t`  
*Defines the receive accelerator configuration.*
- typedef struct `_enet_rx_bd_struct` `enet_rx_bd_struct_t`

- *Defines the receive buffer descriptor structure for the little endian system.*  
• `typedef struct _enet_tx_bd_struct enet_tx_bd_struct_t`  
*Defines the enhanced transmit buffer descriptor structure for the little endian system.*
- `typedef struct _enet_data_error_stats enet_data_error_stats_t`  
*Defines the ENET data error statistics structure.*
- `typedef struct _enet_rx_frame_error enet_rx_frame_error_t`  
*Defines the Rx frame error structure.*
- `typedef struct _enet_transfer_stats enet_transfer_stats_t`  
*Defines the ENET transfer statistics structure.*
- `typedef struct enet_frame_info enet_frame_info_t`  
*Defines the frame info structure.*
- `typedef struct _enet_tx_dirty_ring enet_tx_dirty_ring_t`  
*Defines the ENET transmit dirty addresses ring/queue structure.*
- `typedef void *(*enet_rx_alloc_callback_t)(ENET_Type *base, void *userData, uint8_t ringId)`  
*Defines the ENET Rx memory buffer alloc function pointer.*
- `typedef void(*enet_rx_free_callback_t)(ENET_Type *base, void *buffer, void *userData, uint8_t ringId)`  
*Defines the ENET Rx memory buffer free function pointer.*
- `typedef struct _enet_buffer_config enet_buffer_config_t`  
*Defines the receive buffer descriptor configuration structure.*
- `typedef struct _enet_intcoalesce_config enet_intcoalesce_config_t`  
*Defines the interrupt coalescing configure structure.*
- `typedef struct _enet_avb_config enet_avb_config_t`  
*Defines the ENET AVB Configure structure.*
- `typedef void(*enet_callback_t)(ENET_Type *base, enet_handle_t *handle, uint32_t ringId, enet_event_t event, enet_frame_info_t *frameInfo, void *userData)`  
*ENET callback function.*
- `typedef struct _enet_config enet_config_t`  
*Defines the basic configuration structure for the ENET device.*
- `typedef struct _enet_tx_bd_ring enet_tx_bd_ring_t`  
*Defines the ENET transmit buffer descriptor ring/queue structure.*
- `typedef struct _enet_rx_bd_ring enet_rx_bd_ring_t`  
*Defines the ENET receive buffer descriptor ring/queue structure.*
- `typedef void(*enet_isr_ring_t)(ENET_Type *base, enet_handle_t *handle, uint32_t ringId)`  
*Define interrupt IRQ handler.*

## Enumerations

- `enum {`
- `kStatus_ENET_InitMemoryFail,`
- `kStatus_ENET_RxFrameError = MAKE_STATUS(kStatusGroup_ENET, 1U),`
- `kStatus_ENET_RxFrameFail = MAKE_STATUS(kStatusGroup_ENET, 2U),`
- `kStatus_ENET_RxFrameEmpty = MAKE_STATUS(kStatusGroup_ENET, 3U),`
- `kStatus_ENET_RxFrameDrop = MAKE_STATUS(kStatusGroup_ENET, 4U),`
- `kStatus_ENET_TxFrameOverLen = MAKE_STATUS(kStatusGroup_ENET, 5U),`
- `kStatus_ENET_TxFrameBusy = MAKE_STATUS(kStatusGroup_ENET, 6U),`
- `kStatus_ENET_TxFrameFail = MAKE_STATUS(kStatusGroup_ENET, 7U) }`

*Defines the status return codes for transaction.*

- enum \_enet\_mii\_mode {
   
kENET\_MiiMode = 0U,
   
kENET\_RmiiMode = 1U,
   
kENET\_RgmiiMode = 2U }
   
*Defines the MII/RMII/RGMII mode for data interface between the MAC and the PHY.*
- enum \_enet\_mii\_speed {
   
kENET\_MiiSpeed10M = 0U,
   
kENET\_MiiSpeed100M = 1U,
   
kENET\_MiiSpeed1000M = 2U }
   
*Defines the 10/100/1000 Mbps speed for the MII data interface.*
- enum \_enet\_mii\_duplex {
   
kENET\_MiiHalfDuplex = 0U,
   
kENET\_MiiFullDuplex }
   
*Defines the half or full duplex for the MII data interface.*
- enum \_enet\_mii\_write {
   
kENET\_MiiWriteNoCompliant = 0U,
   
kENET\_MiiWriteValidFrame }
   
*Define the MII opcode for normal MDIO\_CLAUSES\_22 Frame.*
- enum \_enet\_mii\_read {
   
kENET\_MiiReadValidFrame = 2U,
   
kENET\_MiiReadNoCompliant = 3U }
   
*Defines the read operation for the MII management frame.*
- enum \_enet\_mii\_extend\_opcode {
   
kENET\_MiiAddrWrite\_C45 = 0U,
   
kENET\_MiiWriteFrame\_C45 = 1U,
   
kENET\_MiiReadFrame\_C45 = 3U }
   
*Define the MII opcode for extended MDIO\_CLAUSES\_45 Frame.*
- enum \_enet\_special\_control\_flag {
   
kENET\_ControlFlowControlEnable = 0x0001U,
   
kENET\_ControlRxPayloadCheckEnable = 0x0002U,
   
kENET\_ControlRxPadRemoveEnable = 0x0004U,
   
kENET\_ControlRxBroadCastRejectEnable = 0x0008U,
   
kENET\_ControlMacAddrInsert = 0x0010U,
   
kENET\_ControlStoreAndFwdDisable = 0x0020U,
   
kENET\_ControlSMIPreambleDisable = 0x0040U,
   
kENET\_ControlPromiscuousEnable = 0x0080U,
   
kENET\_ControlMIILoopEnable = 0x0100U,
   
kENET\_ControlVLANTagEnable = 0x0200U,
   
kENET\_ControlSVLANEnable = 0x0400U,
   
kENET\_ControlVLANUseSecondTag = 0x0800U }
   
*Defines a special configuration for ENET MAC controller.*
- enum \_enet\_interrupt\_enable {

```

kENET_BabrInterrupt = ENET_EIR_BABR_MASK,
kENET_BabtInterrupt = ENET_EIR_BABT_MASK,
kENET_GraceStopInterrupt = ENET_EIR_GRA_MASK,
kENET_TxFrameInterrupt = ENET_EIR_TXF_MASK,
kENET_TxBufferInterrupt = ENET_EIR_TXB_MASK,
kENET_RxFrameInterrupt = ENET_EIR_RXF_MASK,
kENET_RxBufferInterrupt = ENET_EIR_RXB_MASK,
kENET_MiiInterrupt = ENET_EIR_MII_MASK,
kENET_EBusERInterrupt = ENET_EIR_EBERR_MASK,
kENET_LateCollisionInterrupt = ENET_EIR_LC_MASK,
kENET_RetryLimitInterrupt = ENET_EIR_RL_MASK,
kENET_UnderrunInterrupt = ENET_EIR_UN_MASK,
kENET_PayloadRxInterrupt = ENET_EIR_PLR_MASK,
kENET_WakeupInterrupt = ENET_EIR_WAKEUP_MASK,
kENET_RxFlush2Interrupt = ENET_EIR_RXFLUSH_2_MASK,
kENET_RxFlush1Interrupt = ENET_EIR_RXFLUSH_1_MASK,
kENET_RxFlush0Interrupt = ENET_EIR_RXFLUSH_0_MASK,
kENET_TxFrame2Interrupt = ENET_EIR_TXF2_MASK,
kENET_TxBuffer2Interrupt = ENET_EIR_TXB2_MASK,
kENET_RxFrame2Interrupt = ENET_EIR_RXF2_MASK,
kENET_RxBuffer2Interrupt = ENET_EIR_RXB2_MASK,
kENET_TxFrame1Interrupt = ENET_EIR_TXF1_MASK,
kENET_TxBuffer1Interrupt = ENET_EIR_TXB1_MASK,
kENET_RxFrame1Interrupt = ENET_EIR_RXF1_MASK,
kENET_RxBuffer1Interrupt = ENET_EIR_RXB1_MASK,
kENET_TsAvailInterrupt = ENET_EIR_TS_AVAIL_MASK,
kENET_TsTimerInterrupt = ENET_EIR_TS_TIMER_MASK }

```

*List of interrupts supported by the peripheral.*

- enum `_enet_event` {
   
kENET\_RxEvent,
   
kENET\_TxEvent,
   
kENET\_ErrEvent,
   
kENET\_WakeUpEvent,
   
kENET\_TimeStampEvent,
   
kENET\_TimeStampAvailEvent }

*Defines the common interrupt event for callback use.*

- enum `_enet_idle_slope` {

```
kENET_IdleSlope1 = 1U,
kENET_IdleSlope2 = 2U,
kENET_IdleSlope4 = 4U,
kENET_IdleSlope8 = 8U,
kENET_IdleSlope16 = 16U,
kENET_IdleSlope32 = 32U,
kENET_IdleSlope64 = 64U,
kENET_IdleSlope128 = 128U,
kENET_IdleSlope256 = 256U,
kENET_IdleSlope384 = 384U,
kENET_IdleSlope512 = 512U,
kENET_IdleSlope640 = 640U,
kENET_IdleSlope768 = 768U,
kENET_IdleSlope896 = 896U,
kENET_IdleSlope1024 = 1024U,
kENET_IdleSlope1152 = 1152U,
kENET_IdleSlope1280 = 1280U,
kENET_IdleSlope1408 = 1408U,
kENET_IdleSlope1536 = 1536U }
```

*Defines certain idle slope for bandwidth fraction.*

- enum `_enet_tx_accelerator` {
   
kENET\_TxAccelIsShift16Enabled = ENET\_TACC\_SHIFT16\_MASK,
   
kENET\_TxAccelIpCheckEnabled = ENET\_TACC\_IPCHK\_MASK,
   
kENET\_TxAccelProtoCheckEnabled = ENET\_TACC\_PROCHK\_MASK }

*Defines the transmit accelerator configuration.*

- enum `_enet_rx_accelerator` {
   
kENET\_RxAccelPadRemoveEnabled = ENET\_RACC\_PADREM\_MASK,
   
kENET\_RxAccelIpCheckEnabled = ENET\_RACC\_IPDIS\_MASK,
   
kENET\_RxAccelProtoCheckEnabled = ENET\_RACC\_PRODIS\_MASK,
   
kENET\_RxAccelMacCheckEnabled = ENET\_RACC\_LINEDIS\_MASK,
   
kENET\_RxAccelIsShift16Enabled = ENET\_RACC\_SHIFT16\_MASK }

*Defines the receive accelerator configuration.*

## Functions

- `uint32_t ENET_GetInstance (ENET_Type *base)`
  
*Get the ENET instance from peripheral base address.*

## Variables

- const `clock_ip_name_t s_enetClock []`
  
*Pointers to enet clocks for each instance.*

## Driver version

- `#define FSL_ENET_DRIVER_VERSION (MAKE_VERSION(2, 7, 1))`
  
*Defines the driver version.*

## Control and status region bit masks of the receive buffer descriptor.

Defines the queue number.

- #define ENET\_BUFFDESCRIPTOR\_RX\_EMPTY\_MASK 0x8000U  
*Empty bit mask.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_SOFTOWNER1\_MASK 0x4000U  
*Software owner one mask.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_WRAP\_MASK 0x2000U  
*Next buffer descriptor is the start address.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_SOFTOWNER2\_MASK 0x1000U  
*Software owner two mask.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_LAST\_MASK 0x0800U  
*Last BD of the frame mask.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_MISS\_MASK 0x0100U  
*Received because of the promiscuous mode.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_BROADCAST\_MASK 0x0080U  
*Broadcast packet mask.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_MULTICAST\_MASK 0x0040U  
*Multicast packet mask.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_LENVLIOLATE\_MASK 0x0020U  
*Length violation mask.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_NOOCTET\_MASK 0x0010U  
*Non-octet aligned frame mask.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_CRC\_MASK 0x0004U  
*CRC error mask.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_OVERRUN\_MASK 0x0002U  
*FIFO overrun mask.*
- #define ENET\_BUFFDESCRIPTOR\_RX\_TRUNC\_MASK 0x0001U  
*Frame is truncated mask.*

## Control and status bit masks of the transmit buffer descriptor.

- #define ENET\_BUFFDESCRIPTOR\_TX\_READY\_MASK 0x8000U  
*Ready bit mask.*
- #define ENET\_BUFFDESCRIPTOR\_TX\_SOFTWENER1\_MASK 0x4000U  
*Software owner one mask.*
- #define ENET\_BUFFDESCRIPTOR\_TX\_WRAP\_MASK 0x2000U  
*Wrap buffer descriptor mask.*
- #define ENET\_BUFFDESCRIPTOR\_TX\_SOFTWENER2\_MASK 0x1000U  
*Software owner two mask.*
- #define ENET\_BUFFDESCRIPTOR\_TX\_LAST\_MASK 0x0800U  
*Last BD of the frame mask.*
- #define ENET\_BUFFDESCRIPTOR\_TX\_TRANMITCRC\_MASK 0x0400U  
*Transmit CRC mask.*

## Defines some Ethernet parameters.

- #define ENET\_FRAME\_MAX\_FRAMELEN 1518U  
*Default maximum Ethernet frame size without VLAN tag.*
- #define ENET\_FRAME\_VLAN\_TAGLEN 4U  
*Ethernet single VLAN tag size.*

- #define ENET\_FRAME\_CRC\_LEN 4U  
*CRC size in a frame.*
- #define ENET\_FRAME\_TX\_LEN\_LIMITATION(x) (((x)->RCR & ENET\_RCR\_MAX\_FL\_MASK) >> ENET\_RCR\_MAX\_FL\_SHIFT) - ENET\_FRAME\_CRC\_LEN)
- #define ENET\_FIFO\_MIN\_RX\_FULL 5U  
*ENET minimum receive FIFO full.*
- #define ENET\_RX\_MIN\_BUFFERSIZE 256U  
*ENET minimum buffer size.*
- #define ENET\_PHY\_MAXADDRESS (ENET\_MMFR\_PA\_MASK >> ENET\_MMFR\_PA\_SHIFT)  
*Maximum PHY address.*
- #define ENET\_TX\_INTERRUPT  
*Enet Tx interrupt flag.*
- #define ENET\_RX\_INTERRUPT  
*Enet Rx interrupt flag.*
- #define ENET\_TS\_INTERRUPT ((uint32\_t)kENET\_TsTimerInterrupt | (uint32\_t)kENET\_TsAvailInterrupt)  
*Enet timestamp interrupt flag.*
- #define ENET\_ERR\_INTERRUPT  
*Enet error interrupt flag.*

## Initialization and De-initialization

- void ENET\_GetDefaultConfig (enet\_config\_t \*config)  
*Gets the ENET default configuration structure.*
- status\_t ENET\_Up (ENET\_Type \*base, enet\_handle\_t \*handle, const enet\_config\_t \*config, const enet\_buffer\_config\_t \*bufferConfig, uint8\_t \*macAddr, uint32\_t srcClock\_Hz)  
*Initializes the ENET module.*
- status\_t ENET\_Init (ENET\_Type \*base, enet\_handle\_t \*handle, const enet\_config\_t \*config, const enet\_buffer\_config\_t \*bufferConfig, uint8\_t \*macAddr, uint32\_t srcClock\_Hz)  
*Initializes the ENET module.*
- void ENET\_Down (ENET\_Type \*base)  
*Stops the ENET module.*
- void ENET\_Deinit (ENET\_Type \*base)  
*Deinitializes the ENET module.*
- static void ENET\_Reset (ENET\_Type \*base)  
*Resets the ENET module.*

## MII interface operation

- void ENET\_SetMII (ENET\_Type \*base, enet\_mii\_speed\_t speed, enet\_mii\_duplex\_t duplex)  
*Sets the ENET MII speed and duplex.*
- void ENET\_SetSMI (ENET\_Type \*base, uint32\_t srcClock\_Hz, bool isPreambleDisabled)  
*Sets the ENET SMI(serial management interface)- MII management interface.*
- static bool ENET\_GetSMI (ENET\_Type \*base)  
*Gets the ENET SMI- MII management interface configuration.*
- static uint32\_t ENET\_ReadSMIData (ENET\_Type \*base)  
*Reads data from the PHY register through an SMI interface.*
- static void ENET\_StartSMIWrite (ENET\_Type \*base, uint8\_t phyAddr, uint8\_t regAddr, enet\_mii\_write\_t operation, uint16\_t data)

- static void [ENET\\_StartSMIRead](#) (ENET\_Type \*base, uint8\_t phyAddr, uint8\_t regAddr, [enet\\_mii\\_read\\_t](#) operation)
 

*Sends the MDIO IEEE802.3 Clause 22 format write command.*
- static void [ENET\\_MDIOWrite](#) (ENET\_Type \*base, uint8\_t phyAddr, uint8\_t regAddr, uint16\_t data)
 

*Sends the MDIO IEEE802.3 Clause 22 format read command.*
- status\_t [ENET\\_MDIOWrite](#) (ENET\_Type \*base, uint8\_t phyAddr, uint8\_t regAddr, uint16\_t data)
 

*MDIO write with IEEE802.3 Clause 22 format.*
- status\_t [ENET\\_MDIOWrite](#) (ENET\_Type \*base, uint8\_t phyAddr, uint8\_t regAddr, uint16\_t \*pData)
 

*MDIO read with IEEE802.3 Clause 22 format.*
- static void [ENET\\_StartExtC45SMIWriteReg](#) (ENET\_Type \*base, uint8\_t portAddr, uint8\_t devAddr, uint16\_t regAddr)
 

*Sends the MDIO IEEE802.3 Clause 45 format write register command.*
- static void [ENET\\_StartExtC45SMIWriteData](#) (ENET\_Type \*base, uint8\_t portAddr, uint8\_t devAddr, uint16\_t data)
 

*Sends the MDIO IEEE802.3 Clause 45 format write data command.*
- static void [ENET\\_StartExtC45SMIReadData](#) (ENET\_Type \*base, uint8\_t portAddr, uint8\_t devAddr)
 

*Sends the MDIO IEEE802.3 Clause 45 format read data command.*
- status\_t [ENET\\_MDIOC45Write](#) (ENET\_Type \*base, uint8\_t portAddr, uint8\_t devAddr, uint16\_t regAddr, uint16\_t data)
 

*MDIO write with IEEE802.3 Clause 45 format.*
- status\_t [ENET\\_MDIOC45Read](#) (ENET\_Type \*base, uint8\_t portAddr, uint8\_t devAddr, uint16\_t regAddr, uint16\_t \*pData)
 

*MDIO read with IEEE802.3 Clause 45 format.*
- static void [ENET\\_SetRGMIIClockDelay](#) (ENET\_Type \*base, bool txEnabled, bool rxEnabled)
 

*Control the usage of the delayed tx/rx RGMII clock.*

## MAC Address Filter

- void [ENET\\_SetMacAddr](#) (ENET\_Type \*base, uint8\_t \*macAddr)
 

*Sets the ENET module Mac address.*
- void [ENET\\_GetMacAddr](#) (ENET\_Type \*base, uint8\_t \*macAddr)
 

*Gets the ENET module Mac address.*
- void [ENET\\_AddMulticastGroup](#) (ENET\_Type \*base, uint8\_t \*address)
 

*Adds the ENET device to a multicast group.*
- void [ENET\\_LeaveMulticastGroup](#) (ENET\_Type \*base, uint8\_t \*address)
 

*Moves the ENET device from a multicast group.*

## Other basic operation

- static void [ENET\\_ActiveRead](#) (ENET\_Type \*base)
 

*Activates frame reception for multiple rings.*
- static void [ENET\\_EnableSleepMode](#) (ENET\_Type \*base, bool enable)
 

*Enables/disables the MAC to enter sleep mode.*
- static void [ENET\\_GetAccelFunction](#) (ENET\_Type \*base, uint32\_t \*txAccelOption, uint32\_t \*rxAccelOption)
 

*Gets ENET transmit and receive accelerator functions from MAC controller.*

## Interrupts.

- static void `ENET_EnableInterrupts` (ENET\_Type \*base, uint32\_t mask)  
*Enables the ENET interrupt.*
- static void `ENET_DisableInterrupts` (ENET\_Type \*base, uint32\_t mask)  
*Disables the ENET interrupt.*
- static uint32\_t `ENET_GetInterruptStatus` (ENET\_Type \*base)  
*Gets the ENET interrupt status flag.*
- static void `ENET_ClearInterruptStatus` (ENET\_Type \*base, uint32\_t mask)  
*Clears the ENET interrupt events status flag.*
- void `ENET_SetRxISRHandler` (ENET\_Type \*base, enet\_isr\_ring\_t ISRHandler)  
*Set the second level Rx IRQ handler.*
- void `ENET_SetTxISRHandler` (ENET\_Type \*base, enet\_isr\_ring\_t ISRHandler)  
*Set the second level Tx IRQ handler.*
- void `ENET_SetErrISRHandler` (ENET\_Type \*base, enet\_isr\_t ISRHandler)  
*Set the second level Err IRQ handler.*

## Transactional operation

- void `ENET_GetRxErrBeforeReadFrame` (enet\_handle\_t \*handle, enet\_data\_error\_stats\_t \*eErrorStatic, uint8\_t ringId)  
*Gets the error statistics of a received frame for ENET specified ring.*
- void `ENET_GetStatistics` (ENET\_Type \*base, enet\_transfer\_stats\_t \*statistics)  
*Gets statistical data in transfer.*
- status\_t `ENET_GetRxFrameSize` (enet\_handle\_t \*handle, uint32\_t \*length, uint8\_t ringId)  
*Gets the size of the read frame for specified ring.*
- status\_t `ENET_ReadFrame` (ENET\_Type \*base, enet\_handle\_t \*handle, uint8\_t \*data, uint32\_t length, uint8\_t ringId, uint32\_t \*ts)  
*Reads a frame from the ENET device.*
- status\_t `ENET_SendFrame` (ENET\_Type \*base, enet\_handle\_t \*handle, const uint8\_t \*data, uint32\_t length, uint8\_t ringId, bool tsFlag, void \*context)  
*Transmits an ENET frame for specified ring.*
- status\_t `ENET_SetTxReclaim` (enet\_handle\_t \*handle, bool isEnabled, uint8\_t ringId)  
*Enable or disable tx descriptors reclaim mechanism.*
- void `ENET_ReclaimTxDescriptor` (ENET\_Type \*base, enet\_handle\_t \*handle, uint8\_t ringId)  
*Reclaim tx descriptors.*
- status\_t `ENET_GetRxFrame` (ENET\_Type \*base, enet\_handle\_t \*handle, enet\_rx\_frame\_struct\_t \*rxFrame, uint8\_t ringId)  
*Receives one frame in specified BD ring with zero copy.*
- status\_t `ENET_StartTxFrame` (ENET\_Type \*base, enet\_handle\_t \*handle, enet\_tx\_frame\_struct\_t \*txFrame, uint8\_t ringId)  
*Sends one frame in specified BD ring with zero copy.*
- void `ENET_TransmitIRQHandler` (ENET\_Type \*base, enet\_handle\_t \*handle, uint32\_t ringId)  
*The transmit IRQ handler.*
- void `ENET_ReceiveIRQHandler` (ENET\_Type \*base, enet\_handle\_t \*handle, uint32\_t ringId)  
*The receive IRQ handler.*
- void `ENET_CommonFrame1IRQHandler` (ENET\_Type \*base)  
*the common IRQ handler for the tx/rx irq handler.*
- void `ENET_CommonFrame2IRQHandler` (ENET\_Type \*base)  
*the common IRQ handler for the tx/rx irq handler.*
- void `ENET_ErrorIRQHandler` (ENET\_Type \*base, enet\_handle\_t \*handle)

- Some special IRQ handler including the error, mii, wakeup irq handler.*
- void **ENET\_Ptp1588IRQHandler** (ENET\_Type \*base)  
*the common IRQ handler for the 1588 irq handler.*
  - void **ENET\_CommonFrame0IRQHandler** (ENET\_Type \*base)  
*the common IRQ handler for the tx/rx/error etc irq handler.*

## 11.4 Data Structure Documentation

### 11.4.1 struct \_enet\_rx\_bd\_struct

#### Data Fields

- uint16\_t **length**  
*Buffer descriptor data length.*
- uint16\_t **control**  
*Buffer descriptor control and status.*
- uint32\_t **buffer**  
*Data buffer pointer.*

#### Field Documentation

- (1) uint16\_t **\_enet\_rx\_bd\_struct::length**
- (2) uint16\_t **\_enet\_rx\_bd\_struct::control**
- (3) uint32\_t **\_enet\_rx\_bd\_struct::buffer**

### 11.4.2 struct \_enet\_tx\_bd\_struct

#### Data Fields

- uint16\_t **length**  
*Buffer descriptor data length.*
- uint16\_t **control**  
*Buffer descriptor control and status.*
- uint32\_t **buffer**  
*Data buffer pointer.*

**Field Documentation**

- (1) `uint16_t _enet_tx_bd_struct::length`
- (2) `uint16_t _enet_tx_bd_struct::control`
- (3) `uint32_t _enet_tx_bd_struct::buffer`

**11.4.3 struct \_enet\_data\_error\_stats****Data Fields**

- `uint32_t statsRxLenGreaterErr`  
*Receive length greater than RCR[MAX\_FL].*
- `uint32_t statsRxAlignErr`  
*Receive non-octet alignment.*
- `uint32_t statsRxFcsErr`  
*Receive CRC error.*
- `uint32_t statsRxOverRunErr`  
*Receive over run.*
- `uint32_t statsRxTruncateErr`  
*Receive truncate.*

**Field Documentation**

- (1) `uint32_t _enet_data_error_stats::statsRxLenGreaterErr`
- (2) `uint32_t _enet_data_error_stats::statsRxFcsErr`
- (3) `uint32_t _enet_data_error_stats::statsRxOverRunErr`
- (4) `uint32_t _enet_data_error_stats::statsRxTruncateErr`

**11.4.4 struct \_enet\_rx\_frame\_error****Data Fields**

- `bool statsRxTruncateErr: 1`  
*Receive truncate.*
- `bool statsRxOverRunErr: 1`  
*Receive over run.*
- `bool statsRxFcsErr: 1`  
*Receive CRC error.*
- `bool statsRxAlignErr: 1`  
*Receive non-octet alignment.*
- `bool statsRxLenGreaterErr: 1`  
*Receive length greater than RCR[MAX\_FL].*

**Field Documentation**

- (1) **bool \_enet\_rx\_frame\_error::statsRxTruncateErr**
- (2) **bool \_enet\_rx\_frame\_error::statsRxOverRunErr**
- (3) **bool \_enet\_rx\_frame\_error::statsRxFcsErr**
- (4) **bool \_enet\_rx\_frame\_error::statsRxAlignErr**
- (5) **bool \_enet\_rx\_frame\_error::statsRxLenGreaterErr**

**11.4.5 struct \_enet\_transfer\_stats****Data Fields**

- **uint32\_t statsRxFrameCount**  
*Rx frame number.*
- **uint32\_t statsRxFrameOk**  
*Good Rx frame number.*
- **uint32\_t statsRxCrcErr**  
*Rx frame number with CRC error.*
- **uint32\_t statsRxAlignErr**  
*Rx frame number with alignment error.*
- **uint32\_t statsRxDropInvalidSFD**  
*Dropped frame number due to invalid SFD.*
- **uint32\_t statsRxFifoOverflowErr**  
*Rx FIFO overflow count.*
- **uint32\_t statsTxFrameCount**  
*Tx frame number.*
- **uint32\_t statsTxFrameOk**  
*Good Tx frame number.*
- **uint32\_t statsTxCrcAlignErr**  
*The transmit frame is error.*
- **uint32\_t statsTxFifoUnderRunErr**  
*Tx FIFO underrun count.*

**Field Documentation**

- (1) `uint32_t _enet_transfer_stats::statsRxFrameCount`
- (2) `uint32_t _enet_transfer_stats::statsRxFrameOk`
- (3) `uint32_t _enet_transfer_stats::statsRxCrcErr`
- (4) `uint32_t _enet_transfer_stats::statsRxAlignErr`
- (5) `uint32_t _enet_transfer_stats::statsRxDropInvalidSFD`
- (6) `uint32_t _enet_transfer_stats::statsRxFifoOverflowErr`
- (7) `uint32_t _enet_transfer_stats::statsTxFrameCount`
- (8) `uint32_t _enet_transfer_stats::statsTxFrameOk`
- (9) `uint32_t _enet_transfer_stats::statsTxCrcAlignErr`
- (10) `uint32_t _enet_transfer_stats::statsTxFifoUnderRunErr`

**11.4.6 struct enet\_frame\_info****Data Fields**

- `void * context`  
*User specified data.*

**11.4.7 struct \_enet\_tx\_dirty\_ring****Data Fields**

- `enet_frame_info_t * txDirtyBase`  
*Dirty buffer descriptor base address pointer.*
- `uint16_t txGenIdx`  
*tx generate index.*
- `uint16_t txConsumIdx`  
*tx consume index.*
- `uint16_t txRingLen`  
*tx ring length.*
- `bool isFull`  
*tx ring is full flag.*

**Field Documentation**

- (1) `enet_frame_info_t* _enet_tx_dirty_ring::txDirtyBase`
- (2) `uint16_t _enet_tx_dirty_ring::txGenIdx`
- (3) `uint16_t _enet_tx_dirty_ring::txConsumIdx`
- (4) `uint16_t _enet_tx_dirty_ring::txRingLen`
- (5) `bool _enet_tx_dirty_ring::isFull`

**11.4.8 struct \_enet\_buffer\_config**

Note that for the internal DMA requirements, the buffers have a corresponding alignment requirements.

1. The aligned receive and transmit buffer size must be evenly divisible by ENET\_BUFF\_ALIGNMENT. when the data buffers are in cacheable region when cache is enabled, all those size should be aligned to the maximum value of "ENET\_BUFF\_ALIGNMENT" and the cache line size.
2. The aligned transmit and receive buffer descriptor start address must be at least 64 bit aligned. However, it's recommended to be evenly divisible by ENET\_BUFF\_ALIGNMENT. buffer descriptors should be put in non-cacheable region when cache is enabled.
3. The aligned transmit and receive data buffer start address must be evenly divisible by ENET\_BUFF\_ALIGNMENT. Receive buffers should be continuous with the total size equal to "rxBdNumber \* rxBuffSizeAlign". Transmit buffers should be continuous with the total size equal to "txBdNumber \* txBuffSizeAlign". when the data buffers are in cacheable region when cache is enabled, all those size should be aligned to the maximum value of "ENET\_BUFF\_ALIGNMENT" and the cache line size.

**Data Fields**

- `uint16_t rxBdNumber`  
*Receive buffer descriptor number.*
- `uint16_t txBdNumber`  
*Transmit buffer descriptor number.*
- `uint16_t rxBuffSizeAlign`  
*Aligned receive data buffer size.*
- `uint16_t txBuffSizeAlign`  
*Aligned transmit data buffer size.*
- `volatile enet_rx_bd_struct_t * rxBdStartAddrAlign`  
*Aligned receive buffer descriptor start address: should be non-cacheable.*
- `volatile enet_tx_bd_struct_t * txBdStartAddrAlign`  
*Aligned transmit buffer descriptor start address: should be non-cacheable.*
- `uint8_t * rxBufferAlign`  
*Receive data buffer start address.*
- `uint8_t * txBufferAlign`  
*Transmit data buffer start address.*
- `bool rxMaintainEnable`

- *Receive buffer cache maintain.*
- `bool txMaintainEnable`  
*Transmit buffer cache maintain.*
- `enet_frame_info_t * txFrameInfo`  
*Transmit frame information start address.*

## Field Documentation

- (1) `uint16_t _enet_buffer_config::rxBdNumber`
- (2) `uint16_t _enet_buffer_config::txBdNumber`
- (3) `uint16_t _enet_buffer_config::rxBuffSizeAlign`
- (4) `uint16_t _enet_buffer_config::txBuffSizeAlign`
- (5) `volatile enet_rx_bd_struct_t* _enet_buffer_config::rxBdStartAddrAlign`
- (6) `volatile enet_tx_bd_struct_t* _enet_buffer_config::txBdStartAddrAlign`
- (7) `uint8_t* _enet_buffer_config::rxBufferAlign`
- (8) `uint8_t* _enet_buffer_config::txBufferAlign`
- (9) `bool _enet_buffer_config::rxMaintainEnable`
- (10) `bool _enet_buffer_config::txMaintainEnable`
- (11) `enet_frame_info_t* _enet_buffer_config::txFrameInfo`

### 11.4.9 struct \_enet\_intcoalesce\_config

## Data Fields

- `uint8_t txCoalesceFrameCount [FSL_FEATURE_ENET_QUEUE]`  
*Transmit interrupt coalescing frame count threshold.*
- `uint16_t txCoalesceTimeCount [FSL_FEATURE_ENET_QUEUE]`  
*Transmit interrupt coalescing timer count threshold.*
- `uint8_t rxCoalesceFrameCount [FSL_FEATURE_ENET_QUEUE]`  
*Receive interrupt coalescing frame count threshold.*
- `uint16_t rxCoalesceTimeCount [FSL_FEATURE_ENET_QUEUE]`  
*Receive interrupt coalescing timer count threshold.*

**Field Documentation**

- (1) `uint8_t _enet_intcoalesce_config::txCoalesceFrameCount[FSL_FEATURE_ENET_QUEUE]`
- (2) `uint16_t _enet_intcoalesce_config::txCoalesceTimeCount[FSL_FEATURE_ENET_QUEUE]`
- (3) `uint8_t _enet_intcoalesce_config::rxCoalesceFrameCount[FSL_FEATURE_ENET_QUEUE]`
- (4) `uint16_t _enet_intcoalesce_config::rxCoalesceTimeCount[FSL_FEATURE_ENET_QUEUE]`

**11.4.10 struct \_enet\_avb\_config**

This is used for to configure the extended ring 1 and ring 2.

1. The classification match format is  $(\text{CMP3} \ll 12) | (\text{CMP2} \ll 8) | (\text{CMP1} \ll 4) | \text{CMP0}$ . composed of four 3-bit compared VLAN priority field cmp0~cmp3, cm0 ~ cmp3 are used in parallel.

If CMP1,2,3 are not unused, please set them to the same value as CMP0.

1. The idleSlope is used to calculate the Band Width fraction,  $\text{BW fraction} = 1 / (1 + 512/\text{idleSlope})$ . For avb configuration, the BW fraction of Class 1 and Class 2 combined must not exceed 0.75.

**Data Fields**

- `uint16_t rxClassifyMatch [FSL_FEATURE_ENET_QUEUE-1]`  
*The classification match value for the ring.*
- `enet_idle_slope_t idleSlope [FSL_FEATURE_ENET_QUEUE-1]`  
*The idle slope for certian bandwidth fraction.*

**Field Documentation**

- (1) `uint16_t _enet_avb_config::rxClassifyMatch[FSL_FEATURE_ENET_QUEUE-1]`
- (2) `enet_idle_slope_t _enet_avb_config::idleSlope[FSL_FEATURE_ENET_QUEUE-1]`

**11.4.11 struct \_enet\_config**

Note:

1. macSpecialConfig is used for a special control configuration, A logical OR of "enet\_special\_control\_flag\_t". For a special configuration for MAC, set this parameter to 0.
2. txWatermark is used for a cut-through operation. It is in steps of 64 bytes: 0/1 - 64 bytes written to TX FIFO before transmission of a frame begins. 2 - 128 bytes written to TX FIFO .... 3 - 192 bytes written to TX FIFO .... The maximum of txWatermark is 0x2F - 4032 bytes written to TX FIFO .... txWatermark allows minimizing the transmit latency to set the txWatermark to 0 or 1 or for larger bus access latency 3 or larger due to contention for the system bus.
3. rxFifoFullThreshold is similar to the txWatermark for cut-through operation in RX. It is in 64-bit

- words. The minimum is ENET\_FIFO\_MIN\_RX\_FULL and the maximum is 0xFF. If the end of the frame is stored in FIFO and the frame size if smaller than the txWatermark, the frame is still transmitted. The rule is the same for rxFifoFullThreshold in the receive direction.
4. When "kENET\_ControlFlowControlEnable" is set in the macSpecialConfig, ensure that the pauseDuration, rxFifoEmptyThreshold, and rxFifoStatEmptyThreshold are set for flow control enabled case.
  5. When "kENET\_ControlStoreAndFwdDisabled" is set in the macSpecialConfig, ensure that the rxFifoFullThreshold and txFifoWatermark are set for store and forward disable.
  6. The rxAccelerConfig and txAccelerConfig default setting with 0 - accelerator are disabled. The "enet\_tx\_accelerator\_t" and "enet\_rx\_accelerator\_t" are recommended to be used to enable the transmit and receive accelerator. After the accelerators are enabled, the store and forward feature should be enabled. As a result, kENET\_ControlStoreAndFwdDisabled should not be set.
  7. The intCoalesceCfg can be used in the rx or tx enabled cases to decrease the CPU loading.

## Data Fields

- **uint32\_t macSpecialConfig**  
*Mac special configuration.*
- **uint32\_t interrupt**  
*Mac interrupt source.*
- **uint16\_t rxMaxFrameLen**  
*Receive maximum frame length.*
- **enet\_mii\_mode\_t miiMode**  
*MII mode.*
- **enet\_mii\_speed\_t miiSpeed**  
*MII Speed.*
- **enet\_mii\_duplex\_t miiDuplex**  
*MII duplex.*
- **uint8\_t rxAccelerConfig**  
*Receive accelerator, A logical OR of "enet\_rx\_accelerator\_t".*
- **uint8\_t txAccelerConfig**  
*Transmit accelerator, A logical OR of "enet\_rx\_accelerator\_t".*
- **uint16\_t pauseDuration**  
*For flow control enabled case: Pause duration.*
- **uint8\_t rxFifoEmptyThreshold**  
*For flow control enabled case: when RX FIFO level reaches this value, it makes MAC generate XOFF pause frame.*
- **uint8\_t rxFifoStatEmptyThreshold**  
*For flow control enabled case: number of frames in the receive FIFO, independent of size, that can be accept.*
- **uint8\_t rxFifoFullThreshold**  
*For store and forward disable case, the data required in RX FIFO to notify the MAC receive ready status.*
- **uint8\_t txFifoWatermark**  
*For store and forward disable case, the data required in TX FIFO before a frame transmit start.*
- **enet\_intcoalesce\_config\_t \* intCoalesceCfg**  
*If the interrupt coalescence is not required in the ring n(0,1,2),*

- **uint8\_t ringNum**  
*please set to NULL.*
- **enet\_rx\_alloc\_callback\_t rxBuffAlloc**  
*Callback function to alloc memory, must be provided for zero-copy Rx.*
- **enet\_rx\_free\_callback\_t rxBuffFree**  
*Callback function to free memory, must be provided for zero-copy Rx.*
- **enet\_callback\_t callback**  
*General callback function.*
- **void \* userData**  
*Callback function parameter.*

## Field Documentation

### (1) **uint32\_t \_enet\_config::macSpecialConfig**

A logical OR of "enet\_special\_control\_flag\_t".

### (2) **uint32\_t \_enet\_config::interrupt**

A logical OR of "enet\_interrupt\_enable\_t".

### (3) **uint16\_t \_enet\_config::rxMaxFrameLen**

### (4) **enet\_mii\_mode\_t \_enet\_config::miiMode**

### (5) **enet\_mii\_speed\_t \_enet\_config::miiSpeed**

### (6) **enet\_mii\_duplex\_t \_enet\_config::miiDuplex**

### (7) **uint8\_t \_enet\_config::rxAccelerConfig**

### (8) **uint8\_t \_enet\_config::txAccelerConfig**

### (9) **uint16\_t \_enet\_config::pauseDuration**

### (10) **uint8\_t \_enet\_config::rxFifoEmptyThreshold**

### (11) **uint8\_t \_enet\_config::rxFifoStatEmptyThreshold**

If the limit is reached, reception continues and a pause frame is triggered.

### (12) **uint8\_t \_enet\_config::rxFifoFullThreshold**

### (13) **uint8\_t \_enet\_config::txFifoWatermark**

### (14) **enet\_intcoalesce\_config\_t\* \_enet\_config::intCoalesceCfg**

### (15) **uint8\_t \_enet\_config::ringNum**

default with 1 – single ring.

- (16) `enet_rx_alloc_callback_t _enet_config::rxBuffAlloc`
- (17) `enet_rx_free_callback_t _enet_config::rxBuffFree`
- (18) `enet_callback_t _enet_config::callback`
- (19) `void* _enet_config::userData`

### 11.4.12 struct \_enet\_tx\_bd\_ring

#### Data Fields

- volatile `enet_tx_bd_struct_t * txBdBase`  
*Buffer descriptor base address pointer.*
- `uint16_t txGenIdx`  
*The current available transmit buffer descriptor pointer.*
- `uint16_t txConsumIdx`  
*Transmit consume index.*
- volatile `uint16_t txDescUsed`  
*Transmit descriptor used number.*
- `uint16_t txRingLen`  
*Transmit ring length.*

#### Field Documentation

- (1) `volatile enet_tx_bd_struct_t* _enet_tx_bd_ring::txBdBase`
- (2) `uint16_t _enet_tx_bd_ring::txGenIdx`
- (3) `uint16_t _enet_tx_bd_ring::txConsumIdx`
- (4) `volatile uint16_t _enet_tx_bd_ring::txDescUsed`
- (5) `uint16_t _enet_tx_bd_ring::txRingLen`

### 11.4.13 struct \_enet\_rx\_bd\_ring

#### Data Fields

- volatile `enet_rx_bd_struct_t * rxBdBase`  
*Buffer descriptor base address pointer.*
- `uint16_t rxGenIdx`  
*The current available receive buffer descriptor pointer.*
- `uint16_t rxRingLen`  
*Receive ring length.*

**Field Documentation**

- (1) volatile enet\_rx\_bd\_struct\_t\* \_enet\_rx\_bd\_ring::rxBdBase
- (2) uint16\_t \_enet\_rx\_bd\_ring::rxGenIdx
- (3) uint16\_t \_enet\_rx\_bd\_ring::rxRingLen

**11.4.14 struct \_enet\_handle****Data Fields**

- enet\_rx\_bd\_ring\_t rxBdRing [FSL\_FEATURE\_ENET\_QUEUE]  
*Receive buffer descriptor.*
- enet\_tx\_bd\_ring\_t txBdRing [FSL\_FEATURE\_ENET\_QUEUE]  
*Transmit buffer descriptor.*
- uint16\_t rxBuffSizeAlign [FSL\_FEATURE\_ENET\_QUEUE]  
*Receive buffer size alignment.*
- uint16\_t txBuffSizeAlign [FSL\_FEATURE\_ENET\_QUEUE]  
*Transmit buffer size alignment.*
- bool rxMaintainEnable [FSL\_FEATURE\_ENET\_QUEUE]  
*Receive buffer cache maintain.*
- bool txMaintainEnable [FSL\_FEATURE\_ENET\_QUEUE]  
*Transmit buffer cache maintain.*
- uint8\_t ringNum  
*Number of used rings.*
- enet\_callback\_t callback  
*Callback function.*
- void \* userData  
*Callback function parameter.*
- enet\_tx\_dirty\_ring\_t txDirtyRing [FSL\_FEATURE\_ENET\_QUEUE]  
*Ring to store tx frame information.*
- bool txReclaimEnable [FSL\_FEATURE\_ENET\_QUEUE]  
*Tx reclaim enable flag.*
- enet\_rx\_alloc\_callback\_t rxBuffAlloc  
*Callback function to alloc memory for zero copy Rx.*
- enet\_rx\_free\_callback\_t rxBuffFree  
*Callback function to free memory for zero copy Rx.*
- uint8\_t multicastCount [64]  
*Multicast collisions counter.*

**Field Documentation**

- (1) enet\_rx\_bd\_ring\_t \_enet\_handle::rxBdRing[FSL\_FEATURE\_ENET\_QUEUE]
- (2) enet\_tx\_bd\_ring\_t \_enet\_handle::txBdRing[FSL\_FEATURE\_ENET\_QUEUE]
- (3) uint16\_t \_enet\_handle::rxBuffSizeAlign[FSL\_FEATURE\_ENET\_QUEUE]
- (4) uint16\_t \_enet\_handle::txBuffSizeAlign[FSL\_FEATURE\_ENET\_QUEUE]
- (5) bool \_enet\_handle::rxMaintainEnable[FSL\_FEATURE\_ENET\_QUEUE]
- (6) bool \_enet\_handle::txMaintainEnable[FSL\_FEATURE\_ENET\_QUEUE]
- (7) uint8\_t \_enet\_handle::ringNum
- (8) enet\_callback\_t \_enet\_handle::callback
- (9) void\* \_enet\_handle::userData
- (10) enet\_tx\_dirty\_ring\_t \_enet\_handle::txDirtyRing[FSL\_FEATURE\_ENET\_QUEUE]
- (11) bool \_enet\_handle::txReclaimEnable[FSL\_FEATURE\_ENET\_QUEUE]
- (12) enet\_rx\_alloc\_callback\_t \_enet\_handle::rxBuffAlloc
- (13) enet\_rx\_free\_callback\_t \_enet\_handle::rxBuffFree

## 11.5 Macro Definition Documentation

- 11.5.1 `#define FSL_ENET_DRIVER_VERSION (MAKE_VERSION(2, 7, 1))`
- 11.5.2 `#define ENET_BUFFDESCRIPTOR_RX_EMPTY_MASK 0x8000U`
- 11.5.3 `#define ENET_BUFFDESCRIPTOR_RX_SOFTOWNER1_MASK 0x4000U`
- 11.5.4 `#define ENET_BUFFDESCRIPTOR_RX_WRAP_MASK 0x2000U`
- 11.5.5 `#define ENET_BUFFDESCRIPTOR_RX_SOFTOWNER2_Mask 0x1000U`
- 11.5.6 `#define ENET_BUFFDESCRIPTOR_RX_LAST_MASK 0x0800U`
- 11.5.7 `#define ENET_BUFFDESCRIPTOR_RX_MISS_MASK 0x0100U`
- 11.5.8 `#define ENET_BUFFDESCRIPTOR_RX_BROADCAST_MASK 0x0080U`
- 11.5.9 `#define ENET_BUFFDESCRIPTOR_RX_MULTICAST_MASK 0x0040U`
- 11.5.10 `#define ENET_BUFFDESCRIPTOR_RX_LENVIOLATE_MASK 0x0020U`
- 11.5.11 `#define ENET_BUFFDESCRIPTOR_RX_NOOCTET_MASK 0x0010U`
- 11.5.12 `#define ENET_BUFFDESCRIPTOR_RX_CRC_MASK 0x0004U`
- 11.5.13 `#define ENET_BUFFDESCRIPTOR_RX_OVERRUN_MASK 0x0002U`
- 11.5.14 `#define ENET_BUFFDESCRIPTOR_RX_TRUNC_MASK 0x0001U`
- 11.5.15 `#define ENET_BUFFDESCRIPTOR_TX_READY_MASK 0x8000U`
- 11.5.16 `#define ENET_BUFFDESCRIPTOR_TX_SOFTOWENER1_MASK 0x4000U`
- 11.5.17 `#define ENET_BUFFDESCRIPTOR_TX_WRAP_MASK 0x2000U`
- 11.5.18 `#define ENET_BUFFDESCRIPTOR_TX_SOFTOWENER2_MASK 0x1000U`
- 11.5.19 `#define ENET_BUFFDESCRIPTOR_TX_LAST_MASK 0x0800U`
- 11.5.20 ~~`#define ENET_BUFFDESCRIPTOR_TX_TRANMITCRC_MASK 0x0400U`~~
- 11.5.21 `#define ENET_BUFFDESCRIPTOR_RX_ERR_MASK`

```
(ENET_BUFFDESCRIPTOR_RX_TRUNC_MASK |
 ENET_BUFFDESCRIPTOR_RX_OVERRUN_MASK | \
 ENET_BUFFDESCRIPTOR_RX_LENVLIOLATE_MASK |
 ENET_BUFFDESCRIPTOR_RX_NOOCTET_MASK |
 ENET_BUFFDESCRIPTOR_RX_CRC_MASK)
```

### 11.5.22 #define ENET\_FRAME\_MAX\_FRAMELEN 1518U

### 11.5.23 #define ENET\_FRAME\_VLAN\_TAGLEN 4U

### 11.5.24 #define ENET\_FRAME\_CRC\_LEN 4U

### 11.5.25 #define ENET\_FIFO\_MIN\_RX\_FULL 5U

### 11.5.26 #define ENET\_RX\_MIN\_BUFFERSIZE 256U

### 11.5.27 #define ENET\_PHY\_MAXADDRESS (ENET\_MMFR\_PA\_MASK >> ENET\_MMFR\_PA\_SHIFT)

### 11.5.28 #define ENET\_TX\_INTERRUPT

**Value:**

```
((uint32_t)kENET_TxFrameInterrupt | (uint32_t)
 kENET_TxBufferInterrupt | (uint32_t)
 kENET_TxFramelInterrupt | \
 (uint32_t)kENET_TxBuffer1Interrupt | (uint32_t)
 kENET_TxFrame2Interrupt | \
 (uint32_t)kENET_TxBuffer2Interrupt)
```

### 11.5.29 #define ENET\_RX\_INTERRUPT

**Value:**

```
((uint32_t)kENET_RxFrameInterrupt | (uint32_t)
 kENET_RxBufferInterrupt | (uint32_t)
 kENET_RxFramelInterrupt | \
 (uint32_t)kENET_RxBuffer1Interrupt | (uint32_t)
 kENET_RxFrame2Interrupt | \
 (uint32_t)kENET_RxBuffer2Interrupt)
```

**11.5.30 #define ENET\_TS\_INTERRUPT ((uint32\_t)kENET\_TsTimerInterrupt | (uint32\_t)kENET\_TsAvailInterrupt)**

**11.5.31 #define ENET\_ERR\_INTERRUPT**

**Value:**

```
((uint32_t)kENET_BabrInterrupt | (uint32_t)
 kENET_BabtInterrupt | (uint32_t)kENET_EBusERInterrupt | \
 (uint32_t)kENET_LateCollisionInterrupt | (uint32_t)
 kENET_RetryLimitInterrupt | \
 (uint32_t)kENET_UnderrunInterrupt | (uint32_t)
 kENET_PayloadRxInterrupt)
```

## 11.6 Typedef Documentation

**11.6.1 typedef enum \_enet\_mii\_mode enet\_mii\_mode\_t**

**11.6.2 typedef enum \_enet\_mii\_speed enet\_mii\_speed\_t**

Notice: "kENET\_MiiSpeed1000M" only supported when mii mode is "kENET\_RgmiiMode".

**11.6.3 typedef enum \_enet\_mii\_duplex enet\_mii\_duplex\_t**

**11.6.4 typedef enum \_enet\_mii\_write enet\_mii\_write\_t**

**11.6.5 typedef enum \_enet\_mii\_read enet\_mii\_read\_t**

**11.6.6 typedef enum \_enet\_mii\_extend\_opcode enet\_mii\_extend\_opcode**

**11.6.7 typedef enum \_enet\_special\_control\_flag enet\_special\_control\_flag\_t**

These control flags are provided for special user requirements. Normally, these control flags are unused for ENET initialization. For special requirements, set the flags to macSpecialConfig in the enet\_config\_t. The kENET\_ControlStoreAndFwdDisable is used to disable the FIFO store and forward. FIFO store and forward means that the FIFO read/send is started when a complete frame is stored in TX/RX FIFO. If this flag is set, configure rxFifoFullThreshold and txFifoWatermark in the enet\_config\_t.

**11.6.8 typedef enum \_enet\_interrupt\_enable enet\_interrupt\_enable\_t**

This enumeration uses one-bit encoding to allow a logical OR of multiple members. Members usually map to interrupt enable bits in one or more peripheral registers.

- 11.6.9 `typedef enum _enet_event enet_event_t`**
- 11.6.10 `typedef enum _enet_idle_slope enet_idle_slope_t`**
- 11.6.11 `typedef enum _enet_tx_accelerator enet_tx_accelerator_t`**
- 11.6.12 `typedef enum _enet_rx_accelerator enet_rx_accelerator_t`**
- 11.6.13 `typedef struct _enet_rx_bd_struct enet_rx_bd_struct_t`**
- 11.6.14 `typedef struct _enet_tx_bd_struct enet_tx_bd_struct_t`**
- 11.6.15 `typedef struct _enet_data_error_stats enet_data_error_stats_t`**
- 11.6.16 `typedef struct _enet_rx_frame_error enet_rx_frame_error_t`**
- 11.6.17 `typedef struct _enet_transfer_stats enet_transfer_stats_t`**
- 11.6.18 `typedef struct enet_frame_info enet_frame_info_t`**
- 11.6.19 `typedef struct _enet_tx_dirty_ring enet_tx_dirty_ring_t`**
- 11.6.20 `typedef void*(* enet_rx_alloc_callback_t)(ENET_Type *base, void *userData, uint8_t ringId)`**
- 11.6.21 `typedef void(* enet_rx_free_callback_t)(ENET_Type *base, void *buffer, void *userData, uint8_t ringId)`**
- 11.6.22 `typedef struct _enet_buffer_config enet_buffer_config_t`**

Note that for the internal DMA requirements, the buffers have a corresponding alignment requirements.

1. The aligned receive and transmit buffer size must be evenly divisible by ENET\_BUFF\_ALIGNMENT. when the data buffers are in cacheable region when cache is enabled, all those size should be aligned to the maximum value of "ENET\_BUFF\_ALIGNMENT" and the cache line size.
2. The aligned transmit and receive buffer descriptor start address must be at least 64 bit aligned. However, it's recommended to be evenly divisible by ENET\_BUFF\_ALIGNMENT. buffer descriptors should be put in non-cacheable region when cache is enabled.
3. The aligned transmit and receive data buffer start address must be evenly divisible by ENET\_BUFF\_ALIGNMENT. Receive buffers should be continuous with the total size equal to "rxBdNumber \*

rxBuffSizeAlign". Transmit buffers should be continuous with the total size equal to "txBdNumber \* txBuffSizeAlign". when the data buffers are in cacheable region when cache is enabled, all those size should be aligned to the maximum value of "ENET\_BUFF\_ALIGNMENT" and the cache line size.

### **11.6.23 `typedef struct _enet_intcoalesce_config enet_intcoalesce_config_t`**

### **11.6.24 `typedef struct _enet_avb_config enet_avb_config_t`**

This is used for to configure the extended ring 1 and ring 2.

1. The classification match format is (CMP3 << 12) | (CMP2 << 8) | (CMP1 << 4) | CMP0. composed of four 3-bit compared VLAN priority field cmp0~cmp3, cm0 ~ cmp3 are used in parallel.

If CMP1,2,3 are not unused, please set them to the same value as CMP0.

1. The idleSlope is used to calculate the Band Width fraction, BW fraction = 1 / (1 + 512/idleSlope). For avb configuration, the BW fraction of Class 1 and Class 2 combined must not exceed 0.75.

### **11.6.25 `typedef void(* enet_callback_t)(ENET_Type *base, enet_handle_t *handle, uint32_t ringId, enet_event_t event, enet_frame_info_t *frameInfo, void *userData)`**

### **11.6.26 `typedef struct _enet_config enet_config_t`**

Note:

1. macSpecialConfig is used for a special control configuration, A logical OR of "enet\_special\_control\_flag\_t". For a special configuration for MAC, set this parameter to 0.
2. txWatermark is used for a cut-through operation. It is in steps of 64 bytes: 0/1 - 64 bytes written to TX FIFO before transmission of a frame begins. 2 - 128 bytes written to TX FIFO .... 3 - 192 bytes written to TX FIFO .... The maximum of txWatermark is 0x2F - 4032 bytes written to TX FIFO .... txWatermark allows minimizing the transmit latency to set the txWatermark to 0 or 1 or for larger bus access latency 3 or larger due to contention for the system bus.
3. rxFifoFullThreshold is similar to the txWatermark for cut-through operation in RX. It is in 64-bit words. The minimum is ENET\_FIFO\_MIN\_RX\_FULL and the maximum is 0xFF. If the end of the frame is stored in FIFO and the frame size if smaller than the txWatermark, the frame is still transmitted. The rule is the same for rxFifoFullThreshold in the receive direction.
4. When "kENET\_ControlFlowControlEnable" is set in the macSpecialConfig, ensure that the pause-Duration, rxFifoEmptyThreshold, and rxFifoStatEmptyThreshold are set for flow control enabled case.
5. When "kENET\_ControlStoreAndFwdDisabled" is set in the macSpecialConfig, ensure that the rx-FifoFullThreshold and txFifoWatermark are set for store and forward disable.

6. The rxAccelerConfig and txAccelerConfig default setting with 0 - accelerator are disabled. The "enet\_tx\_accelerator\_t" and "enet\_rx\_accelerator\_t" are recommended to be used to enable the transmit and receive accelerator. After the accelerators are enabled, the store and forward feature should be enabled. As a result, kENET\_ControlStoreAndFwdDisabled should not be set.
7. The intCoalesceCfg can be used in the rx or tx enabled cases to decrease the CPU loading.

### **11.6.27 `typedef struct _enet_tx_bd_ring enet_tx_bd_ring_t`**

### **11.6.28 `typedef struct _enet_rx_bd_ring enet_rx_bd_ring_t`**

### **11.6.29 `typedef void(* enet_isr_ring_t)(ENET_Type *base, enet_handle_t *handle, uint32_t ringId)`**

## **11.7 Enumeration Type Documentation**

### **11.7.1 anonymous enum**

Enumerator

*kStatus\_ENET\_InitMemoryFail* Init fails since buffer memory is not enough.

*kStatus\_ENET\_RxFrameError* A frame received but data error happen.

*kStatus\_ENET\_RxFrameFail* Failed to receive a frame.

*kStatus\_ENET\_RxFrameEmpty* No frame arrive.

*kStatus\_ENET\_RxFrameDrop* Rx frame is dropped since no buffer memory.

*kStatus\_ENET\_TxFrameOverLen* Tx frame over length.

*kStatus\_ENET\_TxFrameBusy* Tx buffer descriptors are under process.

*kStatus\_ENET\_TxFrameFail* Transmit frame fail.

### **11.7.2 `enum _enet_mii_mode`**

Enumerator

*kENET\_MiiMode* MII mode for data interface.

*kENET\_RmiiMode* RMII mode for data interface.

*kENET\_RgmiiMode* RGMII mode for data interface.

### **11.7.3 `enum _enet_mii_speed`**

Notice: "kENET\_MiiSpeed1000M" only supported when mii mode is "kENET\_RgmiiMode".

Enumerator

*kENET\_MiiSpeed10M* Speed 10 Mbps.

***kENET\_MiiSpeed100M*** Speed 100 Mbps.  
***kENET\_MiiSpeed1000M*** Speed 1000M bps.

#### 11.7.4 enum \_enet\_mii\_duplex

Enumerator

***kENET\_MiiHalfDuplex*** Half duplex mode.  
***kENET\_MiiFullDuplex*** Full duplex mode.

#### 11.7.5 enum \_enet\_mii\_write

Enumerator

***kENET\_MiiWriteNoCompliant*** Write frame operation, but not MII-compliant.  
***kENET\_MiiWriteValidFrame*** Write frame operation for a valid MII management frame.

#### 11.7.6 enum \_enet\_mii\_read

Enumerator

***kENET\_MiiReadValidFrame*** Read frame operation for a valid MII management frame.  
***kENET\_MiiReadNoCompliant*** Read frame operation, but not MII-compliant.

#### 11.7.7 enum \_enet\_mii\_extend\_opcode

Enumerator

***kENET\_MiiAddrWrite\_C45*** Address Write operation.  
***kENET\_MiiWriteFrame\_C45*** Write frame operation for a valid MII management frame.  
***kENET\_MiiReadFrame\_C45*** Read frame operation for a valid MII management frame.

#### 11.7.8 enum \_enet\_special\_control\_flag

These control flags are provided for special user requirements. Normally, these control flags are unused for ENET initialization. For special requirements, set the flags to macSpecialConfig in the enet\_config\_t. The kENET\_ControlStoreAndFwdDisable is used to disable the FIFO store and forward. FIFO store and forward means that the FIFO read/send is started when a complete frame is stored in TX/RX FIFO. If this flag is set, configure rxFifoFullThreshold and txFifoWatermark in the enet\_config\_t.

Enumerator

- kENET\_ControlFlowControlEnable*** Enable ENET flow control: pause frame.
- kENET\_ControlRxPayloadCheckEnable*** Enable ENET receive payload length check.
- kENET\_ControlRxPadRemoveEnable*** Padding is removed from received frames.
- kENET\_ControlRxBroadCastRejectEnable*** Enable broadcast frame reject.
- kENET\_ControlMacAddrInsert*** Enable MAC address insert.
- kENET\_ControlStoreAndFwdDisable*** Enable FIFO store and forward.
- kENET\_ControlSMIPreambleDisable*** Enable SMI preamble.
- kENET\_ControlPromiscuousEnable*** Enable promiscuous mode.
- kENET\_ControlMIILoopEnable*** Enable ENET MII loop back.
- kENET\_ControlVLANTagEnable*** Enable normal VLAN (single vlan tag).
- kENET\_ControlSVLANEnable*** Enable S-VLAN.
- kENET\_ControlVLANUseSecondTag*** Enable extracting the second vlan tag for further processing.

### 11.7.9 enum \_enet\_interrupt\_enable

This enumeration uses one-bit encoding to allow a logical OR of multiple members. Members usually map to interrupt enable bits in one or more peripheral registers.

Enumerator

- kENET\_BabrInterrupt*** Babbling receive error interrupt source.
- kENET\_BabtInterrupt*** Babbling transmit error interrupt source.
- kENET\_GraceStopInterrupt*** Graceful stop complete interrupt source.
- kENET\_TxFrameInterrupt*** TX FRAME interrupt source.
- kENET\_TxBufferInterrupt*** TX BUFFER interrupt source.
- kENET\_RxFrameInterrupt*** RX FRAME interrupt source.
- kENET\_RxBufferInterrupt*** RX BUFFER interrupt source.
- kENET\_MiiInterrupt*** MII interrupt source.
- kENET\_EBusERInterrupt*** Ethernet bus error interrupt source.
- kENET\_LateCollisionInterrupt*** Late collision interrupt source.
- kENET\_RetryLimitInterrupt*** Collision Retry Limit interrupt source.
- kENET\_UnderrunInterrupt*** Transmit FIFO underrun interrupt source.
- kENET\_PayloadRxInterrupt*** Payload Receive error interrupt source.
- kENET\_WakeupInterrupt*** WAKEUP interrupt source.
- kENET\_RxFlush2Interrupt*** Rx DMA ring2 flush indication.
- kENET\_RxFlush1Interrupt*** Rx DMA ring1 flush indication.
- kENET\_RxFlush0Interrupt*** RX DMA ring0 flush indication.
- kENET\_TxFrame2Interrupt*** Tx frame interrupt for Tx ring/class 2.
- kENET\_TxBuffer2Interrupt*** Tx buffer interrupt for Tx ring/class 2.
- kENET\_RxFrame2Interrupt*** Rx frame interrupt for Rx ring/class 2.
- kENET\_RxBuffer2Interrupt*** Rx buffer interrupt for Rx ring/class 2.
- kENET\_TxFrame1Interrupt*** Tx frame interrupt for Tx ring/class 1.
- kENET\_TxBuffer1Interrupt*** Tx buffer interrupt for Tx ring/class 1.

***kENET\_RxFrame1Interrupt*** Rx frame interrupt for Rx ring/class 1.

***kENET\_RxBuffer1Interrupt*** Rx buffer interrupt for Rx ring/class 1.

***kENET\_TsAvailInterrupt*** TS AVAIL interrupt source for PTP.

***kENET\_TsTimerInterrupt*** TS WRAP interrupt source for PTP.

### 11.7.10 enum \_enet\_event

Enumerator

***kENET\_RxEvent*** Receive event.

***kENET\_TxEvent*** Transmit event.

***kENET\_ErrEvent*** Error event: BABR/BABT/EBERR/LC/RL/UN/PLR .

***kENET\_WakeUpEvent*** Wake up from sleep mode event.

***kENET\_TimeStampEvent*** Time stamp event.

***kENET\_TimeStampAvailEvent*** Time stamp available event.

### 11.7.11 enum \_enet\_idle\_slope

Enumerator

***kENET\_IdleSlope1*** The bandwidth fraction is about 0.002.

***kENET\_IdleSlope2*** The bandwidth fraction is about 0.003.

***kENET\_IdleSlope4*** The bandwidth fraction is about 0.008.

***kENET\_IdleSlope8*** The bandwidth fraction is about 0.02.

***kENET\_IdleSlope16*** The bandwidth fraction is about 0.03.

***kENET\_IdleSlope32*** The bandwidth fraction is about 0.06.

***kENET\_IdleSlope64*** The bandwidth fraction is about 0.11.

***kENET\_IdleSlope128*** The bandwidth fraction is about 0.20.

***kENET\_IdleSlope256*** The bandwidth fraction is about 0.33.

***kENET\_IdleSlope384*** The bandwidth fraction is about 0.43.

***kENET\_IdleSlope512*** The bandwidth fraction is about 0.50.

***kENET\_IdleSlope640*** The bandwidth fraction is about 0.56.

***kENET\_IdleSlope768*** The bandwidth fraction is about 0.60.

***kENET\_IdleSlope896*** The bandwidth fraction is about 0.64.

***kENET\_IdleSlope1024*** The bandwidth fraction is about 0.67.

***kENET\_IdleSlope1152*** The bandwidth fraction is about 0.69.

***kENET\_IdleSlope1280*** The bandwidth fraction is about 0.71.

***kENET\_IdleSlope1408*** The bandwidth fraction is about 0.73.

***kENET\_IdleSlope1536*** The bandwidth fraction is about 0.75.

### 11.7.12 enum \_enet\_tx\_accelerator

Enumerator

- kENET\_TxAccelIsShift16Enabled*** Transmit FIFO shift-16.
- kENET\_TxAccelIpCheckEnabled*** Insert IP header checksum.
- kENET\_TxAccelProtoCheckEnabled*** Insert protocol checksum.

### 11.7.13 enum \_enet\_rx\_accelerator

Enumerator

- kENET\_RxAccelPadRemoveEnabled*** Padding removal for short IP frames.
- kENET\_RxAccelIpCheckEnabled*** Discard with wrong IP header checksum.
- kENET\_RxAccelProtoCheckEnabled*** Discard with wrong protocol checksum.
- kENET\_RxAccelMacCheckEnabled*** Discard with Mac layer errors.
- kENET\_RxAccelIsShift16Enabled*** Receive FIFO shift-16.

## 11.8 Function Documentation

### 11.8.1 uint32\_t ENET\_GetInstance ( ENET\_Type \* *base* )

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

Returns

ENET instance.

### 11.8.2 void ENET\_GetDefaultConfig ( enet\_config\_t \* *config* )

The purpose of this API is to get the default ENET MAC controller configure structure for [ENET\\_Init\(\)](#). User may use the initialized structure unchanged in [ENET\\_Init\(\)](#), or modify some fields of the structure before calling [ENET\\_Init\(\)](#). Example:

```
enet_config_t config;
ENET_GetDefaultConfig(&config);
```

## Parameters

|               |                                                          |
|---------------|----------------------------------------------------------|
| <i>config</i> | The ENET mac controller configuration structure pointer. |
|---------------|----------------------------------------------------------|

**11.8.3 status\_t ENET\_Up ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, const enet\_config\_t \* *config*, const enet\_buffer\_config\_t \* *bufferConfig*, uint8\_t \* *macAddr*, uint32\_t *srcClock\_Hz* )**

This function initializes the module with the ENET configuration.

## Note

ENET has two buffer descriptors legacy buffer descriptors and enhanced IEEE 1588 buffer descriptors. The legacy descriptor is used by default. To use the IEEE 1588 feature, use the enhanced IEEE 1588 buffer descriptor by defining "ENET\_ENHANCEDBUFFERDESCRIPTOR\_MODE" and calling ENET\_Ptp1588Configure() to configure the 1588 feature and related buffers after calling [ENET\\_Up\(\)](#).

## Parameters

|                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>         | ENET peripheral base address.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <i>handle</i>       | ENET handler pointer.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <i>config</i>       | ENET mac configuration structure pointer. The "enet_config_t" type mac configuration return from ENET_GetDefaultConfig can be used directly. It is also possible to verify the Mac configuration using other methods.                                                                                                                                                                                                                                                                                      |
| <i>bufferConfig</i> | ENET buffer configuration structure pointer. The buffer configuration should be prepared for ENET Initialization. It is the start address of "ringNum" enet_buffer_config structures. To support added multi-ring features in some soc and compatible with the previous enet driver version. For single ring supported, this bufferConfig is a buffer configure structure pointer, for multi-ring supported and used case, this bufferConfig pointer should be a buffer configure structure array pointer. |

|                    |                                                                           |
|--------------------|---------------------------------------------------------------------------|
| <i>macAddr</i>     | ENET mac address of Ethernet device. This MAC address should be provided. |
| <i>srcClock_Hz</i> | The internal module clock source for MII clock.                           |

Return values

|                                     |                                               |
|-------------------------------------|-----------------------------------------------|
| <i>kStatus_Success</i>              | Succeed to initialize the ethernet driver.    |
| <i>kStatus_ENET_Init-MemoryFail</i> | Init fails since buffer memory is not enough. |

#### 11.8.4 status\_t ENET\_Init( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, const enet\_config\_t \* *config*, const enet\_buffer\_config\_t \* *bufferConfig*, uint8\_t \* *macAddr*, uint32\_t *srcClock\_Hz* )

This function ungates the module clock and initializes it with the ENET configuration.

Note

ENET has two buffer descriptors legacy buffer descriptors and enhanced IEEE 1588 buffer descriptors. The legacy descriptor is used by default. To use the IEEE 1588 feature, use the enhanced IEEE 1588 buffer descriptor by defining "ENET\_ENHANCEDBUFFERDESCRIPTOR\_MODE" and calling ENET\_Ptp1588Configure() to configure the 1588 feature and related buffers after calling [ENET\\_Init\(\)](#).

Parameters

|                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>         | ENET peripheral base address.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <i>handle</i>       | ENET handler pointer.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <i>config</i>       | ENET mac configuration structure pointer. The "enet_config_t" type mac configuration return from ENET_GetDefaultConfig can be used directly. It is also possible to verify the Mac configuration using other methods.                                                                                                                                                                                                                                                                                      |
| <i>bufferConfig</i> | ENET buffer configuration structure pointer. The buffer configuration should be prepared for ENET Initialization. It is the start address of "ringNum" enet_buffer_config structures. To support added multi-ring features in some soc and compatible with the previous enet driver version. For single ring supported, this bufferConfig is a buffer configure structure pointer, for multi-ring supported and used case, this bufferConfig pointer should be a buffer configure structure array pointer. |

|                    |                                                                           |
|--------------------|---------------------------------------------------------------------------|
| <i>macAddr</i>     | ENET mac address of Ethernet device. This MAC address should be provided. |
| <i>srcClock_Hz</i> | The internal module clock source for MII clock.                           |

Return values

|                                     |                                               |
|-------------------------------------|-----------------------------------------------|
| <i>kStatus_Success</i>              | Succeed to initialize the ethernet driver.    |
| <i>kStatus_ENET_Init-MemoryFail</i> | Init fails since buffer memory is not enough. |

### 11.8.5 void ENET\_Down ( ENET\_Type \* *base* )

This function disables the ENET module.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

### 11.8.6 void ENET\_Deinit ( ENET\_Type \* *base* )

This function gates the module clock, clears ENET interrupts, and disables the ENET module.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

### 11.8.7 static void ENET\_Reset ( ENET\_Type \* *base* ) [inline], [static]

This function restores the ENET module to reset state. Note that this function sets all registers to reset state. As a result, the ENET module can't work after calling this function.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

### 11.8.8 void ENET\_SetMII ( ENET\_Type \* *base*, enet\_mii\_speed\_t *speed*, enet\_mii\_duplex\_t *duplex* )

This API is provided to dynamically change the speed and duplex for MAC.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ENET peripheral base address. |
| <i>speed</i>  | The speed of the RMII mode.   |
| <i>duplex</i> | The duplex of the RMII mode.  |

### 11.8.9 void ENET\_SetSMI ( ENET\_Type \* *base*, uint32\_t *srcClock\_Hz*, bool *isPreambleDisabled* )

Parameters

|                           |                                                                                                                                                   |
|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>               | ENET peripheral base address.                                                                                                                     |
| <i>srcClock_Hz</i>        | This is the ENET module clock frequency. See clock distribution.                                                                                  |
| <i>isPreambleDisabled</i> | The preamble disable flag. <ul style="list-style-type: none"> <li>• true Enables the preamble.</li> <li>• false Disables the preamble.</li> </ul> |

### 11.8.10 static bool ENET\_GetSMI ( ENET\_Type \* *base* ) [inline], [static]

This API is used to get the SMI configuration to check whether the MII management interface has been set.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

Returns

The SMI setup status true or false.

### 11.8.11 static uint32\_t ENET\_ReadSMIData ( ENET\_Type \* *base* ) [inline], [static]

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

Returns

The data read from PHY

**11.8.12 static void ENET\_StartSMIWrite ( ENET\_Type \* *base*, uint8\_t *phyAddr*, uint8\_t *regAddr*, enet\_mii\_write\_t *operation*, uint16\_t *data* ) [inline], [static]**

After calling this function, need to check whether the transmission is over then do next MDIO operation. For ease of use, encapsulated [ENET\\_MDIOWrite\(\)](#) can be called. For customized requirements, implement with combining separated APIs.

Parameters

|                  |                                              |
|------------------|----------------------------------------------|
| <i>base</i>      | ENET peripheral base address.                |
| <i>phyAddr</i>   | The PHY address. Range from 0 ~ 31.          |
| <i>regAddr</i>   | The PHY register address. Range from 0 ~ 31. |
| <i>operation</i> | The write operation.                         |
| <i>data</i>      | The data written to PHY.                     |

**11.8.13 static void ENET\_StartSMIRead ( ENET\_Type \* *base*, uint8\_t *phyAddr*, uint8\_t *regAddr*, enet\_mii\_read\_t *operation* ) [inline], [static]**

After calling this function, need to check whether the transmission is over then do next MDIO operation. For ease of use, encapsulated [ENET\\_MDIORRead\(\)](#) can be called. For customized requirements, implement with combining separated APIs.

Parameters

|                |                                     |
|----------------|-------------------------------------|
| <i>base</i>    | ENET peripheral base address.       |
| <i>phyAddr</i> | The PHY address. Range from 0 ~ 31. |

|                  |                                              |
|------------------|----------------------------------------------|
| <i>regAddr</i>   | The PHY register address. Range from 0 ~ 31. |
| <i>operation</i> | The read operation.                          |

### 11.8.14 status\_t ENET\_MDIOWrite ( ENET\_Type \* *base*, uint8\_t *phyAddr*, uint8\_t *regAddr*, uint16\_t *data* )

Parameters

|                |                                      |
|----------------|--------------------------------------|
| <i>base</i>    | ENET peripheral base address.        |
| <i>phyAddr</i> | The PHY address. Range from 0 ~ 31.  |
| <i>regAddr</i> | The PHY register. Range from 0 ~ 31. |
| <i>data</i>    | The data written to PHY.             |

Returns

kStatus\_Success MDIO access succeeds.  
kStatus\_Timeout MDIO access timeout.

### 11.8.15 status\_t ENET\_MDIORRead ( ENET\_Type \* *base*, uint8\_t *phyAddr*, uint8\_t *regAddr*, uint16\_t \* *pData* )

Parameters

|                |                                      |
|----------------|--------------------------------------|
| <i>base</i>    | ENET peripheral base address.        |
| <i>phyAddr</i> | The PHY address. Range from 0 ~ 31.  |
| <i>regAddr</i> | The PHY register. Range from 0 ~ 31. |
| <i>pData</i>   | The data read from PHY.              |

Returns

kStatus\_Success MDIO access succeeds.  
kStatus\_Timeout MDIO access timeout.

### 11.8.16 static void ENET\_StartExtC45SMIWriteReg ( ENET\_Type \* *base*, uint8\_t *portAddr*, uint8\_t *devAddr*, uint16\_t *regAddr* ) [inline], [static]

After calling this function, need to check whether the transmission is over then do next MDIO operation. For ease of use, encapsulated [ENET\\_MDIODC45Write\(\)](#)/[ENET\\_MDIODC45Read\(\)](#) can be called. For

customized requirements, implement with combining separated APIs.

Parameters

|                 |                                     |
|-----------------|-------------------------------------|
| <i>base</i>     | ENET peripheral base address.       |
| <i>portAddr</i> | The MDIO port address(PHY address). |
| <i>devAddr</i>  | The device address.                 |
| <i>regAddr</i>  | The PHY register address.           |

### 11.8.17 static void ENET\_StartExtC45SMIWriteData ( ENET\_Type \* *base*, uint8\_t *portAddr*, uint8\_t *devAddr*, uint16\_t *data* ) [inline], [static]

After calling this function, need to check whether the transmission is over then do next MDIO operation. For ease of use, encapsulated [ENET\\_MDIODC45Write\(\)](#) can be called. For customized requirements, implement with combining separated APIs.

Parameters

|                 |                                     |
|-----------------|-------------------------------------|
| <i>base</i>     | ENET peripheral base address.       |
| <i>portAddr</i> | The MDIO port address(PHY address). |
| <i>devAddr</i>  | The device address.                 |
| <i>data</i>     | The data written to PHY.            |

### 11.8.18 static void ENET\_StartExtC45SMIReadData ( ENET\_Type \* *base*, uint8\_t *portAddr*, uint8\_t *devAddr* ) [inline], [static]

After calling this function, need to check whether the transmission is over then do next MDIO operation. For ease of use, encapsulated [ENET\\_MDIODC45Read\(\)](#) can be called. For customized requirements, implement with combining separated APIs.

Parameters

|                 |                                     |
|-----------------|-------------------------------------|
| <i>base</i>     | ENET peripheral base address.       |
| <i>portAddr</i> | The MDIO port address(PHY address). |
| <i>devAddr</i>  | The device address.                 |

### 11.8.19 status\_t ENET\_MDIODC45Write ( ENET\_Type \* *base*, uint8\_t *portAddr*, uint8\_t *devAddr*, uint16\_t *regAddr*, uint16\_t *data* )

Parameters

|                 |                                     |
|-----------------|-------------------------------------|
| <i>base</i>     | ENET peripheral base address.       |
| <i>portAddr</i> | The MDIO port address(PHY address). |
| <i>devAddr</i>  | The device address.                 |
| <i>regAddr</i>  | The PHY register address.           |
| <i>data</i>     | The data written to PHY.            |

Returns

kStatus\_Success MDIO access succeeds.  
kStatus\_Timeout MDIO access timeout.

### 11.8.20 status\_t ENET\_MDIOD45Read ( ENET\_Type \* *base*, uint8\_t *portAddr*, uint8\_t *devAddr*, uint16\_t *regAddr*, uint16\_t \* *pData* )

Parameters

|                 |                                     |
|-----------------|-------------------------------------|
| <i>base</i>     | ENET peripheral base address.       |
| <i>portAddr</i> | The MDIO port address(PHY address). |
| <i>devAddr</i>  | The device address.                 |
| <i>regAddr</i>  | The PHY register address.           |
| <i>pData</i>    | The data read from PHY.             |

Returns

kStatus\_Success MDIO access succeeds.  
kStatus\_Timeout MDIO access timeout.

### 11.8.21 static void ENET\_SetRGMIIClockDelay ( ENET\_Type \* *base*, bool *txEnabled*, bool *rxEnabled* ) [inline], [static]

Parameters

|                  |                                                                 |
|------------------|-----------------------------------------------------------------|
| <i>base</i>      | ENET peripheral base address.                                   |
| <i>txEnabled</i> | Enable or disable to generate the delayed version of RGMII_TXC. |
| <i>rxEnabled</i> | Enable or disable to use the delayed version of RGMII_RXC.      |

**11.8.22 void ENET\_SetMacAddr ( ENET\_Type \* *base*, uint8\_t \* *macAddr* )**

Parameters

|                |                                                                                                   |
|----------------|---------------------------------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                                                     |
| <i>macAddr</i> | The six-byte Mac address pointer. The pointer is allocated by application and input into the API. |

**11.8.23 void ENET\_GetMacAddr ( ENET\_Type \* *base*, uint8\_t \* *macAddr* )**

Parameters

|                |                                                                                                   |
|----------------|---------------------------------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                                                     |
| <i>macAddr</i> | The six-byte Mac address pointer. The pointer is allocated by application and input into the API. |

**11.8.24 void ENET\_AddMulticastGroup ( ENET\_Type \* *base*, uint8\_t \* *address* )**

Parameters

|                |                                                                        |
|----------------|------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                          |
| <i>address</i> | The six-byte multicast group address which is provided by application. |

**11.8.25 void ENET\_LeaveMulticastGroup ( ENET\_Type \* *base*, uint8\_t \* *address* )**

Parameters

|                |                                                                        |
|----------------|------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                          |
| <i>address</i> | The six-byte multicast group address which is provided by application. |

### 11.8.26 static void ENET\_ActiveRead ( ENET\_Type \* *base* ) [inline], [static]

This function is to active the enet read process.

Note

This must be called after the MAC configuration and state are ready. It must be called after the [ENET\\_Init\(\)](#). This should be called when the frame reception is required.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

### 11.8.27 static void ENET\_EnableSleepMode ( ENET\_Type \* *base*, bool *enable* ) [inline], [static]

This function is used to set the MAC enter sleep mode. When entering sleep mode, the magic frame wakeup interrupt should be enabled to wake up MAC from the sleep mode and reset it to normal mode.

Parameters

|               |                                                   |
|---------------|---------------------------------------------------|
| <i>base</i>   | ENET peripheral base address.                     |
| <i>enable</i> | True enable sleep mode, false disable sleep mode. |

### 11.8.28 static void ENET\_GetAccelFunction ( ENET\_Type \* *base*, uint32\_t \* *txAccelOption*, uint32\_t \* *rxAccelOption* ) [inline], [static]

Parameters

|                      |                                                                                                                                                |
|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>          | ENET peripheral base address.                                                                                                                  |
| <i>txAccelOption</i> | The transmit accelerator option. The "enet_tx_accelerator_t" is recommended to be used to as the mask to get the exact the accelerator option. |
| <i>rxAccelOption</i> | The receive accelerator option. The "enet_rx_accelerator_t" is recommended to be used to as the mask to get the exact the accelerator option.  |

### 11.8.29 static void ENET\_EnableInterrupts ( ENET\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function enables the ENET interrupt according to the provided mask. The mask is a logical OR of enumeration members. See [enet\\_interrupt\\_enable\\_t](#). For example, to enable the TX frame interrupt and RX frame interrupt, do the following.

```
* ENET_EnableInterrupts(ENET, kENET_TxFrameInterrupt |
* kENET_RxFrameInterrupt);
*
```

Parameters

|             |                                                                                                              |
|-------------|--------------------------------------------------------------------------------------------------------------|
| <i>base</i> | ENET peripheral base address.                                                                                |
| <i>mask</i> | ENET interrupts to enable. This is a logical OR of the enumeration <a href="#">enet_interrupt_enable_t</a> . |

### 11.8.30 static void ENET\_DisableInterrupts ( ENET\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function disables the ENET interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [enet\\_interrupt\\_enable\\_t](#). For example, to disable the TX frame interrupt and RX frame interrupt, do the following.

```
* ENET_DisableInterrupts(ENET, kENET_TxFrameInterrupt |
* kENET_RxFrameInterrupt);
*
```

Parameters

|             |                                                                                                               |
|-------------|---------------------------------------------------------------------------------------------------------------|
| <i>base</i> | ENET peripheral base address.                                                                                 |
| <i>mask</i> | ENET interrupts to disable. This is a logical OR of the enumeration <a href="#">enet_interrupt_enable_t</a> . |

### 11.8.31 static uint32\_t ENET\_GetInterruptStatus ( ENET\_Type \* *base* ) [inline], [static]

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

## Returns

The event status of the interrupt source. This is the logical OR of members of the enumeration [enet\\_interrupt\\_enable\\_t](#).

### 11.8.32 static void ENET\_ClearInterruptStatus ( ENET\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function clears enabled ENET interrupts according to the provided mask. The mask is a logical OR of enumeration members. See the [enet\\_interrupt\\_enable\\_t](#). For example, to clear the TX frame interrupt and RX frame interrupt, do the following.

```
* ENET_ClearInterruptStatus(ENET,
 kENET_TxFrameInterrupt | kENET_RxFrameInterrupt);
*
```

## Parameters

|             |                                                                                                                                     |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | ENET peripheral base address.                                                                                                       |
| <i>mask</i> | ENET interrupt source to be cleared. This is the logical OR of members of the enumeration <a href="#">enet_interrupt_enable_t</a> . |

### 11.8.33 void ENET\_SetRxISRHandler ( ENET\_Type \* *base*, enet\_isr\_ring\_t *ISRHandler* )

## Parameters

|                   |                               |
|-------------------|-------------------------------|
| <i>base</i>       | ENET peripheral base address. |
| <i>ISRHandler</i> | The handler to install.       |

### 11.8.34 void ENET\_SetTxISRHandler ( ENET\_Type \* *base*, enet\_isr\_ring\_t *ISRHandler* )

Parameters

|                   |                               |
|-------------------|-------------------------------|
| <i>base</i>       | ENET peripheral base address. |
| <i>ISRHandler</i> | The handler to install.       |

### 11.8.35 void ENET\_SetErrISRHandler ( ENET\_Type \* *base*, enet\_isr\_t *ISRHandler* )

Parameters

|                   |                               |
|-------------------|-------------------------------|
| <i>base</i>       | ENET peripheral base address. |
| <i>ISRHandler</i> | The handler to install.       |

### 11.8.36 void ENET\_GetRxErrBeforeReadFrame ( enet\_handle\_t \* *handle*, enet\_data\_error\_stats\_t \* *eErrorStatic*, uint8\_t *ringId* )

This API must be called after the ENET\_GetRxFrameSize and before the ENET\_ReadFrame(). If the ENET\_GetRxFrameSize returns kStatus\_ENET\_RxFrameError, the ENET\_GetRxErrBeforeReadFrame can be used to get the exact error statistics. This is an example.

```
* status = ENET_GetRxFrameSize(&g_handle, &length, 0);
* if (status == kStatus_ENET_RxFrameError)
* {
* Comments: Get the error information of the received frame.
* ENET_GetRxErrBeforeReadFrame(&g_handle, &eErrStatic, 0);
* Comments: update the receive buffer.
* ENET_ReadFrame(EXAMPLE_ENET, &g_handle, NULL, 0);
* }
*
```

Parameters

|                     |                                                                                             |
|---------------------|---------------------------------------------------------------------------------------------|
| <i>handle</i>       | The ENET handler structure pointer. This is the same handler pointer used in the ENET_Init. |
| <i>eErrorStatic</i> | The error statistics structure pointer.                                                     |
| <i>ringId</i>       | The ring index, range from 0 ~ (FSL_FEATURE_ENET_INSTANCE_QUEUEEn(x) - 1).                  |

### 11.8.37 void ENET\_GetStatistics ( ENET\_Type \* *base*, enet\_transfer\_stats\_t \* *statistics* )

Parameters

|                   |                                   |
|-------------------|-----------------------------------|
| <i>base</i>       | ENET peripheral base address.     |
| <i>statistics</i> | The statistics structure pointer. |

### 11.8.38 status\_t ENET\_GetRxFrameSize ( enet\_handle\_t \* *handle*, uint32\_t \* *length*, uint8\_t *ringId* )

This function gets a received frame size from the ENET buffer descriptors.

Note

The FCS of the frame is automatically removed by MAC and the size is the length without the FCS. After calling ENET\_GetRxFrameSize, [ENET\\_ReadFrame\(\)](#) should be called to receive frame and update the BD if the result is not "kStatus\_ENET\_RxFrameEmpty".

Parameters

|               |                                                                                     |
|---------------|-------------------------------------------------------------------------------------|
| <i>handle</i> | The ENET handler structure. This is the same handler pointer used in the ENET_Init. |
| <i>length</i> | The length of the valid frame received.                                             |
| <i>ringId</i> | The ring index or ring number.                                                      |

Return values

|                                   |                                                                                                                                      |
|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| <i>kStatus_ENET_RxFrame-Empty</i> | No frame received. Should not call ENET_ReadFrame to read frame.                                                                     |
| <i>kStatus_ENET_RxFrame-Error</i> | Data error happens. ENET_ReadFrame should be called with NULL data and NULL length to update the receive buffers.                    |
| <i>kStatus_Success</i>            | Receive a frame Successfully then the ENET_ReadFrame should be called with the right data buffer and the captured data length input. |

### 11.8.39 status\_t ENET\_ReadFrame ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, uint8\_t \* *data*, uint32\_t *length*, uint8\_t *ringId*, uint32\_t \* *ts* )

This function reads a frame (both the data and the length) from the ENET buffer descriptors. User can get timestamp through ts pointer if the ts is not NULL.

## Note

It doesn't store the timestamp in the receive timestamp queue. The ENET\_GetRxFrameSize should be used to get the size of the prepared data buffer. This API uses memcpy to copy data from DMA buffer to application buffer, 4 bytes aligned data buffer in 32 bits platforms provided by user may let compiler use optimization instruction to reduce time consumption. This is an example:

```

* uint32_t length;
* enet_handle_t g_handle;
* Comments: Get the received frame size firstly.
* status = ENET_GetRxFrameSize(&g_handle, &length, 0);
* if (length != 0)
* {
* Comments: Allocate memory here with the size of "length"
* uint8_t *data = memory allocate interface;
* if (!data)
* {
* ENET_ReadFrame(ENET, &g_handle, NULL, 0, 0, NULL);
* Comments: Add the console warning log.
* }
* else
* {
* status = ENET_ReadFrame(ENET, &g_handle, data, length, 0, NULL);
* Comments: Call stack input API to deliver the data to stack
* }
* }
* else if (status == kStatus_ENET_RxFrameError)
* {
* Comments: Update the received buffer when a error frame is received.
* ENET_ReadFrame(ENET, &g_handle, NULL, 0, 0, NULL);
* }
*

```

## Parameters

|               |                                                                                                    |
|---------------|----------------------------------------------------------------------------------------------------|
| <i>base</i>   | ENET peripheral base address.                                                                      |
| <i>handle</i> | The ENET handler structure. This is the same handler pointer used in the ENET_Init.                |
| <i>data</i>   | The data buffer provided by user to store the frame which memory size should be at least "length". |
| <i>length</i> | The size of the data buffer which is still the length of the received frame.                       |
| <i>ringId</i> | The ring index or ring number.                                                                     |
| <i>ts</i>     | The timestamp address to store received timestamp.                                                 |

## Returns

The execute status, successful or failure.

#### 11.8.40 status\_t ENET\_SendFrame ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, const uint8\_t \* *data*, uint32\_t *length*, uint8\_t *ringId*, bool *tsFlag*, void \* *context* )

## Note

The CRC is automatically appended to the data. Input the data to send without the CRC. This API uses memcpy to copy data from DMA buffer to application buffer, 4 bytes aligned data buffer in 32 bits platforms provided by user may let compiler use optimization instruction to reduce time consumption.

## Parameters

|                |                                                                                   |
|----------------|-----------------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                                     |
| <i>handle</i>  | The ENET handler pointer. This is the same handler pointer used in the ENET_Init. |
| <i>data</i>    | The data buffer provided by user to send.                                         |
| <i>length</i>  | The length of the data to send.                                                   |
| <i>ringId</i>  | The ring index or ring number.                                                    |
| <i>tsFlag</i>  | Timestamp enable flag.                                                            |
| <i>context</i> | Used by user to handle some events after transmit over.                           |

## Return values

|                                 |                                                                                                                                                                                                                                                   |
|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>kStatus_Success</i>          | Send frame succeed.                                                                                                                                                                                                                               |
| <i>kStatus_ENET_TxFrameBusy</i> | Transmit buffer descriptor is busy under transmission. The transmit busy happens when the data send rate is over the MAC capacity. The waiting mechanism is recommended to be added after each call return with <i>kStatus_ENET_TxFrameBusy</i> . |

### 11.8.41 status\_t ENET\_SetTxReclaim ( enet\_handle\_t \* *handle*, bool *isEnable*, uint8\_t *ringId* )

## Note

This function must be called when no pending send frame action. Set enable if you want to reclaim context or timestamp in interrupt.

## Parameters

|                 |                                                                                   |
|-----------------|-----------------------------------------------------------------------------------|
| <i>handle</i>   | The ENET handler pointer. This is the same handler pointer used in the ENET_Init. |
| <i>isEnable</i> | Enable or disable flag.                                                           |
| <i>ringId</i>   | The ring index or ring number.                                                    |

Return values

|                        |                                       |
|------------------------|---------------------------------------|
| <i>kStatus_Success</i> | Succeed to enable/disable Tx reclaim. |
| <i>kStatus_Fail</i>    | Fail to enable/disable Tx reclaim.    |

### 11.8.42 void ENET\_ReclaimTxDescriptor ( **ENET\_Type** \* *base*, **enet\_handle\_t** \* *handle*, **uint8\_t** *ringId* )

This function is used to update the tx descriptor status and store the tx timestamp when the 1588 feature is enabled. This is called by the transmit interrupt IRQ handler after the complete of a frame transmission.

Parameters

|               |                                                                                   |
|---------------|-----------------------------------------------------------------------------------|
| <i>base</i>   | ENET peripheral base address.                                                     |
| <i>handle</i> | The ENET handler pointer. This is the same handler pointer used in the ENET_Init. |
| <i>ringId</i> | The ring index or ring number.                                                    |

### 11.8.43 **status\_t** ENET\_GetRxFrame ( **ENET\_Type** \* *base*, **enet\_handle\_t** \* *handle*, **enet\_rx\_frame\_struct\_t** \* *rxFrame*, **uint8\_t** *ringId* )

This function uses the user-defined allocation and free callbacks. Every time application gets one frame through this function, driver stores the buffer address(es) in enet\_buffer\_struct\_t and allocate new buffer(s) for the BD(s). If there's no memory buffer in the pool, this function drops current one frame to keep the Rx frame in BD ring is as fresh as possible.

Note

Application must provide a memory pool including at least BD number + n buffers in order for this function to work properly, because each BD must always take one buffer while driver is running, then other extra n buffer(s) can be taken by application. Here n is the ceil(max\_frame\_length(set by RCR) / bd\_rx\_size(set by MRBR)). Application must also provide an array structure in rxFrame->rxBuffArray with n index to receive one complete frame in any case.

Parameters

|                |                                                                                   |
|----------------|-----------------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                                     |
| <i>handle</i>  | The ENET handler pointer. This is the same handler pointer used in the ENET_Init. |
| <i>rxFrame</i> | The received frame information structure provided by user.                        |
| <i>ringId</i>  | The ring index or ring number.                                                    |

Return values

|                                   |                                                                 |
|-----------------------------------|-----------------------------------------------------------------|
| <i>kStatus_Success</i>            | Succeed to get one frame and allocate new memory for Rx buffer. |
| <i>kStatus_ENET_RxFrame-Empty</i> | There's no Rx frame in the BD.                                  |
| <i>kStatus_ENET_RxFrame-Error</i> | There's issue in this receiving.                                |
| <i>kStatus_ENET_RxFrame-Drop</i>  | There's no new buffer memory for BD, drop this frame.           |

#### 11.8.44 status\_t ENET\_StartTxFrame ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, enet\_tx\_frame\_struct\_t \* *txFrame*, uint8\_t *ringId* )

This function supports scattered buffer transmit, user needs to provide the buffer array.

Note

Tx reclaim should be enabled to ensure the Tx buffer ownership can be given back to application after Tx is over.

Parameters

|                |                                                                                   |
|----------------|-----------------------------------------------------------------------------------|
| <i>base</i>    | ENET peripheral base address.                                                     |
| <i>handle</i>  | The ENET handler pointer. This is the same handler pointer used in the ENET_Init. |
| <i>txFrame</i> | The Tx frame structure.                                                           |
| <i>ringId</i>  | The ring index or ring number.                                                    |

Return values

|                                     |                                                                        |
|-------------------------------------|------------------------------------------------------------------------|
| <i>kStatus_Success</i>              | Succeed to send one frame.                                             |
| <i>kStatus_ENET_TxFrame-Busy</i>    | The BD is not ready for Tx or the reclaim operation still not finishs. |
| <i>kStatus_ENET_TxFrame-OverLen</i> | The Tx frame length is over max ethernet frame length.                 |

#### 11.8.45 void ENET\_TransmitIRQHandler ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, uint32\_t *ringId* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ENET peripheral base address. |
| <i>handle</i> | The ENET handler pointer.     |
| <i>ringId</i> | The ring id or ring number.   |

#### 11.8.46 void ENET\_ReceiveIRQHandler ( ENET\_Type \* *base*, enet\_handle\_t \* *handle*, uint32\_t *ringId* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ENET peripheral base address. |
| <i>handle</i> | The ENET handler pointer.     |
| <i>ringId</i> | The ring id or ring number.   |

#### 11.8.47 void ENET\_CommonFrame1IRQHandler ( ENET\_Type \* *base* )

This is used for the combined tx/rx interrupt for multi-ring (frame 1).

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

#### 11.8.48 void ENET\_CommonFrame2IRQHandler ( ENET\_Type \* *base* )

This is used for the combined tx/rx interrupt for multi-ring (frame 2).

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

#### 11.8.49 void ENET\_ErrorIRQHandler ( ENET\_Type \* *base*, enet\_handle\_t \* *handle* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ENET peripheral base address. |
| <i>handle</i> | The ENET handler pointer.     |

### 11.8.50 void ENET\_Ptp1588IRQHandler ( ENET\_Type \* *base* )

This is used for the 1588 timer interrupt.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

### 11.8.51 void ENET\_CommonFrame0IRQHandler ( ENET\_Type \* *base* )

This is used for the combined tx/rx/error interrupt for single/mutli-ring (frame 0).

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ENET peripheral base address. |
|-------------|-------------------------------|

## 11.9 Variable Documentation

### 11.9.1 const clock\_ip\_name\_t s\_enetClock[]

## Chapter 12

# FlexCAN: Flex Controller Area Network Driver

### 12.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Flex Controller Area Network (FlexCAN) module of MCUXpresso SDK devices.

### Modules

- [FlexCAN Driver](#)

## 12.2 FlexCAN Driver

### 12.2.1 Overview

This section describes the programming interface of the FlexCAN driver. The FlexCAN driver configures FlexCAN module and provides functional and transactional interfaces to build the FlexCAN application.

### 12.2.2 Typical use case

#### 12.2.2.1 Message Buffer Send Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/flexcan

#### 12.2.2.2 Message Buffer Receive Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/flexcan

#### 12.2.2.3 Receive FIFO Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/flexcan

## Data Structures

- [`struct \_flexcan\_memory\_error\_report\_status`](#)  
*FlexCAN memory error register status structure.* [More...](#)
- [`struct \_flexcan\_frame`](#)  
*FlexCAN message frame structure.* [More...](#)
- [`struct \_flexcan\_timing\_config`](#)  
*FlexCAN protocol timing characteristic configuration structure.* [More...](#)
- [`struct \_flexcan\_config`](#)  
*FlexCAN module configuration structure.* [More...](#)
- [`struct \_flexcan\_rx\_mb\_config`](#)  
*FlexCAN Receive Message Buffer configuration structure.* [More...](#)
- [`struct \_flexcan\_rx\_fifo\_config`](#)  
*FlexCAN Legacy Rx FIFO configuration structure.* [More...](#)
- [`struct \_flexcan\_mb\_transfer`](#)  
*FlexCAN Message Buffer transfer.* [More...](#)
- [`struct \_flexcan\_fifo\_transfer`](#)  
*FlexCAN Rx FIFO transfer.* [More...](#)
- [`struct \_flexcan\_handle`](#)  
*FlexCAN handle structure.* [More...](#)

## Macros

- #define **FLEXCAN\_ID\_STD**(id) (((uint32\_t)((uint32\_t)(id)) << CAN\_ID\_STD\_SHIFT)) & CAN\_ID\_STD\_MASK)
 

*FlexCAN frame length helper macro.*
- #define **FLEXCAN\_ID\_EXT**(id)
 

*Extend Frame ID helper macro.*
- #define **FLEXCAN\_RX\_MB\_STD\_MASK**(id, rtr, ide)
 

*FlexCAN Rx Message Buffer Mask helper macro.*
- #define **FLEXCAN\_RX\_MB\_EXT\_MASK**(id, rtr, ide)
 

*Extend Rx Message Buffer Mask helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_A**(id, rtr, ide)
 

*FlexCAN Legacy Rx FIFO Mask helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_B\_HIGH**(id, rtr, ide)
 

*Standard Rx FIFO Mask helper macro Type B upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_B\_LOW**(id, rtr, ide)
 

*Standard Rx FIFO Mask helper macro Type B lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_HIGH**(id) (((uint32\_t)(id)&0x7F8) << 21)
 

*Standard Rx FIFO Mask helper macro Type C upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_MID\_HIGH**(id) (((uint32\_t)(id)&0x7F8) << 13)
 

*Standard Rx FIFO Mask helper macro Type C mid-upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_MID\_LOW**(id) (((uint32\_t)(id)&0x7F8) << 5)
 

*Standard Rx FIFO Mask helper macro Type C mid-lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_LOW**(id) (((uint32\_t)(id)&0x7F8) >> 3)
 

*Standard Rx FIFO Mask helper macro Type C lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_A**(id, rtr, ide)
 

*Extend Rx FIFO Mask helper macro Type A helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_B\_HIGH**(id, rtr, ide)
 

*Extend Rx FIFO Mask helper macro Type B upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_B\_LOW**(id, rtr, ide)
 

*Extend Rx FIFO Mask helper macro Type B lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_HIGH**(id) ((**FLEXCAN\_ID\_EXT**(id) & 0x1FE00000) << 3)
 

*Extend Rx FIFO Mask helper macro Type C upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_MID\_HIGH**(id)
 

*Extend Rx FIFO Mask helper macro Type C mid-upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_MID\_LOW**(id)
 

*Extend Rx FIFO Mask helper macro Type C mid-lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_LOW**(id) ((**FLEXCAN\_ID\_EXT**(id) & 0x1FE00000) >> 21)
 

*Extend Rx FIFO Mask helper macro Type C lower part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_A**(id, rtr, ide) **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_A**(id, rtr, ide)
 

*FlexCAN Rx FIFO Filter helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_B\_HIGH**(id, rtr, ide)
 

*Standard Rx FIFO Filter helper macro Type B upper part helper macro.*
- #define **FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_B\_LOW**(id, rtr, ide)

- Standard Rx FIFO Filter helper macro Type B lower part helper macro.
- #define **FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_HIGH**(id)
  - Standard Rx FIFO Filter helper macro Type C upper part helper macro.
- #define **FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_MID\_HIGH**(id)
  - Standard Rx FIFO Filter helper macro Type C mid-upper part helper macro.
- #define **FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_MID\_LOW**(id)
  - Standard Rx FIFO Filter helper macro Type C mid-lower part helper macro.
- #define **FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_LOW**(id)
  - Standard Rx FIFO Filter helper macro Type C lower part helper macro.
- #define **FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_A**(id, rtr, ide) **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_A**(id, rtr, ide)
  - Extend Rx FIFO Filter helper macro Type A helper macro.
- #define **FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_B\_HIGH**(id, rtr, ide)
  - Extend Rx FIFO Filter helper macro Type B upper part helper macro.
- #define **FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_B\_LOW**(id, rtr, ide)
  - Extend Rx FIFO Filter helper macro Type B lower part helper macro.
- #define **FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_HIGH**(id)
  - Extend Rx FIFO Filter helper macro Type C upper part helper macro.
- #define **FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_MID\_HIGH**(id)
  - Extend Rx FIFO Filter helper macro Type C mid-upper part helper macro.
- #define **FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_MID\_LOW**(id)
  - Extend Rx FIFO Filter helper macro Type C mid-lower part helper macro.
- #define **FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_LOW**(id) **FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_LOW**(id)
  - Extend Rx FIFO Filter helper macro Type C lower part helper macro.
- #define **FLEXCAN\_MECR\_INT\_MASK**(x) (((uint64\_t)((uint64\_t)(x)) << 16)) & 0xD00000000-U)
  - FlexCAN interrupt/status flag helper macro.
- #define **FLEXCAN\_MEMORY\_ENHANCED\_RX\_FIFO\_INIT\_FLAG** (0U)
  - FlexCAN Enhanced Rx FIFO base address helper macro.
- #define **FLEXCAN\_CALLBACK**(x) void(x)(CAN\_Type \* base, flexcan\_handle\_t \* handle, status\_t status, uint64\_t result, void \*userData)
  - FlexCAN transfer callback function.

## Typedefs

- typedef enum **\_flexcan\_frame\_format** flexcan\_frame\_format\_t
  - FlexCAN frame format.
- typedef enum **\_flexcan\_frame\_type** flexcan\_frame\_type\_t
  - FlexCAN frame type.
- typedef enum **\_flexcan\_clock\_source** flexcan\_clock\_source\_t
  - FlexCAN clock source.
- typedef enum **\_flexcan\_wake\_up\_source** flexcan\_wake\_up\_source\_t
  - FlexCAN wake up source.
- typedef enum **\_flexcan\_rx\_fifo\_filter\_type** flexcan\_rx\_fifo\_filter\_type\_t
  - FlexCAN Rx Fifo Filter type.
- typedef enum

- [\\_flexcan\\_rx\\_fifo\\_priority flexcan\\_rx\\_fifo\\_priority\\_t](#)  
*FlexCAN Enhanced/Legacy Rx FIFO priority.*
- [typedef enum \\_flexcan\\_memory\\_error\\_type flexcan\\_memory\\_error\\_type\\_t](#)  
*FlexCAN Memory Error Type.*
- [typedef enum \\_flexcan\\_memory\\_access\\_type flexcan\\_memory\\_access\\_type\\_t](#)  
*FlexCAN Memory Access Type.*
- [typedef enum \\_flexcan\\_byte\\_error\\_syndrome flexcan\\_byte\\_error\\_syndrome\\_t](#)  
*FlexCAN Memory Error Byte Syndrome.*
- [typedef struct \\_flexcan\\_memory\\_error\\_report\\_status flexcan\\_memory\\_error\\_report\\_status\\_t](#)  
*FlexCAN memory error register status structure.*
- [typedef struct \\_flexcan\\_frame flexcan\\_frame\\_t](#)  
*FlexCAN message frame structure.*
- [typedef struct \\_flexcan\\_timing\\_config flexcan\\_timing\\_config\\_t](#)  
*FlexCAN protocol timing characteristic configuration structure.*
- [typedef struct \\_flexcan\\_config flexcan\\_config\\_t](#)  
*FlexCAN module configuration structure.*
- [typedef struct \\_flexcan\\_rx\\_mb\\_config flexcan\\_rx\\_mb\\_config\\_t](#)  
*FlexCAN Receive Message Buffer configuration structure.*
- [typedef struct \\_flexcan\\_rx\\_fifo\\_config flexcan\\_rx\\_fifo\\_config\\_t](#)  
*FlexCAN Legacy Rx FIFO configuration structure.*
- [typedef struct \\_flexcan\\_mb\\_transfer flexcan\\_mb\\_transfer\\_t](#)  
*FlexCAN Message Buffer transfer.*
- [typedef struct \\_flexcan\\_fifo\\_transfer flexcan\\_fifo\\_transfer\\_t](#)  
*FlexCAN Rx FIFO transfer.*
- [typedef struct \\_flexcan\\_handle flexcan\\_handle\\_t](#)  
*FlexCAN handle structure definition.*

## Enumerations

- enum {
   
kStatus\_FLEXCAN\_TxBusy = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 0),
   
kStatus\_FLEXCAN\_TxIdle = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 1),
   
kStatus\_FLEXCAN\_TxSwitchToRx,
   
kStatus\_FLEXCAN\_RxBusy = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 3),
   
kStatus\_FLEXCAN\_RxIdle = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 4),
   
kStatus\_FLEXCAN\_RxOverflow = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 5),
   
kStatus\_FLEXCAN\_RxFifoBusy = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 6),
   
kStatus\_FLEXCAN\_RxFifoIdle = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 7),
   
kStatus\_FLEXCAN\_RxFifoOverflow = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 8),
   
kStatus\_FLEXCAN\_RxFifoWarning = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 9),
   
kStatus\_FLEXCAN\_RxFifoDisabled,
   
kStatus\_FLEXCAN\_ErrorStatus = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 11),
   
kStatus\_FLEXCAN\_WakeUp = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 12),
   
kStatus\_FLEXCAN\_UnHandled = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 13),
   
kStatus\_FLEXCAN\_RxRemote = MAKE\_STATUS(kStatusGroup\_FLEXCAN, 14) }
- FlexCAN transfer status.*
- enum \_flexcan\_frame\_format {
   
kFLEXCAN\_FrameFormatStandard = 0x0U,
   
kFLEXCAN\_FrameFormatExtend = 0x1U }
- FlexCAN frame format.*
- enum \_flexcan\_frame\_type {
   
kFLEXCAN\_FrameTypeData = 0x0U,
   
kFLEXCAN\_FrameTypeRemote = 0x1U }
- FlexCAN frame type.*
- enum \_flexcan\_clock\_source {
   
kFLEXCAN\_ClkSrcOsc = 0x0U,
   
kFLEXCAN\_ClkSrcPeri = 0x1U,
   
kFLEXCAN\_ClkSrc0 = 0x0U,
   
kFLEXCAN\_ClkSrc1 = 0x1U }
- FlexCAN clock source.*
- enum \_flexcan\_wake\_up\_source {
   
kFLEXCAN\_WakeupSrcUnfiltered = 0x0U,
   
kFLEXCAN\_WakeupSrcFiltered = 0x1U }
- FlexCAN wake up source.*
- enum \_flexcan\_rx\_fifo\_filter\_type {
   
kFLEXCAN\_RxFifoFilterTypeA = 0x0U,
   
kFLEXCAN\_RxFifoFilterTypeB,
   
kFLEXCAN\_RxFifoFilterTypeC,
   
kFLEXCAN\_RxFifoFilterTypeD = 0x3U }
- FlexCAN Rx Fifo Filter type.*
- enum \_flexcan\_rx\_fifo\_priority {
   
kFLEXCAN\_RxFifoPrioLow = 0x0U,
   
kFLEXCAN\_RxFifoPrioHigh = 0x1U }

*FlexCAN Enhanced/Legacy Rx FIFO priority.*

- enum `_flexcan_interrupt_enable` {
   
    `kFLEXCAN_BusOffInterruptEnable` = CAN\_CTRL1\_BOFFMSK\_MASK,
   
    `kFLEXCAN_ErrorInterruptEnable` = CAN\_CTRL1\_ERRMSK\_MASK,
   
    `kFLEXCAN_TxWarningInterruptEnable` = CAN\_CTRL1\_TWRNMSK\_MASK,
   
    `kFLEXCAN_RxWarningInterruptEnable` = CAN\_CTRL1\_RWRNMSK\_MASK,
   
    `kFLEXCAN_WakeUpInterruptEnable` = CAN\_MCR\_WAKMSK\_MASK,
   
    `kFLEXCAN_HostAccessNCErrorInterruptEnable` = FLEXCAN\_MEGR\_INT\_MASK(CAN\_ME-CR\_HANCEI\_MSK\_MASK),
   
    `kFLEXCAN_FlexCanAccessNCErrorInterruptEnable` = FLEXCAN\_MEGR\_INT\_MASK(CAN\_MECR\_FANCEI\_MSK\_MASK),
   
    `kFLEXCAN_HostOrFlexCanCErrorInterruptEnable` = FLEXCAN\_MEGR\_INT\_MASK(CAN\_ME-CR\_CEI\_MSK\_MASK) }

*FlexCAN interrupt enable enumerations.*

- enum `_flexcan_flags` {
   
    `kFLEXCAN_SynchFlag` = CAN\_ESR1\_SYNCH\_MASK,
   
    `kFLEXCAN_TxWarningIntFlag` = CAN\_ESR1\_TWRNINT\_MASK,
   
    `kFLEXCAN_RxWarningIntFlag` = CAN\_ESR1\_RWRNINT\_MASK,
   
    `kFLEXCAN_IdleFlag` = CAN\_ESR1\_IDLE\_MASK,
   
    `kFLEXCAN_FaultConfinementFlag` = CAN\_ESR1\_FLTCONF\_MASK,
   
    `kFLEXCAN_TransmittingFlag` = CAN\_ESR1\_TX\_MASK,
   
    `kFLEXCAN_ReceivingFlag` = CAN\_ESR1\_RX\_MASK,
   
    `kFLEXCAN_BusOffIntFlag` = CAN\_ESR1\_BOFFINT\_MASK,
   
    `kFLEXCAN_ErrorIntFlag` = CAN\_ESR1\_ERRINT\_MASK,
   
    `kFLEXCAN_WakeUpIntFlag` = CAN\_ESR1\_WAKINT\_MASK ,
   
    `kFLEXCAN_HostAccessNonCorrectableErrorIntFlag` = FLEXCAN\_MEGR\_INT\_MASK(CAN\_ERRSR\_HANCEIF\_MASK),
   
    `kFLEXCAN_FlexCanAccessNonCorrectableErrorIntFlag` = FLEXCAN\_MEGR\_INT\_MASK(CAN\_ERRSR\_FANCEIF\_MASK),
   
    `kFLEXCAN_CorrectableErrorIntFlag` = FLEXCAN\_MEGR\_INT\_MASK(CAN\_ERRSR\_CEIF-MASK),
   
    `kFLEXCAN_HostAccessNonCorrectableErrorOverrunFlag` = FLEXCAN\_MEGR\_INT\_MASK(CAN\_ERRSR\_HANCEIOF\_MASK),
   
    `kFLEXCAN_FlexCanAccessNonCorrectableErrorOverrunFlag` = FLEXCAN\_MEGR\_INT\_MASK(CAN\_ERRSR\_FANCEIOF\_MASK),
   
    `kFLEXCAN_CorrectableErrorOverrunFlag` = FLEXCAN\_MEGR\_INT\_MASK(CAN\_ERRSR\_CEOF\_MASK),
   
    `kFLEXCAN_AllMemoryErrorFlag` }

*FlexCAN status flags.*

- enum `_flexcan_error_flags` {

```
kFLEXCAN_TxErrorWarningFlag = CAN_ESR1_TXWRN_MASK,
kFLEXCAN_RxErrorWarningFlag = CAN_ESR1_RXWRN_MASK,
kFLEXCAN_StuffingError = CAN_ESR1_STFERR_MASK,
kFLEXCAN_FormError = CAN_ESR1_FRMERR_MASK,
kFLEXCAN_CrcError = CAN_ESR1_CRCERR_MASK,
kFLEXCAN_AckError = CAN_ESR1_ACKERR_MASK,
kFLEXCAN_Bit0Error = CAN_ESR1_BIT0ERR_MASK,
kFLEXCAN_Bit1Error = CAN_ESR1_BIT1ERR_MASK }
```

*FlexCAN error status flags.*

- enum {
   
kFLEXCAN\_RxFifoOverflowFlag = CAN\_IFLAG1\_BUFI7I\_MASK,
 kFLEXCAN\_RxFifoWarningFlag = CAN\_IFLAG1\_BUFI6I\_MASK,
 kFLEXCAN\_RxFifoFrameAvlFlag = CAN\_IFLAG1\_BUFI5I\_MASK }

*FlexCAN Legacy Rx FIFO status flags.*

- enum \_flexcan\_memory\_error\_type {
   
kFLEXCAN\_CorrectableError = 0U,
 kFLEXCAN\_NonCorrectableError }
  
- enum \_flexcan\_memory\_access\_type {
   
kFLEXCAN\_MoveOutFlexCanAccess = 0U,
 kFLEXCAN\_MoveInAccess,
 kFLEXCAN\_TxArbitrationAccess,
 kFLEXCAN\_RxMatchingAccess,
 kFLEXCAN\_MoveOutHostAccess }

*FlexCAN Memory Access Type.*

- enum \_flexcan\_byte\_error\_syndrome {
   
kFLEXCAN\_NoError = 0U,
 kFLEXCAN\_ParityBits0Error = 1U,
 kFLEXCAN\_ParityBits1Error = 2U,
 kFLEXCAN\_ParityBits2Error = 4U,
 kFLEXCAN\_ParityBits3Error = 8U,
 kFLEXCAN\_ParityBits4Error = 16U,
 kFLEXCAN\_DataBits0Error = 28U,
 kFLEXCAN\_DataBits1Error = 22U,
 kFLEXCAN\_DataBits2Error = 19U,
 kFLEXCAN\_DataBits3Error = 25U,
 kFLEXCAN\_DataBits4Error = 26U,
 kFLEXCAN\_DataBits5Error = 7U,
 kFLEXCAN\_DataBits6Error = 21U,
 kFLEXCAN\_DataBits7Error = 14U,
 kFLEXCAN\_AllZeroError = 6U,
 kFLEXCAN\_AllOneError = 31U,
 kFLEXCAN\_NonCorrectableErrors }

*FlexCAN Memory Error Byte Syndrome.*

## Driver version

- #define **FSL\_FLEXCAN\_DRIVER\_VERSION** (MAKE\_VERSION(2, 11, 4))  
*FlexCAN driver version.*

## Initialization and deinitialization

- void **FLEXCAN\_EnterFreezeMode** (CAN\_Type \*base)  
*Enter FlexCAN Freeze Mode.*
- void **FLEXCAN\_ExitFreezeMode** (CAN\_Type \*base)  
*Exit FlexCAN Freeze Mode.*
- uint32\_t **FLEXCAN\_GetInstance** (CAN\_Type \*base)  
*Get the FlexCAN instance from peripheral base address.*
- bool **FLEXCAN\_CalculateImprovedTimingValues** (CAN\_Type \*base, uint32\_t bitRate, uint32\_t sourceClock\_Hz, flexcan\_timing\_config\_t \*pTimingConfig)  
*Calculates the improved timing values by specific bit Rates for classical CAN.*
- void **FLEXCAN\_Init** (CAN\_Type \*base, const flexcan\_config\_t \*pConfig, uint32\_t sourceClock\_Hz)  
*Initializes a FlexCAN instance.*
- void **FLEXCAN\_Deinit** (CAN\_Type \*base)  
*De-initializes a FlexCAN instance.*
- void **FLEXCAN\_GetDefaultConfig** (flexcan\_config\_t \*pConfig)  
*Gets the default configuration structure.*

## Configuration.

- void **FLEXCAN\_SetTimingConfig** (CAN\_Type \*base, const flexcan\_timing\_config\_t \*pConfig)  
*Sets the FlexCAN classical CAN protocol timing characteristic.*
- status\_t **FLEXCAN\_SetBitRate** (CAN\_Type \*base, uint32\_t sourceClock\_Hz, uint32\_t bitRate\_Bps)  
*Set bit rate of FlexCAN classical CAN frame or CAN FD frame nominal phase.*
- void **FLEXCAN\_SetRxMbGlobalMask** (CAN\_Type \*base, uint32\_t mask)  
*Sets the FlexCAN receive message buffer global mask.*
- void **FLEXCAN\_SetRxFifoGlobalMask** (CAN\_Type \*base, uint32\_t mask)  
*Sets the FlexCAN receive FIFO global mask.*
- void **FLEXCAN\_SetRxIndividualMask** (CAN\_Type \*base, uint8\_t maskIdx, uint32\_t mask)  
*Sets the FlexCAN receive individual mask.*
- void **FLEXCAN\_SetTxMbConfig** (CAN\_Type \*base, uint8\_t mbIdx, bool enable)  
*Configures a FlexCAN transmit message buffer.*
- void **FLEXCAN\_SetRxMbConfig** (CAN\_Type \*base, uint8\_t mbIdx, const flexcan\_rx\_mb\_config\_t \*pRxMbConfig, bool enable)  
*Configures a FlexCAN Receive Message Buffer.*
- void **FLEXCAN\_SetRxFifoConfig** (CAN\_Type \*base, const flexcan\_rx\_fifo\_config\_t \*pRxFifoConfig, bool enable)  
*Configures the FlexCAN Legacy Rx FIFO.*

## Status

- static uint64\_t **FLEXCAN\_GetStatusFlags** (CAN\_Type \*base)  
*Gets the FlexCAN module interrupt flags.*
- static void **FLEXCAN\_ClearStatusFlags** (CAN\_Type \*base, uint64\_t mask)  
*Clears status flags with the provided mask.*
- static void **FLEXCAN\_GetBusErrCount** (CAN\_Type \*base, uint8\_t \*txErrBuf, uint8\_t \*rxErrBuf)  
*Gets the FlexCAN Bus Error Counter value.*
- static uint64\_t **FLEXCAN\_GetMbStatusFlags** (CAN\_Type \*base, uint64\_t mask)  
*Gets the FlexCAN Message Buffer interrupt flags.*
- static void **FLEXCAN\_ClearMbStatusFlags** (CAN\_Type \*base, uint64\_t mask)  
*Clears the FlexCAN Message Buffer interrupt flags.*
- void **FLEXCAN\_GetMemoryErrorReportStatus** (CAN\_Type \*base, **flexcan\_memory\_error\_report\_status\_t** \*errorStatus)  
*Gets the FlexCAN Memory Error Report registers status.*

## Interrupts

- static void **FLEXCAN\_EnableInterrupts** (CAN\_Type \*base, uint64\_t mask)  
*Enables FlexCAN interrupts according to the provided mask.*
- static void **FLEXCAN\_DisableInterrupts** (CAN\_Type \*base, uint64\_t mask)  
*Disables FlexCAN interrupts according to the provided mask.*
- static void **FLEXCAN\_EnableMbInterrupts** (CAN\_Type \*base, uint64\_t mask)  
*Enables FlexCAN Message Buffer interrupts.*
- static void **FLEXCAN\_DisableMbInterrupts** (CAN\_Type \*base, uint64\_t mask)  
*Disables FlexCAN Message Buffer interrupts.*

## DMA Control

- void **FLEXCAN\_EnableRxFifoDMA** (CAN\_Type \*base, bool enable)  
*Enables or disables the FlexCAN Rx FIFO DMA request.*
- static uintptr\_t **FLEXCAN\_GetRxFifoHeadAddr** (CAN\_Type \*base)  
*Gets the Rx FIFO Head address.*

## Bus Operations

- static void **FLEXCAN\_Enable** (CAN\_Type \*base, bool enable)  
*Enables or disables the FlexCAN module operation.*
- **status\_t FLEXCAN\_WriteTxMb** (CAN\_Type \*base, uint8\_t mbIdx, const **flexcan\_frame\_t** \*pTxFrame)  
*Writes a FlexCAN Message to the Transmit Message Buffer.*
- **status\_t FLEXCAN\_ReadRxMb** (CAN\_Type \*base, uint8\_t mbIdx, **flexcan\_frame\_t** \*pRxFrame)  
*Reads a FlexCAN Message from Receive Message Buffer.*
- **status\_t FLEXCAN\_ReadRxFifo** (CAN\_Type \*base, **flexcan\_frame\_t** \*pRxFrame)  
*Reads a FlexCAN Message from Legacy Rx FIFO.*

## Transactional

- `status_t FLEXCAN_TransferSendBlocking (CAN_Type *base, uint8_t mbIdx, flexcan_frame_t *pTxFrame)`  
*Performs a polling send transaction on the CAN bus.*
- `status_t FLEXCAN_TransferReceiveBlocking (CAN_Type *base, uint8_t mbIdx, flexcan_frame_t *pRxFrame)`  
*Performs a polling receive transaction on the CAN bus.*
- `status_t FLEXCAN_TransferReceiveFifoBlocking (CAN_Type *base, flexcan_frame_t *pRxFrame)`  
*Performs a polling receive transaction from Legacy Rx FIFO on the CAN bus.*
- `void FLEXCAN_TransferCreateHandle (CAN_Type *base, flexcan_handle_t *handle, flexcan_transfer_callback_t callback, void *userData)`  
*Initializes the FlexCAN handle.*
- `status_t FLEXCAN_TransferSendNonBlocking (CAN_Type *base, flexcan_handle_t *handle, flexcan_mb_transfer_t *pMbXfer)`  
*Sends a message using IRQ.*
- `status_t FLEXCAN_TransferReceiveNonBlocking (CAN_Type *base, flexcan_handle_t *handle, flexcan_mb_transfer_t *pMbXfer)`  
*Receives a message using IRQ.*
- `status_t FLEXCAN_TransferReceiveFifoNonBlocking (CAN_Type *base, flexcan_handle_t *handle, flexcan_fifo_transfer_t *pFifoXfer)`  
*Receives a message from Rx FIFO using IRQ.*
- `status_t FLEXCAN_TransferGetReceiveFifoCount (CAN_Type *base, flexcan_handle_t *handle, size_t *count)`  
*Gets the Legacy Rx Fifo transfer status during a interrupt non-blocking receive.*
- `uint32_t FLEXCAN_GetTimeStamp (flexcan_handle_t *handle, uint8_t mbIdx)`  
*Gets the detail index of Mailbox's Timestamp by handle.*
- `void FLEXCAN_TransferAbortSend (CAN_Type *base, flexcan_handle_t *handle, uint8_t mbIdx)`  
*Aborts the interrupt driven message send process.*
- `void FLEXCAN_TransferAbortReceive (CAN_Type *base, flexcan_handle_t *handle, uint8_t mbIdx)`  
*Aborts the interrupt driven message receive process.*
- `void FLEXCAN_TransferAbortReceiveFifo (CAN_Type *base, flexcan_handle_t *handle)`  
*Aborts the interrupt driven message receive from Rx FIFO process.*
- `void FLEXCAN_TransferHandleIRQ (CAN_Type *base, flexcan_handle_t *handle)`  
*FlexCAN IRQ handle function.*

### 12.2.3 Data Structure Documentation

#### 12.2.3.1 struct \_flexcan\_memory\_error\_report\_status

This structure contains the memory access properties that caused a memory error access. It is used as the parameter of `FLEXCAN_GetMemoryErrorReportStatus()` function. And user can use `FLEXCAN_GetMemoryErrorReportStatus` to get the status of the last memory error access.

## Data Fields

- **flexcan\_memory\_error\_type\_t errorType**  
*The type of memory error that giving rise to the report.*
- **flexcan\_memory\_access\_type\_t accessType**  
*The type of memory access that giving rise to the memory error.*
- **uint16\_t accessAddress**  
*The address where memory error detected.*
- **uint32\_t errorData**  
*The raw data word read from memory with error.*
- **bool byteIsRead**  
*The byte n (0~3) was read or not.*

## Field Documentation

- (1) **flexcan\_memory\_error\_type\_t \_flexcan\_memory\_error\_report\_status::errorType**
- (2) **flexcan\_memory\_access\_type\_t \_flexcan\_memory\_error\_report\_status::accessType**
- (3) **uint16\_t \_flexcan\_memory\_error\_report\_status::accessAddress**
- (4) **uint32\_t \_flexcan\_memory\_error\_report\_status::errorData**
- (5) **bool \_flexcan\_memory\_error\_report\_status::byteIsRead**

The type of error and which bit in byte (n) is affected by the error.

### 12.2.3.2 struct \_flexcan\_frame

#### Field Documentation

- (1) `uint32_t _flexcan_frame::timestamp`
- (2) `uint32_t _flexcan_frame::length`
- (3) `uint32_t _flexcan_frame::type`
- (4) `uint32_t _flexcan_frame::format`
- (5) `uint32_t _flexcan_frame::__pad0__`
- (6) `uint32_t _flexcan_frame::idhit`
- (7) `uint32_t _flexcan_frame::id`
- (8) `uint32_t _flexcan_frame::dataWord0`
- (9) `uint32_t _flexcan_frame::dataWord1`
- (10) `uint8_t _flexcan_frame::dataByte3`
- (11) `uint8_t _flexcan_frame::dataByte2`
- (12) `uint8_t _flexcan_frame::dataByte1`
- (13) `uint8_t _flexcan_frame::dataByte0`
- (14) `uint8_t _flexcan_frame::dataByte7`
- (15) `uint8_t _flexcan_frame::dataByte6`
- (16) `uint8_t _flexcan_frame::dataByte5`
- (17) `uint8_t _flexcan_frame::dataByte4`

### 12.2.3.3 struct \_flexcan\_timing\_config

#### Data Fields

- `uint16_t preDivider`  
*Classic CAN or CAN FD nominal phase bit rate prescaler.*
- `uint8_t rJumpwidth`  
*Classic CAN or CAN FD nominal phase Re-sync Jump Width.*
- `uint8_t phaseSeg1`  
*Classic CAN or CAN FD nominal phase Segment 1.*
- `uint8_t phaseSeg2`  
*Classic CAN or CAN FD nominal phase Segment 2.*
- `uint8_t propSeg`

*Classic CAN or CAN FD nominal phase Propagation Segment.*

### Field Documentation

- (1) `uint16_t _flexcan_timing_config::preDivider`
- (2) `uint8_t _flexcan_timing_config::rJumpwidth`
- (3) `uint8_t _flexcan_timing_config::phaseSeg1`
- (4) `uint8_t _flexcan_timing_config::phaseSeg2`
- (5) `uint8_t _flexcan_timing_config::propSeg`

#### 12.2.3.4 struct \_flexcan\_config

**Deprecated** Do not use the baudRate. It has been superceded bitRate

Do not use the baudRateFD. It has been superceded bitRateFD

### Data Fields

- `flexcan_clock_source_t clkSrc`  
*Clock source for FlexCAN Protocol Engine.*
- `flexcan_wake_up_source_t wakeupSrc`  
*Wake up source selection.*
- `uint8_t maxMbNum`  
*The maximum number of Message Buffers used by user.*
- `bool enableLoopBack`  
*Enable or Disable Loop Back Self Test Mode.*
- `bool enableTimerSync`  
*Enable or Disable Timer Synchronization.*
- `bool enableSelfWakeup`  
*Enable or Disable Self Wakeup Mode.*
- `bool enableIndividMask`  
*Enable or Disable Rx Individual Mask and Queue feature.*
- `bool disableSelfReception`  
*Enable or Disable Self Reflection.*
- `bool enableListenOnlyMode`  
*Enable or Disable Listen Only Mode.*
- `bool enableSupervisorMode`  
*Enable or Disable Supervisor Mode, enable this mode will make registers allow only Supervisor access.*
- `bool enableDoze`  
*Enable or Disable Doze Mode.*
- `bool enableMemoryErrorControl`  
*Enable or Disable the memory errors detection and correction mechanism.*
- `bool enableNonCorrectableErrorEnterFreeze`  
*Enable or Disable Non-Correctable Errors In FlexCAN Access Put Device In Freeze Mode.*
- `uint32_t baudRate`  
*FlexCAN bit rate in bps, for classical CAN or CANFD nominal phase.*
- `uint32_t bitRate`

*FlexCAN bit rate in bps, for classical CAN or CANFD nominal phase.*

### Field Documentation

- (1) `uint32_t _flexcan_config::baudRate`
- (2) `uint32_t _flexcan_config::bitRate`
- (3) `flexcan_clock_source_t _flexcan_config::clkSrc`
- (4) `flexcan_wake_up_source_t _flexcan_config::wakeupSrc`
- (5) `uint8_t _flexcan_config::maxMbNum`
- (6) `bool _flexcan_config::enableLoopBack`
- (7) `bool _flexcan_config::enableTimerSync`
- (8) `bool _flexcan_config::enableSelfWakeup`
- (9) `bool _flexcan_config::enableIndividMask`
- (10) `bool _flexcan_config::disableSelfReception`
- (11) `bool _flexcan_config::enableListenOnlyMode`
- (12) `bool _flexcan_config::enableSupervisorMode`
- (13) `bool _flexcan_config::enableDoze`
- (14) `bool _flexcan_config::enableMemoryErrorControl`
- (15) `bool _flexcan_config::enableNonCorrectableErrorEnterFreeze`

#### 12.2.3.5 struct \_flexcan\_rx\_mb\_config

This structure is used as the parameter of [FLEXCAN\\_SetRxMbConfig\(\)](#) function. The [FLEXCAN\\_SetRxMbConfig\(\)](#) function is used to configure FlexCAN Receive Message Buffer. The function abort previous receiving process, clean the Message Buffer and activate the Rx Message Buffer using given Message Buffer setting.

### Data Fields

- `uint32_t id`  
*CAN Message Buffer Frame Identifier, should be set using [FLEXCAN\\_ID\\_EXT\(\)](#) or [FLEXCAN\\_ID\\_STD\(\)](#) macro.*
- `flexcan_frame_format_t format`  
*CAN Frame Identifier format(Standard or Extend).*
- `flexcan_frame_type_t type`  
*CAN Frame Type(Data or Remote).*

**Field Documentation**

- (1) `uint32_t _flexcan_rx_mb_config::id`
- (2) `flexcan_frame_format_t _flexcan_rx_mb_config::format`
- (3) `flexcan_frame_type_t _flexcan_rx_mb_config::type`

**12.2.3.6 struct \_flexcan\_rx\_fifo\_config****Data Fields**

- `uint32_t * idFilterTable`  
*Pointer to the FlexCAN Legacy Rx FIFO identifier filter table.*
- `uint8_t idFilterNum`  
*The FlexCAN Legacy Rx FIFO Filter elements quantity.*
- `flexcan_rx_fifo_filter_type_t idFilterType`  
*The FlexCAN Legacy Rx FIFO Filter type.*
- `flexcan_rx_fifo_priority_t priority`  
*The FlexCAN Legacy Rx FIFO receive priority.*

**Field Documentation**

- (1) `uint32_t* _flexcan_rx_fifo_config::idFilterTable`
- (2) `uint8_t _flexcan_rx_fifo_config::idFilterNum`
- (3) `flexcan_rx_fifo_filter_type_t _flexcan_rx_fifo_config::idFilterType`
- (4) `flexcan_rx_fifo_priority_t _flexcan_rx_fifo_config::priority`

**12.2.3.7 struct \_flexcan\_mb\_transfer****Data Fields**

- `flexcan_frame_t * frame`  
*The buffer of CAN Message to be transfer.*
- `uint8_t mbIdx`  
*The index of Message buffer used to transfer Message.*

**Field Documentation**

- (1) `flexcan_frame_t* _flexcan_mb_transfer::frame`
- (2) `uint8_t _flexcan_mb_transfer::mbIdx`

**12.2.3.8 struct \_flexcan\_fifo\_transfer****Data Fields**

- `flexcan_frame_t * frame`

- **size\_t frameNum**  
*The buffer of CAN Message to be received from Legacy Rx FIFO.*

*Number of CAN Message need to be received from Legacy or Enhanced Rx FIFO.*

## Field Documentation

(1) **flexcan\_frame\_t\* \_flexcan\_fifo\_transfer::frame**

(2) **size\_t \_flexcan\_fifo\_transfer::frameNum**

### 12.2.3.9 struct \_flexcan\_handle

#### Data Fields

- **flexcan\_transfer\_callback\_t callback**  
*Callback function.*
- **void \*userData**  
*FlexCAN callback function parameter.*
- **flexcan\_frame\_t \*volatile mbFrameBuf [CAN\_WORD1\_COUNT]**  
*The buffer for received CAN data from Message Buffers.*
- **flexcan\_frame\_t \*volatile rxFifoFrameBuf**  
*The buffer for received CAN data from Legacy Rx FIFO.*
- **size\_t rxFifoFrameNum**  
*The number of CAN messages remaining to be received from Legacy or Enhanced Rx FIFO.*
- **size\_t rxFifoTransferTotalNum**  
*Total CAN Message number need to be received from Legacy or Enhanced Rx FIFO.*
- **volatile uint8\_t mbState [CAN\_WORD1\_COUNT]**  
*Message Buffer transfer state.*
- **volatile uint8\_t rxFifoState**  
*Rx FIFO transfer state.*
- **volatile uint32\_t timestamp [CAN\_WORD1\_COUNT]**  
*Mailbox transfer timestamp.*

**Field Documentation**

- (1) `flexcan_transfer_callback_t _flexcan_handle::callback`
- (2) `void* _flexcan_handle::userData`
- (3) `flexcan_frame_t* volatile _flexcan_handle::mbFrameBuf[CAN_WORD1_COUNT]`
- (4) `flexcan_frame_t* volatile _flexcan_handle::rxFifoFrameBuf`
- (5) `size_t _flexcan_handle::rxFifoFrameNum`
- (6) `size_t _flexcan_handle::rxFifoTransferTotalNum`
- (7) `volatile uint8_t _flexcan_handle::mbState[CAN_WORD1_COUNT]`
- (8) `volatile uint8_t _flexcan_handle::rxFifoState`
- (9) `volatile uint32_t _flexcan_handle::timestamp[CAN_WORD1_COUNT]`

**12.2.4 Macro Definition Documentation****12.2.4.1 #define FSL\_FLEXCAN\_DRIVER\_VERSION (MAKE\_VERSION(2, 11, 4))****12.2.4.2 #define FLEXCAN\_ID\_STD( *id* ) (((uint32\_t)((uint32\_t)(*id*) << CAN\_ID\_STD\_SHIFT)) & CAN\_ID\_STD\_MASK)**

FlexCAN Frame ID helper macro. Standard Frame ID helper macro.

**12.2.4.3 #define FLEXCAN\_ID\_EXT( *id* )****Value:**

```
((uint32_t)((uint32_t)(id) << CAN_ID_EXT_SHIFT)) & \
(CAN_ID_EXT_MASK | CAN_ID_STD_MASK)
```

**12.2.4.4 #define FLEXCAN\_RX\_MB\_STD\_MASK( *id*, *rtr*, *ide* )****Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
FLEXCAN_ID_STD(id)
```

Standard Rx Message Buffer Mask helper macro.

**12.2.4.5 #define FLEXCAN\_RX\_MB\_EXT\_MASK( id, rtr, ide )****Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
 FLEXCAN_ID_EXT(id))
```

**12.2.4.6 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_A( id, rtr, ide )****Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
 (FLEXCAN_ID_STD(id) << 1))
```

Standard Rx FIFO Mask helper macro Type A helper macro.

**12.2.4.7 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_B\_HIGH( id, rtr, ide )****Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
 ((uint32_t)(id)&0x7FF) << 19))
```

**12.2.4.8 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_B\_LOW( id, rtr, ide )****Value:**

```
((uint32_t)((uint32_t)(rtr) << 15) | (uint32_t)((uint32_t)(ide) << 14)) | \
 ((uint32_t)(id)&0x7FF) << 3))
```

**12.2.4.9 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_HIGH( id ) (((uint32\_t)(id)&0x7F8) << 21)****12.2.4.10 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_MID\_HIGH( id ) (((uint32\_t)(id)&0x7F8) << 13)****12.2.4.11 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_MID\_LOW( id ) (((uint32\_t)(id)&0x7F8) << 5)****12.2.4.12 #define FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_C\_LOW( id ) (((uint32\_t)(id)&0x7F8) >> 3)****12.2.4.13 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_A( id, rtr, ide )****Value:**

```
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
(FLEXCAN_ID_EXT(id) << 1))
```

#### **12.2.4.14 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_B\_HIGH( id, rtr, ide )**

**Value:**

```
(\
((uint32_t)((uint32_t)(rtr) << 31) | (uint32_t)((uint32_t)(ide) << 30)) | \
((FLEXCAN_ID_EXT(id) & 0x1FFF8000) \
<< 1)) \ \
```

#### **12.2.4.15 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_B\_LOW( id, rtr, ide )**

**Value:**

```
((uint32_t)((uint32_t)(rtr) << 15) | (uint32_t)((uint32_t)(ide) << 14)) | \
((FLEXCAN_ID_EXT(id) & 0x1FFF8000) >> \
15)) \
```

#### **12.2.4.16 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_HIGH( id )** **((FLEXCAN\_ID\_EXT(id) & 0x1FE00000) << 3)**

#### **12.2.4.17 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_MID\_HIGH( id )**

**Value:**

```
((FLEXCAN_ID_EXT(id) & 0x1FE00000) >> \
5) \
```

#### **12.2.4.18 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_MID\_LOW( id )**

**Value:**

```
((FLEXCAN_ID_EXT(id) & 0x1FE00000) >> \
13) \
```

#### **12.2.4.19 #define FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_C\_LOW( id )** **((FLEXCAN\_ID\_EXT(id) & 0x1FE00000) >> 21)**

#### **12.2.4.20 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_A( id, rtr, ide )** **FLEXCAN\_RX\_FIFO\_STD\_MASK\_TYPE\_A(id, rtr, ide)**

Standard Rx FIFO Filter helper macro Type A helper macro.

**12.2.4.21 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_B\_HIGH( *id*, *rtr*, *ide* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_B_HIGH(\
 id, rtr, ide)
```

**12.2.4.22 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_B\_LOW( *id*, *rtr*, *ide* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_B_LOW(\
 id, rtr, ide)
```

**12.2.4.23 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_HIGH( *id* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_HIGH(\
 id)
```

**12.2.4.24 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_MID\_HIGH( *id* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_MID_HIGH(\
 id)
```

**12.2.4.25 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_MID\_LOW( *id* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_MID_LOW(\
 id)
```

**12.2.4.26 #define FLEXCAN\_RX\_FIFO\_STD\_FILTER\_TYPE\_C\_LOW( *id* )****Value:**

```
FLEXCAN_RX_FIFO_STD_MASK_TYPE_C_LOW(\
 id)
```

- 12.2.4.27 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_A( *id*, *rtr*, *ide* ) FLEXCAN\_RX\_FIFO\_EXT\_MASK\_TYPE\_A(*id*, *rtr*, *ide*)
- 12.2.4.28 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_B\_HIGH( *id*, *rtr*, *ide* )

**Value:**

```
FLEXCAN_RX_FIFO_EXT_MASK_TYPE_B_HIGH(\
 id, rtr, ide)
```

- 12.2.4.29 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_B\_LOW( *id*, *rtr*, *ide* )

**Value:**

```
FLEXCAN_RX_FIFO_EXT_MASK_TYPE_B_LOW(\
 id, rtr, ide)
```

- 12.2.4.30 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_HIGH( *id* )

**Value:**

```
FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_HIGH(\
 id)
```

- 12.2.4.31 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_MID\_HIGH( *id* )

**Value:**

```
FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_MID_HIGH(\
 id)
```

- 12.2.4.32 #define FLEXCAN\_RX\_FIFO\_EXT\_FILTER\_TYPE\_C\_MID\_LOW( *id* )

**Value:**

```
FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_MID_LOW(\
 id)
```

- 12.2.4.33 `#define FLEXCAN_RX_FIFO_EXT_FILTER_TYPE_C_LOW( id ) FLEXCAN_RX_FIFO_EXT_MASK_TYPE_C_LOW(id)`
- 12.2.4.34 `#define FLEXCAN_MECR_INT_MASK( x ) (((uint64_t)((uint64_t)(x)) << 16)) & 0xD00000000U)`
- 12.2.4.35 `#define FLEXCAN_MEMORY_ENHANCED_RX_FIFO_INIT_FLAG (0U)`
- 12.2.4.36 `#define FLEXCAN_CALLBACK( x ) void(x)(CAN_Type * base, flexcan_handle_t * handle, status_t status, uint64_t result, void *userData)`

The FlexCAN transfer callback returns a value from the underlying layer. If the status equals to kStatus\_FLEXCAN\_ErrorStatus, the result parameter is the Content of FlexCAN status register which can be used to get the working status(or error status) of FlexCAN module. If the status equals to other FlexCAN Message Buffer transfer status, the result is the index of Message Buffer that generate transfer event. If the status equals to other FlexCAN Message Buffer transfer status, the result is meaningless and should be Ignored.

## 12.2.5 Typedef Documentation

12.2.5.1 `typedef enum _flexcan_frame_format flexcan_frame_format_t`

12.2.5.2 `typedef enum _flexcan_frame_type flexcan_frame_type_t`

12.2.5.3 `typedef enum _flexcan_clock_source flexcan_clock_source_t`

**Deprecated** Do not use the kFLEXCAN\_ClkSrcOs. It has been superceded kFLEXCAN\_ClkSrc0

Do not use the kFLEXCAN\_ClkSrcPeri. It has been superceded kFLEXCAN\_ClkSrc1

12.2.5.4 `typedef enum _flexcan_wake_up_source flexcan_wake_up_source_t`

12.2.5.5 `typedef enum _flexcan_rx_fifo_filter_type flexcan_rx_fifo_filter_type_t`

12.2.5.6 `typedef enum _flexcan_rx_fifo_priority flexcan_rx_fifo_priority_t`

The matching process starts from the Rx MB(or Enhanced/Legacy Rx FIFO) with higher priority. If no MB(or Enhanced/Legacy Rx FIFO filter) is satisfied, the matching process goes on with the Enhanced-/Legacy Rx FIFO(or Rx MB) with lower priority.

### **12.2.5.7 `typedef struct _flexcan_memory_error_report_status flexcan_memory_error_report_status_t`**

This structure contains the memory access properties that caused a memory error access. It is used as the parameter of [FLEXCAN\\_GetMemoryErrorReportStatus\(\)](#) function. And user can use FLEXCAN\_GetMemoryErrorReportStatus to get the status of the last memory error access.

### **12.2.5.8 `typedef struct _flexcan_frame flexcan_frame_t`**

### **12.2.5.9 `typedef struct _flexcan_timing_config flexcan_timing_config_t`**

### **12.2.5.10 `typedef struct _flexcan_config flexcan_config_t`**

**Deprecated** Do not use the baudRate. It has been superceded bitRate

Do not use the baudRateFD. It has been superceded bitRateFD

### **12.2.5.11 `typedef struct _flexcan_rx_mb_config flexcan_rx_mb_config_t`**

This structure is used as the parameter of [FLEXCAN\\_SetRxMbConfig\(\)](#) function. The [FLEXCAN\\_SetRxMbConfig\(\)](#) function is used to configure FlexCAN Receive Message Buffer. The function abort previous receiving process, clean the Message Buffer and activate the Rx Message Buffer using given Message Buffer setting.

### **12.2.5.12 `typedef struct _flexcan_rx_fifo_config flexcan_rx_fifo_config_t`**

### **12.2.5.13 `typedef struct _flexcan_mb_transfer flexcan_mb_transfer_t`**

### **12.2.5.14 `typedef struct _flexcan_fifo_transfer flexcan_fifo_transfer_t`**

### **12.2.5.15 `typedef struct _flexcan_handle flexcan_handle_t`**

## **12.2.6 Enumeration Type Documentation**

### **12.2.6.1 anonymous enum**

Enumerator

*kStatus\_FLEXCAN\_TxBusy* Tx Message Buffer is Busy.

*kStatus\_FLEXCAN\_TxIdle* Tx Message Buffer is Idle.

*kStatus\_FLEXCAN\_TxSwitchToRx* Remote Message is send out and Message buffer changed to Receive one.

*kStatus\_FLEXCAN\_RxBusy* Rx Message Buffer is Busy.

*kStatus\_FLEXCAN\_RxIdle* Rx Message Buffer is Idle.  
*kStatus\_FLEXCAN\_RxOverflow* Rx Message Buffer is Overflowed.  
*kStatus\_FLEXCAN\_RxFifoBusy* Rx Message FIFO is Busy.  
*kStatus\_FLEXCAN\_RxFifoIdle* Rx Message FIFO is Idle.  
*kStatus\_FLEXCAN\_RxFifoOverflow* Rx Message FIFO is overflowed.  
*kStatus\_FLEXCAN\_RxFifoWarning* Rx Message FIFO is almost overflowed.  
*kStatus\_FLEXCAN\_RxFifoDisabled* Rx Message FIFO is disabled during reading.  
*kStatus\_FLEXCAN\_ErrorStatus* FlexCAN Module Error and Status.  
*kStatus\_FLEXCAN\_WakeUp* FlexCAN is waken up from STOP mode.  
*kStatus\_FLEXCAN\_UnHandled* UnHadled Interrupt asserted.  
*kStatus\_FLEXCAN\_RxRemote* Rx Remote Message Received in Mail box.

### 12.2.6.2 enum \_flexcan\_frame\_format

Enumerator

*kFLEXCAN\_FrameFormatStandard* Standard frame format attribute.  
*kFLEXCAN\_FrameFormatExtend* Extend frame format attribute.

### 12.2.6.3 enum \_flexcan\_frame\_type

Enumerator

*kFLEXCAN\_FrameTypeData* Data frame type attribute.  
*kFLEXCAN\_FrameTypeRemote* Remote frame type attribute.

### 12.2.6.4 enum \_flexcan\_clock\_source

**Deprecated** Do not use the *kFLEXCAN\_ClkSrcOs*. It has been superceded *kFLEXCAN\_ClkSrc0*  
Do not use the *kFLEXCAN\_ClkSrcPeri*. It has been superceded *kFLEXCAN\_ClkSrc1*

Enumerator

*kFLEXCAN\_ClkSrcOsc* FlexCAN Protocol Engine clock from Oscillator.  
*kFLEXCAN\_ClkSrcPeri* FlexCAN Protocol Engine clock from Peripheral Clock.  
*kFLEXCAN\_ClkSrc0* FlexCAN Protocol Engine clock selected by user as SRC == 0.  
*kFLEXCAN\_ClkSrc1* FlexCAN Protocol Engine clock selected by user as SRC == 1.

### 12.2.6.5 enum \_flexcan\_wake\_up\_source

Enumerator

***kFLEXCAN\_WakeupSrcUnfiltered*** FlexCAN uses unfiltered Rx input to detect edge.

***kFLEXCAN\_WakeupSrcFiltered*** FlexCAN uses filtered Rx input to detect edge.

### 12.2.6.6 enum \_flexcan\_rx\_fifo\_filter\_type

Enumerator

***kFLEXCAN\_RxFifoFilterTypeA*** One full ID (standard and extended) per ID Filter element.

***kFLEXCAN\_RxFifoFilterTypeB*** Two full standard IDs or two partial 14-bit ID slices per ID Filter Table element.

***kFLEXCAN\_RxFifoFilterTypeC*** Four partial 8-bit Standard or extended ID slices per ID Filter Table element.

***kFLEXCAN\_RxFifoFilterTypeD*** All frames rejected.

### 12.2.6.7 enum \_flexcan\_rx\_fifo\_priority

The matching process starts from the Rx MB(or Enhanced/Legacy Rx FIFO) with higher priority. If no MB(or Enhanced/Legacy Rx FIFO filter) is satisfied, the matching process goes on with the Enhanced-/Legacy Rx FIFO(or Rx MB) with lower priority.

Enumerator

***kFLEXCAN\_RxFifoPrioLow*** Matching process start from Rx Message Buffer first.

***kFLEXCAN\_RxFifoPrioHigh*** Matching process start from Enhanced/Legacy Rx FIFO first.

### 12.2.6.8 enum \_flexcan\_interrupt\_enable

This provides constants for the FlexCAN interrupt enable enumerations for use in the FlexCAN functions.

Note

FlexCAN Message Buffers and Legacy Rx FIFO interrupts not included in.

Enumerator

***kFLEXCAN\_BusOffInterruptEnable*** Bus Off interrupt, use bit 15.

***kFLEXCAN\_ErrorInterruptEnable*** CAN Error interrupt, use bit 14.

***kFLEXCAN\_TxWarningInterruptEnable*** Tx Warning interrupt, use bit 11.

***kFLEXCAN\_RxWarningInterruptEnable*** Rx Warning interrupt, use bit 10.

***kFLEXCAN\_WakeUpInterruptEnable*** Self Wake Up interrupt, use bit 26.

***kFLEXCAN\_HostAccessNCErrorInterruptEnable*** Host Access With Non-Correctable Errors interrupt, use high word bit 0.

***kFLEXCAN\_FlexCanAccessNCErrorInterruptEnable*** FlexCAN Access With Non-Correctable Errors interrupt, use high word bit 2.

***kFLEXCAN\_HostOrFlexCanCErrorInterruptEnable*** Host or FlexCAN Access With Correctable Errors interrupt, use high word bit 3.

### 12.2.6.9 enum \_flexcan\_flags

This provides constants for the FlexCAN status flags for use in the FlexCAN functions.

#### Note

The CPU read action clears the bits corresponding to the FLEXCAN\_ErrorFlag macro, therefore user need to read status flags and distinguish which error is occur using [\\_flexcan\\_error\\_flags](#) enumerations.

#### Enumerator

***kFLEXCAN\_SynchFlag*** CAN Synchronization Status.

***kFLEXCAN\_TxWarningIntFlag*** Tx Warning Interrupt Flag.

***kFLEXCAN\_RxWarningIntFlag*** Rx Warning Interrupt Flag.

***kFLEXCAN\_IdleFlag*** FlexCAN In IDLE Status.

***kFLEXCAN\_FaultConfinementFlag*** FlexCAN Fault Confinement State.

***kFLEXCAN\_TransmittingFlag*** FlexCAN In Transmission Status.

***kFLEXCAN\_ReceivingFlag*** FlexCAN In Reception Status.

***kFLEXCAN\_BusOffIntFlag*** Bus Off Interrupt Flag.

***kFLEXCAN\_ErrorIntFlag*** CAN Error Interrupt Flag.

***kFLEXCAN\_WakeUpIntFlag*** Self Wake-Up Interrupt Flag.

***kFLEXCAN\_HostAccessNonCorrectableErrorIntFlag*** Host Access With Non-Correctable Error Interrupt Flag.

***kFLEXCAN\_FlexCanAccessNonCorrectableErrorIntFlag*** FlexCAN Access With Non-Correctable Error Interrupt Flag.

***kFLEXCAN\_CorrectableErrorIntFlag*** Correctable Error Interrupt Flag.

***kFLEXCAN\_HostAccessNonCorrectableErrorOverrunFlag*** Host Access With Non-Correctable Error Interrupt Overrun Flag.

***kFLEXCAN\_FlexCanAccessNonCorrectableErrorOverrunFlag*** FlexCAN Access With Non-Correctable Error Interrupt Overrun Flag.

***kFLEXCAN\_CorrectableErrorOverrunFlag*** Correctable Error Interrupt Overrun Flag.

***kFLEXCAN\_AllMemoryErrorFlag*** All Memory Error Flags.

### 12.2.6.10 enum \_flexcan\_error\_flags

The FlexCAN Error Status enumerations is used to report current error of the FlexCAN bus. This enumerations should be used with KFLEXCAN\_ErrorFlag in [\\_flexcan\\_flags](#) enumerations to determine which error is generated.

Enumerator

- kFLEXCAN\_TxErrorWarningFlag*** Tx Error Warning Status.
- kFLEXCAN\_RxErrorWarningFlag*** Rx Error Warning Status.
- kFLEXCAN\_StuffingError*** Stuffing Error.
- kFLEXCAN\_FormError*** Form Error.
- kFLEXCAN\_CrcError*** Cyclic Redundancy Check Error.
- kFLEXCAN\_AckError*** Received no ACK on transmission.
- kFLEXCAN\_Bit0Error*** Unable to send dominant bit.
- kFLEXCAN\_Bit1Error*** Unable to send recessive bit.

### 12.2.6.11 anonymous enum

The FlexCAN Legacy Rx FIFO Status enumerations are used to determine the status of the Rx FIFO. Because Rx FIFO occupy the MB0 ~ MB7 (Rx Fifo filter also occupies more Message Buffer space), Rx FIFO status flags are mapped to the corresponding Message Buffer status flags.

Enumerator

- kFLEXCAN\_RxFifoOverflowFlag*** Rx FIFO overflow flag.
- kFLEXCAN\_RxFifoWarningFlag*** Rx FIFO almost full flag.
- kFLEXCAN\_RxFifoFrameAvlFlag*** Frames available in Rx FIFO flag.

### 12.2.6.12 enum \_flexcan\_memory\_error\_type

Enumerator

- kFLEXCAN\_CorrectableError*** The memory error is correctable which means on bit error.
- kFLEXCAN\_NonCorrectableError*** The memory error is non-correctable which means two bit errors.

### 12.2.6.13 enum \_flexcan\_memory\_access\_type

Enumerator

- kFLEXCAN\_MoveOutFlexCanAccess*** The memory error was detected during move-out FlexCAN access.
- kFLEXCAN\_MoveInAccess*** The memory error was detected during move-in FlexCAN access.

***kFLEXCAN\_TxArbitrationAccess*** The memory error was detected during Tx Arbitration FlexCAN access.

***kFLEXCAN\_RxMatchingAccess*** The memory error was detected during Rx Matching FlexCAN access.

***kFLEXCAN\_MoveOutHostAccess*** The memory error was detected during Rx Matching Host (CPU) access.

#### 12.2.6.14 enum \_flexcan\_byte\_error\_syndrome

Enumerator

***kFLEXCAN\_NoError*** No bit error in this byte.

***kFLEXCAN\_ParityBits0Error*** Parity bit 0 error in this byte.

***kFLEXCAN\_ParityBits1Error*** Parity bit 1 error in this byte.

***kFLEXCAN\_ParityBits2Error*** Parity bit 2 error in this byte.

***kFLEXCAN\_ParityBits3Error*** Parity bit 3 error in this byte.

***kFLEXCAN\_ParityBits4Error*** Parity bit 4 error in this byte.

***kFLEXCAN\_DataBits0Error*** Data bit 0 error in this byte.

***kFLEXCAN\_DataBits1Error*** Data bit 1 error in this byte.

***kFLEXCAN\_DataBits2Error*** Data bit 2 error in this byte.

***kFLEXCAN\_DataBits3Error*** Data bit 3 error in this byte.

***kFLEXCAN\_DataBits4Error*** Data bit 4 error in this byte.

***kFLEXCAN\_DataBits5Error*** Data bit 5 error in this byte.

***kFLEXCAN\_DataBits6Error*** Data bit 6 error in this byte.

***kFLEXCAN\_DataBits7Error*** Data bit 7 error in this byte.

***kFLEXCAN\_AllZeroError*** All-zeros non-correctable error in this byte.

***kFLEXCAN\_AllOneError*** All-ones non-correctable error in this byte.

***kFLEXCAN\_NonCorrectableErrors*** Non-correctable error in this byte.

#### 12.2.7 Function Documentation

##### 12.2.7.1 void FLEXCAN\_EnterFreezeMode ( CAN\_Type \* *base* )

This function makes the FlexCAN work under Freeze Mode.

Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | FlexCAN peripheral base address. |
|-------------|----------------------------------|

##### 12.2.7.2 void FLEXCAN\_ExitFreezeMode ( CAN\_Type \* *base* )

This function makes the FlexCAN leave Freeze Mode.

Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | FlexCAN peripheral base address. |
|-------------|----------------------------------|

### 12.2.7.3 **uint32\_t FLEXCAN\_GetInstance ( CAN\_Type \* *base* )**

Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | FlexCAN peripheral base address. |
|-------------|----------------------------------|

Returns

FlexCAN instance.

### 12.2.7.4 **bool FLEXCAN\_CalculateImprovedTimingValues ( CAN\_Type \* *base*, uint32\_t *bitRate*, uint32\_t *sourceClock\_Hz*, flexcan\_timing\_config\_t \* *pTimingConfig* )**

This function use to calculates the Classical CAN timing values according to the given bit rate. The Calculated timing values will be set in CTRL1/CBT/ENCBT register. The calculation is based on the recommendation of the CiA 301 v4.2.0 and previous version document.

Parameters

|                       |                                                                                         |
|-----------------------|-----------------------------------------------------------------------------------------|
| <i>base</i>           | FlexCAN peripheral base address.                                                        |
| <i>bitRate</i>        | The classical CAN speed in bps defined by user, should be less than or equal to 1-Mbps. |
| <i>sourceClock_Hz</i> | The Source clock frequency in Hz.                                                       |
| <i>pTimingConfig</i>  | Pointer to the FlexCAN timing configuration structure.                                  |

Returns

TRUE if timing configuration found, FALSE if failed to find configuration.

### 12.2.7.5 **void FLEXCAN\_Init ( CAN\_Type \* *base*, const flexcan\_config\_t \* *pConfig*, uint32\_t *sourceClock\_Hz* )**

This function initializes the FlexCAN module with user-defined settings. This example shows how to set up the flexcan\_config\_t parameters and how to call the FLEXCAN\_Init function by passing in these parameters.

```

* flexcan_config_t flexcanConfig;
* flexcanConfig.clkSrc = kFLEXCAN_ClkSrc0;
* flexcanConfig.bitRate = 1000000U;
* flexcanConfig.maxMbNum = 16;
* flexcanConfig.enableLoopBack = false;
* flexcanConfig.enableSelfWakeup = false;
* flexcanConfig.enableIndividMask = false;
* flexcanConfig.enableDoze = false;
* flexcanConfig.disableSelfReception = false;
* flexcanConfig.enableListenOnlyMode = false;
* flexcanConfig.timingConfig = timingConfig;
* FLEXCAN_Init(CAN0, &flexcanConfig, 40000000UL);
*

```

#### Parameters

|                       |                                                       |
|-----------------------|-------------------------------------------------------|
| <i>base</i>           | FlexCAN peripheral base address.                      |
| <i>pConfig</i>        | Pointer to the user-defined configuration structure.  |
| <i>sourceClock_Hz</i> | FlexCAN Protocol Engine clock source frequency in Hz. |

#### 12.2.7.6 void FLEXCAN\_Deinit ( CAN\_Type \* *base* )

This function disables the FlexCAN module clock and sets all register values to the reset value.

#### Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | FlexCAN peripheral base address. |
|-------------|----------------------------------|

#### 12.2.7.7 void FLEXCAN\_GetDefaultConfig ( flexcan\_config\_t \* *pConfig* )

This function initializes the FlexCAN configuration structure to default values. The default values are as follows. *flexcanConfig->clkSrc* = *kFLEXCAN\_ClkSrc0*; *flexcanConfig->bitRate* = *1000000U*; *flexcanConfig->bitRateFD* = *2000000U*; *flexcanConfig->maxMbNum* = *16*; *flexcanConfig->enableLoopBack* = *false*; *flexcanConfig->enableSelfWakeup* = *false*; *flexcanConfig->enableIndividMask* = *false*; *flexcanConfig->disableSelfReception* = *false*; *flexcanConfig->enableListenOnlyMode* = *false*; *flexcanConfig->enableDoze* = *false*; *flexcanConfig->enableMemoryErrorControl* = *true*; *flexcanConfig->enableNonCorrectableErrorEnterFreeze* = *true*; *flexcanConfig.timingConfig* = *timingConfig*;

#### Parameters

|                |                                                 |
|----------------|-------------------------------------------------|
| <i>pConfig</i> | Pointer to the FlexCAN configuration structure. |
|----------------|-------------------------------------------------|

### 12.2.7.8 void FLEXCAN\_SetTimingConfig ( CAN\_Type \* *base*, const flexcan\_timing\_config\_t \* *pConfig* )

This function gives user settings to classical CAN or CAN FD nominal phase timing characteristic. The function is for an experienced user. For less experienced users, call the [FLEXCAN\\_SetBitRate\(\)](#) instead.

Note

Calling [FLEXCAN\\_SetTimingConfig\(\)](#) overrides the bit rate set in [FLEXCAN\\_Init\(\)](#) or [FLEXCAN\\_SetBitRate\(\)](#).

Parameters

|                |                                                |
|----------------|------------------------------------------------|
| <i>base</i>    | FlexCAN peripheral base address.               |
| <i>pConfig</i> | Pointer to the timing configuration structure. |

### 12.2.7.9 status\_t FLEXCAN\_SetBitRate ( CAN\_Type \* *base*, uint32\_t *sourceClock\_Hz*, uint32\_t *bitRate\_Bps* )

This function set the bit rate of classical CAN frame or CAN FD frame nominal phase base on [FLEXCAN\\_CalculateImprovedTimingValues\(\)](#) API calculated timing values.

Note

Calling [FLEXCAN\\_SetBitRate\(\)](#) overrides the bit rate set in [FLEXCAN\\_Init\(\)](#).

Parameters

|                       |                                  |
|-----------------------|----------------------------------|
| <i>base</i>           | FlexCAN peripheral base address. |
| <i>sourceClock_Hz</i> | Source Clock in Hz.              |
| <i>bitRate_Bps</i>    | Bit rate in Bps.                 |

Returns

kStatus\_Success - Set CAN baud rate (only Nominal phase) successfully.

### 12.2.7.10 void FLEXCAN\_SetRxMbGlobalMask ( CAN\_Type \* *base*, uint32\_t *mask* )

This function sets the global mask for the FlexCAN message buffer in a matching process. The configuration is only effective when the Rx individual mask is disabled in the [FLEXCAN\\_Init\(\)](#).

Parameters

|             |                                      |
|-------------|--------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.     |
| <i>mask</i> | Rx Message Buffer Global Mask value. |

#### 12.2.7.11 void FLEXCAN\_SetRx\_fifoGlobalMask ( CAN\_Type \* *base*, uint32\_t *mask* )

This function sets the global mask for FlexCAN FIFO in a matching process.

Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | FlexCAN peripheral base address. |
| <i>mask</i> | Rx Fifo Global Mask value.       |

#### 12.2.7.12 void FLEXCAN\_SetRxIndividualMask ( CAN\_Type \* *base*, uint8\_t *maskIdx*, uint32\_t *mask* )

This function sets the individual mask for the FlexCAN matching process. The configuration is only effective when the Rx individual mask is enabled in the [FLEXCAN\\_Init\(\)](#). If the Rx FIFO is disabled, the individual mask is applied to the corresponding Message Buffer. If the Rx FIFO is enabled, the individual mask for Rx FIFO occupied Message Buffer is applied to the Rx Filter with the same index. Note that only the first 32 individual masks can be used as the Rx FIFO filter mask.

Parameters

|                |                                  |
|----------------|----------------------------------|
| <i>base</i>    | FlexCAN peripheral base address. |
| <i>maskIdx</i> | The Index of individual Mask.    |
| <i>mask</i>    | Rx Individual Mask value.        |

#### 12.2.7.13 void FLEXCAN\_SetTxMbConfig ( CAN\_Type \* *base*, uint8\_t *mbIdx*, bool *enable* )

This function aborts the previous transmission, cleans the Message Buffer, and configures it as a Transmit Message Buffer.

Parameters

|               |                                                                                                                                                                 |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.                                                                                                                                |
| <i>mbIdx</i>  | The Message Buffer index.                                                                                                                                       |
| <i>enable</i> | Enable/disable Tx Message Buffer. <ul style="list-style-type: none"><li>• true: Enable Tx Message Buffer.</li><li>• false: Disable Tx Message Buffer.</li></ul> |

#### 12.2.7.14 void FLEXCAN\_SetRxMbConfig ( CAN\_Type \* *base*, uint8\_t *mbIdx*, const flexcan\_rx\_mb\_config\_t \* *pRxMbConfig*, bool *enable* )

This function cleans a FlexCAN build-in Message Buffer and configures it as a Receive Message Buffer.

Parameters

|                    |                                                                                                                                                                 |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>        | FlexCAN peripheral base address.                                                                                                                                |
| <i>mbIdx</i>       | The Message Buffer index.                                                                                                                                       |
| <i>pRxMbConfig</i> | Pointer to the FlexCAN Message Buffer configuration structure.                                                                                                  |
| <i>enable</i>      | Enable/disable Rx Message Buffer. <ul style="list-style-type: none"><li>• true: Enable Rx Message Buffer.</li><li>• false: Disable Rx Message Buffer.</li></ul> |

#### 12.2.7.15 void FLEXCAN\_SetRxFifoConfig ( CAN\_Type \* *base*, const flexcan\_rx\_fifo\_config\_t \* *pRxFifoConfig*, bool *enable* )

This function configures the FlexCAN Rx FIFO with given configuration.

Note

Legacy Rx FIFO only can receive classic CAN message.

Parameters

|                      |                                                                                                            |
|----------------------|------------------------------------------------------------------------------------------------------------|
| <i>base</i>          | FlexCAN peripheral base address.                                                                           |
| <i>pRxFifoConfig</i> | Pointer to the FlexCAN Legacy Rx FIFO configuration structure. Can be NULL when enable parameter is false. |

|               |                                                                                                                                                           |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>enable</i> | Enable/disable Legacy Rx FIFO. <ul style="list-style-type: none"> <li>• true: Enable Legacy Rx FIFO.</li> <li>• false: Disable Legacy Rx FIFO.</li> </ul> |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|

### 12.2.7.16 static uint64\_t FLEXCAN\_GetStatusFlags ( CAN\_Type \* *base* ) [inline], [static]

This function gets all FlexCAN status flags. The flags are returned as the logical OR value of the enumerators [\\_flexcan\\_flags](#). To check the specific status, compare the return value with enumerators in [\\_flexcan\\_flags](#).

Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | FlexCAN peripheral base address. |
|-------------|----------------------------------|

Returns

FlexCAN status flags which are ORed by the enumerators in the [\\_flexcan\\_flags](#).

### 12.2.7.17 static void FLEXCAN\_ClearStatusFlags ( CAN\_Type \* *base*, uint64\_t *mask* ) [inline], [static]

This function clears the FlexCAN status flags with a provided mask. An automatically cleared flag can't be cleared by this function.

Parameters

|             |                                                                                            |
|-------------|--------------------------------------------------------------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.                                                           |
| <i>mask</i> | The status flags to be cleared, it is logical OR value of <a href="#">_flexcan_flags</a> . |

### 12.2.7.18 static void FLEXCAN\_GetBusErrCount ( CAN\_Type \* *base*, uint8\_t \* *txErrBuf*, uint8\_t \* *rxErrBuf* ) [inline], [static]

This function gets the FlexCAN Bus Error Counter value for both Tx and Rx direction. These values may be needed in the upper layer error handling.

Parameters

|                 |                                         |
|-----------------|-----------------------------------------|
| <i>base</i>     | FlexCAN peripheral base address.        |
| <i>txErrBuf</i> | Buffer to store Tx Error Counter value. |
| <i>rxErrBuf</i> | Buffer to store Rx Error Counter value. |

#### 12.2.7.19 static uint64\_t FLEXCAN\_GetMbStatusFlags ( CAN\_Type \* *base*, uint64\_t *mask* ) [inline], [static]

This function gets the interrupt flags of a given Message Buffers.

Parameters

|             |                                       |
|-------------|---------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.      |
| <i>mask</i> | The ORed FlexCAN Message Buffer mask. |

Returns

The status of given Message Buffers.

#### 12.2.7.20 static void FLEXCAN\_ClearMbStatusFlags ( CAN\_Type \* *base*, uint64\_t *mask* ) [inline], [static]

This function clears the interrupt flags of a given Message Buffers.

Parameters

|             |                                       |
|-------------|---------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.      |
| <i>mask</i> | The ORed FlexCAN Message Buffer mask. |

#### 12.2.7.21 void FLEXCAN\_GetMemoryErrorReportStatus ( CAN\_Type \* *base*, flexcan\_memory\_error\_report\_status\_t \* *errorStatus* )

This function gets the FlexCAN Memory Error Report registers status.

Parameters

|                    |                                                                    |
|--------------------|--------------------------------------------------------------------|
| <i>base</i>        | FlexCAN peripheral base address.                                   |
| <i>errorStatus</i> | Pointer to FlexCAN Memory Error Report registers status structure. |

**12.2.7.22 static void FLEXCAN\_EnableInterrupts ( CAN\_Type \* *base*, uint64\_t *mask* )  
[inline], [static]**

This function enables the FlexCAN interrupts according to the provided mask. The mask is a logical OR of enumeration members, see [\\_flexcan\\_interrupt\\_enable](#).

Parameters

|             |                                                                                     |
|-------------|-------------------------------------------------------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.                                                    |
| <i>mask</i> | The interrupts to enable. Logical OR of <a href="#">_flexcan_interrupt_enable</a> . |

### 12.2.7.23 static void FLEXCAN\_DisableInterrupts ( CAN\_Type \* *base*, uint64\_t *mask* ) [inline], [static]

This function disables the FlexCAN interrupts according to the provided mask. The mask is a logical OR of enumeration members, see [\\_flexcan\\_interrupt\\_enable](#).

Parameters

|             |                                                                                      |
|-------------|--------------------------------------------------------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.                                                     |
| <i>mask</i> | The interrupts to disable. Logical OR of <a href="#">_flexcan_interrupt_enable</a> . |

### 12.2.7.24 static void FLEXCAN\_EnableMbInterrupts ( CAN\_Type \* *base*, uint64\_t *mask* ) [inline], [static]

This function enables the interrupts of given Message Buffers.

Parameters

|             |                                       |
|-------------|---------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.      |
| <i>mask</i> | The ORed FlexCAN Message Buffer mask. |

### 12.2.7.25 static void FLEXCAN\_DisableMbInterrupts ( CAN\_Type \* *base*, uint64\_t *mask* ) [inline], [static]

This function disables the interrupts of given Message Buffers.

Parameters

|             |                                       |
|-------------|---------------------------------------|
| <i>base</i> | FlexCAN peripheral base address.      |
| <i>mask</i> | The ORed FlexCAN Message Buffer mask. |

### 12.2.7.26 void FLEXCAN\_EnableRxFifoDMA ( CAN\_Type \* *base*, bool *enable* )

This function enables or disables the DMA feature of FlexCAN build-in Rx FIFO.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.  |
| <i>enable</i> | true to enable, false to disable. |

### 12.2.7.27 static uintptr\_t FLEXCAN\_GetRxFifoHeadAddr ( CAN\_Type \* *base* ) [inline], [static]

This function returns the FlexCAN Rx FIFO Head address, which is mainly used for the DMA/eDMA use case.

Parameters

|             |                                  |
|-------------|----------------------------------|
| <i>base</i> | FlexCAN peripheral base address. |
|-------------|----------------------------------|

Returns

FlexCAN Rx FIFO Head address.

### 12.2.7.28 static void FLEXCAN\_Enable ( CAN\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the FlexCAN module.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | FlexCAN base pointer.             |
| <i>enable</i> | true to enable, false to disable. |

### 12.2.7.29 status\_t FLEXCAN\_WriteTxMb ( CAN\_Type \* *base*, uint8\_t *mbIdx*, const flexcan\_frame\_t \* *pTxFrame* )

This function writes a CAN Message to the specified Transmit Message Buffer and changes the Message Buffer state to start CAN Message transmit. After that the function returns immediately.

Parameters

|                 |                                          |
|-----------------|------------------------------------------|
| <i>base</i>     | FlexCAN peripheral base address.         |
| <i>mbIdx</i>    | The FlexCAN Message Buffer index.        |
| <i>pTxFrame</i> | Pointer to CAN message frame to be sent. |

Return values

|                        |                                          |
|------------------------|------------------------------------------|
| <i>kStatus_Success</i> | - Write Tx Message Buffer Successfully.  |
| <i>kStatus_Fail</i>    | - Tx Message Buffer is currently in use. |

### 12.2.7.30 status\_t FLEXCAN\_ReadRxMb ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_frame\_t \* *pRxFrame* )

This function reads a CAN message from a specified Receive Message Buffer. The function fills a receive CAN message frame structure with just received data and activates the Message Buffer again. The function returns immediately.

Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>base</i>     | FlexCAN peripheral base address.                      |
| <i>mbIdx</i>    | The FlexCAN Message Buffer index.                     |
| <i>pRxFrame</i> | Pointer to CAN message frame structure for reception. |

Return values

|                                    |                                                                           |
|------------------------------------|---------------------------------------------------------------------------|
| <i>kStatus_Success</i>             | - Rx Message Buffer is full and has been read successfully.               |
| <i>kStatus_FLEXCAN_Rx-Overflow</i> | - Rx Message Buffer is already overflowed and has been read successfully. |
| <i>kStatus_Fail</i>                | - Rx Message Buffer is empty.                                             |

### 12.2.7.31 status\_t FLEXCAN\_ReadRxFifo ( CAN\_Type \* *base*, flexcan\_frame\_t \* *pRxFrame* )

This function reads a CAN message from the FlexCAN Legacy Rx FIFO.

Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>base</i>     | FlexCAN peripheral base address.                      |
| <i>pRxFrame</i> | Pointer to CAN message frame structure for reception. |

Return values

|                        |                                           |
|------------------------|-------------------------------------------|
| <i>kStatus_Success</i> | - Read Message from Rx FIFO successfully. |
| <i>kStatus_Fail</i>    | - Rx FIFO is not enabled.                 |

### 12.2.7.32 status\_t FLEXCAN\_TransferSendBlocking ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_frame\_t \* *pTxFrame* )

Note

A transfer handle does not need to be created before calling this API.

Parameters

|                 |                                          |
|-----------------|------------------------------------------|
| <i>base</i>     | FlexCAN peripheral base pointer.         |
| <i>mbIdx</i>    | The FlexCAN Message Buffer index.        |
| <i>pTxFrame</i> | Pointer to CAN message frame to be sent. |

Return values

|                        |                                          |
|------------------------|------------------------------------------|
| <i>kStatus_Success</i> | - Write Tx Message Buffer Successfully.  |
| <i>kStatus_Fail</i>    | - Tx Message Buffer is currently in use. |

### 12.2.7.33 status\_t FLEXCAN\_TransferReceiveBlocking ( CAN\_Type \* *base*, uint8\_t *mbIdx*, flexcan\_frame\_t \* *pRxFrame* )

Note

A transfer handle does not need to be created before calling this API.

Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>base</i>     | FlexCAN peripheral base pointer.                      |
| <i>mbIdx</i>    | The FlexCAN Message Buffer index.                     |
| <i>pRxFrame</i> | Pointer to CAN message frame structure for reception. |

Return values

|                                    |                                                                           |
|------------------------------------|---------------------------------------------------------------------------|
| <i>kStatus_Success</i>             | - Rx Message Buffer is full and has been read successfully.               |
| <i>kStatus_FLEXCAN_Rx-Overflow</i> | - Rx Message Buffer is already overflowed and has been read successfully. |
| <i>kStatus_Fail</i>                | - Rx Message Buffer is empty.                                             |

### 12.2.7.34 status\_t FLEXCAN\_TransferReceiveFifoBlocking ( CAN\_Type \* *base*, flexcan\_frame\_t \* *pRxFrame* )

## Note

A transfer handle does not need to be created before calling this API.

## Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>base</i>     | FlexCAN peripheral base pointer.                      |
| <i>pRxFrame</i> | Pointer to CAN message frame structure for reception. |

## Return values

|                        |                                           |
|------------------------|-------------------------------------------|
| <i>kStatus_Success</i> | - Read Message from Rx FIFO successfully. |
| <i>kStatus_Fail</i>    | - Rx FIFO is not enabled.                 |

### 12.2.7.35 void FLEXCAN\_TransferCreateHandle ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the FlexCAN handle, which can be used for other FlexCAN transactional APIs. Usually, for a specified FlexCAN instance, call this API once to get the initialized handle.

## Parameters

|                 |                                         |
|-----------------|-----------------------------------------|
| <i>base</i>     | FlexCAN peripheral base address.        |
| <i>handle</i>   | FlexCAN handle pointer.                 |
| <i>callback</i> | The callback function.                  |
| <i>userData</i> | The parameter of the callback function. |

### 12.2.7.36 status\_t FLEXCAN\_TransferSendNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_mb\_transfer\_t \* *pMbXfer* )

This function sends a message using IRQ. This is a non-blocking function, which returns right away. When messages have been sent out, the send callback function is called.

## Parameters

|                |                                                                                            |
|----------------|--------------------------------------------------------------------------------------------|
| <i>base</i>    | FlexCAN peripheral base address.                                                           |
| <i>handle</i>  | FlexCAN handle pointer.                                                                    |
| <i>pMbXfer</i> | FlexCAN Message Buffer transfer structure. See the <a href="#">flexcan_mb_transfer_t</a> . |

Return values

|                                |                                                       |
|--------------------------------|-------------------------------------------------------|
| <i>kStatus_Success</i>         | Start Tx Message Buffer sending process successfully. |
| <i>kStatus_Fail</i>            | Write Tx Message Buffer failed.                       |
| <i>kStatus_FLEXCAN_Tx-Busy</i> | Tx Message Buffer is in use.                          |

#### 12.2.7.37 status\_t FLEXCAN\_TransferReceiveNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_mb\_transfer\_t \* *pMbXfer* )

This function receives a message using IRQ. This is non-blocking function, which returns right away. When the message has been received, the receive callback function is called.

Parameters

|                |                                                                                            |
|----------------|--------------------------------------------------------------------------------------------|
| <i>base</i>    | FlexCAN peripheral base address.                                                           |
| <i>handle</i>  | FlexCAN handle pointer.                                                                    |
| <i>pMbXfer</i> | FlexCAN Message Buffer transfer structure. See the <a href="#">flexcan_mb_transfer_t</a> . |

Return values

|                                |                                                           |
|--------------------------------|-----------------------------------------------------------|
| <i>kStatus_Success</i>         | - Start Rx Message Buffer receiving process successfully. |
| <i>kStatus_FLEXCAN_Rx-Busy</i> | - Rx Message Buffer is in use.                            |

#### 12.2.7.38 status\_t FLEXCAN\_TransferReceiveFifoNonBlocking ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, flexcan\_fifo\_transfer\_t \* *pFifoXfer* )

This function receives a message using IRQ. This is a non-blocking function, which returns right away. When all messages have been received, the receive callback function is called.

Parameters

|                  |                                                                                       |
|------------------|---------------------------------------------------------------------------------------|
| <i>base</i>      | FlexCAN peripheral base address.                                                      |
| <i>handle</i>    | FlexCAN handle pointer.                                                               |
| <i>pFifoXfer</i> | FlexCAN Rx FIFO transfer structure. See the <a href="#">flexcan_fifo_transfer_t</a> . |

Return values

|                                    |                                                 |
|------------------------------------|-------------------------------------------------|
| <i>kStatus_Success</i>             | - Start Rx FIFO receiving process successfully. |
| <i>kStatus_FLEXCAN_Rx-FifoBusy</i> | - Rx FIFO is currently in use.                  |

### 12.2.7.39 **status\_t FLEXCAN\_TransferGetReceiveFifoCount ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, size\_t \* *count* )**

Parameters

|               |                                                                        |
|---------------|------------------------------------------------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.                                       |
| <i>handle</i> | FlexCAN handle pointer.                                                |
| <i>count</i>  | Number of CAN messages receive so far by the non-blocking transaction. |

Return values

|                                |                                |
|--------------------------------|--------------------------------|
| <i>kStatus_InvalidArgument</i> | count is Invalid.              |
| <i>kStatus_Success</i>         | Successfully return the count. |

### 12.2.7.40 **uint32\_t FLEXCAN\_GetTimeStamp ( flexcan\_handle\_t \* *handle*, uint8\_t *mbIdx* )**

Then function can only be used when calling non-blocking Data transfer (TX/RX) API, After TX/R-X data transfer done (User can get the status by handler's callback function), we can get the detail index of Mailbox's timestamp by handle, Detail non-blocking data transfer API (TX/RX) contain. -FLEXCAN\_TransferSendNonBlocking -FLEXCAN\_TransferFDSendNonBlocking -FLEXCAN\_TransferReceiveNonBlocking -FLEXCAN\_TransferFDReceiveNonBlocking -FLEXCAN\_TransferReceiveFifoNonBlocking

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>handle</i> | FlexCAN handle pointer.           |
| <i>mbIdx</i>  | The FlexCAN Message Buffer index. |

Return values

|            |                                                     |
|------------|-----------------------------------------------------|
| <i>the</i> | index of mailbox 's timestamp stored in the handle. |
|------------|-----------------------------------------------------|

#### 12.2.7.41 void FLEXCAN\_TransferAbortSend ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, uint8\_t *mbIdx* )

This function aborts the interrupt driven message send process.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.  |
| <i>handle</i> | FlexCAN handle pointer.           |
| <i>mbIdx</i>  | The FlexCAN Message Buffer index. |

#### 12.2.7.42 void FLEXCAN\_TransferAbortReceive ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle*, uint8\_t *mbIdx* )

This function aborts the interrupt driven message receive process.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | FlexCAN peripheral base address.  |
| <i>handle</i> | FlexCAN handle pointer.           |
| <i>mbIdx</i>  | The FlexCAN Message Buffer index. |

#### 12.2.7.43 void FLEXCAN\_TransferAbortReceiveFifo ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle* )

This function aborts the interrupt driven message receive from Rx FIFO process.

Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | FlexCAN peripheral base address. |
| <i>handle</i> | FlexCAN handle pointer.          |

#### 12.2.7.44 void FLEXCAN\_TransferHandleIRQ ( CAN\_Type \* *base*, flexcan\_handle\_t \* *handle* )

This function handles the FlexCAN Error, the Message Buffer, and the Rx FIFO IRQ request.

## Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | FlexCAN peripheral base address. |
| <i>handle</i> | FlexCAN handle pointer.          |

# Chapter 13

## GPC: General Power Controller Driver

### 13.1 Overview

The MCUXpresso SDK provides a peripheral driver for the General Power Controller (GPC) module of MCUXpresso SDK devices.

API functions are provided to configure the system about working in dedicated power mode. There are mainly about enabling the power for memory, enabling the wakeup sources for STOP modes, and power up/down operations for various peripherals.

### Macros

- #define `GPC_PCG_TIME_SLOT_TOTAL_NUMBER` GPC\_SLT\_CFG\_PU\_COUNT  
*Total number of the timeslot.*

### Typedefs

- `typedef struct _gpc_lpm_config gpc_lpm_config_t`  
*configuration for enter DSM mode*

### Enumerations

- `enum _gpc_lpm_mode {`  
  `kGPC_RunMode = 0U,`  
  `kGPC_WaitMode = 1U,`  
  `kGPC_StopMode = 2U }`  
*GPC LPM mode definition.*
- `enum _gpc_pgc_ack_sel {`  
  `kGPC_DummyPGCPowerUpAck = GPC_PGC_ACK_SEL_DUMMY_PGC_PUP_ACK_MASK,`  
  `kGPC_VirtualPGCPowerUpAck = GPC_PGC_ACK_SEL_VIRTUAL_PGC_PUP_ACK_MASK,`  
  `kGPC_DummyPGCPowerDownAck = GPC_PGC_ACK_SEL_DUMMY_PGC_PDN_ACK_MASK,`  
  `kGPC_VirtualPGCPowerDownAck = GPC_PGC_ACK_SEL_VIRTUAL_PGC_PDN_ACK_MASK,`  
  `kGPC_NocPGCPowerUpAck = GPC_PGC_ACK_SEL_NOC_PGC_PUP_ACK,`  
  `kGPC_NocPGCPowerDownAck = GPC_PGC_ACK_SEL_NOC_PGC_PDN_ACK }`  
*PGC ack signal selection.*
- `enum _gpc_standby_count {`

```

kGPC_StandbyCounter4CkilClk = 0U,
kGPC_StandbyCounter8CkilClk = 1U,
kGPC_StandbyCounter16CkilClk = 2U,
kGPC_StandbyCounter32CkilClk = 3U,
kGPC_StandbyCounter64CkilClk = 4U,
kGPC_StandbyCounter128CkilClk = 5U,
kGPC_StandbyCounter256CkilClk = 6U,
kGPC_StandbyCounter512CkilClk = 7U }

```

*Standby counter which GPC will wait between PMIC\_STBY\_REQ negation and assertion of PMIC\_READY.*

## Functions

- static void [GPC\\_AllowIRQs](#) (GPC\_Type \*base)  
*Allow all the IRQ/Events within the charge of GPC.*
- static void [GPC\\_DisallowIRQs](#) (GPC\_Type \*base)  
*Disallow all the IRQ/Events within the charge of GPC.*
- static uint32\_t [GPC\\_GetLpmMode](#) (GPC\_Type \*base)  
*Get current LPM mode.*
- void [GPC\\_EnableIRQ](#) (GPC\_Type \*base, uint32\_t irqId)  
*Enable the IRQ.*
- void [GPC\\_DisableIRQ](#) (GPC\_Type \*base, uint32\_t irqId)  
*Disable the IRQ.*
- bool [GPC\\_GetIRQStatusFlag](#) (GPC\_Type \*base, uint32\_t irqId)  
*Get the IRQ/Event flag.*
- static void [GPC\\_DsmTriggerMask](#) (GPC\_Type \*base, bool enable)  
*Mask the DSM trigger.*
- static void [GPC\\_WFIMask](#) (GPC\_Type \*base, bool enable)  
*Mask the WFI.*
- static void [GPC\\_SelectPGCAckSignal](#) (GPC\_Type \*base, uint32\_t mask)  
*Select the PGC ACK signal.*
- static void [GPC\\_PowerDownRequestMask](#) (GPC\_Type \*base, bool enable)  
*Power down request to virtual PGC mask or not.*
- static void [GPC\\_PGCMapping](#) (GPC\_Type \*base, uint32\_t mask)  
*PGC CPU Mapping.*
- static void [GPC\\_TimeSlotConfigureForPUS](#) (GPC\_Type \*base, uint8\_t slotIndex, uint32\_t value)  
*Time slot configure.*
- void [GPC\\_EnterWaitMode](#) (GPC\_Type \*base, [gpc\\_lpm\\_config\\_t](#) \*config)  
*Enter WAIT mode.*
- void [GPC\\_EnterStopMode](#) (GPC\_Type \*base, [gpc\\_lpm\\_config\\_t](#) \*config)  
*Enter STOP mode.*
- void [GPC\\_Init](#) (GPC\_Type \*base, uint32\_t powerUpSlot, uint32\_t powerDownSlot)  
*GPC init function.*

## Driver version

- #define [FSL\\_GPC\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 2, 0))  
*GPC driver version 2.2.0.*

## 13.2 Macro Definition Documentation

**13.2.1 #define FSL\_GPC\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 0))**

## 13.3 Enumeration Type Documentation

**13.3.1 enum \_gpc\_lpm\_mode**

Enumerator

*kGPC\_RunMode* run mode  
*kGPC\_WaitMode* wait mode  
*kGPC\_StopMode* stop mode

**13.3.2 enum \_gpc\_pgc\_ack\_sel**

Enumerator

*kGPC\_DummyPGCPowerUpAck* dummy power up ack signal  
*kGPC\_VirtualPGCPowerUpAck* virtual pgc power up ack signal  
*kGPC\_DummyPGCPowerDownAck* dummy power down ack signal  
*kGPC\_VirtualPGCPowerDownAck* virtual pgc power down ack signal  
*kGPC\_NocPGCPowerUpAck* NOC power up ack signal.  
*kGPC\_NocPGCPowerDownAck* NOC power.

**13.3.3 enum \_gpc\_standby\_count**

Enumerator

*kGPC\_StandbyCounter4CkilClk* 4 ckil clocks  
*kGPC\_StandbyCounter8CkilClk* 8 ckil clocks  
*kGPC\_StandbyCounter16CkilClk* 16 ckil clocks  
*kGPC\_StandbyCounter32CkilClk* 32 ckil clocks  
*kGPC\_StandbyCounter64CkilClk* 64 ckil clocks  
*kGPC\_StandbyCounter128CkilClk* 128 ckil clocks  
*kGPC\_StandbyCounter256CkilClk* 256 ckil clocks  
*kGPC\_StandbyCounter512CkilClk* 512 ckil clocks

## 13.4 Function Documentation

**13.4.1 static void GPC\_AllowIRQs ( GPC\_Type \* *base* ) [inline], [static]**

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPC peripheral base address. |
|-------------|------------------------------|

### 13.4.2 static void GPC\_DisallowIRQs ( GPC\_Type \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPC peripheral base address. |
|-------------|------------------------------|

### 13.4.3 static uint32\_t GPC\_GetLpmMode ( GPC\_Type \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPC peripheral base address. |
|-------------|------------------------------|

Return values

|            |                               |
|------------|-------------------------------|
| <i>lpm</i> | mode, reference _gpc_lpm_mode |
|------------|-------------------------------|

### 13.4.4 void GPC\_EnableIRQ ( GPC\_Type \* *base*, uint32\_t *irqId* )

Parameters

|              |                                                                                              |
|--------------|----------------------------------------------------------------------------------------------|
| <i>base</i>  | GPC peripheral base address.                                                                 |
| <i>irqId</i> | ID number of IRQ to be enabled, available range is 0-127,reference SOC headerfile IRQn_Type. |

### 13.4.5 void GPC\_DisableIRQ ( GPC\_Type \* *base*, uint32\_t *irqId* )

Parameters

|              |                                                                                               |
|--------------|-----------------------------------------------------------------------------------------------|
| <i>base</i>  | GPC peripheral base address.                                                                  |
| <i>irqId</i> | ID number of IRQ to be disabled, available range is 0-127,reference SOC headerfile IRQn_Type. |

### 13.4.6 **bool GPC\_GetIRQStatusFlag ( GPC\_Type \* *base*, uint32\_t *irqId* )**

Parameters

|              |                                                                                              |
|--------------|----------------------------------------------------------------------------------------------|
| <i>base</i>  | GPC peripheral base address.                                                                 |
| <i>irqId</i> | ID number of IRQ to be enabled, available range is 0-127,reference SOC headerfile IRQn_Type. |

Returns

Indicated IRQ/Event is asserted or not.

### 13.4.7 **static void GPC\_DsmTriggerMask ( GPC\_Type \* *base*, bool *enable* ) [inline], [static]**

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>base</i>   | GPC peripheral base address.                |
| <i>enable</i> | true to enable mask, false to disable mask. |

### 13.4.8 **static void GPC\_WFIMask ( GPC\_Type \* *base*, bool *enable* ) [inline], [static]**

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>base</i>   | GPC peripheral base address.                |
| <i>enable</i> | true to enable mask, false to disable mask. |

### 13.4.9 **static void GPC\_SelectPGCAckSignal ( GPC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPC peripheral base address. |
| <i>mask</i> | reference _gpc_pgc_ack_sel.  |

#### 13.4.10 static void GPC\_PowerDownRequestMask ( **GPC\_Type** \* *base*, **bool** *enable* ) [inline], [static]

Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | GPC peripheral base address.     |
| <i>enable</i> | true to mask, false to not mask. |

#### 13.4.11 static void GPC\_PGCMapping ( **GPC\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

|             |                                                  |
|-------------|--------------------------------------------------|
| <i>base</i> | GPC peripheral base address.                     |
| <i>mask</i> | mask value reference PGC CPU mapping definition. |

#### 13.4.12 static void GPC\_TimeSlotConfigureForPUS ( **GPC\_Type** \* *base*, **uint8\_t** *slotIndex*, **uint32\_t** *value* ) [inline], [static]

Parameters

|                  |                              |
|------------------|------------------------------|
| <i>base</i>      | GPC peripheral base address. |
| <i>slotIndex</i> | time slot index.             |
| <i>value</i>     | value to be configured       |

#### 13.4.13 void GPC\_EnterWaitMode ( **GPC\_Type** \* *base*, **gpc\_lpm\_config\_t** \* *config* )

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | GPC peripheral base address. |
| <i>config</i> | lpm mode configurations.     |

**13.4.14 void GPC\_EnterStopMode ( GPC\_Type \* *base*, gpc\_lpm\_config\_t \* *config* )**

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | GPC peripheral base address. |
| <i>config</i> | lpm mode configurations.     |

**13.4.15 void GPC\_Init ( GPC\_Type \* *base*, uint32\_t *powerUpSlot*, uint32\_t *powerDownSlot* )**

Parameters

|                       |                              |
|-----------------------|------------------------------|
| <i>base</i>           | GPC peripheral base address. |
| <i>powerUpSlot</i>    | power up slot number.        |
| <i>powerDown-Slot</i> | power down slot number.      |

# Chapter 14

## GPT: General Purpose Timer

### 14.1 Overview

The MCUXpresso SDK provides a driver for the General Purpose Timer (GPT) of MCUXpresso SDK devices.

### 14.2 Function groups

The gpt driver supports the generation of PWM signals, input capture, and setting up the timer match conditions.

#### 14.2.1 Initialization and deinitialization

The function [GPT\\_Init\(\)](#) initializes the gpt with specified configurations. The function [GPT\\_GetDefaultConfig\(\)](#) gets the default configurations. The initialization function configures the restart/free-run mode and input selection when running.

The function [GPT\\_Deinit\(\)](#) stops the timer and turns off the module clock.

### 14.3 Typical use case

#### 14.3.1 GPT interrupt example

Set up a channel to trigger a periodic interrupt after every 1 second. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/gpt

## Data Structures

- struct [\\_gpt\\_init\\_config](#)  
*Structure to configure the running mode.* [More...](#)

## Typedefs

- typedef enum [\\_gpt\\_clock\\_source](#) [gpt\\_clock\\_source\\_t](#)  
*List of clock sources.*
- typedef enum [\\_gpt\\_input\\_capture\\_channel](#) [gpt\\_input\\_capture\\_channel\\_t](#)  
*List of input capture channel number.*
- typedef enum [\\_gpt\\_input\\_operation\\_mode](#) [gpt\\_input\\_operation\\_mode\\_t](#)  
*List of input capture operation mode.*

- `typedef enum _gpt_output_compare_channel gpt_output_compare_channel_t`  
*List of output compare channel number.*
- `typedef enum _gpt_output_operation_mode gpt_output_operation_mode_t`  
*List of output compare operation mode.*
- `typedef enum _gpt_interrupt_enable gpt_interrupt_enable_t`  
*List of GPT interrupts.*
- `typedef enum _gpt_status_flag gpt_status_flag_t`  
*Status flag.*
- `typedef struct _gpt_init_config gpt_config_t`  
*Structure to configure the running mode.*

## Enumerations

- `enum _gpt_clock_source {`  
`kGPT_ClockSource_Off = 0U,`  
`kGPT_ClockSource_Pерiph = 1U,`  
`kGPT_ClockSource_HighFreq = 2U,`  
`kGPT_ClockSource_Ext = 3U,`  
`kGPT_ClockSource_LowFreq = 4U,`  
`kGPT_ClockSource_Osc = 5U }`  
*List of clock sources.*
- `enum _gpt_input_capture_channel {`  
`kGPT_InputCapture_Channel1 = 0U,`  
`kGPT_InputCapture_Channel2 = 1U }`  
*List of input capture channel number.*
- `enum _gpt_input_operation_mode {`  
`kGPT_InputOperation_Disabled = 0U,`  
`kGPT_InputOperation_RiseEdge = 1U,`  
`kGPT_InputOperation_FallEdge = 2U,`  
`kGPT_InputOperation_BothEdge = 3U }`  
*List of input capture operation mode.*
- `enum _gpt_output_compare_channel {`  
`kGPT_OutputCompare_Channel1 = 0U,`  
`kGPT_OutputCompare_Channel2 = 1U,`  
`kGPT_OutputCompare_Channel3 = 2U }`  
*List of output compare channel number.*
- `enum _gpt_output_operation_mode {`  
`kGPT_OutputOperation_Disconnected = 0U,`  
`kGPT_OutputOperation_Toggle = 1U,`  
`kGPT_OutputOperation_Clear = 2U,`  
`kGPT_OutputOperation_Set = 3U,`  
`kGPT_OutputOperation_Activelow = 4U }`  
*List of output compare operation mode.*
- `enum _gpt_interrupt_enable {`

```
kGPT_OutputCompare1InterruptEnable = GPT_IR_OF1IE_MASK,
kGPT_OutputCompare2InterruptEnable = GPT_IR_OF2IE_MASK,
kGPT_OutputCompare3InterruptEnable = GPT_IR_OF3IE_MASK,
kGPT_InputCapture1InterruptEnable = GPT_IR_IF1IE_MASK,
kGPT_InputCapture2InterruptEnable = GPT_IR_IF2IE_MASK,
kGPT_RollOverFlagInterruptEnable = GPT_IR_ROVIE_MASK }
```

*List of GPT interrupts.*

- enum `_gpt_status_flag` {
 

```
kGPT_OutputCompare1Flag = GPT_SR_OF1_MASK,
kGPT_OutputCompare2Flag = GPT_SR_OF2_MASK,
kGPT_OutputCompare3Flag = GPT_SR_OF3_MASK,
kGPT_InputCapture1Flag = GPT_SR_IF1_MASK,
kGPT_InputCapture2Flag = GPT_SR_IF2_MASK,
kGPT_RollOverFlag = GPT_SR_ROV_MASK }
```

*Status flag.*

## Driver version

- #define `FSL_GPT_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 4)`)

## Initialization and deinitialization

- void `GPT_Init` (GPT\_Type \*base, const `gpt_config_t` \*initConfig)
 

*Initialize GPT to reset state and initialize running mode.*
- void `GPT_Deinit` (GPT\_Type \*base)
 

*Disables the module and gates the GPT clock.*
- void `GPT_GetDefaultConfig` (`gpt_config_t` \*config)
 

*Fills in the GPT configuration structure with default settings.*

## Software Reset

- static void `GPT_SoftwareReset` (GPT\_Type \*base)
 

*Software reset of GPT module.*

## Clock source and frequency control

- static void `GPT_SetClockSource` (GPT\_Type \*base, `gpt_clock_source_t` gptClkSource)
 

*Set clock source of GPT.*
- static `gpt_clock_source_t` `GPT_GetClockSource` (GPT\_Type \*base)
 

*Get clock source of GPT.*
- static void `GPT_SetClockDivider` (GPT\_Type \*base, uint32\_t divider)
 

*Set pre scaler of GPT.*
- static uint32\_t `GPT_GetClockDivider` (GPT\_Type \*base)
 

*Get clock divider in GPT module.*
- static void `GPT_SetOscClockDivider` (GPT\_Type \*base, uint32\_t divider)
 

*OSC 24M pre-scaler before selected by clock source.*
- static uint32\_t `GPT_GetOscClockDivider` (GPT\_Type \*base)
 

*Get OSC 24M clock divider in GPT module.*

## Timer Start and Stop

- static void `GPT_StartTimer` (GPT\_Type \*base)  
*Start GPT timer.*
- static void `GPT_StopTimer` (GPT\_Type \*base)  
*Stop GPT timer.*

## Read the timer period

- static uint32\_t `GPT_GetCurrentTimerCount` (GPT\_Type \*base)  
*Reads the current GPT counting value.*

## GPT Input/Output Signal Control

- static void `GPT_SetInputOperationMode` (GPT\_Type \*base, `gpt_input_capture_channel_t` channel, `gpt_input_operation_mode_t` mode)  
*Set GPT operation mode of input capture channel.*
- static `gpt_input_operation_mode_t` `GPT_GetInputOperationMode` (GPT\_Type \*base, `gpt_input_capture_channel_t` channel)  
*Get GPT operation mode of input capture channel.*
- static uint32\_t `GPT_GetInputCaptureValue` (GPT\_Type \*base, `gpt_input_capture_channel_t` channel)  
*Get GPT input capture value of certain channel.*
- static void `GPT_SetOutputOperationMode` (GPT\_Type \*base, `gpt_output_compare_channel_t` channel, `gpt_output_operation_mode_t` mode)  
*Set GPT operation mode of output compare channel.*
- static `gpt_output_operation_mode_t` `GPT_GetOutputOperationMode` (GPT\_Type \*base, `gpt_output_compare_channel_t` channel)  
*Get GPT operation mode of output compare channel.*
- static void `GPT_SetOutputCompareValue` (GPT\_Type \*base, `gpt_output_compare_channel_t` channel, uint32\_t value)  
*Set GPT output compare value of output compare channel.*
- static uint32\_t `GPT_GetOutputCompareValue` (GPT\_Type \*base, `gpt_output_compare_channel_t` channel)  
*Get GPT output compare value of output compare channel.*
- static void `GPT_ForceOutput` (GPT\_Type \*base, `gpt_output_compare_channel_t` channel)  
*Force GPT output action on output compare channel, ignoring comparator.*

## GPT Interrupt and Status Interface

- static void `GPT_EnableInterrupts` (GPT\_Type \*base, uint32\_t mask)  
*Enables the selected GPT interrupts.*
- static void `GPT_DisableInterrupts` (GPT\_Type \*base, uint32\_t mask)  
*Disables the selected GPT interrupts.*
- static uint32\_t `GPT_GetEnabledInterrupts` (GPT\_Type \*base)  
*Gets the enabled GPT interrupts.*

## Status Interface

- static uint32\_t `GPT_GetStatusFlags` (GPT\_Type \*base, `gpt_status_flag_t` flags)

- static void [GPT\\_ClearStatusFlags](#) (GPT\_Type \*base, gpt\_status\_flag\_t flags)  
*Clears the GPT status flags.*

## 14.4 Data Structure Documentation

### 14.4.1 struct \_gpt\_init\_config

#### Data Fields

- [gpt\\_clock\\_source\\_t clockSource](#)  
*clock source for GPT module.*
- [uint32\\_t divider](#)  
*clock divider (prescaler+1) from clock source to counter.*
- [bool enableFreeRun](#)  
*true: FreeRun mode, false: Restart mode.*
- [bool enableRunInWait](#)  
*GPT enabled in wait mode.*
- [bool enableRunInStop](#)  
*GPT enabled in stop mode.*
- [bool enableRunInDoze](#)  
*GPT enabled in doze mode.*
- [bool enableRunInDbg](#)  
*GPT enabled in debug mode.*
- [bool enableMode](#)  
*true: counter reset to 0 when enabled;  
false: counter retain its value when enabled.*

#### Field Documentation

- (1) [gpt\\_clock\\_source\\_t \\_gpt\\_init\\_config::clockSource](#)
- (2) [uint32\\_t \\_gpt\\_init\\_config::divider](#)
- (3) [bool \\_gpt\\_init\\_config::enableFreeRun](#)
- (4) [bool \\_gpt\\_init\\_config::enableRunInWait](#)
- (5) [bool \\_gpt\\_init\\_config::enableRunInStop](#)
- (6) [bool \\_gpt\\_init\\_config::enableRunInDoze](#)
- (7) [bool \\_gpt\\_init\\_config::enableRunInDbg](#)
- (8) [bool \\_gpt\\_init\\_config::enableMode](#)

## 14.5 Typedef Documentation

### 14.5.1 [typedef enum \\_gpt\\_clock\\_source gpt\\_clock\\_source\\_t](#)

Note

Actual number of clock sources is SoC dependent

#### **14.5.2 `typedef enum _gpt_input_capture_channel gpt_input_capture_channel_t`**

#### **14.5.3 `typedef enum _gpt_input_operation_mode gpt_input_operation_mode_t`**

#### **14.5.4 `typedef enum _gpt_output_compare_channel gpt_output_compare_channel_t`**

#### **14.5.5 `typedef enum _gpt_output_operation_mode gpt_output_operation_mode_t`**

#### **14.5.6 `typedef enum _gpt_status_flag gpt_status_flag_t`**

#### **14.5.7 `typedef struct _gpt_init_config gpt_config_t`**

### **14.6 Enumeration Type Documentation**

#### **14.6.1 `enum _gpt_clock_source`**

Note

Actual number of clock sources is SoC dependent

Enumerator

*kGPT\_ClockSource\_Off* GPT Clock Source Off.

*kGPT\_ClockSource\_Pерiph* GPT Clock Source from Peripheral Clock.

*kGPT\_ClockSource\_HighFreq* GPT Clock Source from High Frequency Reference Clock.

*kGPT\_ClockSource\_Ext* GPT Clock Source from external pin.

*kGPT\_ClockSource\_LowFreq* GPT Clock Source from Low Frequency Reference Clock.

*kGPT\_ClockSource\_Osc* GPT Clock Source from Crystal oscillator.

#### **14.6.2 `enum _gpt_input_capture_channel`**

Enumerator

*kGPT\_InputCapture\_Channel1* GPT Input Capture Channel1.

*kGPT\_InputCapture\_Channel2* GPT Input Capture Channel2.

### 14.6.3 enum \_gpt\_input\_operation\_mode

Enumerator

*kGPT\_InputOperation\_Disabled* Don't capture.

*kGPT\_InputOperation\_RiseEdge* Capture on rising edge of input pin.

*kGPT\_InputOperation\_FallEdge* Capture on falling edge of input pin.

*kGPT\_InputOperation\_BothEdge* Capture on both edges of input pin.

### 14.6.4 enum \_gpt\_output\_compare\_channel

Enumerator

*kGPT\_OutputCompare\_Channel1* Output Compare Channel1.

*kGPT\_OutputCompare\_Channel2* Output Compare Channel2.

*kGPT\_OutputCompare\_Channel3* Output Compare Channel3.

### 14.6.5 enum \_gpt\_output\_operation\_mode

Enumerator

*kGPT\_OutputOperation\_Disconnected* Don't change output pin.

*kGPT\_OutputOperation\_Toggle* Toggle output pin.

*kGPT\_OutputOperation\_Clear* Set output pin low.

*kGPT\_OutputOperation\_Set* Set output pin high.

*kGPT\_OutputOperation\_Activelow* Generate a active low pulse on output pin.

### 14.6.6 enum \_gpt\_interrupt\_enable

Enumerator

*kGPT\_OutputCompare1InterruptEnable* Output Compare Channel1 interrupt enable.

*kGPT\_OutputCompare2InterruptEnable* Output Compare Channel2 interrupt enable.

*kGPT\_OutputCompare3InterruptEnable* Output Compare Channel3 interrupt enable.

*kGPT\_InputCapture1InterruptEnable* Input Capture Channel1 interrupt enable.

*kGPT\_InputCapture2InterruptEnable* Input Capture Channell1 interrupt enable.

*kGPT\_RollOverFlagInterruptEnable* Counter rolled over interrupt enable.

### 14.6.7 enum \_gpt\_status\_flag

Enumerator

- kGPT\_OutputCompare1Flag* Output compare channel 1 event.
- kGPT\_OutputCompare2Flag* Output compare channel 2 event.
- kGPT\_OutputCompare3Flag* Output compare channel 3 event.
- kGPT\_InputCapture1Flag* Input Capture channel 1 event.
- kGPT\_InputCapture2Flag* Input Capture channel 2 event.
- kGPT\_RollOverFlag* Counter reaches maximum value and rolled over to 0 event.

## 14.7 Function Documentation

### 14.7.1 void GPT\_Init ( *GPT\_Type* \* *base*, *const gpt\_config\_t* \* *initConfig* )

Parameters

|                   |                                 |
|-------------------|---------------------------------|
| <i>base</i>       | GPT peripheral base address.    |
| <i>initConfig</i> | GPT mode setting configuration. |

### 14.7.2 void GPT\_Deinit ( *GPT\_Type* \* *base* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPT peripheral base address. |
|-------------|------------------------------|

### 14.7.3 void GPT\_GetDefaultConfig ( *gpt\_config\_t* \* *config* )

The default values are:

```
* config->clockSource = kGPT_ClockSource_Periph;
* config->divider = 1U;
* config->enableRunInStop = true;
* config->enableRunInWait = true;
* config->enableRunInDoze = false;
* config->enableRunInDbg = false;
* config->enableFreeRun = false;
* config->enableMode = true;
*
```

Parameters

|               |                                              |
|---------------|----------------------------------------------|
| <i>config</i> | Pointer to the user configuration structure. |
|---------------|----------------------------------------------|

#### 14.7.4 static void GPT\_SoftwareReset ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPT peripheral base address. |
|-------------|------------------------------|

#### 14.7.5 static void GPT\_SetClockSource ( **GPT\_Type** \* *base*, **gpt\_clock\_source\_t** *gptClkSource* ) [inline], [static]

Parameters

|                     |                                                                            |
|---------------------|----------------------------------------------------------------------------|
| <i>base</i>         | GPT peripheral base address.                                               |
| <i>gptClkSource</i> | Clock source (see <a href="#">gpt_clock_source_t</a> typedef enumeration). |

#### 14.7.6 static **gpt\_clock\_source\_t** GPT\_GetClockSource ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPT peripheral base address. |
|-------------|------------------------------|

Returns

clock source (see [gpt\\_clock\\_source\\_t](#) typedef enumeration).

#### 14.7.7 static void GPT\_SetClockDivider ( **GPT\_Type** \* *base*, **uint32\_t** *divider* ) [inline], [static]

Parameters

|                |                              |
|----------------|------------------------------|
| <i>base</i>    | GPT peripheral base address. |
| <i>divider</i> | Divider of GPT (1-4096).     |

#### 14.7.8 static uint32\_t GPT\_GetClockDivider ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPT peripheral base address. |
|-------------|------------------------------|

Returns

clock divider in GPT module (1-4096).

#### 14.7.9 static void GPT\_SetOscClockDivider ( **GPT\_Type** \* *base*, uint32\_t *divider* ) [inline], [static]

Parameters

|                |                              |
|----------------|------------------------------|
| <i>base</i>    | GPT peripheral base address. |
| <i>divider</i> | OSC Divider(1-16).           |

#### 14.7.10 static uint32\_t GPT\_GetOscClockDivider ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPT peripheral base address. |
|-------------|------------------------------|

Returns

OSC clock divider in GPT module (1-16).

#### 14.7.11 static void GPT\_StartTimer ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPT peripheral base address. |
|-------------|------------------------------|

#### 14.7.12 static void GPT\_StopTimer ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPT peripheral base address. |
|-------------|------------------------------|

#### 14.7.13 static uint32\_t GPT\_GetCurrentTimerCount ( **GPT\_Type** \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | GPT peripheral base address. |
|-------------|------------------------------|

Returns

Current GPT counter value.

#### 14.7.14 static void GPT\_SetInputOperationMode ( **GPT\_Type** \* *base*, **gpt\_input\_capture\_channel\_t** *channel*, **gpt\_input\_operation\_mode\_t** *mode* ) [inline], [static]

Parameters

|                |                                                                                                        |
|----------------|--------------------------------------------------------------------------------------------------------|
| <i>base</i>    | GPT peripheral base address.                                                                           |
| <i>channel</i> | GPT capture channel (see <a href="#">gpt_input_capture_channel_t</a> typedef enumeration).             |
| <i>mode</i>    | GPT input capture operation mode (see <a href="#">gpt_input_operation_mode_t</a> typedef enumeration). |

#### 14.7.15 static **gpt\_input\_operation\_mode\_t** GPT\_GetInputOperationMode ( **GPT\_Type** \* *base*, **gpt\_input\_capture\_channel\_t** *channel* ) [inline], [static]

Parameters

|                |                                                                                            |
|----------------|--------------------------------------------------------------------------------------------|
| <i>base</i>    | GPT peripheral base address.                                                               |
| <i>channel</i> | GPT capture channel (see <a href="#">gpt_input_capture_channel_t</a> typedef enumeration). |

Returns

GPT input capture operation mode (see [gpt\\_input\\_operation\\_mode\\_t](#) typedef enumeration).

#### 14.7.16 static uint32\_t GPT\_GetInputCaptureValue ( **GPT\_Type** \* *base*, **gpt\_input\_capture\_channel\_t** *channel* ) [inline], [static]

Parameters

|                |                                                                                            |
|----------------|--------------------------------------------------------------------------------------------|
| <i>base</i>    | GPT peripheral base address.                                                               |
| <i>channel</i> | GPT capture channel (see <a href="#">gpt_input_capture_channel_t</a> typedef enumeration). |

Returns

GPT input capture value.

#### 14.7.17 static void GPT\_SetOutputOperationMode ( **GPT\_Type** \* *base*, **gpt\_output\_compare\_channel\_t** *channel*, **gpt\_output\_operation\_mode\_t** *mode* ) [inline], [static]

Parameters

|                |                                                                                                    |
|----------------|----------------------------------------------------------------------------------------------------|
| <i>base</i>    | GPT peripheral base address.                                                                       |
| <i>channel</i> | GPT output compare channel (see <a href="#">gpt_output_compare_channel_t</a> typedef enumeration). |
| <i>mode</i>    | GPT output operation mode (see <a href="#">gpt_output_operation_mode_t</a> typedef enumeration).   |

#### 14.7.18 static **gpt\_output\_operation\_mode\_t** GPT\_GetOutputOperationMode ( **GPT\_Type** \* *base*, **gpt\_output\_compare\_channel\_t** *channel* ) [inline], [static]

Parameters

|                |                                                                                                    |
|----------------|----------------------------------------------------------------------------------------------------|
| <i>base</i>    | GPT peripheral base address.                                                                       |
| <i>channel</i> | GPT output compare channel (see <a href="#">gpt_output_compare_channel_t</a> typedef enumeration). |

Returns

GPT output operation mode (see [gpt\\_output\\_operation\\_mode\\_t](#) typedef enumeration).

**14.7.19 static void GPT\_SetOutputCompareValue ( GPT\_Type \* *base*, gpt\_output\_compare\_channel\_t *channel*, uint32\_t *value* ) [inline], [static]**

Parameters

|                |                                                                                                    |
|----------------|----------------------------------------------------------------------------------------------------|
| <i>base</i>    | GPT peripheral base address.                                                                       |
| <i>channel</i> | GPT output compare channel (see <a href="#">gpt_output_compare_channel_t</a> typedef enumeration). |
| <i>value</i>   | GPT output compare value.                                                                          |

**14.7.20 static uint32\_t GPT\_GetOutputCompareValue ( GPT\_Type \* *base*, gpt\_output\_compare\_channel\_t *channel* ) [inline], [static]**

Parameters

|                |                                                                                                    |
|----------------|----------------------------------------------------------------------------------------------------|
| <i>base</i>    | GPT peripheral base address.                                                                       |
| <i>channel</i> | GPT output compare channel (see <a href="#">gpt_output_compare_channel_t</a> typedef enumeration). |

Returns

GPT output compare value.

**14.7.21 static void GPT\_ForceOutput ( GPT\_Type \* *base*, gpt\_output\_compare\_channel\_t *channel* ) [inline], [static]**

Parameters

|                |                                                                                                    |
|----------------|----------------------------------------------------------------------------------------------------|
| <i>base</i>    | GPT peripheral base address.                                                                       |
| <i>channel</i> | GPT output compare channel (see <a href="#">gpt_output_compare_channel_t</a> typedef enumeration). |

#### 14.7.22 static void GPT\_EnableInterrupts ( *GPT\_Type* \* *base*, *uint32\_t* *mask* ) [[inline](#)], [[static](#)]

Parameters

|             |                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | GPT peripheral base address.                                                                                        |
| <i>mask</i> | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">gpt_interrupt_enable_t</a> |

#### 14.7.23 static void GPT\_DisableInterrupts ( *GPT\_Type* \* *base*, *uint32\_t* *mask* ) [[inline](#)], [[static](#)]

Parameters

|             |                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | GPT peripheral base address                                                                                          |
| <i>mask</i> | The interrupts to disable. This is a logical OR of members of the enumeration <a href="#">gpt_interrupt_enable_t</a> |

#### 14.7.24 static *uint32\_t* GPT\_GetEnabledInterrupts ( *GPT\_Type* \* *base* ) [[inline](#)], [[static](#)]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | GPT peripheral base address |
|-------------|-----------------------------|

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [gpt\\_interrupt\\_enable\\_t](#)

#### 14.7.25 static *uint32\_t* GPT\_GetStatusFlags ( *GPT\_Type* \* *base*, *gpt\_status\_flag\_t* *flags* ) [[inline](#)], [[static](#)]

Parameters

|              |                                                                                  |
|--------------|----------------------------------------------------------------------------------|
| <i>base</i>  | GPT peripheral base address.                                                     |
| <i>flags</i> | GPT status flag mask (see <a href="#">gpt_status_flag_t</a> for bit definition). |

Returns

GPT status, each bit represents one status flag.

#### 14.7.26 static void GPT\_ClearStatusFlags ( GPT\_Type \* *base*, gpt\_status\_flag\_t *flags* ) [inline], [static]

Parameters

|              |                                                                                  |
|--------------|----------------------------------------------------------------------------------|
| <i>base</i>  | GPT peripheral base address.                                                     |
| <i>flags</i> | GPT status flag mask (see <a href="#">gpt_status_flag_t</a> for bit definition). |

# Chapter 15

## GPIO: General-Purpose Input/Output Driver

### 15.1 Overview

The MCUXpresso SDK provides a peripheral driver for the General-Purpose Input/Output (GPIO) module of MCUXpresso SDK devices.

### 15.2 Typical use case

#### 15.2.1 Input Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/gpio

### Data Structures

- struct [\\_gpio\\_pin\\_config](#)  
*GPIO Init structure definition. [More...](#)*

### Typedefs

- typedef enum [\\_gpio\\_pin\\_direction](#) [gpio\\_pin\\_direction\\_t](#)  
*GPIO direction definition.*
- typedef enum [\\_gpio\\_interrupt\\_mode](#) [gpio\\_interrupt\\_mode\\_t](#)  
*GPIO interrupt mode definition.*
- typedef struct [\\_gpio\\_pin\\_config](#) [gpio\\_pin\\_config\\_t](#)  
*GPIO Init structure definition.*

### Enumerations

- enum [\\_gpio\\_pin\\_direction](#) {  
  [kGPIO\\_DigitalInput](#) = 0U,  
  [kGPIO\\_DigitalOutput](#) = 1U }  
*GPIO direction definition.*
- enum [\\_gpio\\_interrupt\\_mode](#) {  
  [kGPIO\\_NoIntmode](#) = 0U,  
  [kGPIO\\_IntLowLevel](#) = 1U,  
  [kGPIO\\_IntHighLevel](#) = 2U,  
  [kGPIO\\_IntRisingEdge](#) = 3U,  
  [kGPIO\\_IntFallingEdge](#) = 4U,  
  [kGPIO\\_IntRisingOrFallingEdge](#) = 5U }  
*GPIO interrupt mode definition.*

## Driver version

- #define **FSL\_GPIO\_DRIVER\_VERSION** (MAKE\_VERSION(2, 0, 6))  
*GPIO driver version.*

## GPIO Initialization and Configuration functions

- void **GPIO\_PinInit** (GPIO\_Type \*base, uint32\_t pin, const **gpio\_pin\_config\_t** \*Config)  
*Initializes the GPIO peripheral according to the specified parameters in the initConfig.*

## GPIO Reads and Write Functions

- void **GPIO\_PinWrite** (GPIO\_Type \*base, uint32\_t pin, uint8\_t output)  
*Sets the output level of the individual GPIO pin to logic 1 or 0.*
- static void **GPIO\_WritePinOutput** (GPIO\_Type \*base, uint32\_t pin, uint8\_t output)  
*Sets the output level of the individual GPIO pin to logic 1 or 0.*
- static void **GPIO\_PortSet** (GPIO\_Type \*base, uint32\_t mask)  
*Sets the output level of the multiple GPIO pins to the logic 1.*
- static void **GPIO\_SetPinsOutput** (GPIO\_Type \*base, uint32\_t mask)  
*Sets the output level of the multiple GPIO pins to the logic 1.*
- static void **GPIO\_PortClear** (GPIO\_Type \*base, uint32\_t mask)  
*Sets the output level of the multiple GPIO pins to the logic 0.*
- static void **GPIO\_ClearPinsOutput** (GPIO\_Type \*base, uint32\_t mask)  
*Sets the output level of the multiple GPIO pins to the logic 0.*
- static void **GPIO\_PortToggle** (GPIO\_Type \*base, uint32\_t mask)  
*Reverses the current output logic of the multiple GPIO pins.*
- static uint32\_t **GPIO\_PinRead** (GPIO\_Type \*base, uint32\_t pin)  
*Reads the current input value of the GPIO port.*
- static uint32\_t **GPIO\_ReadPinInput** (GPIO\_Type \*base, uint32\_t pin)  
*Reads the current input value of the GPIO port.*

## GPIO Reads Pad Status Functions

- static uint8\_t **GPIO\_PinReadPadStatus** (GPIO\_Type \*base, uint32\_t pin)  
*Reads the current GPIO pin pad status.*
- static uint8\_t **GPIO\_ReadPadStatus** (GPIO\_Type \*base, uint32\_t pin)  
*Reads the current GPIO pin pad status.*

## Interrupts and flags management functions

- void **GPIO\_PinSetInterruptConfig** (GPIO\_Type \*base, uint32\_t pin, **gpio\_interrupt\_mode\_t** pinInterruptMode)  
*Sets the current pin interrupt mode.*
- static void **GPIO\_SetPinInterruptConfig** (GPIO\_Type \*base, uint32\_t pin, **gpio\_interrupt\_mode\_t** pinInterruptMode)  
*Sets the current pin interrupt mode.*
- static void **GPIO\_PortEnableInterrupts** (GPIO\_Type \*base, uint32\_t mask)  
*Enables the specific pin interrupt.*
- static void **GPIO\_EnableInterrupts** (GPIO\_Type \*base, uint32\_t mask)  
*Enables the specific pin interrupt.*
- static void **GPIO\_PortDisableInterrupts** (GPIO\_Type \*base, uint32\_t mask)

- static void [GPIO\\_DisableInterrupts](#) (GPIO\_Type \*base, uint32\_t mask)
 

*Disables the specific pin interrupt.*
- static uint32\_t [GPIO\\_PortGetInterruptFlags](#) (GPIO\_Type \*base)
 

*Disables the specific pin interrupt.*
- static uint32\_t [GPIO\\_GetPinsInterruptFlags](#) (GPIO\_Type \*base)
 

*Reads individual pin interrupt status.*
- static void [GPIO\\_PortClearInterruptFlags](#) (GPIO\_Type \*base, uint32\_t mask)
 

*Reads individual pin interrupt status.*
- static void [GPIO\\_ClearPinsInterruptFlags](#) (GPIO\_Type \*base, uint32\_t mask)
 

*Clears pin interrupt flag.*
- static void [GPIO\\_DisableInterrupts](#) (GPIO\_Type \*base, uint32\_t mask)
 

*Clears pin interrupt flag.*

## 15.3 Data Structure Documentation

### 15.3.1 struct \_gpio\_pin\_config

#### Data Fields

- [gpio\\_pin\\_direction\\_t](#) direction
 

*Specifies the pin direction.*
- [uint8\\_t](#) outputLogic
 

*Set a default output logic, which has no use in input.*
- [gpio\\_interrupt\\_mode\\_t](#) interruptMode
 

*Specifies the pin interrupt mode, a value of [gpio\\_interrupt\\_mode\\_t](#).*

#### Field Documentation

- (1) [gpio\\_pin\\_direction\\_t](#) \_gpio\_pin\_config::direction
- (2) [gpio\\_interrupt\\_mode\\_t](#) \_gpio\_pin\_config::interruptMode

## 15.4 Macro Definition Documentation

### 15.4.1 #define FSL\_GPIO\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 6))

## 15.5 Typedef Documentation

### 15.5.1 [typedef enum \\_gpio\\_pin\\_direction gpio\\_pin\\_direction\\_t](#)

### 15.5.2 [typedef enum \\_gpio\\_interrupt\\_mode gpio\\_interrupt\\_mode\\_t](#)

### 15.5.3 [typedef struct \\_gpio\\_pin\\_config gpio\\_pin\\_config\\_t](#)

## 15.6 Enumeration Type Documentation

### 15.6.1 enum \_gpio\_pin\_direction

Enumerator

*kGPIO\_DigitalInput* Set current pin as digital input.

*kGPIO\_DigitalOutput* Set current pin as digital output.

### 15.6.2 enum \_gpio\_interrupt\_mode

Enumerator

*kGPIO\_NoIntmode* Set current pin general IO functionality.

*kGPIO\_IntLowLevel* Set current pin interrupt is low-level sensitive.

*kGPIO\_IntHighLevel* Set current pin interrupt is high-level sensitive.

*kGPIO\_IntRisingEdge* Set current pin interrupt is rising-edge sensitive.

*kGPIO\_IntFallingEdge* Set current pin interrupt is falling-edge sensitive.

*kGPIO\_IntRisingOrFallingEdge* Enable the edge select bit to override the ICR register's configuration.

## 15.7 Function Documentation

### 15.7.1 void GPIO\_PinInit ( **GPIO\_Type** \* *base*, **uint32\_t** *pin*, const **gpio\_pin\_config\_t** \* *Config* )

Parameters

|               |                                                                                                       |
|---------------|-------------------------------------------------------------------------------------------------------|
| <i>base</i>   | GPIO base pointer.                                                                                    |
| <i>pin</i>    | Specifies the pin number                                                                              |
| <i>Config</i> | pointer to a <a href="#">gpio_pin_config_t</a> structure that contains the configuration information. |

### 15.7.2 void GPIO\_PinWrite ( **GPIO\_Type** \* *base*, **uint32\_t** *pin*, **uint8\_t** *output* )

Parameters

|               |                                                                                                                                   |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | GPIO base pointer.                                                                                                                |
| <i>pin</i>    | GPIO port pin number.                                                                                                             |
| <i>output</i> | GPIO pin output logic level.<br>• 0: corresponding pin output low-logic level.<br>• 1: corresponding pin output high-logic level. |

### 15.7.3 static void GPIO\_WritePinOutput ( **GPIO\_Type** \* *base*, **uint32\_t** *pin*, **uint8\_t** *output* ) [inline], [static]

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PinWrite](#).

### 15.7.4 static void GPIO\_PortSet ( **GPIO\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.) |
| <i>mask</i> | GPIO pin number macro                                          |

### 15.7.5 static void GPIO\_SetPinsOutput ( **GPIO\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PortSet](#).

### 15.7.6 static void GPIO\_PortClear ( **GPIO\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

---

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.) |
| <i>mask</i> | GPIO pin number macro                                          |

**15.7.7 static void GPIO\_Clear PinsOutput ( GPIO\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PortClear](#).

**15.7.8 static void GPIO\_PortToggle ( GPIO\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | GPIO peripheral base pointer (GPIO1, GPIO2, GPIO3, and so on.) |
| <i>mask</i> | GPIO pin number macro                                          |

**15.7.9 static uint32\_t GPIO\_PinRead ( GPIO\_Type \* *base*, uint32\_t *pin* )  
[inline], [static]**

Parameters

|             |                       |
|-------------|-----------------------|
| <i>base</i> | GPIO base pointer.    |
| <i>pin</i>  | GPIO port pin number. |

Return values

|             |                   |
|-------------|-------------------|
| <i>GPIO</i> | port input value. |
|-------------|-------------------|

**15.7.10 static uint32\_t GPIO\_ReadPinInput ( GPIO\_Type \* *base*, uint32\_t *pin* )  
[inline], [static]**

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PinRead](#).

15.7.11 **static uint8\_t GPIO\_PinReadPadStatus ( GPIO\_Type \* *base*, uint32\_t *pin* )**  
[**inline**], [**static**]

Parameters

|             |                       |
|-------------|-----------------------|
| <i>base</i> | GPIO base pointer.    |
| <i>pin</i>  | GPIO port pin number. |

Return values

|             |                       |
|-------------|-----------------------|
| <i>GPIO</i> | pin pad status value. |
|-------------|-----------------------|

### 15.7.12 static uint8\_t GPIO\_ReadPadStatus ( *GPIO\_Type* \* *base*, *uint32\_t* *pin* ) [inline], [static]

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PinReadPadStatus](#).

### 15.7.13 void GPIO\_PinSetInterruptConfig ( *GPIO\_Type* \* *base*, *uint32\_t* *pin*, *gpio\_interrupt\_mode\_t* *pinInterruptMode* )

Parameters

|                          |                                                                                                            |
|--------------------------|------------------------------------------------------------------------------------------------------------|
| <i>base</i>              | GPIO base pointer.                                                                                         |
| <i>pin</i>               | GPIO port pin number.                                                                                      |
| <i>pinInterrupt-Mode</i> | pointer to a <a href="#">gpio_interrupt_mode_t</a> structure that contains the interrupt mode information. |

### 15.7.14 static void GPIO\_SetPinInterruptConfig ( *GPIO\_Type* \* *base*, *uint32\_t* *pin*, *gpio\_interrupt\_mode\_t* *pinInterruptMode* ) [inline], [static]

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PinSetInterruptConfig](#).

### 15.7.15 static void GPIO\_PortEnableInterrupts ( *GPIO\_Type* \* *base*, *uint32\_t* *mask* ) [inline], [static]

Parameters

|             |                        |
|-------------|------------------------|
| <i>base</i> | GPIO base pointer.     |
| <i>mask</i> | GPIO pin number macro. |

**15.7.16 static void GPIO\_EnableInterrupts ( GPIO\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

|             |                        |
|-------------|------------------------|
| <i>base</i> | GPIO base pointer.     |
| <i>mask</i> | GPIO pin number macro. |

**15.7.17 static void GPIO\_PortDisableInterrupts ( GPIO\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

|             |                        |
|-------------|------------------------|
| <i>base</i> | GPIO base pointer.     |
| <i>mask</i> | GPIO pin number macro. |

**15.7.18 static void GPIO\_DisableInterrupts ( GPIO\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

**Deprecated** Do not use this function. It has been superceded by [GPIO\\_PortDisableInterrupts](#).

**15.7.19 static uint32\_t GPIO\_PortGetInterruptFlags ( GPIO\_Type \* *base* )  
[inline], [static]**

Parameters

---

|             |                    |
|-------------|--------------------|
| <i>base</i> | GPIO base pointer. |
|-------------|--------------------|

Return values

|                |                            |
|----------------|----------------------------|
| <i>current</i> | pin interrupt status flag. |
|----------------|----------------------------|

### **15.7.20 static uint32\_t GPIO\_GetPinsInterruptFlags ( GPIO\_Type \* *base* ) [inline], [static]**

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | GPIO base pointer. |
|-------------|--------------------|

Return values

|                |                            |
|----------------|----------------------------|
| <i>current</i> | pin interrupt status flag. |
|----------------|----------------------------|

### **15.7.21 static void GPIO\_PortClearInterruptFlags ( GPIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

Status flags are cleared by writing a 1 to the corresponding bit position.

Parameters

|             |                        |
|-------------|------------------------|
| <i>base</i> | GPIO base pointer.     |
| <i>mask</i> | GPIO pin number macro. |

### **15.7.22 static void GPIO\_ClearPinsInterruptFlags ( GPIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

Status flags are cleared by writing a 1 to the corresponding bit position.

Parameters

|             |                        |
|-------------|------------------------|
| <i>base</i> | GPIO base pointer.     |
| <i>mask</i> | GPIO pin number macro. |

# Chapter 16

## I2C: Inter-Integrated Circuit Driver

### 16.1 Overview

#### Modules

- I2C CMSIS Driver
- I2C Driver
- I2C FreeRTOS Driver

## 16.2 I2C Driver

### 16.2.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Inter-Integrated Circuit (I2C) module of MCUXpresso SDK devices.

The I2C driver includes functional APIs and transactional APIs.

Functional APIs target the low-level APIs. Functional APIs can be used for the I2C master/slave initialization/configuration/operation for optimization/customization purpose. Using the functional APIs requires knowing the I2C master peripheral and how to organize functional APIs to meet the application requirements. The I2C functional operation groups provide the functional APIs set.

Transactional APIs target the high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code using the functional APIs or accessing the hardware registers.

Transactional APIs support asynchronous transfer. This means that the functions [I2C\\_MasterTransferNonBlocking\(\)](#) set up the interrupt non-blocking transfer. When the transfer completes, the upper layer is notified through a callback function with the status.

### 16.2.2 Typical use case

#### 16.2.2.1 Master Operation in functional method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/i2c

#### 16.2.2.2 Master Operation in interrupt transactional method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/i2c

#### 16.2.2.3 Slave Operation in functional method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/i2c

#### 16.2.2.4 Slave Operation in interrupt transactional method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/i2c

## Data Structures

- struct [\\_i2c\\_master\\_config](#)

- struct [\\_i2c\\_master\\_transfer](#)  
*I2C master transfer structure. [More...](#)*
- struct [\\_i2c\\_master\\_handle](#)  
*I2C master handle structure. [More...](#)*
- struct [\\_i2c\\_slave\\_config](#)  
*I2C slave user configuration. [More...](#)*
- struct [\\_i2c\\_slave\\_transfer](#)  
*I2C slave transfer structure. [More...](#)*
- struct [\\_i2c\\_slave\\_handle](#)  
*I2C slave handle structure. [More...](#)*

## Macros

- #define [I2C\\_RETRY\\_TIMES](#) 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/  
*Retry times for waiting flag.*

## TypeDefs

- typedef enum [\\_i2c\\_direction](#) [i2c\\_direction\\_t](#)  
*The direction of master and slave transfers.*
- typedef struct [\\_i2c\\_master\\_config](#) [i2c\\_master\\_config\\_t](#)  
*I2C master user configuration.*
- typedef struct [\\_i2c\\_master\\_handle](#) [i2c\\_master\\_handle\\_t](#)  
*I2C master handle typedef.*
- typedef void(\* [i2c\\_master\\_transfer\\_callback\\_t](#) )(I2C\_Type \*base, [i2c\\_master\\_handle\\_t](#) \*handle, [status\\_t](#) status, void \*userData)  
*I2C master transfer callback typedef.*
- typedef struct [\\_i2c\\_master\\_transfer](#) [i2c\\_master\\_transfer\\_t](#)  
*I2C master transfer structure.*
- typedef enum [\\_i2c\\_slave\\_transfer\\_event](#) [i2c\\_slave\\_transfer\\_event\\_t](#)  
*Set of events sent to the callback for nonblocking slave transfers.*
- typedef struct [\\_i2c\\_slave\\_handle](#) [i2c\\_slave\\_handle\\_t](#)  
*I2C slave handle typedef.*
- typedef struct [\\_i2c\\_slave\\_config](#) [i2c\\_slave\\_config\\_t](#)  
*I2C slave user configuration.*
- typedef struct [\\_i2c\\_slave\\_transfer](#) [i2c\\_slave\\_transfer\\_t](#)  
*I2C slave transfer structure.*
- typedef void(\* [i2c\\_slave\\_transfer\\_callback\\_t](#) )(I2C\_Type \*base, [i2c\\_slave\\_transfer\\_t](#) \*xfer, void \*userData)  
*I2C slave transfer callback typedef.*

## Enumerations

- enum {
   
kStatus\_I2C\_Busy = MAKE\_STATUS(kStatusGroup\_I2C, 0),
   
kStatus\_I2C\_Idle = MAKE\_STATUS(kStatusGroup\_I2C, 1),
   
kStatus\_I2C\_Nak = MAKE\_STATUS(kStatusGroup\_I2C, 2),
   
kStatus\_I2C\_ArbitrationLost = MAKE\_STATUS(kStatusGroup\_I2C, 3),
   
kStatus\_I2C\_Timeout = MAKE\_STATUS(kStatusGroup\_I2C, 4),
   
kStatus\_I2C\_Addr\_Nak = MAKE\_STATUS(kStatusGroup\_I2C, 5) }

*I2C status return codes.*

- enum \_i2c\_flags {
   
kI2C\_ReceiveNakFlag = I2C\_I2SR\_RXAK\_MASK,
   
kI2C\_IntPendingFlag = I2C\_I2SR\_IIF\_MASK,
   
kI2C\_TransferDirectionFlag = I2C\_I2SR\_SRW\_MASK,
   
kI2C\_ArbitrationLostFlag = I2C\_I2SR\_IAL\_MASK,
   
kI2C\_BusBusyFlag = I2C\_I2SR\_IBB\_MASK,
   
kI2C\_AddressMatchFlag = I2C\_I2SR\_IAAS\_MASK,
   
kI2C\_TransferCompleteFlag = I2C\_I2SR\_ICF\_MASK }

*I2C peripheral flags.*

- enum \_i2c\_interrupt\_enable { kI2C\_GlobalInterruptEnable = I2C\_I2CR\_IIEN\_MASK }

*I2C feature interrupt source.*

- enum \_i2c\_direction {
   
kI2C\_Write = 0x0U,
   
kI2C\_Read = 0x1U }

*The direction of master and slave transfers.*

- enum \_i2c\_master\_transfer\_flags {
   
kI2C\_TransferDefaultFlag = 0x0U,
   
kI2C\_TransferNoStartFlag = 0x1U,
   
kI2C\_TransferRepeatedStartFlag = 0x2U,
   
kI2C\_TransferNoStopFlag = 0x4U }

*I2C transfer control flag.*

- enum \_i2c\_slave\_transfer\_event {
   
kI2C\_SlaveAddressMatchEvent = 0x01U,
   
kI2C\_SlaveTransmitEvent = 0x02U,
   
kI2C\_SlaveReceiveEvent = 0x04U,
   
kI2C\_SlaveTransmitAckEvent = 0x08U,
   
kI2C\_SlaveCompletionEvent = 0x20U,
   
kI2C\_SlaveAllEvents }

*Set of events sent to the callback for nonblocking slave transfers.*

## Driver version

- #define **FSL\_I2C\_DRIVER\_VERSION** (MAKE\_VERSION(2, 0, 7))
- I2C driver version.*

## Initialization and deinitialization

- void **I2C\_MasterInit** (I2C\_Type \*base, const **i2c\_master\_config\_t** \*masterConfig, uint32\_t srcClock\_Hz)  
*Initializes the I2C peripheral.*
- void **I2C\_MasterDeinit** (I2C\_Type \*base)  
*De-initializes the I2C master peripheral.*
- void **I2C\_MasterGetDefaultConfig** (**i2c\_master\_config\_t** \*masterConfig)  
*Sets the I2C master configuration structure to default values.*
- void **I2C\_SlaveInit** (I2C\_Type \*base, const **i2c\_slave\_config\_t** \*slaveConfig)  
*Initializes the I2C peripheral.*
- void **I2C\_SlaveDeinit** (I2C\_Type \*base)  
*De-initializes the I2C slave peripheral.*
- void **I2C\_SlaveGetDefaultConfig** (**i2c\_slave\_config\_t** \*slaveConfig)  
*Sets the I2C slave configuration structure to default values.*
- static void **I2C\_Enable** (I2C\_Type \*base, bool enable)  
*Enables or disables the I2C peripheral operation.*

## Status

- static uint32\_t **I2C\_MasterGetStatusFlags** (I2C\_Type \*base)  
*Gets the I2C status flags.*
- static void **I2C\_MasterClearStatusFlags** (I2C\_Type \*base, uint32\_t statusMask)  
*Clears the I2C status flag state.*
- static uint32\_t **I2C\_SlaveGetStatusFlags** (I2C\_Type \*base)  
*Gets the I2C status flags.*
- static void **I2C\_SlaveClearStatusFlags** (I2C\_Type \*base, uint32\_t statusMask)  
*Clears the I2C status flag state.*

## Interrupts

- void **I2C\_EnableInterrupts** (I2C\_Type \*base, uint32\_t mask)  
*Enables I2C interrupt requests.*
- void **I2C\_DisableInterrupts** (I2C\_Type \*base, uint32\_t mask)  
*Disables I2C interrupt requests.*

## Bus Operations

- void **I2C\_MasterSetBaudRate** (I2C\_Type \*base, uint32\_t baudRate\_Bps, uint32\_t srcClock\_Hz)  
*Sets the I2C master transfer baud rate.*
- **status\_t I2C\_MasterStart** (I2C\_Type \*base, uint8\_t address, **i2c\_direction\_t** direction)  
*Sends a START on the I2C bus.*
- **status\_t I2C\_MasterStop** (I2C\_Type \*base)  
*Sends a STOP signal on the I2C bus.*
- **status\_t I2C\_MasterRepeatedStart** (I2C\_Type \*base, uint8\_t address, **i2c\_direction\_t** direction)  
*Sends a REPEATED START on the I2C bus.*

- `status_t I2C_MasterWriteBlocking (I2C_Type *base, const uint8_t *txBuff, size_t txSize, uint32_t flags)`  
*Performs a polling send transaction on the I2C bus.*
- `status_t I2C_MasterReadBlocking (I2C_Type *base, uint8_t *rxBuff, size_t rxSize, uint32_t flags)`  
*Performs a polling receive transaction on the I2C bus.*
- `status_t I2C_SlaveWriteBlocking (I2C_Type *base, const uint8_t *txBuff, size_t txSize)`  
*Performs a polling send transaction on the I2C bus.*
- `status_t I2C_SlaveReadBlocking (I2C_Type *base, uint8_t *rxBuff, size_t rxSize)`  
*Performs a polling receive transaction on the I2C bus.*
- `status_t I2C_MasterTransferBlocking (I2C_Type *base, i2c_master_transfer_t *xfer)`  
*Performs a master polling transfer on the I2C bus.*

## Transactional

- `void I2C_MasterTransferCreateHandle (I2C_Type *base, i2c_master_handle_t *handle, i2c_master_transfer_callback_t callback, void *userData)`  
*Initializes the I2C handle which is used in transactional functions.*
- `status_t I2C_MasterTransferNonBlocking (I2C_Type *base, i2c_master_handle_t *handle, i2c_master_transfer_t *xfer)`  
*Performs a master interrupt non-blocking transfer on the I2C bus.*
- `status_t I2C_MasterTransferGetCount (I2C_Type *base, i2c_master_handle_t *handle, size_t *count)`  
*Gets the master transfer status during a interrupt non-blocking transfer.*
- `status_t I2C_MasterTransferAbort (I2C_Type *base, i2c_master_handle_t *handle)`  
*Aborts an interrupt non-blocking transfer early.*
- `void I2C_MasterTransferHandleIRQ (I2C_Type *base, void *i2cHandle)`  
*Master interrupt handler.*
- `void I2C_SlaveTransferCreateHandle (I2C_Type *base, i2c_slave_handle_t *handle, i2c_slave_transfer_callback_t callback, void *userData)`  
*Initializes the I2C handle which is used in transactional functions.*
- `status_t I2C_SlaveTransferNonBlocking (I2C_Type *base, i2c_slave_handle_t *handle, uint32_t eventMask)`  
*Starts accepting slave transfers.*
- `void I2C_SlaveTransferAbort (I2C_Type *base, i2c_slave_handle_t *handle)`  
*Aborts the slave transfer.*
- `status_t I2C_SlaveTransferGetCount (I2C_Type *base, i2c_slave_handle_t *handle, size_t *count)`  
*Gets the slave transfer remaining bytes during a interrupt non-blocking transfer.*
- `void I2C_SlaveTransferHandleIRQ (I2C_Type *base, void *i2cHandle)`  
*Slave interrupt handler.*

### 16.2.3 Data Structure Documentation

#### 16.2.3.1 struct \_i2c\_master\_config

##### Data Fields

- `bool enableMaster`

- **uint32\_t baudRate\_Bps**  
*Baud rate configuration of I2C peripheral.*

### Field Documentation

- (1) **bool \_i2c\_master\_config::enableMaster**
- (2) **uint32\_t \_i2c\_master\_config::baudRate\_Bps**

### 16.2.3.2 struct \_i2c\_master\_transfer

#### Data Fields

- **uint32\_t flags**  
*A transfer flag which controls the transfer.*
- **uint8\_t slaveAddress**  
*7-bit slave address.*
- **i2c\_direction\_t direction**  
*A transfer direction, read or write.*
- **uint32\_t subaddress**  
*A sub address.*
- **uint8\_t subaddressSize**  
*A size of the command buffer.*
- **uint8\_t \*volatile data**  
*A transfer buffer.*
- **volatile size\_t dataSize**  
*A transfer size.*

### Field Documentation

- (1) **uint32\_t \_i2c\_master\_transfer::flags**
- (2) **uint8\_t \_i2c\_master\_transfer::slaveAddress**
- (3) **i2c\_direction\_t \_i2c\_master\_transfer::direction**
- (4) **uint32\_t \_i2c\_master\_transfer::subaddress**

Transferred MSB first.

- (5) `uint8_t _i2c_master_transfer::subaddressSize`
- (6) `uint8_t* volatile _i2c_master_transfer::data`
- (7) `volatile size_t _i2c_master_transfer::dataSize`

### 16.2.3.3 struct \_i2c\_master\_handle

#### Data Fields

- `i2c_master_transfer_t transfer`  
*I2C master transfer copy.*
- `size_t transferSize`  
*Total bytes to be transferred.*
- `uint8_t state`  
*A transfer state maintained during transfer.*
- `i2c_master_transfer_callback_t completionCallback`  
*A callback function called when the transfer is finished.*
- `void * userData`  
*A callback parameter passed to the callback function.*

#### Field Documentation

- (1) `i2c_master_transfer_t _i2c_master_handle::transfer`
- (2) `size_t _i2c_master_handle::transferSize`
- (3) `uint8_t _i2c_master_handle::state`
- (4) `i2c_master_transfer_callback_t _i2c_master_handle::completionCallback`
- (5) `void* _i2c_master_handle::userData`

### 16.2.3.4 struct \_i2c\_slave\_config

#### Data Fields

- `bool enableSlave`  
*Enables the I2C peripheral at initialization time.*
- `uint16_t slaveAddress`  
*A slave address configuration.*

## Field Documentation

- (1) **bool \_i2c\_slave\_config::enableSlave**
- (2) **uint16\_t \_i2c\_slave\_config::slaveAddress**

### 16.2.3.5 struct \_i2c\_slave\_transfer

#### Data Fields

- **i2c\_slave\_transfer\_event\_t event**  
*A reason that the callback is invoked.*
- **uint8\_t \*volatile data**  
*A transfer buffer.*
- **volatile size\_t dataSize**  
*A transfer size.*
- **status\_t completionStatus**  
*Success or error code describing how the transfer completed.*
- **size\_t transferredCount**  
*A number of bytes actually transferred since the start or since the last repeated start.*

## Field Documentation

- (1) **i2c\_slave\_transfer\_event\_t \_i2c\_slave\_transfer::event**
- (2) **uint8\_t\* volatile \_i2c\_slave\_transfer::data**
- (3) **volatile size\_t \_i2c\_slave\_transfer::dataSize**
- (4) **status\_t \_i2c\_slave\_transfer::completionStatus**

Only applies for [kI2C\\_SlaveCompletionEvent](#).

- (5) **size\_t \_i2c\_slave\_transfer::transferredCount**

### 16.2.3.6 struct \_i2c\_slave\_handle

#### Data Fields

- **volatile uint8\_t state**  
*A transfer state maintained during transfer.*
- **i2c\_slave\_transfer\_t transfer**  
*I2C slave transfer copy.*
- **uint32\_t eventMask**  
*A mask of enabled events.*
- **i2c\_slave\_transfer\_callback\_t callback**  
*A callback function called at the transfer event.*
- **void \*userData**  
*A callback parameter passed to the callback.*

## Field Documentation

- (1) volatile uint8\_t \_i2c\_slave\_handle::state
- (2) i2c\_slave\_transfer\_t \_i2c\_slave\_handle::transfer
- (3) uint32\_t \_i2c\_slave\_handle::eventMask
- (4) i2c\_slave\_transfer\_callback\_t \_i2c\_slave\_handle::callback
- (5) void\* \_i2c\_slave\_handle::userData

## 16.2.4 Macro Definition Documentation

**16.2.4.1 #define FSL\_I2C\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 7))**

**16.2.4.2 #define I2C\_RETRY\_TIMES 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/**

## 16.2.5 Typedef Documentation

**16.2.5.1 typedef enum \_i2c\_direction i2c\_direction\_t**

**16.2.5.2 typedef struct \_i2c\_master\_config i2c\_master\_config\_t**

**16.2.5.3 typedef struct \_i2c\_master\_handle i2c\_master\_handle\_t**

**16.2.5.4 typedef void(\* i2c\_master\_transfer\_callback\_t)(I2C\_Type \*base, i2c\_master\_handle\_t \*handle, status\_t status, void \*userData)**

**16.2.5.5 typedef struct \_i2c\_master\_transfer i2c\_master\_transfer\_t**

**16.2.5.6 typedef enum \_i2c\_slave\_transfer\_event i2c\_slave\_transfer\_event\_t**

These event enumerations are used for two related purposes. First, a bit mask created by OR'ing together events is passed to [I2C\\_SlaveTransferNonBlocking\(\)](#) to specify which events to enable. Then, when the slave callback is invoked, it is passed the current event through its *transfer* parameter.

## Note

These enumerations are meant to be OR'd together to form a bit mask of events.

**16.2.5.7 `typedef struct _i2c_slave_handle i2c_slave_handle_t`****16.2.5.8 `typedef struct _i2c_slave_config i2c_slave_config_t`****16.2.5.9 `typedef struct _i2c_slave_transfer i2c_slave_transfer_t`****16.2.5.10 `typedef void(* i2c_slave_transfer_callback_t)(I2C_Type *base, i2c_slave_transfer_t *xfer, void *userData)`****16.2.6 Enumeration Type Documentation****16.2.6.1 anonymous enum**

## Enumerator

*kStatus\_I2C\_Busy* I2C is busy with current transfer.

*kStatus\_I2C\_Idle* Bus is Idle.

*kStatus\_I2C\_Nak* NAK received during transfer.

*kStatus\_I2C\_ArbitrationLost* Arbitration lost during transfer.

*kStatus\_I2C\_Timeout* Timeout polling status flags.

*kStatus\_I2C\_Addr\_Nak* NAK received during the address probe.

**16.2.6.2 `enum _i2c_flags`**

The following status register flags can be cleared:

- [kI2C\\_ArbitrationLostFlag](#)
- [kI2C\\_IntPendingFlag](#)

## Note

These enumerations are meant to be OR'd together to form a bit mask.

## Enumerator

*kI2C\_ReceiveNakFlag* I2C receive NAK flag.

*kI2C\_IntPendingFlag* I2C interrupt pending flag.

*kI2C\_TransferDirectionFlag* I2C transfer direction flag.

*kI2C\_ArbitrationLostFlag* I2C arbitration lost flag.

*kI2C\_BusBusyFlag* I2C bus busy flag.

*kI2C\_AddressMatchFlag* I2C address match flag.

*kI2C\_TransferCompleteFlag* I2C transfer complete flag.

### 16.2.6.3 enum \_i2c\_interrupt\_enable

Enumerator

**kI2C\_GlobalInterruptEnable** I2C global interrupt.

### 16.2.6.4 enum \_i2c\_direction

Enumerator

**kI2C\_Write** Master transmits to the slave.

**kI2C\_Read** Master receives from the slave.

### 16.2.6.5 enum \_i2c\_master\_transfer\_flags

Enumerator

**kI2C\_TransferDefaultFlag** A transfer starts with a start signal, stops with a stop signal.

**kI2C\_TransferNoStartFlag** A transfer starts without a start signal, only support write only or write+read with no start flag, do not support read only with no start flag.

**kI2C\_TransferRepeatedStartFlag** A transfer starts with a repeated start signal.

**kI2C\_TransferNoStopFlag** A transfer ends without a stop signal.

### 16.2.6.6 enum \_i2c\_slave\_transfer\_event

These event enumerations are used for two related purposes. First, a bit mask created by OR'ing together events is passed to [I2C\\_SlaveTransferNonBlocking\(\)](#) to specify which events to enable. Then, when the slave callback is invoked, it is passed the current event through its *transfer* parameter.

Note

These enumerations are meant to be OR'd together to form a bit mask of events.

Enumerator

**kI2C\_SlaveAddressMatchEvent** Received the slave address after a start or repeated start.

**kI2C\_SlaveTransmitEvent** A callback is requested to provide data to transmit (slave-transmitter role).

**kI2C\_SlaveReceiveEvent** A callback is requested to provide a buffer in which to place received data (slave-receiver role).

**kI2C\_SlaveTransmitAckEvent** A callback needs to either transmit an ACK or NACK.

**kI2C\_SlaveCompletionEvent** A stop was detected or finished transfer, completing the transfer.

**kI2C\_SlaveAllEvents** A bit mask of all available events.

## 16.2.7 Function Documentation

### 16.2.7.1 void I2C\_MasterInit ( **I2C\_Type** \* *base*, const **i2c\_master\_config\_t** \* *masterConfig*, uint32\_t *srcClock\_Hz* )

Call this API to ungate the I2C clock and configure the I2C with master configuration.

#### Note

This API should be called at the beginning of the application. Otherwise, any operation to the I2C module can cause a hard fault because the clock is not enabled. The configuration structure can be custom filled or it can be set with default values by using the [I2C\\_MasterGetDefaultConfig\(\)](#). After calling this API, the master is ready to transfer. This is an example.

```
* i2c_master_config_t config = {
* .enableMaster = true,
* .baudRate_Bps = 100000
* };
* I2C_MasterInit(I2C0, &config, 12000000U);
*
```

#### Parameters

|                     |                                                 |
|---------------------|-------------------------------------------------|
| <i>base</i>         | I2C base pointer                                |
| <i>masterConfig</i> | A pointer to the master configuration structure |
| <i>srcClock_Hz</i>  | I2C peripheral clock frequency in Hz            |

### 16.2.7.2 void I2C\_MasterDeinit ( **I2C\_Type** \* *base* )

Call this API to gate the I2C clock. The I2C master module can't work unless the I2C\_MasterInit is called.

#### Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | I2C base pointer |
|-------------|------------------|

### 16.2.7.3 void I2C\_MasterGetDefaultConfig ( **i2c\_master\_config\_t** \* *masterConfig* )

The purpose of this API is to get the configuration structure initialized for use in the [I2C\\_MasterInit\(\)](#). Use the initialized structure unchanged in the [I2C\\_MasterInit\(\)](#) or modify the structure before calling the [I2C\\_MasterInit\(\)](#). This is an example.

```
* i2c_master_config_t config;
* I2C_MasterGetDefaultConfig(&config);
*
```

## Parameters

|                     |                                                  |
|---------------------|--------------------------------------------------|
| <i>masterConfig</i> | A pointer to the master configuration structure. |
|---------------------|--------------------------------------------------|

**16.2.7.4 void I2C\_SlaveInit ( I2C\_Type \* *base*, const i2c\_slave\_config\_t \* *slaveConfig* )**

Call this API to ungate the I2C clock and initialize the I2C with the slave configuration.

## Note

This API should be called at the beginning of the application. Otherwise, any operation to the I2C module can cause a hard fault because the clock is not enabled. The configuration structure can partly be set with default values by [I2C\\_SlaveGetDefaultConfig\(\)](#) or it can be custom filled by the user. This is an example.

```
* i2c_slave_config_t config = {
* .enableSlave = true,
* .slaveAddress = 0x1DU,
* };
* I2C_SlaveInit(I2C0, &config);
*
```

## Parameters

|                    |                                                |
|--------------------|------------------------------------------------|
| <i>base</i>        | I2C base pointer                               |
| <i>slaveConfig</i> | A pointer to the slave configuration structure |

**16.2.7.5 void I2C\_SlaveDeinit ( I2C\_Type \* *base* )**

Calling this API gates the I2C clock. The I2C slave module can't work unless the I2C\_SlaveInit is called to enable the clock.

## Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | I2C base pointer |
|-------------|------------------|

**16.2.7.6 void I2C\_SlaveGetDefaultConfig ( i2c\_slave\_config\_t \* *slaveConfig* )**

The purpose of this API is to get the configuration structure initialized for use in the [I2C\\_SlaveInit\(\)](#). Modify fields of the structure before calling the [I2C\\_SlaveInit\(\)](#). This is an example.

```
* i2c_slave_config_t config;
* I2C_SlaveGetDefaultConfig(&config);
*
```

Parameters

|                    |                                                 |
|--------------------|-------------------------------------------------|
| <i>slaveConfig</i> | A pointer to the slave configuration structure. |
|--------------------|-------------------------------------------------|

#### 16.2.7.7 static void I2C\_Enable ( I2C\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                      |
|---------------|------------------------------------------------------|
| <i>base</i>   | I2C base pointer                                     |
| <i>enable</i> | Pass true to enable and false to disable the module. |

#### 16.2.7.8 static uint32\_t I2C\_MasterGetStatusFlags ( I2C\_Type \* *base* ) [inline], [static]

Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | I2C base pointer |
|-------------|------------------|

Returns

status flag, use status flag to AND [\\_i2c\\_flags](#) to get the related status.

#### 16.2.7.9 static void I2C\_MasterClearStatusFlags ( I2C\_Type \* *base*, uint32\_t *statusMask* ) [inline], [static]

The following status register flags can be cleared kI2C\_ArbitrationLostFlag and kI2C\_IntPendingFlag.

Parameters

|                   |                                                                                                                                                                                                                                    |
|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>       | I2C base pointer                                                                                                                                                                                                                   |
| <i>statusMask</i> | The status flag mask, defined in type i2c_status_flag_t. The parameter can be any combination of the following values: <ul style="list-style-type: none"> <li>• kI2C_ArbitrationLostFlag</li> <li>• kI2C_IntPendingFlag</li> </ul> |

#### 16.2.7.10 static uint32\_t I2C\_SlaveGetStatusFlags ( I2C\_Type \* *base* ) [inline], [static]

Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | I2C base pointer |
|-------------|------------------|

Returns

status flag, use status flag to AND [\\_i2c\\_flags](#) to get the related status.

#### 16.2.7.11 static void I2C\_SlaveClearStatusFlags ( I2C\_Type \* *base*, uint32\_t *statusMask* ) [inline], [static]

The following status register flags can be cleared kI2C\_ArbitrationLostFlag and kI2C\_IntPendingFlag

Parameters

|                   |                                                                                                                                                                                                           |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>       | I2C base pointer                                                                                                                                                                                          |
| <i>statusMask</i> | <p>The status flag mask, defined in type i2c_status_flag_t. The parameter can be any combination of the following values:</p> <ul style="list-style-type: none"> <li>• kI2C_IntPendingFlagFlag</li> </ul> |

#### 16.2.7.12 void I2C\_EnableInterrupts ( I2C\_Type \* *base*, uint32\_t *mask* )

Parameters

|             |                                                                                                                                                                                                                                                                                                 |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | I2C base pointer                                                                                                                                                                                                                                                                                |
| <i>mask</i> | <p>interrupt source The parameter can be combination of the following source if defined:</p> <ul style="list-style-type: none"> <li>• kI2C_GlobalInterruptEnable</li> <li>• kI2C_StopDetectInterruptEnable/kI2C_StartDetectInterruptEnable</li> <li>• kI2C_SdaTimeoutInterruptEnable</li> </ul> |

#### 16.2.7.13 void I2C\_DisableInterrupts ( I2C\_Type \* *base*, uint32\_t *mask* )

Parameters

|             |                                                                                                                                                                                                                                                                                      |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | I2C base pointer                                                                                                                                                                                                                                                                     |
| <i>mask</i> | interrupt source The parameter can be combination of the following source if defined: <ul style="list-style-type: none"><li>• kI2C_GlobalInterruptEnable</li><li>• kI2C_StopDetectInterruptEnable/kI2C_StartDetectInterruptEnable</li><li>• kI2C_SdaTimeoutInterruptEnable</li></ul> |

#### 16.2.7.14 void I2C\_MasterSetBaudRate ( I2C\_Type \* *base*, uint32\_t *baudRate\_Bps*, uint32\_t *srcClock\_Hz* )

Parameters

|                     |                            |
|---------------------|----------------------------|
| <i>base</i>         | I2C base pointer           |
| <i>baudRate_Bps</i> | the baud rate value in bps |
| <i>srcClock_Hz</i>  | Source clock               |

#### 16.2.7.15 status\_t I2C\_MasterStart ( I2C\_Type \* *base*, uint8\_t *address*, i2c\_direction\_t *direction* )

This function is used to initiate a new master mode transfer by sending the START signal. The slave address is sent following the I2C START signal.

Parameters

|                  |                                               |
|------------------|-----------------------------------------------|
| <i>base</i>      | I2C peripheral base pointer                   |
| <i>address</i>   | 7-bit slave device address.                   |
| <i>direction</i> | Master transfer directions(transmit/receive). |

Return values

|                         |                                     |
|-------------------------|-------------------------------------|
| <i>kStatus_Success</i>  | Successfully send the start signal. |
| <i>kStatus_I2C_Busy</i> | Current bus is busy.                |

#### 16.2.7.16 status\_t I2C\_MasterStop ( I2C\_Type \* *base* )

Return values

|                            |                                    |
|----------------------------|------------------------------------|
| <i>kStatus_Success</i>     | Successfully send the stop signal. |
| <i>kStatus_I2C_Timeout</i> | Send stop signal failed, timeout.  |

#### 16.2.7.17 status\_t I2C\_MasterRepeatedStart ( *I2C\_Type \* base*, *uint8\_t address*, *i2c\_direction\_t direction* )

Parameters

|                  |                                               |
|------------------|-----------------------------------------------|
| <i>base</i>      | I2C peripheral base pointer                   |
| <i>address</i>   | 7-bit slave device address.                   |
| <i>direction</i> | Master transfer directions(transmit/receive). |

Return values

|                         |                                                             |
|-------------------------|-------------------------------------------------------------|
| <i>kStatus_Success</i>  | Successfully send the start signal.                         |
| <i>kStatus_I2C_Busy</i> | Current bus is busy but not occupied by current I2C master. |

#### 16.2.7.18 status\_t I2C\_MasterWriteBlocking ( *I2C\_Type \* base*, *const uint8\_t \* txBuff*, *size\_t txSize*, *uint32\_t flags* )

Parameters

|               |                                                                                                                                                                     |
|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | The I2C peripheral base pointer.                                                                                                                                    |
| <i>txBuff</i> | The pointer to the data to be transferred.                                                                                                                          |
| <i>txSize</i> | The length in bytes of the data to be transferred.                                                                                                                  |
| <i>flags</i>  | Transfer control flag to decide whether need to send a stop, use <i>kI2C_TransferDefaultFlag</i> to issue a stop and <i>kI2C_TransferNoStop</i> to not send a stop. |

Return values

|                                    |                                              |
|------------------------------------|----------------------------------------------|
| <i>kStatus_Success</i>             | Successfully complete the data transmission. |
| <i>kStatus_I2C_ArbitrationLost</i> | Transfer error, arbitration lost.            |
| <i>kStatus_I2C_Nak</i>             | Transfer error, receive NAK during transfer. |

### 16.2.7.19 status\_t I2C\_MasterReadBlocking ( *I2C\_Type \* base*, *uint8\_t \* rxBuff*, *size\_t rxSize*, *uint32\_t flags* )

Note

The I2C\_MasterReadBlocking function stops the bus before reading the final byte. Without stopping the bus prior for the final read, the bus issues another read, resulting in garbage data being read into the data register.

Parameters

|               |                                                                                                                                                       |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | I2C peripheral base pointer.                                                                                                                          |
| <i>rxBuff</i> | The pointer to the data to store the received data.                                                                                                   |
| <i>rxSize</i> | The length in bytes of the data to be received.                                                                                                       |
| <i>flags</i>  | Transfer control flag to decide whether need to send a stop, use kI2C_TransferDefaultFlag to issue a stop and kI2C_TransferNoStop to not send a stop. |

Return values

|                            |                                              |
|----------------------------|----------------------------------------------|
| <i>kStatus_Success</i>     | Successfully complete the data transmission. |
| <i>kStatus_I2C_Timeout</i> | Send stop signal failed, timeout.            |

### 16.2.7.20 status\_t I2C\_SlaveWriteBlocking ( *I2C\_Type \* base*, *const uint8\_t \* txBuff*, *size\_t txSize* )

Parameters

|               |                                                    |
|---------------|----------------------------------------------------|
| <i>base</i>   | The I2C peripheral base pointer.                   |
| <i>txBuff</i> | The pointer to the data to be transferred.         |
| <i>txSize</i> | The length in bytes of the data to be transferred. |

Return values

|                                    |                                              |
|------------------------------------|----------------------------------------------|
| <i>kStatus_Success</i>             | Successfully complete the data transmission. |
| <i>kStatus_I2C_ArbitrationLost</i> | Transfer error, arbitration lost.            |
| <i>kStatus_I2C_Nak</i>             | Transfer error, receive NAK during transfer. |

### 16.2.7.21 status\_t I2C\_SlaveReadBlocking ( *I2C\_Type \* base*, *uint8\_t \* rxBuff*, *size\_t rxSize* )

Parameters

|               |                                                     |
|---------------|-----------------------------------------------------|
| <i>base</i>   | I2C peripheral base pointer.                        |
| <i>rxBuff</i> | The pointer to the data to store the received data. |
| <i>rxSize</i> | The length in bytes of the data to be received.     |

### 16.2.7.22 status\_t I2C\_MasterTransferBlocking ( I2C\_Type \* *base*, i2c\_master\_transfer\_t \* *xfer* )

Note

The API does not return until the transfer succeeds or fails due to arbitration lost or receiving a NAK.

Parameters

|             |                                    |
|-------------|------------------------------------|
| <i>base</i> | I2C peripheral base address.       |
| <i>xfer</i> | Pointer to the transfer structure. |

Return values

|                                     |                                              |
|-------------------------------------|----------------------------------------------|
| <i>kStatus_Success</i>              | Successfully complete the data transmission. |
| <i>kStatus_I2C_Busy</i>             | Previous transmission still not finished.    |
| <i>kStatus_I2C_Timeout</i>          | Transfer error, wait signal timeout.         |
| <i>kStatus_I2C_Arbitration-Lost</i> | Transfer error, arbitration lost.            |
| <i>kStatus_I2C_Nak</i>              | Transfer error, receive NAK during transfer. |

### 16.2.7.23 void I2C\_MasterTransferCreateHandle ( I2C\_Type \* *base*, i2c\_master\_handle\_t \* *handle*, i2c\_master\_transfer\_callback\_t *callback*, void \* *userData* )

Parameters

|                 |                                                                       |
|-----------------|-----------------------------------------------------------------------|
| <i>base</i>     | I2C base pointer.                                                     |
| <i>handle</i>   | pointer to i2c_master_handle_t structure to store the transfer state. |
| <i>callback</i> | pointer to user callback function.                                    |
| <i>userData</i> | user parameter passed to the callback function.                       |

### 16.2.7.24 status\_t I2C\_MasterTransferNonBlocking ( *I2C\_Type \* base*, *i2c\_master\_handle\_t \* handle*, *i2c\_master\_transfer\_t \* xfer* )

Note

Calling the API returns immediately after transfer initiates. The user needs to call I2C\_MasterGetTransferCount to poll the transfer status to check whether the transfer is finished. If the return status is not kStatus\_I2C\_Busy, the transfer is finished.

Parameters

|               |                                                                           |
|---------------|---------------------------------------------------------------------------|
| <i>base</i>   | I2C base pointer.                                                         |
| <i>handle</i> | pointer to i2c_master_handle_t structure which stores the transfer state. |
| <i>xfer</i>   | pointer to i2c_master_transfer_t structure.                               |

Return values

|                            |                                           |
|----------------------------|-------------------------------------------|
| <i>kStatus_Success</i>     | Successfully start the data transmission. |
| <i>kStatus_I2C_Busy</i>    | Previous transmission still not finished. |
| <i>kStatus_I2C_Timeout</i> | Transfer error, wait signal timeout.      |

### 16.2.7.25 status\_t I2C\_MasterTransferGetCount ( *I2C\_Type \* base*, *i2c\_master\_handle\_t \* handle*, *size\_t \* count* )

Parameters

|               |                                                                           |
|---------------|---------------------------------------------------------------------------|
| <i>base</i>   | I2C base pointer.                                                         |
| <i>handle</i> | pointer to i2c_master_handle_t structure which stores the transfer state. |
| <i>count</i>  | Number of bytes transferred so far by the non-blocking transaction.       |

Return values

|                                |                                |
|--------------------------------|--------------------------------|
| <i>kStatus_InvalidArgument</i> | count is Invalid.              |
| <i>kStatus_Success</i>         | Successfully return the count. |

### 16.2.7.26 status\_t I2C\_MasterTransferAbort ( *I2C\_Type \* base*, *i2c\_master\_handle\_t \* handle* )

## Note

This API can be called at any time when an interrupt non-blocking transfer initiates to abort the transfer early.

## Parameters

|               |                                                                          |
|---------------|--------------------------------------------------------------------------|
| <i>base</i>   | I2C base pointer.                                                        |
| <i>handle</i> | pointer to i2c_master_handle_t structure which stores the transfer state |

## Return values

|                            |                                  |
|----------------------------|----------------------------------|
| <i>kStatus_I2C_Timeout</i> | Timeout during polling flag.     |
| <i>kStatus_Success</i>     | Successfully abort the transfer. |

**16.2.7.27 void I2C\_MasterTransferHandleIRQ ( I2C\_Type \* *base*, void \* *i2cHandle* )**

## Parameters

|                  |                                           |
|------------------|-------------------------------------------|
| <i>base</i>      | I2C base pointer.                         |
| <i>i2cHandle</i> | pointer to i2c_master_handle_t structure. |

**16.2.7.28 void I2C\_SlaveTransferCreateHandle ( I2C\_Type \* *base*, i2c\_slave\_handle\_t \* *handle*, i2c\_slave\_transfer\_callback\_t *callback*, void \* *userData* )**

## Parameters

|                 |                                                                      |
|-----------------|----------------------------------------------------------------------|
| <i>base</i>     | I2C base pointer.                                                    |
| <i>handle</i>   | pointer to i2c_slave_handle_t structure to store the transfer state. |
| <i>callback</i> | pointer to user callback function.                                   |
| <i>userData</i> | user parameter passed to the callback function.                      |

**16.2.7.29 status\_t I2C\_SlaveTransferNonBlocking ( I2C\_Type \* *base*, i2c\_slave\_handle\_t \* *handle*, uint32\_t *eventMask* )**

Call this API after calling the [I2C\\_SlaveInit\(\)](#) and [I2C\\_SlaveTransferCreateHandle\(\)](#) to start processing transactions driven by an I2C master. The slave monitors the I2C bus and passes events to the callback that was passed into the call to [I2C\\_SlaveTransferCreateHandle\(\)](#). The callback is always invoked from the interrupt context.

The set of events received by the callback is customizable. To do so, set the *eventMask* parameter to the OR'd combination of `i2c_slave_transfer_event_t` enumerators for the events you wish to receive. The `kI2C_SlaveTransmitEvent` and `kLPI2C_SlaveReceiveEvent` events are always enabled and do not need to be included in the mask. Alternatively, pass 0 to get a default set of only the transmit and receive events that are always enabled. In addition, the `kI2C_SlaveAllEvents` constant is provided as a convenient way to enable all events.

#### Parameters

|                  |                                                                                                                                                                                                                                                                                              |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>      | The I2C peripheral base address.                                                                                                                                                                                                                                                             |
| <i>handle</i>    | Pointer to <code>i2c_slave_handle_t</code> structure which stores the transfer state.                                                                                                                                                                                                        |
| <i>eventMask</i> | Bit mask formed by OR'ing together <code>i2c_slave_transfer_event_t</code> enumerators to specify which events to send to the callback. Other accepted values are 0 to get a default set of only the transmit and receive events, and <code>kI2C_SlaveAllEvents</code> to enable all events. |

#### Return values

|                               |                                                           |
|-------------------------------|-----------------------------------------------------------|
| <code>kStatus_Success</code>  | Slave transfers were successfully started.                |
| <code>kStatus_I2C_Busy</code> | Slave transfers have already been started on this handle. |

### 16.2.7.30 void I2C\_SlaveTransferAbort ( `I2C_Type * base`, `i2c_slave_handle_t * handle` )

#### Note

This API can be called at any time to stop slave for handling the bus events.

#### Parameters

|               |                                                                                       |
|---------------|---------------------------------------------------------------------------------------|
| <i>base</i>   | I2C base pointer.                                                                     |
| <i>handle</i> | pointer to <code>i2c_slave_handle_t</code> structure which stores the transfer state. |

### 16.2.7.31 `status_t I2C_SlaveTransferGetCount ( I2C_Type * base, i2c_slave_handle_t * handle, size_t * count )`

#### Parameters

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | I2C base pointer.                                                   |
| <i>handle</i> | pointer to <code>i2c_slave_handle_t</code> structure.               |
| <i>count</i>  | Number of bytes transferred so far by the non-blocking transaction. |

Return values

|                                |                                |
|--------------------------------|--------------------------------|
| <i>kStatus_InvalidArgument</i> | count is Invalid.              |
| <i>kStatus_Success</i>         | Successfully return the count. |

#### 16.2.7.32 void I2C\_SlaveTransferHandleIRQ ( **I2C\_Type \* base**, **void \* i2cHandle** )

Parameters

|                  |                                                                         |
|------------------|-------------------------------------------------------------------------|
| <i>base</i>      | I2C base pointer.                                                       |
| <i>i2cHandle</i> | pointer to i2c_slave_handle_t structure which stores the transfer state |

## 16.3 I2C FreeRTOS Driver

### 16.3.1 Overview

#### Driver version

- `#define FSL_I2C_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 0, 7))`  
*I2C FreeRTOS driver version.*

#### I2C RTOS Operation

- `status_t I2C_RTOS_Init (i2c_rtos_handle_t *handle, I2C_Type *base, const i2c_master_config_t *masterConfig, uint32_t srcClock_Hz)`  
*Initializes I2C.*
- `status_t I2C_RTOS_Deinit (i2c_rtos_handle_t *handle)`  
*Deinitializes the I2C.*
- `status_t I2C_RTOS_Transfer (i2c_rtos_handle_t *handle, i2c_master_transfer_t *transfer)`  
*Performs the I2C transfer.*

### 16.3.2 Macro Definition Documentation

#### 16.3.2.1 `#define FSL_I2C_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 0, 7))`

### 16.3.3 Function Documentation

#### 16.3.3.1 `status_t I2C_RTOS_Init ( i2c_rtos_handle_t * handle, I2C_Type * base, const i2c_master_config_t * masterConfig, uint32_t srcClock_Hz )`

This function initializes the I2C module and the related RTOS context.

Parameters

|                           |                                                                          |
|---------------------------|--------------------------------------------------------------------------|
| <code>handle</code>       | The RTOS I2C handle, the pointer to an allocated space for RTOS context. |
| <code>base</code>         | The pointer base address of the I2C instance to initialize.              |
| <code>masterConfig</code> | The configuration structure to set-up I2C in master mode.                |
| <code>srcClock_Hz</code>  | The frequency of an input clock of the I2C module.                       |

Returns

status of the operation.

### 16.3.3.2 status\_t I2C\_RRTOS\_Deinit ( i2c\_rtos\_handle\_t \* handle )

This function deinitializes the I2C module and the related RTOS context.

Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | The RTOS I2C handle. |
|---------------|----------------------|

### **16.3.3.3 status\_t I2C\_RTOS\_Transfer ( i2c\_rtos\_handle\_t \* *handle*, i2c\_master\_transfer\_t \* *transfer* )**

This function performs the I2C transfer according to the data given in the transfer structure.

Parameters

|                 |                                                 |
|-----------------|-------------------------------------------------|
| <i>handle</i>   | The RTOS I2C handle.                            |
| <i>transfer</i> | A structure specifying the transfer parameters. |

Returns

status of the operation.

## 16.4 I2C CMSIS Driver

This section describes the programming interface of the I2C Cortex Microcontroller Software Interface Standard (CMSIS) driver. This driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method see <http://www.keil.com/pack/doc/cmsis/Driver/html/index.html>.

The I2C CMSIS driver includes transactional APIs.

Transactional APIs are transaction target high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code accessing the hardware registers.

### 16.4.1 I2C CMSIS Driver

#### 16.4.1.1 Master Operation in interrupt transactional method

```
void I2C_MasterSignalEvent_t(uint32_t event)
{
 if (event == ARM_I2C_EVENT_TRANSFER_DONE)
 {
 g_MasterCompletionFlag = true;
 }
}
/*Init I2C1*/
Driver_I2C1.Initialize(I2C_MasterSignalEvent_t);

Driver_I2C1.PowerControl(ARM_POWER_FULL);

/*config transmit speed/
Driver_I2C1.Control(ARM_I2C_BUS_SPEED, ARM_I2C_BUS_SPEED_STANDARD);

/*start transmit*/
Driver_I2C1.MasterTransmit(I2C_MASTER_SLAVE_ADDR, g_master_buff, I2C_DATA_LENGTH, false);

/* Wait for transfer completed. */
while (!g_MasterCompletionFlag)
{
}
g_MasterCompletionFlag = false;
```

#### 16.4.1.2 Slave Operation in interrupt transactional method

```
void I2C_SlaveSignalEvent_t(uint32_t event)
{
 /* Transfer done */
 if (event == ARM_I2C_EVENT_TRANSFER_DONE)
 {
 g_SlaveCompletionFlag = true;
 }
}
/*Init I2C1*/
Driver_I2C1.Initialize(I2C_SlaveSignalEvent_t);
```

```
Driver_I2C1.PowerControl(ARM_POWER_FULL);

/*config slave addr*/
Driver_I2C1.Control(ARM_I2C_OWN_ADDRESS, I2C_MASTER_SLAVE_ADDR);

/*start transfer*/
Driver_I2C1.SlaveReceive(g_slave_buff, I2C_DATA_LENGTH);

/* Wait for transfer completed. */
while (!g_SlaveCompletionFlag)
{
}
g_SlaveCompletionFlag = false;
```

# Chapter 17

## PWM: Pulse Width Modulation Driver

### 17.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Pulse Width Modulation (PWM) module of MCUXpresso SDK devices.

### 17.2 PWM Driver

#### 17.2.1 Initialization and deinitialization

The function [PWM\\_Init\(\)](#) initializes the PWM with a specified configurations. The function [PWM\\_GetDefaultConfig\(\)](#) gets the default configurations. The initialization function configures the PWM for the requested register update mode for registers with buffers.

The function [PWM\\_Deinit\(\)](#) disables the PWM counter and turns off the module clock.

### 17.3 Typical use case

#### 17.3.1 PWM output

Output PWM signal on PWM3 module with different dutycycles. Periodically update the PWM signal duty cycle. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver-examples/pwm

### Typedefs

- `typedef enum _pwm_clock_source pwm_clock_source_t`  
*PWM clock source select.*
- `typedef enum _pwm_fifo_water_mark pwm_fifo_water_mark_t`  
*PWM FIFO water mark select.*
- `typedef enum _pwm_byte_data_swap pwm_byte_data_swap_t`  
*PWM byte data swap select.*
- `typedef enum _pwm_half_word_data_swap pwm_half_word_data_swap_t`  
*PWM half-word data swap select.*
- `typedef enum _pwm_output_configuration pwm_output_configuration_t`  
*PWM Output Configuration.*
- `typedef enum _pwm_sample_repeat pwm_sample_repeat_t`  
*PWM FIFO sample repeat It determines the number of times each sample from the FIFO is to be used.*
- `typedef enum _pwm_interrupt_enable pwm_interrupt_enable_t`  
*List of PWM interrupt options.*
- `typedef enum _pwm_status_flags pwm_status_flags_t`

- *List of PWM status flags.*
- `typedef enum _pwm_fifo_available pwm_fifo_available_t`  
*List of PWM FIFO available.*

## Enumerations

- `enum _pwm_clock_source {`  
 `kPWM_PeripheralClock = 1U,`  
 `kPWM_HighFrequencyClock,`  
 `kPWM_LowFrequencyClock }`  
*PWM clock source select.*
- `enum _pwm_fifo_water_mark {`  
 `kPWM_FIFOWaterMark_1 = 0U,`  
 `kPWM_FIFOWaterMark_2,`  
 `kPWM_FIFOWaterMark_3,`  
 `kPWM_FIFOWaterMark_4 }`  
*PWM FIFO water mark select.*
- `enum _pwm_byte_data_swap {`  
 `kPWM_BytNoSwap = 0U,`  
 `kPWM_BytSwap }`  
*PWM byte data swap select.*
- `enum _pwm_half_word_data_swap {`  
 `kPWM_HalfWordNoSwap = 0U,`  
 `kPWM_HalfWordSwap }`  
*PWM half-word data swap select.*
- `enum _pwm_output_configuration {`  
 `kPWM_SetAtRolloverAndClearAtcomparison = 0U,`  
 `kPWM_ClearAtRolloverAndSetAtcomparison,`  
 `kPWM_NoConfigure }`  
*PWM Output Configuration.*
- `enum _pwm_sample_repeat {`  
 `kPWM_EachSampleOnce = 0u,`  
 `kPWM_EachSampltwice,`  
 `kPWM_EachSampleFourTimes,`  
 `kPWM_EachSampleEightTimes }`  
*PWM FIFO sample repeat It determines the number of times each sample from the FIFO is to be used.*
- `enum _pwm_interrupt_enable {`  
 `kPWM_FIFOEmptyInterruptEnable = (1U << 0),`  
 `kPWM_RolloverInterruptEnable = (1U << 1),`  
 `kPWM_CompareInterruptEnable = (1U << 2) }`  
*List of PWM interrupt options.*
- `enum _pwm_status_flags {`  
 `kPWM_FIFOEmptyFlag = (1U << 3),`  
 `kPWM_RolloverFlag = (1U << 4),`  
 `kPWM_CompareFlag = (1U << 5),`  
 `kPWM_FIFOWriteErrorFlag }`  
*List of PWM status flags.*

- enum \_pwm\_fifo\_available {
 kPWM\_NoDataInFIFOFlag = 0U,
 kPWM\_OneWordInFIFOFlag,
 kPWM\_TwoWordsInFIFOFlag,
 kPWM\_ThreeWordsInFIFOFlag,
 kPWM\_FourWordsInFIFOFlag
 }

*List of PWM FIFO available.*

## Functions

- static void **PWM\_SoftwareReset** (PWM\_Type \*base)  
*Software reset.*
- static void **PWM\_SetPeriodValue** (PWM\_Type \*base, uint32\_t value)  
*Sets the PWM period value.*
- static uint32\_t **PWM\_GetPeriodValue** (PWM\_Type \*base)  
*Gets the PWM period value.*
- static uint32\_t **PWM\_GetCounterValue** (PWM\_Type \*base)  
*Gets the PWM counter value.*

## Driver version

- #define **FSL\_PWM\_DRIVER\_VERSION** (MAKE\_VERSION(2, 0, 0))  
*Version 2.0.0.*

## Initialization and deinitialization

- status\_t PWM\_Init** (PWM\_Type \*base, const pwm\_config\_t \*config)  
*Ungates the PWM clock and configures the peripheral for basic operation.*
- void **PWM\_Deinit** (PWM\_Type \*base)  
*Gate the PWM submodule clock.*
- void **PWM\_GetDefaultConfig** (pwm\_config\_t \*config)  
*Fill in the PWM config struct with the default settings.*

## PWM start and stop.

- static void **PWM\_StartTimer** (PWM\_Type \*base)  
*Starts the PWM counter when the PWM is enabled.*
- static void **PWM\_StopTimer** (PWM\_Type \*base)  
*Stops the PWM counter when the pwm is disabled.*

## Interrupt Interface

- static void **PWM\_EnableInterrupts** (PWM\_Type \*base, uint32\_t mask)  
*Enables the selected PWM interrupts.*
- static void **PWM\_DisableInterrupts** (PWM\_Type \*base, uint32\_t mask)  
*Disables the selected PWM interrupts.*
- static uint32\_t **PWM\_GetEnabledInterrupts** (PWM\_Type \*base)  
*Gets the enabled PWM interrupts.*

## Status Interface

- static uint32\_t [PWM\\_GetStatusFlags](#) (PWM\_Type \*base)  
*Gets the PWM status flags.*
- static void [PWM\\_clearStatusFlags](#) (PWM\_Type \*base, uint32\_t mask)  
*Clears the PWM status flags.*
- static uint32\_t [PWM\\_GetFIFOAvailable](#) (PWM\_Type \*base)  
*Gets the PWM FIFO available.*

## Sample Interface

- static void [PWM\\_SetSampleValue](#) (PWM\_Type \*base, uint32\_t value)  
*Sets the PWM sample value.*
- static uint32\_t [PWM\\_GetSampleValue](#) (PWM\_Type \*base)  
*Gets the PWM sample value.*

## 17.4 Typedef Documentation

### 17.4.1 `typedef enum _pwm_clock_source pwm_clock_source_t`

### 17.4.2 `typedef enum _pwm_fifo_water_mark pwm_fifo_water_mark_t`

Sets the data level at which the FIFO empty flag will be set

### 17.4.3 `typedef enum _pwm_byte_data_swap pwm_byte_data_swap_t`

It determines the byte ordering of the 16-bit data when it goes into the FIFO from the sample register.

### 17.4.4 `typedef enum _pwm_half_word_data_swap pwm_half_word_data_swap_t`

## 17.5 Enumeration Type Documentation

### 17.5.1 `enum _pwm_clock_source`

Enumerator

*kPWM\_PeripheralClock* The Peripheral clock is used as the clock.

*kPWM\_HighFrequencyClock* High-frequency reference clock is used as the clock.

*kPWM\_LowFrequencyClock* Low-frequency reference clock(32KHz) is used as the clock.

### 17.5.2 `enum _pwm_fifo_water_mark`

Sets the data level at which the FIFO empty flag will be set

Enumerator

***kPWM\_FIFOWaterMark\_1*** FIFO empty flag is set when there are more than or equal to 1 empty slots.

***kPWM\_FIFOWaterMark\_2*** FIFO empty flag is set when there are more than or equal to 2 empty slots.

***kPWM\_FIFOWaterMark\_3*** FIFO empty flag is set when there are more than or equal to 3 empty slots.

***kPWM\_FIFOWaterMark\_4*** FIFO empty flag is set when there are more than or equal to 4 empty slots.

### 17.5.3 enum \_pwm\_byte\_data\_swap

It determines the byte ordering of the 16-bit data when it goes into the FIFO from the sample register.

Enumerator

***kPWM\_ByteNoSwap*** byte ordering remains the same

***kPWM\_ByteSwap*** byte ordering is reversed

### 17.5.4 enum \_pwm\_half\_word\_data\_swap

Enumerator

***kPWM\_HalfWordNoSwap*** Half word swapping does not take place.

***kPWM\_HalfWordSwap*** Half word from write data bus are swapped.

### 17.5.5 enum \_pwm\_output\_configuration

Enumerator

***kPWM\_SetAtRolloverAndClearAtcomparison*** Output pin is set at rollover and cleared at comparison.

***kPWM\_ClearAtRolloverAndSetAtcomparison*** Output pin is cleared at rollover and set at comparison.

***kPWM\_NoConfigure*** PWM output is disconnected.

### 17.5.6 enum \_pwm\_sample\_repeat

Enumerator

***kPWM\_EachSampleOnce*** Use each sample once.

**kPWM\_EachSampleTwice** Use each sample twice.

**kPWM\_EachSampleFourTimes** Use each sample four times.

**kPWM\_EachSampleEightTimes** Use each sample eight times.

### 17.5.7 enum \_pwm\_interrupt\_enable

Enumerator

**kPWM\_FIFOEmptyInterruptEnable** This bit controls the generation of the FIFO Empty interrupt.

**kPWM\_RolloverInterruptEnable** This bit controls the generation of the Rollover interrupt.

**kPWM\_CompareInterruptEnable** This bit controls the generation of the Compare interrupt.

### 17.5.8 enum \_pwm\_status\_flags

Enumerator

**kPWM\_FIFOEmptyFlag** This bit indicates the FIFO data level in comparison to the water level set by FWM field in the control register.

**kPWM\_RolloverFlag** This bit shows that a roll-over event has occurred.

**kPWM\_CompareFlag** This bit shows that a compare event has occurred.

**kPWM\_FIFOWriteErrorFlag** This bit shows that an attempt has been made to write FIFO when it is full.

### 17.5.9 enum \_pwm\_fifo\_available

Enumerator

**kPWM\_NoDataInFIFOFlag** No data available.

**kPWM\_OneWordInFIFOFlag** 1 word of data in FIFO

**kPWM\_TwoWordsInFIFOFlag** 2 word of data in FIFO

**kPWM\_ThreeWordsInFIFOFlag** 3 word of data in FIFO

**kPWM\_FourWordsInFIFOFlag** 4 word of data in FIFO

## 17.6 Function Documentation

### 17.6.1 status\_t PWM\_Init ( PWM\_Type \* *base*, const pwm\_config\_t \* *config* )

Note

This API should be called at the beginning of the application using the PWM driver.

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>base</i>   | PWM peripheral base address             |
| <i>config</i> | Pointer to user's PWM config structure. |

Returns

kStatus\_Success means success; else failed.

### 17.6.2 void PWM\_Deinit ( PWM\_Type \* *base* )

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PWM peripheral base address |
|-------------|-----------------------------|

### 17.6.3 void PWM\_GetDefaultConfig ( pwm\_config\_t \* *config* )

The default values are:

```
* config->enableStopMode = false;
* config->enableDozeMode = false;
* config->enableWaitMode = false;
* config->enableDozeMode = false;
* config->clockSource = kPWM_LowFrequencyClock;
* config->prescale = 0U;
* config->outputConfig = kPWM_SetAtRolloverAndClearAtcomparison;
* config->fifoWater = kPWM_FIFOWaterMark_2;
* config->sampleRepeat = kPWM_EachSampleOnce;
* config->byteSwap = kPWM_ByteNoSwap;
* config->halfWordSwap = kPWM_HalfWordNoSwap;
*
```

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to user's PWM config structure. |
|---------------|-----------------------------------------|

### 17.6.4 static void PWM\_StartTimer ( PWM\_Type \* *base* ) [inline], [static]

When the PWM is enabled, it begins a new period, the output pin is set to start a new period while the prescaler and counter are released and counting begins.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PWM peripheral base address |
|-------------|-----------------------------|

### 17.6.5 static void PWM\_StopTimer ( **PWM\_Type** \* *base* ) [inline], [static]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PWM peripheral base address |
|-------------|-----------------------------|

### 17.6.6 static void PWM\_SoftwareReset ( **PWM\_Type** \* *base* ) [inline], [static]

PWM is reset when this bit is set to 1. It is a self clearing bit. Setting this bit resets all the registers to their reset values except for the STOPEN, DOZEN, WAITEN, and DBGEN bits in this control register.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PWM peripheral base address |
|-------------|-----------------------------|

### 17.6.7 static void PWM\_EnableInterrupts ( **PWM\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

|             |                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | PWM peripheral base address                                                                                         |
| <i>mask</i> | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">pwm_interrupt_enable_t</a> |

### 17.6.8 static void PWM\_DisableInterrupts ( **PWM\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

Parameters

|             |                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | PWM peripheral base address                                                                                          |
| <i>mask</i> | The interrupts to disable. This is a logical OR of members of the enumeration <a href="#">pwm_interrupt_enable_t</a> |

### 17.6.9 static uint32\_t PWM\_GetEnabledInterrupts ( **PWM\_Type** \* *base* ) [[inline](#)], [[static](#)]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PWM peripheral base address |
|-------------|-----------------------------|

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [pwm\\_interrupt\\_enable\\_t](#)

### 17.6.10 static uint32\_t PWM\_GetStatusFlags ( **PWM\_Type** \* *base* ) [[inline](#)], [[static](#)]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PWM peripheral base address |
|-------------|-----------------------------|

Returns

The status flags. This is the logical OR of members of the enumeration [pwm\\_status\\_flags\\_t](#)

### 17.6.11 static void PWM\_clearStatusFlags ( **PWM\_Type** \* *base*, uint32\_t *mask* ) [[inline](#)], [[static](#)]

Parameters

---

|             |                                                                                                                  |
|-------------|------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | PWM peripheral base address                                                                                      |
| <i>mask</i> | The status flags to clear. This is a logical OR of members of the enumeration <a href="#">pwm_status_flags_t</a> |

### 17.6.12 static uint32\_t PWM\_GetFIFOAvailable ( PWM\_Type \* *base* ) [inline], [static]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PWM peripheral base address |
|-------------|-----------------------------|

Returns

The status flags. This is the logical OR of members of the enumeration [pwm\\_fifo\\_available\\_t](#)

### 17.6.13 static void PWM\_SetSampleValue ( PWM\_Type \* *base*, uint32\_t *value* ) [inline], [static]

Parameters

|              |                                                                                                                                        |
|--------------|----------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>  | PWM peripheral base address                                                                                                            |
| <i>value</i> | The sample value. This is the input to the 4x16 FIFO. The value in this register denotes the value of the sample being currently used. |

### 17.6.14 static uint32\_t PWM\_GetSampleValue ( PWM\_Type \* *base* ) [inline], [static]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PWM peripheral base address |
|-------------|-----------------------------|

Returns

The sample value. It can be read only when the PWM is enable.

### 17.6.15 static void PWM\_SetPeriodValue ( PWM\_Type \* *base*, uint32\_t *value* ) [inline], [static]

Parameters

|              |                                                                                                                                                                                                                          |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>  | PWM peripheral base address                                                                                                                                                                                              |
| <i>value</i> | The period value. The PWM period register (PWM_PWMPR) determines the period of the PWM output signal. Writing 0xFFFF to this register will achieve the same result as writing 0xFFFE. PWMO (Hz) = PCLK(Hz) / (period +2) |

#### 17.6.16 static uint32\_t PWM\_GetPeriodValue ( PWM\_Type \* *base* ) [inline], [static]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PWM peripheral base address |
|-------------|-----------------------------|

Returns

The period value. The PWM period register (PWM\_PWMPR) determines the period of the PWM output signal.

#### 17.6.17 static uint32\_t PWM\_GetCounterValue ( PWM\_Type \* *base* ) [inline], [static]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | PWM peripheral base address |
|-------------|-----------------------------|

Returns

The counter value. The current count value.

# Chapter 18

## UART: Universal Asynchronous Receiver/Transmitter Driver

### 18.1 Overview

#### Modules

- [UART CMSIS Driver](#)
- [UART Driver](#)
- [UART FreeRTOS Driver](#)
- [UART SDMA Driver](#)

## 18.2 UART Driver

### 18.2.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Universal Asynchronous Receiver/Transmitter (UART) module of MCUXpresso SDK devices.

The UART driver includes functional APIs and transactional APIs.

Functional APIs are used for UART initialization/configuration/operation for the purpose of optimization/customization. Using the functional API requires the knowledge of the UART peripheral and how to organize functional APIs to meet the application requirements. All functional APIs use the peripheral base address as the first parameter. UART functional operation groups provide the functional API set.

Transactional APIs can be used to enable the peripheral quickly and in the application if the code size and performance of transactional APIs can satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code. All transactional APIs use the `uart_handle_t` as the second parameter. Initialize the handle by calling the [UART\\_TransferCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer, which means that the functions [UART\\_TransferSendNonBlocking\(\)](#) and [UART\\_TransferReceiveNonBlocking\(\)](#) set up an interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_UART_TxIdle` and `kStatus_UART_RxIdle`.

Transactional receive APIs support the ring buffer. Prepare the memory for the ring buffer and pass in the start address and size while calling the [UART\\_TransferCreateHandle\(\)](#). If passing NULL, the ring buffer feature is disabled. When the ring buffer is enabled, the received data is saved to the ring buffer in the background. The [UART\\_TransferReceiveNonBlocking\(\)](#) function first gets data from the ring buffer. If the ring buffer does not have enough data, the function first returns the data in the ring buffer and then saves the received data to user memory. When all data is received, the upper layer is informed through a callback with the `kStatus_UART_RxIdle`.

If the receive ring buffer is full, the upper layer is informed through a callback with the `kStatus_UART_RxRingBufferOverrun`. In the callback function, the upper layer reads data out from the ring buffer. If not, existing data is overwritten by the new data.

The ring buffer size is specified when creating the handle. Note that one byte is reserved for the ring buffer maintenance. When creating handle using the following code.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/uart. In this example, the buffer size is 32, but only 31 bytes are used for saving data.

### 18.2.2 Typical use case

#### 18.2.2.1 UART Send/receive using a polling method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/uart

### 18.2.2.2 UART Send/receive using an interrupt method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/uart

### 18.2.2.3 UART Receive using the ringbuffer feature

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/uart

### 18.2.2.4 UART automatic baud rate detect feature

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/uart

## Data Structures

- struct `_uart_config`  
*UART configuration structure.* [More...](#)
- struct `_uart_transfer`  
*UART transfer structure.* [More...](#)
- struct `_uart_handle`  
*UART handle structure.* [More...](#)

## Macros

- #define `UART_RETRY_TIMES` 0U /\* Defining to zero means to keep waiting for the flag until it is assert/deassert. \*/  
*Retry times for waiting flag.*

## TypeDefs

- typedef enum `_uart_data_bits` `uart_data_bits_t`  
*UART data bits count.*
- typedef enum `_uart_parity_mode` `uart_parity_mode_t`  
*UART parity mode.*
- typedef enum `_uart_stop_bit_count` `uart_stop_bit_count_t`  
*UART stop bit count.*
- typedef enum `_uart_idle_condition` `uart_idle_condition_t`  
*UART idle condition detect.*
- typedef struct `_uart_config` `uart_config_t`  
*UART configuration structure.*
- typedef struct `_uart_transfer` `uart_transfer_t`  
*UART transfer structure.*
- typedef struct `_uart_handle` `uart_handle_t`  
*Forward declaration of the handle typedef.*

- `typedef void(* uart_transfer_callback_t )(UART_Type *base, uart_handle_t *handle, status_t status, void *userData)`  
*UART transfer callback function.*

## Enumerations

- `enum {`  
 `kStatus_UART_TxBusy = MAKE_STATUS(kStatusGroup_IUART, 0),`  
 `kStatus_UART_RxBusy = MAKE_STATUS(kStatusGroup_IUART, 1),`  
 `kStatus_UART_TxIdle = MAKE_STATUS(kStatusGroup_IUART, 2),`  
 `kStatus_UART_RxIdle = MAKE_STATUS(kStatusGroup_IUART, 3),`  
 `kStatus_UART_TxWatermarkTooLarge = MAKE_STATUS(kStatusGroup_IUART, 4),`  
 `kStatus_UART_RxWatermarkTooLarge = MAKE_STATUS(kStatusGroup_IUART, 5),`  
 `kStatus_UART_FlagCannotClearManually,`  
 `kStatus_UART_Error = MAKE_STATUS(kStatusGroup_IUART, 7),`  
 `kStatus_UART_RxRingBufferOverrun = MAKE_STATUS(kStatusGroup_IUART, 8),`  
 `kStatus_UART_RxHardwareOverrun = MAKE_STATUS(kStatusGroup_IUART, 9),`  
 `kStatus_UART_NoiseError = MAKE_STATUS(kStatusGroup_IUART, 10),`  
 `kStatus_UART_FramingError = MAKE_STATUS(kStatusGroup_IUART, 11),`  
 `kStatus_UART_ParityError = MAKE_STATUS(kStatusGroup_IUART, 12),`  
 `kStatus_UART_BaudrateNotSupport,`  
 `kStatus_UART_BreakDetect = MAKE_STATUS(kStatusGroup_IUART, 14),`  
 `kStatus_UART_Timeout = MAKE_STATUS(kStatusGroup_IUART, 15) }`

*Error codes for the UART driver.*

- `enum _uart_data_bits {`  
 `kUART_SevenDataBits = 0x0U,`  
 `kUART_EightDataBits = 0x1U }`  
*UART data bits count.*
- `enum _uart_parity_mode {`  
 `kUART_ParityDisabled = 0x0U,`  
 `kUART_ParityEven = 0x2U,`  
 `kUART_ParityOdd = 0x3U }`  
*UART parity mode.*
- `enum _uart_stop_bit_count {`  
 `kUART_OneStopBit = 0x0U,`  
 `kUART_TwoStopBit = 0x1U }`  
*UART stop bit count.*
- `enum _uart_idle_condition {`  
 `kUART_IdleFor4Frames = 0x0U,`  
 `kUART_IdleFor8Frames = 0x1U,`  
 `kUART_IdleFor16Frames = 0x2U,`  
 `kUART_IdleFor32Frames = 0x3U }`  
*UART idle condition detect.*
- `enum _uart_interrupt_enable`  
*This structure contains the settings for all of the UART interrupt configurations.*
- `enum {`

```

kUART_RxCharReadyFlag = 0x0000000FU,
kUART_RxErrorFlag = 0x0000000EU,
kUART_RxOverrunErrorFlag = 0x0000000DU,
kUART_RxFrameErrorFlag = 0x0000000CU,
kUART_RxBreakDetectFlag = 0x0000000BU,
kUART_RxParityErrorFlag = 0x0000000AU,
kUART_ParityErrorFlag = 0x0094000FU,
kUART_RtsStatusFlag = 0x0094000EU,
kUART_TxReadyFlag = 0x0094000DU,
kUART_RtsDeltaFlag = 0x0094000CU,
kUART_EscapeFlag = 0x0094000BU,
kUART_FrameErrorFlag = 0x0094000AU,
kUART_RxReadyFlag = 0x00940009U,
kUART_AgingTimerFlag = 0x00940008U,
kUART_DtrDeltaFlag = 0x00940007U,
kUART_RxDsFlag = 0x00940006U,
kUART_tAWakeFlag = 0x00940005U,
kUART_AwakeFlag = 0x00940004U,
kUART_Rs485SlaveAddrMatchFlag = 0x00940003U,
kUART_AutoBaudFlag = 0x0098000FU,
kUART_TxEmptyFlag = 0x0098000EU,
kUART_DtrFlag = 0x0098000DU,
kUART_IdleFlag = 0x0098000CU,
kUART_AutoBaudCntStopFlag = 0x0098000BU,
kUART_RiDeltaFlag = 0x0098000AU,
kUART_RiFlag = 0x00980009U,
kUART_IrFlag = 0x00980008U,
kUART_WakeFlag = 0x00980007U,
kUART_DcdDeltaFlag = 0x00980006U,
kUART_DcdFlag = 0x00980005U,
kUART_RtsFlag = 0x00980004U,
kUART_TxCompleteFlag = 0x00980003U,
kUART_BreakDetectFlag = 0x00980002U,
kUART_RxOverrunFlag = 0x00980001U,
kUART_RxDataReadyFlag = 0x00980000U }

```

*UART status flags.*

## Functions

- `uint32_t UART_GetInstance (UART_Type *base)`  
*Get the UART instance from peripheral base address.*

## Variables

- `void * s_uartHandle []`  
*Pointers to uart handles for each instance.*

## Driver version

- `#define FSL_UART_DRIVER_VERSION (MAKE_VERSION(2, 3, 2))`  
*UART driver version.*

## Software Reset

- `static void UART_SoftwareReset (UART_Type *base)`  
*Resets the UART using software.*

## Initialization and deinitialization

- `status_t UART_Init (UART_Type *base, const uart_config_t *config, uint32_t srcClock_Hz)`  
*Initializes an UART instance with the user configuration structure and the peripheral clock.*
- `void UART_Deinit (UART_Type *base)`  
*Deinitializes a UART instance.*
- `void UART_GetDefaultConfig (uart_config_t *config)`  
*l*
- `status_t UART_SetBaudRate (UART_Type *base, uint32_t baudRate_Bps, uint32_t srcClock_Hz)`  
*Sets the UART instance baud rate.*
- `static void UART_Enable (UART_Type *base)`  
*This function is used to Enable the UART Module.*
- `static void UART_SetIdleCondition (UART_Type *base, uart_idle_condition_t condition)`  
*This function is used to configure the IDLE line condition.*
- `static void UART_Disable (UART_Type *base)`  
*This function is used to Disable the UART Module.*

## Status

- `bool UART_GetStatusFlag (UART_Type *base, uint32_t flag)`  
*This function is used to get the current status of specific UART status flag(including interrupt flag).*
- `void UART_ClearStatusFlag (UART_Type *base, uint32_t flag)`  
*This function is used to clear the current status of specific UART status flag.*

## Interrupts

- `void UART_EnableInterrupts (UART_Type *base, uint32_t mask)`  
*Enables UART interrupts according to the provided mask.*
- `void UART_DisableInterrupts (UART_Type *base, uint32_t mask)`

- `uint32_t UART_GetEnabledInterrupts (UART_Type *base)`  
*Disables the UART interrupts according to the provided mask.*

## Bus Operations

- `static void UART_EnableTx (UART_Type *base, bool enable)`  
*Enables or disables the UART transmitter.*
- `static void UART_EnableRx (UART_Type *base, bool enable)`  
*Enables or disables the UART receiver.*
- `static void UART_WriteByte (UART_Type *base, uint8_t data)`  
*Writes to the transmitter register.*
- `static uint8_t UART_ReadByte (UART_Type *base)`  
*Reads the receiver register.*
- `status_t UART_WriteBlocking (UART_Type *base, const uint8_t *data, size_t length)`  
*Writes to the TX register using a blocking method.*
- `status_t UART_ReadBlocking (UART_Type *base, uint8_t *data, size_t length)`  
*Read RX data register using a blocking method.*

## Transactional

- `void UART_TransferCreateHandle (UART_Type *base, uart_handle_t *handle, uart_transfer_t callback, void *userData)`  
*Initializes the UART handle.*
- `void UART_TransferStartRingBuffer (UART_Type *base, uart_handle_t *handle, uint8_t *ringBuffer, size_t ringBufferSize)`  
*Sets up the RX ring buffer.*
- `void UART_TransferStopRingBuffer (UART_Type *base, uart_handle_t *handle)`  
*Aborts the background transfer and uninstalls the ring buffer.*
- `size_t UART_TransferGetRxRingBufferLength (uart_handle_t *handle)`  
*Get the length of received data in RX ring buffer.*
- `status_t UART_TransferSendNonBlocking (UART_Type *base, uart_handle_t *handle, uart_transfer_t *xfer)`  
*Transmits a buffer of data using the interrupt method.*
- `void UART_TransferAbortSend (UART_Type *base, uart_handle_t *handle)`  
*Aborts the interrupt-driven data transmit.*
- `status_t UART_TransferGetSendCount (UART_Type *base, uart_handle_t *handle, uint32_t *count)`  
*Gets the number of bytes written to the UART TX register.*
- `status_t UART_TransferReceiveNonBlocking (UART_Type *base, uart_handle_t *handle, uart_transfer_t *xfer, size_t *receivedBytes)`  
*Receives a buffer of data using an interrupt method.*
- `void UART_TransferAbortReceive (UART_Type *base, uart_handle_t *handle)`  
*Aborts the interrupt-driven data receiving.*
- `status_t UART_TransferGetReceiveCount (UART_Type *base, uart_handle_t *handle, uint32_t *count)`  
*Gets the number of bytes that have been received.*
- `void UART_TransferHandleIRQ (UART_Type *base, void *irqHandle)`

*UART IRQ handle function.*

## DMA control functions.

- static void [UART\\_EnableTxDMA](#) (UART\_Type \*base, bool enable)  
*Enables or disables the UART transmitter DMA request.*
- static void [UART\\_EnableRxDMA](#) (UART\_Type \*base, bool enable)  
*Enables or disables the UART receiver DMA request.*

## FIFO control functions.

- static void [UART\\_SetTxFifoWatermark](#) (UART\_Type \*base, uint8\_t watermark)  
*This function is used to set the watermark of UART Tx FIFO.*
- static void [UART\\_SetRxRTSWatermark](#) (UART\_Type \*base, uint8\_t watermark)  
*This function is used to set the watermark of UART RTS deassertion.*
- static void [UART\\_SetRxFifoWatermark](#) (UART\_Type \*base, uint8\_t watermark)  
*This function is used to set the watermark of UART Rx FIFO.*

## Auto baud rate detection.

- static void [UART\\_EnableAutoBaudRate](#) (UART\_Type \*base, bool enable)  
*This function is used to set the enable condition of Automatic Baud Rate Detection feature.*
- static bool [UART\\_IsAutoBaudRateComplete](#) (UART\_Type \*base)  
*This function is used to read if the automatic baud rate detection has finished.*

### 18.2.3 Data Structure Documentation

#### 18.2.3.1 struct \_uart\_config

##### Data Fields

- uint32\_t [baudRate\\_Bps](#)  
*UART baud rate.*
- [uart\\_parity\\_mode\\_t](#) [parityMode](#)  
*Parity error check mode of this module.*
- [uart\\_data\\_bits\\_t](#) [dataBitsCount](#)  
*Data bits count, eight (default), seven.*
- [uart\\_stop\\_bit\\_count\\_t](#) [stopBitCount](#)  
*Number of stop bits in one frame.*
- uint8\_t [txFifoWatermark](#)  
*TX FIFO watermark.*
- uint8\_t [rxFifoWatermark](#)  
*RX FIFO watermark.*
- uint8\_t [rxRTSWatermark](#)  
*RX RTS watermark, RX FIFO data count being larger than this triggers RTS deassertion.*

- bool `enableAutoBaudRate`  
*Enable automatic baud rate detection.*
- bool `enableTx`  
*Enable TX.*
- bool `enableRx`  
*Enable RX.*
- bool `enableRxRTS`  
*RX RTS enable.*
- bool `enableTxCTS`  
*TX CTS enable.*

### Field Documentation

- (1) `uint32_t _uart_config::baudRate_Bps`
- (2) `uart_parity_mode_t _uart_config::parityMode`
- (3) `uart_stop_bit_count_t _uart_config::stopBitCount`

### 18.2.3.2 struct \_uart\_transfer

#### Data Fields

- `size_t dataSize`  
*The byte count to be transfer.*
- `uint8_t * data`  
*The buffer of data to be transfer.*
- `uint8_t * rxData`  
*The buffer to receive data.*
- `const uint8_t * txData`  
*The buffer of data to be sent.*

### Field Documentation

- (1) `uint8_t* _uart_transfer::data`
- (2) `uint8_t* _uart_transfer::rxData`
- (3) `const uint8_t* _uart_transfer::txData`
- (4) `size_t _uart_transfer::dataSize`

### 18.2.3.3 struct \_uart\_handle

#### Data Fields

- `const uint8_t *volatile txData`  
*Address of remaining data to send.*
- `volatile size_t txDataSize`  
*Size of the remaining data to send.*
- `size_t txDataSizeAll`

- **uint8\_t \*volatile rxData**  
*Size of the data to send out.*
- **volatile size\_t rxDataSize**  
*Address of remaining data to receive.*
- **size\_t rxDataSizeAll**  
*Size of the remaining data to receive.*
- **uint8\_t \* rxRingBuffer**  
*Size of the data to receive.*
- **size\_t rxRingBufferSize**  
*Start address of the receiver ring buffer.*
- **volatile uint16\_t rxRingBufferHead**  
*Size of the ring buffer.*
- **volatile uint16\_t rxRingBufferTail**  
*Index for the driver to store received data into ring buffer.*
- **uart\_transfer\_callback\_t callback**  
*Index for the user to get data from the ring buffer.*
- **void \* userData**  
*Callback function.*
- **volatile uint8\_t txState**  
*UART callback function parameter.*
- **volatile uint8\_t rxState**  
*TX transfer state.*
- **volatile uint8\_t rxState**  
*RX transfer state.*



## Field Documentation

- (1) `const uint8_t* volatile _uart_handle::txData`
- (2) `volatile size_t _uart_handle::txDataSize`
- (3) `size_t _uart_handle::txDataSizeAll`
- (4) `uint8_t* volatile _uart_handle::rxData`
- (5) `volatile size_t _uart_handle::rxDataSize`
- (6) `size_t _uart_handle::rxDataSizeAll`
- (7) `uint8_t* _uart_handle::rxRingBuffer`
- (8) `size_t _uart_handle::rxRingBufferSize`
- (9) `volatile uint16_t _uart_handle::rxRingBufferHead`
- (10) `volatile uint16_t _uart_handle::rxRingBufferTail`
- (11) `uart_transfer_callback_t _uart_handle::callback`
- (12) `void* _uart_handle::userData`
- (13) `volatile uint8_t _uart_handle::txState`

### 18.2.4 Macro Definition Documentation

**18.2.4.1 #define FSL\_UART\_DRIVER\_VERSION (MAKE\_VERSION(2, 3, 2))**

**18.2.4.2 #define UART\_RETRY\_TIMES 0U /\* Defining to zero means to keep waiting for the flag until it is assert/deassert. \*/**

### 18.2.5 Typedef Documentation

**18.2.5.1 typedef enum \_uart\_data\_bits uart\_data\_bits\_t**

**18.2.5.2 typedef enum \_uart\_parity\_mode uart\_parity\_mode\_t**

**18.2.5.3 typedef enum \_uart\_stop\_bit\_count uart\_stop\_bit\_count\_t**

**18.2.5.4 typedef enum \_uart\_idle\_condition uart\_idle\_condition\_t**

**18.2.5.5 typedef struct \_uart\_config uart\_config\_t**

**18.2.5.6 typedef struct \_uart\_transfer uart\_transfer\_t**

**18.2.5.7 typedef struct \_uart\_handle uart\_handle\_t**

**18.2.5.8 typedef void(\* uart\_transfer\_callback\_t)(UART\_Type \*base, uart\_handle\_t**

*kStatus\_UART\_RxBusy* Receiver is busy.  
*kStatus\_UART\_TxIdle* UART transmitter is idle.  
*kStatus\_UART\_RxIdle* UART receiver is idle.  
*kStatus\_UART\_TxWatermarkTooLarge* TX FIFO watermark too large.  
*kStatus\_UART\_RxWatermarkTooLarge* RX FIFO watermark too large.  
*kStatus\_UART\_FlagCannotClearManually* UART flag can't be manually cleared.  
*kStatus\_UART\_Error* Error happens on UART.  
*kStatus\_UART\_RxRingBufferOverrun* UART RX software ring buffer overrun.  
*kStatus\_UART\_RxHardwareOverrun* UART RX receiver overrun.  
*kStatus\_UART\_NoiseError* UART noise error.  
*kStatus\_UART\_FramingError* UART framing error.  
*kStatus\_UART\_ParityError* UART parity error.  
*kStatus\_UART\_BaudrateNotSupport* Baudrate is not support in current clock source.  
*kStatus\_UART\_BreakDetect* Receiver detect BREAK signal.  
*kStatus\_UART\_Timeout* UART times out.

### 18.2.6.2 enum \_uart\_data\_bits

Enumerator

*kUART\_SevenDataBits* Seven data bit.  
*kUART\_EightDataBits* Eight data bit.

### 18.2.6.3 enum \_uart\_parity\_mode

Enumerator

*kUART\_ParityDisabled* Parity disabled.  
*kUART\_ParityEven* Even error check is selected.  
*kUART\_ParityOdd* Odd error check is selected.

### 18.2.6.4 enum \_uart\_stop\_bit\_count

Enumerator

*kUART\_OneStopBit* One stop bit.  
*kUART\_TwoStopBit* Two stop bits.

### 18.2.6.5 enum \_uart\_idle\_condition

Enumerator

*kUART\_IdleFor4Frames* Idle for more than 4 frames.

***kUART\_IdleFor8Frames*** Idle for more than 8 frames.  
***kUART\_IdleFor16Frames*** Idle for more than 16 frames.  
***kUART\_IdleFor32Frames*** Idle for more than 32 frames.

### 18.2.6.6 enum \_uart\_interrupt\_enable

### 18.2.6.7 anonymous enum

This provides constants for the UART status flags for use in the UART functions.

Enumerator

***kUART\_RxCharReadyFlag*** Rx Character Ready Flag.  
***kUART\_RxErrorFlag*** Rx Error Detect Flag.  
***kUART\_RxOverrunErrorFlag*** Rx Overrun Flag.  
***kUART\_RxFrameErrorFlag*** Rx Frame Error Flag.  
***kUART\_RxBreakDetectFlag*** Rx Break Detect Flag.  
***kUART\_RxParityErrorFlag*** Rx Parity Error Flag.  
***kUART\_ParityErrorFlag*** Parity Error Interrupt Flag.  
***kUART\_RtsStatusFlag*** RTS\_B Pin Status Flag.  
***kUART\_TxReadyFlag*** Transmitter Ready Interrupt/DMA Flag.  
***kUART\_RtsDeltaFlag*** RTS Delta Flag.  
***kUART\_EscapeFlag*** Escape Sequence Interrupt Flag.  
***kUART\_FrameErrorFlag*** Frame Error Interrupt Flag.  
***kUART\_RxReadyFlag*** Receiver Ready Interrupt/DMA Flag.  
***kUART\_AgingTimerFlag*** Aging Timer Interrupt Flag.  
***kUART\_DtrDeltaFlag*** DTR Delta Flag.  
***kUART\_RxDsFlag*** Receiver IDLE Interrupt Flag.  
***kUART\_tAIRWakeFlag*** Asynchronous IR WAKE Interrupt Flag.  
***kUART\_AwakeFlag*** Asynchronous WAKE Interrupt Flag.  
***kUART\_Rs485SlaveAddrMatchFlag*** RS-485 Slave Address Detected Interrupt Flag.  
***kUART\_AutoBaudFlag*** Automatic Baud Rate Detect Complete Flag.  
***kUART\_TxEmptyFlag*** Transmit Buffer FIFO Empty.  
***kUART\_DtrFlag*** DTR edge triggered interrupt flag.  
***kUART\_IdleFlag*** Idle Condition Flag.  
***kUART\_AutoBaudCntStopFlag*** Auto-baud Counter Stopped Flag.  
***kUART\_RiDeltaFlag*** Ring Indicator Delta Flag.  
***kUART\_RiFlag*** Ring Indicator Input Flag.  
***kUART\_IrFlag*** Serial Infrared Interrupt Flag.  
***kUART\_WakeFlag*** Wake Flag.  
***kUART\_DcdDeltaFlag*** Data Carrier Detect Delta Flag.  
***kUART\_DcdFlag*** Data Carrier Detect Input Flag.  
***kUART\_RtsFlag*** RTS Edge Triggered Interrupt Flag.  
***kUART\_TxCompleteFlag*** Transmitter Complete Flag.

*kUART\_BreakDetectFlag* BREAK Condition Detected Flag.

*kUART\_RxOverrunFlag* Overrun Error Flag.

*kUART\_RxDataReadyFlag* Receive Data Ready Flag.

## 18.2.7 Function Documentation

### 18.2.7.1 `uint32_t UART_GetInstance( UART_Type * base )`

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

Returns

UART instance.

### 18.2.7.2 `static void UART_SoftwareReset( UART_Type * base ) [inline], [static]`

This function resets the transmit and receive state machines, all FIFOs and register USR1, USR2, UBIR, UBMR, UBRC , URXD, UTXD and UTS[6-3]

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

### 18.2.7.3 `status_t UART_Init( UART_Type * base, const uart_config_t * config, uint32_t srcClock_Hz )`

This function configures the UART module with user-defined settings. Call the [UART\\_GetDefaultConfig\(\)](#) function to configure the configuration structure and get the default configuration. The example below shows how to use this API to configure the UART.

```
* uart_config_t uartConfig;
* uartConfig.baudRate_Bps = 115200U;
* uartConfig.parityMode = kUART_ParityDisabled;
* uartConfig.dataBitsCount = kUART_EightDataBits;
* uartConfig.stopBitCount = kUART_OneStopBit;
* uartConfig.txFifoWatermark = 2;
* uartConfig.rxFifoWatermark = 1;
* uartConfig.enableAutoBaudrate = false;
* uartConfig.enableTx = true;
* uartConfig.enableRx = true;
* UART_Init(UART1, &uartConfig, 24000000U);
*
```

Parameters

|                    |                                                    |
|--------------------|----------------------------------------------------|
| <i>base</i>        | UART peripheral base address.                      |
| <i>config</i>      | Pointer to a user-defined configuration structure. |
| <i>srcClock_Hz</i> | UART clock source frequency in HZ.                 |

Return values

|                        |                         |
|------------------------|-------------------------|
| <i>kStatus_Success</i> | UART initialize succeed |
|------------------------|-------------------------|

#### 18.2.7.4 void **UART\_Deinit** ( **UART\_Type** \* *base* )

This function waits for transmit to complete, disables TX and RX, and disables the UART clock.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

#### 18.2.7.5 void **UART\_GetDefaultConfig** ( **uart\_config\_t** \* *config* )

Gets the default configuration structure.

This function initializes the UART configuration structure to a default value. The default values are:  
: uartConfig->baudRate\_Bps = 115200U; uartConfig->parityMode = kUART\_ParityDisabled; uartConfig->dataBitsCount = kUART\_EightDataBits; uartConfig->stopBitCount = kUART\_OneStopBit; uartConfig->txFifoWatermark = 2; uartConfig->rxFifoWatermark = 1; uartConfig->enableAutoBaudrate = flase; uartConfig->enableTx = false; uartConfig->enableRx = false;

Parameters

|               |                                       |
|---------------|---------------------------------------|
| <i>config</i> | Pointer to a configuration structure. |
|---------------|---------------------------------------|

#### 18.2.7.6 status\_t **UART\_SetBaudRate** ( **UART\_Type** \* *base*, **uint32\_t** *baudRate\_Bps*, **uint32\_t** *srcClock\_Hz* )

This function configures the UART module baud rate. This function is used to update the UART module baud rate after the UART module is initialized by the **UART\_Init**.

```
* UART_SetBaudRate(UART1, 115200U, 20000000U);
*
```

Parameters

|                     |                                    |
|---------------------|------------------------------------|
| <i>base</i>         | UART peripheral base address.      |
| <i>baudRate_Bps</i> | UART baudrate to be set.           |
| <i>srcClock_Hz</i>  | UART clock source frequency in Hz. |

Return values

|                                         |                                                      |
|-----------------------------------------|------------------------------------------------------|
| <i>kStatus_UART_Baudrate-NotSupport</i> | Baudrate is not support in the current clock source. |
| <i>kStatus_Success</i>                  | Set baudrate succeeded.                              |

#### 18.2.7.7 static void UART\_Enable ( **UART\_Type** \* *base* ) [inline], [static]

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | UART base pointer. |
|-------------|--------------------|

#### 18.2.7.8 static void UART\_SetIdleCondition ( **UART\_Type** \* *base*, **uart\_idle\_condition\_t condition** ) [inline], [static]

Parameters

|                  |                                                                                          |
|------------------|------------------------------------------------------------------------------------------|
| <i>base</i>      | UART base pointer.                                                                       |
| <i>condition</i> | IDLE line detect condition of the enumerators in <a href="#">uart_idle_condition_t</a> . |

#### 18.2.7.9 static void UART\_Disable ( **UART\_Type** \* *base* ) [inline], [static]

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | UART base pointer. |
|-------------|--------------------|

#### 18.2.7.10 bool UART\_GetStatusFlag ( **UART\_Type** \* *base*, **uint32\_t flag** )

The available status flag can be select from [uart\\_status\\_flag\\_t](#) enumeration.

Parameters

|             |                       |
|-------------|-----------------------|
| <i>base</i> | UART base pointer.    |
| <i>flag</i> | Status flag to check. |

Return values

|                |                                     |
|----------------|-------------------------------------|
| <i>current</i> | state of corresponding status flag. |
|----------------|-------------------------------------|

### 18.2.7.11 void **UART\_ClearStatusFlag** ( **UART\_Type** \* *base*, **uint32\_t** *flag* )

The available status flag can be select from `uart_status_flag_t` enumeration.

Parameters

|             |                       |
|-------------|-----------------------|
| <i>base</i> | UART base pointer.    |
| <i>flag</i> | Status flag to clear. |

### 18.2.7.12 void **UART\_EnableInterrupts** ( **UART\_Type** \* *base*, **uint32\_t** *mask* )

This function enables the UART interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [\\_uart\\_interrupt\\_enable](#). For example, to enable TX empty interrupt and RX data ready interrupt, do the following.

```
* UART_EnableInterrupts(UART1, kUART_TxEmptyEnable | kUART_RxDataReadyEnable);
*
```

Parameters

|             |                                                                                  |
|-------------|----------------------------------------------------------------------------------|
| <i>base</i> | UART peripheral base address.                                                    |
| <i>mask</i> | The interrupts to enable. Logical OR of <a href="#">_uart_interrupt_enable</a> . |

### 18.2.7.13 void **UART\_DisableInterrupts** ( **UART\_Type** \* *base*, **uint32\_t** *mask* )

This function disables the UART interrupts according to the provided mask. The mask is a logical OR of enumeration members. See [\\_uart\\_interrupt\\_enable](#). For example, to disable TX empty interrupt and RX data ready interrupt do the following.

```
* UART_EnableInterrupts(UART1, kUART_TxEmptyEnable | kUART_RxDataReadyEnable);
*
```

Parameters

|             |                                                                                   |
|-------------|-----------------------------------------------------------------------------------|
| <i>base</i> | UART peripheral base address.                                                     |
| <i>mask</i> | The interrupts to disable. Logical OR of <a href="#">_uart_interrupt_enable</a> . |

#### 18.2.7.14 `uint32_t UART_GetEnabledInterrupts ( UART_Type * base )`

This function gets the enabled UART interrupts. The enabled interrupts are returned as the logical OR value of the enumerators [\\_uart\\_interrupt\\_enable](#). To check a specific interrupt enable status, compare the return value with enumerators in [\\_uart\\_interrupt\\_enable](#). For example, to check whether the TX empty interrupt is enabled:

```
* uint32_t enabledInterrupts = UART_GetEnabledInterrupts\(UART1\);
*
* if (kUART_TxEmptyEnable & enabledInterrupts)
* {
* ...
* }
*
```

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

Returns

UART interrupt flags which are logical OR of the enumerators in [\\_uart\\_interrupt\\_enable](#).

#### 18.2.7.15 `static void UART_EnableTx ( UART_Type * base, bool enable ) [inline], [static]`

This function enables or disables the UART transmitter.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | UART peripheral base address.     |
| <i>enable</i> | True to enable, false to disable. |

#### 18.2.7.16 `static void UART_EnableRx ( UART_Type * base, bool enable ) [inline], [static]`

This function enables or disables the UART receiver.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | UART peripheral base address.     |
| <i>enable</i> | True to enable, false to disable. |

#### 18.2.7.17 static void UART\_WriteByte ( **UART\_Type** \* *base*, **uint8\_t** *data* ) [inline], [static]

This function is used to write data to transmitter register. The upper layer must ensure that the TX register is empty or that the TX FIFO has room before calling this function.

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | UART peripheral base address.  |
| <i>data</i> | Data write to the TX register. |

#### 18.2.7.18 static **uint8\_t** UART\_ReadByte ( **UART\_Type** \* *base* ) [inline], [static]

This function is used to read data from receiver register. The upper layer must ensure that the receiver register is full or that the RX FIFO has data before calling this function.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | UART peripheral base address. |
|-------------|-------------------------------|

Returns

Data read from data register.

#### 18.2.7.19 status\_t UART\_WriteBlocking ( **UART\_Type** \* *base*, **const uint8\_t** \* *data*, **size\_t** *length* )

This function polls the TX register, waits for the TX register to be empty or for the TX FIFO to have room and writes data to the TX buffer.

Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>base</i>   | UART peripheral base address.       |
| <i>data</i>   | Start address of the data to write. |
| <i>length</i> | Size of the data to write.          |

Return values

|                             |                                         |
|-----------------------------|-----------------------------------------|
| <i>kStatus_UART_Timeout</i> | Transmission timed out and was aborted. |
| <i>kStatus_Success</i>      | Successfully wrote all data.            |

#### 18.2.7.20 **status\_t UART\_ReadBlocking ( UART\_Type \* *base*, uint8\_t \* *data*, size\_t *length* )**

This function polls the RX register, waits for the RX register to be full or for RX FIFO to have data, and reads data from the TX register.

Parameters

|               |                                                         |
|---------------|---------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                           |
| <i>data</i>   | Start address of the buffer to store the received data. |
| <i>length</i> | Size of the buffer.                                     |

Return values

|                                        |                                                 |
|----------------------------------------|-------------------------------------------------|
| <i>kStatus_UART_Rx-HardwareOverrun</i> | Receiver overrun occurred while receiving data. |
| <i>kStatus_UART_Noise-Error</i>        | A noise error occurred while receiving data.    |
| <i>kStatus_UART_Framing-Error</i>      | A framing error occurred while receiving data.  |
| <i>kStatus_UART_Parity-Error</i>       | A parity error occurred while receiving data.   |
| <i>kStatus_UART_Timeout</i>            | Transmission timed out and was aborted.         |
| <i>kStatus_Success</i>                 | Successfully received all data.                 |

#### 18.2.7.21 **void UART\_TransferCreateHandle ( UART\_Type \* *base*, uart\_handle\_t \* *handle*, uart\_transfer\_callback\_t *callback*, void \* *userData* )**

This function initializes the UART handle which can be used for other UART transactional APIs. Usually, for a specified UART instance, call this API once to get the initialized handle.

## Parameters

|                 |                                         |
|-----------------|-----------------------------------------|
| <i>base</i>     | UART peripheral base address.           |
| <i>handle</i>   | UART handle pointer.                    |
| <i>callback</i> | The callback function.                  |
| <i>userData</i> | The parameter of the callback function. |

**18.2.7.22 void UART\_TransferStartRingBuffer ( **UART\_Type** \* *base*, **uart\_handle\_t** \* *handle*, **uint8\_t** \* *ringBuffer*, **size\_t** *ringBufferSize* )**

This function sets up the RX ring buffer to a specific UART handle.

When the RX ring buffer is used, data received are stored into the ring buffer even when the user doesn't call the [UART\\_TransferReceiveNonBlocking\(\)](#) API. If data is already received in the ring buffer, the user can get the received data from the ring buffer directly.

## Note

When using the RX ring buffer, one byte is reserved for internal use. In other words, if *ringBufferSize* is 32, only 31 bytes are used for saving data.

## Parameters

|                       |                                                                                                  |
|-----------------------|--------------------------------------------------------------------------------------------------|
| <i>base</i>           | UART peripheral base address.                                                                    |
| <i>handle</i>         | UART handle pointer.                                                                             |
| <i>ringBuffer</i>     | Start address of the ring buffer for background receiving. Pass NULL to disable the ring buffer. |
| <i>ringBufferSize</i> | Size of the ring buffer.                                                                         |

**18.2.7.23 void UART\_TransferStopRingBuffer ( **UART\_Type** \* *base*, **uart\_handle\_t** \* *handle* )**

This function aborts the background transfer and uninstalls the ring buffer.

## Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |

### 18.2.7.24 size\_t **UART\_TransferGetRxRingBufferLength** ( **uart\_handle\_t \* handle** )

Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | UART handle pointer. |
|---------------|----------------------|

Returns

Length of received data in RX ring buffer.

### 18.2.7.25 status\_t **UART\_TransferSendNonBlocking** ( **UART\_Type \* base, uart\_handle\_t \* handle, uart\_transfer\_t \* xfer** )

This function sends data using an interrupt method. This is a non-blocking function, which returns directly without waiting for all data to be written to the TX register. When all data is written to the TX register in the ISR, the UART driver calls the callback function and passes the [kStatus\\_UART\\_TxIdle](#) as status parameter.

Note

The [kStatus\\_UART\\_TxIdle](#) is passed to the upper layer when all data is written to the TX register. However, it does not ensure that all data is sent out. Before disabling the TX, check the [kUART\\_TxTransmissionCompleteFlag](#) to ensure that the TX is finished.

Parameters

|               |                                                                |
|---------------|----------------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                                  |
| <i>handle</i> | UART handle pointer.                                           |
| <i>xfer</i>   | UART transfer structure. See <a href="#">uart_transfer_t</a> . |

Return values

|                                |                                                                                    |
|--------------------------------|------------------------------------------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully start the data transmission.                                          |
| <i>kStatus_UART_TxBusy</i>     | Previous transmission still not finished; data not all written to TX register yet. |
| <i>kStatus_InvalidArgument</i> | Invalid argument.                                                                  |

### 18.2.7.26 void **UART\_TransferAbortSend** ( **UART\_Type** \* *base*, **uart\_handle\_t** \* *handle* )

This function aborts the interrupt-driven data sending. The user can get the remainBytes to find out how many bytes are not sent out.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |

### 18.2.7.27 status\_t **UART\_TransferGetSendCount** ( **UART\_Type** \* *base*, **uart\_handle\_t** \* *handle*, **uint32\_t** \* *count* )

This function gets the number of bytes written to the UART TX register by using the interrupt method.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |
| <i>count</i>  | Send bytes count.             |

Return values

|                                      |                                                       |
|--------------------------------------|-------------------------------------------------------|
| <i>kStatus_NoTransferIn-Progress</i> | No send in progress.                                  |
| <i>kStatus_InvalidArgument</i>       | The parameter is invalid.                             |
| <i>kStatus_Success</i>               | Get successfully through the parameter <i>count</i> ; |

### 18.2.7.28 status\_t **UART\_TransferReceiveNonBlocking** ( **UART\_Type** \* *base*, **uart\_handle\_t** \* *handle*, **uart\_transfer\_t** \* *xfer*, **size\_t** \* *receivedBytes* )

This function receives data using an interrupt method. This is a non-blocking function, which returns without waiting for all data to be received. If the RX ring buffer is used and not empty, the data in the ring buffer is copied and the parameter *receivedBytes* shows how many bytes are copied from the ring

buffer. After copying, if the data in the ring buffer is not enough to read, the receive request is saved by the UART driver. When the new data arrives, the receive request is serviced first. When all data is received, the UART driver notifies the upper layer through a callback function and passes the status parameter [k\\_Status\\_UART\\_RxIdle](#). For example, the upper layer needs 10 bytes but there are only 5 bytes in the ring buffer. The 5 bytes are copied to the *xfer->data* and this function returns with the parameter *receivedBytes* set to 5. For the left 5 bytes, newly arrived data is saved from the *xfer->data[5]*. When 5 bytes are received, the UART driver notifies the upper layer. If the RX ring buffer is not enabled, this function enables the RX and RX interrupt to receive data to the *xfer->data*. When all data is received, the upper layer is notified.

#### Parameters

|                      |                                                                |
|----------------------|----------------------------------------------------------------|
| <i>base</i>          | UART peripheral base address.                                  |
| <i>handle</i>        | UART handle pointer.                                           |
| <i>xfer</i>          | UART transfer structure, see <a href="#">uart_transfer_t</a> . |
| <i>receivedBytes</i> | Bytes received from the ring buffer directly.                  |

#### Return values

|                                |                                                      |
|--------------------------------|------------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully queue the transfer into transmit queue. |
| <i>kStatus_UART_RxBusy</i>     | Previous receive request is not finished.            |
| <i>kStatus_InvalidArgument</i> | Invalid argument.                                    |

### 18.2.7.29 void **UART\_TransferAbortReceive** ( **UART\_Type \* base**, **uart\_handle\_t \* handle** )

This function aborts the interrupt-driven data receiving. The user can get the *remainBytes* to know how many bytes are not received yet.

#### Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |

### 18.2.7.30 status\_t **UART\_TransferGetReceiveCount** ( **UART\_Type \* base**, **uart\_handle\_t \* handle**, **uint32\_t \* count** )

This function gets the number of bytes that have been received.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | UART peripheral base address. |
| <i>handle</i> | UART handle pointer.          |
| <i>count</i>  | Receive bytes count.          |

Return values

|                                      |                                                       |
|--------------------------------------|-------------------------------------------------------|
| <i>kStatus_NoTransferIn-Progress</i> | No receive in progress.                               |
| <i>kStatus_InvalidArgument</i>       | Parameter is invalid.                                 |
| <i>kStatus_Success</i>               | Get successfully through the parameter <i>count</i> ; |

### 18.2.7.31 void **UART\_TransferHandleIRQ** ( **UART\_Type \* base, void \* irqHandle** )

This function handles the UART transmit and receive IRQ request.

Parameters

|                  |                               |
|------------------|-------------------------------|
| <i>base</i>      | UART peripheral base address. |
| <i>irqHandle</i> | UART handle pointer.          |

### 18.2.7.32 static void **UART\_EnableTxDMA** ( **UART\_Type \* base, bool enable** ) [**inline**], [**static**]

This function enables or disables the transmit request when the transmitter has one or more slots available in the TxFIFO. The fill level in the TxFIFO that generates the DMA request is controlled by the TXTL bits.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | UART peripheral base address.     |
| <i>enable</i> | True to enable, false to disable. |

### 18.2.7.33 static void **UART\_EnableRxDMA** ( **UART\_Type \* base, bool enable** ) [**inline**], [**static**]

This function enables or disables the receive request when the receiver has data in the RxFIFO. The fill level in the RxFIFO at which a DMA request is generated is controlled by the RXTL bits .

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | UART peripheral base address.     |
| <i>enable</i> | True to enable, false to disable. |

#### 18.2.7.34 static void UART\_SetTxFifoWatermark ( **UART\_Type** \* *base*, **uint8\_t** *watermark* ) [inline], [static]

A maskable interrupt is generated whenever the data level in the Tx FIFO falls below the Tx FIFO watermark.

Parameters

|                  |                        |
|------------------|------------------------|
| <i>base</i>      | UART base pointer.     |
| <i>watermark</i> | The Tx FIFO watermark. |

#### 18.2.7.35 static void UART\_SetRxRTSWatermark ( **UART\_Type** \* *base*, **uint8\_t** *watermark* ) [inline], [static]

The RTS signal deasserts whenever the data count in Rx FIFO reaches the Rx RTS watermark.

Parameters

|                  |                       |
|------------------|-----------------------|
| <i>base</i>      | UART base pointer.    |
| <i>watermark</i> | The Rx RTS watermark. |

#### 18.2.7.36 static void UART\_SetRxFifoWatermark ( **UART\_Type** \* *base*, **uint8\_t** *watermark* ) [inline], [static]

A maskable interrupt is generated whenever the data level in the Rx FIFO reaches the Rx FIFO watermark.

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | UART base pointer. |
|-------------|--------------------|

|                  |                        |
|------------------|------------------------|
| <i>watermark</i> | The Rx FIFO watermark. |
|------------------|------------------------|

### 18.2.7.37 static void UART\_EnableAutoBaudRate ( **UART\_Type** \* *base*, **bool** *enable* ) [**inline**], [**static**]

Parameters

|               |                                                                                                                                                                                                                                |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | UART base pointer.                                                                                                                                                                                                             |
| <i>enable</i> | Enable/Disable Automatic Baud Rate Detection feature. <ul style="list-style-type: none"> <li>• true: Enable Automatic Baud Rate Detection feature.</li> <li>• false: Disable Automatic Baud Rate Detection feature.</li> </ul> |

### 18.2.7.38 static bool UART\_IsAutoBaudRateComplete ( **UART\_Type** \* *base* ) [**inline**], [**static**]

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | UART base pointer. |
|-------------|--------------------|

Returns

- true: Automatic baud rate detection has finished.
- false: Automatic baud rate detection has not finished.

## 18.2.8 Variable Documentation

### 18.2.8.1 **void\*** **s\_uartHandle[]**

## 18.3 UART FreeRTOS Driver

### 18.3.1 Overview

#### Data Structures

- struct `_uart_rtos_config`  
*UART configuration structure.* [More...](#)

#### Typedefs

- typedef struct `_uart_rtos_config` `uart_rtos_config_t`  
*UART configuration structure.*

#### Driver version

- #define `FSL_UART_FREERTOS_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 1)`)  
*UART FreeRTOS driver version 2.1.1.*

#### UART RTOS Operation

- int `UART_RTOS_Init` (`uart_rtos_handle_t *handle, uart_handle_t *t_handle, const uart_rtos_config_t *cfg`)  
*Initializes a UART instance for operation in RTOS.*
- int `UART_RTOS_Deinit` (`uart_rtos_handle_t *handle`)  
*Deinitializes a UART instance for operation.*

#### UART transactional Operation

- int `UART_RTOS_Send` (`uart_rtos_handle_t *handle, uint8_t *buffer, uint32_t length`)  
*Sends data in the background.*
- int `UART_RTOS_Receive` (`uart_rtos_handle_t *handle, uint8_t *buffer, uint32_t length, size_t *received`)  
*Receives data.*

### 18.3.2 Data Structure Documentation

#### 18.3.2.1 struct `_uart_rtos_config`

##### Data Fields

- `UART_Type * base`  
*UART base address.*

- `uint32_t srclk`  
*UART source clock in Hz.*
- `uint32_t baudrate`  
*Desired communication speed.*
- `uart_parity_mode_t parity`  
*Parity setting.*
- `uart_stop_bit_count_t stopbits`  
*Number of stop bits to use.*
- `uint8_t * buffer`  
*Buffer for background reception.*
- `uint32_t buffer_size`  
*Size of buffer for background reception.*

### 18.3.3 Macro Definition Documentation

#### 18.3.3.1 `#define FSL_UART_FREERTOS_DRIVER_VERSION(MAKE_VERSION(2, 1, 1))`

### 18.3.4 Function Documentation

#### 18.3.4.1 `int UART_RTOS_Init( uart_rtos_handle_t * handle, uart_handle_t * t_handle, const uart_rtos_config_t * cfg )`

Parameters

|                       |                                                                                     |
|-----------------------|-------------------------------------------------------------------------------------|
| <code>handle</code>   | The RTOS UART handle, the pointer to an allocated space for RTOS context.           |
| <code>t_handle</code> | The pointer to the allocated space to store the transactional layer internal state. |
| <code>cfg</code>      | The pointer to the parameters required to configure the UART after initialization.  |

Returns

0 succeed; otherwise fail.

#### 18.3.4.2 `int UART_RTOS_Deinit( uart_rtos_handle_t * handle )`

This function deinitializes the UART module, sets all register values to reset value, and frees the resources.

Parameters

|               |                       |
|---------------|-----------------------|
| <i>handle</i> | The RTOS UART handle. |
|---------------|-----------------------|

#### 18.3.4.3 int **UART\_RTOS\_Send** ( *uart\_rtos\_handle\_t \* handle, uint8\_t \* buffer, uint32\_t length* )

This function sends data. It is a synchronous API. If the hardware buffer is full, the task is in the blocked state.

Parameters

|               |                                    |
|---------------|------------------------------------|
| <i>handle</i> | The RTOS UART handle.              |
| <i>buffer</i> | The pointer to the buffer to send. |
| <i>length</i> | The number of bytes to send.       |

#### 18.3.4.4 int **UART\_RTOS\_Receive** ( *uart\_rtos\_handle\_t \* handle, uint8\_t \* buffer, uint32\_t length, size\_t \* received* )

This function receives data from UART. It is a synchronous API. If data is immediately available, it is returned immediately and the number of bytes received.

Parameters

|                 |                                                                                         |
|-----------------|-----------------------------------------------------------------------------------------|
| <i>handle</i>   | The RTOS UART handle.                                                                   |
| <i>buffer</i>   | The pointer to the buffer to write received data.                                       |
| <i>length</i>   | The number of bytes to receive.                                                         |
| <i>received</i> | The pointer to a variable of <i>size_t</i> where the number of received data is filled. |

## 18.4 UART SDMA Driver

### 18.4.1 Overview

#### Data Structures

- struct `_uart_sdma_handle`  
*UART sDMA handle.* [More...](#)

#### Typedefs

- `typedef void(* uart_sdma_transfer_callback_t )(UART_Type *base, uart_sdma_handle_t *handle, status_t status, void *userData)`  
*UART transfer callback function.*

#### Driver version

- `#define FSL_UART_SDMA_DRIVER_VERSION (MAKE_VERSION(2, 3, 0))`  
*UART SDMA driver version.*

#### sDMA transactional

- `void UART_TransferCreateHandleSDMA (UART_Type *base, uart_sdma_handle_t *handle, uart_sdma_transfer_callback_t callback, void *userData, sdma_handle_t *txSdmaHandle, sdma_handle_t *rxSdmaHandle, uint32_t eventSourceTx, uint32_t eventSourceRx)`  
*Initializes the UART handle which is used in transactional functions.*
- `status_t UART_SendSDMA (UART_Type *base, uart_sdma_handle_t *handle, uart_transfer_t *xfer)`  
*Sends data using sDMA.*
- `status_t UART_ReceiveSDMA (UART_Type *base, uart_sdma_handle_t *handle, uart_transfer_t *xfer)`  
*Receives data using sDMA.*
- `void UART_TransferAbortSendSDMA (UART_Type *base, uart_sdma_handle_t *handle)`  
*Aborts the sent data using sDMA.*
- `void UART_TransferAbortReceiveSDMA (UART_Type *base, uart_sdma_handle_t *handle)`  
*Aborts the receive data using sDMA.*
- `void UART_TransferSdmaHandleIRQ (UART_Type *base, void *uartSdmaHandle)`  
*UART IRQ handle function.*

## 18.4.2 Data Structure Documentation

### 18.4.2.1 struct \_uart\_sdma\_handle

#### Data Fields

- `uart_sdma_transfer_callback_t callback`  
*Callback function.*
- `void *userData`  
*UART callback function parameter.*
- `size_t rxDataSizeAll`  
*Size of the data to receive.*
- `size_t txDataSizeAll`  
*Size of the data to send out.*
- `sdma_handle_t *txSdmaHandle`  
*The sDMA TX channel used.*
- `sdma_handle_t *rxSdmaHandle`  
*The sDMA RX channel used.*
- `volatile uint8_t txState`  
*TX transfer state.*
- `volatile uint8_t rxState`  
*RX transfer state.*

## Field Documentation

- (1) `uart_sdma_transfer_callback_t _uart_sdma_handle::callback`
- (2) `void* _uart_sdma_handle::userData`
- (3) `size_t _uart_sdma_handle::rxDataSizeAll`
- (4) `size_t _uart_sdma_handle::txDataSizeAll`
- (5) `sdma_handle_t* _uart_sdma_handle::txSdmaHandle`
- (6) `sdma_handle_t* _uart_sdma_handle::rxSdmaHandle`
- (7) `volatile uint8_t _uart_sdma_handle::txState`

## 18.4.3 Macro Definition Documentation

18.4.3.1 `#define FSL_UART_SDMA_DRIVER_VERSION (MAKE_VERSION(2, 3, 0))`

## 18.4.4 Typedef Documentation

18.4.4.1 `typedef void(* uart_sdma_transfer_callback_t)(UART_Type *base,  
uart_sdma_handle_t *handle, status_t status, void *userData)`

## 18.4.5 Function Documentation

18.4.5.1 `void UART_TransferCreateHandleSDMA ( UART_Type * base,  
uart_sdma_handle_t * handle, uart_sdma_transfer_callback_t callback, void *  
userData, sdma_handle_t * txSdmaHandle, sdma_handle_t * rxSdmaHandle,  
uint32_t eventSourceTx, uint32_t eventSourceRx )`

Parameters

|                      |                                                           |
|----------------------|-----------------------------------------------------------|
| <i>base</i>          | UART peripheral base address.                             |
| <i>handle</i>        | Pointer to the <code>uart_sdma_handle_t</code> structure. |
| <i>callback</i>      | UART callback, NULL means no callback.                    |
| <i>userData</i>      | User callback function data.                              |
| <i>rxSdmaHandle</i>  | User-requested DMA handle for RX DMA transfer.            |
| <i>txSdmaHandle</i>  | User-requested DMA handle for TX DMA transfer.            |
| <i>eventSourceTx</i> | Eventsource for TX DMA transfer.                          |
| <i>eventSourceRx</i> | Eventsource for RX DMA transfer.                          |

#### 18.4.5.2 `status_t UART_SendSDMA ( UART_Type * base, uart_sdma_handle_t * handle, uart_transfer_t * xfer )`

This function sends data using sDMA. This is a non-blocking function, which returns right away. When all data is sent, the send callback function is called.

Parameters

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                                       |
| <i>handle</i> | UART handle pointer.                                                |
| <i>xfer</i>   | UART sDMA transfer structure. See <a href="#">uart_transfer_t</a> . |

Return values

|                                |                                 |
|--------------------------------|---------------------------------|
| <i>kStatus_Success</i>         | if succeeded; otherwise failed. |
| <i>kStatus_UART_TxBusy</i>     | Previous transfer ongoing.      |
| <i>kStatus_InvalidArgument</i> | Invalid argument.               |

#### 18.4.5.3 `status_t UART_ReceiveSDMA ( UART_Type * base, uart_sdma_handle_t * handle, uart_transfer_t * xfer )`

This function receives data using sDMA. This is a non-blocking function, which returns right away. When all data is received, the receive callback function is called.

Parameters

|               |                                                                     |
|---------------|---------------------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                                       |
| <i>handle</i> | Pointer to the <code>uart_sdma_handle_t</code> structure.           |
| <i>xfer</i>   | UART sDMA transfer structure. See <a href="#">uart_transfer_t</a> . |

Return values

|                                |                                 |
|--------------------------------|---------------------------------|
| <i>kStatus_Success</i>         | if succeeded; otherwise failed. |
| <i>kStatus_UART_RxBusy</i>     | Previous transfer ongoing.      |
| <i>kStatus_InvalidArgument</i> | Invalid argument.               |

#### 18.4.5.4 void `UART_TransferAbortSendSDMA` ( `UART_Type * base, uart_sdma_handle_t * handle` )

This function aborts sent data using sDMA.

Parameters

|               |                                                           |
|---------------|-----------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                             |
| <i>handle</i> | Pointer to the <code>uart_sdma_handle_t</code> structure. |

#### 18.4.5.5 void `UART_TransferAbortReceiveSDMA` ( `UART_Type * base, uart_sdma_handle_t * handle` )

This function aborts receive data using sDMA.

Parameters

|               |                                                           |
|---------------|-----------------------------------------------------------|
| <i>base</i>   | UART peripheral base address.                             |
| <i>handle</i> | Pointer to the <code>uart_sdma_handle_t</code> structure. |

#### 18.4.5.6 void `UART_TransferSdmaHandleIRQ` ( `UART_Type * base, void * uartSdmaHandle` )

This function handles the UART transmit complete IRQ request and invoke user callback.

## Parameters

|                        |                               |
|------------------------|-------------------------------|
| <i>base</i>            | UART peripheral base address. |
| <i>uartSdma-Handle</i> | UART handle pointer.          |

## 18.5 UART CMSIS Driver

This section describes the programming interface of the UART Cortex Microcontroller Software Interface Standard (CMSIS) driver. And this driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method please refer to <http://www.-keil.com/pack/doc/cmsis/Driver/html/index.html>.

The UART driver includes transactional APIs.

Transactional APIs can be used to enable the peripheral quickly and in the application if the code size and performance of transactional APIs can satisfy the requirements. If the code size and performance are critical requirements please write custom code.

### 18.5.1 Function groups

#### 18.5.1.1 UART CMSIS GetVersion Operation

This function group will return the UART CMSIS Driver version to user.

#### 18.5.1.2 UART CMSIS GetCapabilities Operation

This function group will return the capabilities of this driver.

#### 18.5.1.3 UART CMSIS Initialize and Uninitialize Operation

This function will initialize and uninitialized the uart instance . And this API must be called before you configure an uart instance or after you Deinit an uart instance.The right steps to start an instance is that you must initialize the instance which been selected firstly,then you can power on the instance.After these all have been done,you can configure the instance by using control operation.If you want to Uninitialize the instance, you must power off the instance first.

#### 18.5.1.4 UART CMSIS Transfer Operation

This function group controls the transfer, send/receive data.

#### 18.5.1.5 UART CMSIS Status Operation

This function group gets the UART transfer status.

### 18.5.1.6 UART CMSIS Control Operation

This function can configure an instance ,set baudrate for uart, get current baudrate ,set transfer data bits and other control command.

# Chapter 19

## MU: Messaging Unit

### 19.1 Overview

The MCUXpresso SDK provides a driver for the MU module of MCUXpresso SDK devices.

### 19.2 Function description

The MU driver provides these functions:

- Functions to initialize the MU module.
- Functions to send and receive messages.
- Functions for MU flags for both MU sides.
- Functions for status flags and interrupts.
- Other miscellaneous functions.

#### 19.2.1 MU initialization

The function [MU\\_Init\(\)](#) initializes the MU module and enables the MU clock. It should be called before any other MU functions.

The function [MU\\_Deinit\(\)](#) deinitializes the MU module and disables the MU clock. No MU functions can be called after this function.

#### 19.2.2 MU message

The MU message must be sent when the transmit register is empty. The MU driver provides blocking API and non-blocking API to send message.

The [MU\\_SendMsgNonBlocking\(\)](#) function writes a message to the MU transmit register without checking the transmit register status. The upper layer should check that the transmit register is empty before calling this function. This function can be used in the ISR for better performance.

The [MU\\_SendMsg\(\)](#) function is a blocking function. It waits until the transmit register is empty and sends the message.

Correspondingly, there are blocking and non-blocking APIs for receiving a message. The [MU\\_ReadMsgNonBlocking\(\)](#) function is a non-blocking API. The [MU\\_ReadMsg\(\)](#) function is the blocking API.

### 19.2.3 MU flags

The MU driver provides 3-bit general purpose flags. When the flags are set on one side, they are reflected on the other side.

The MU flags must be set when the previous flags have been updated to the other side. The MU driver provides a non-blocking function and a blocking function. The blocking function [MU\\_SetFlags\(\)](#) waits until previous flags have been updated to the other side and then sets flags. The non-blocking function sets the flags directly. Ensure that the kMU\_FlagsUpdatingFlag is not pending before calling this function.

The function [MU\\_GetFlags\(\)](#) gets the MU flags on the current side.

### 19.2.4 Status and interrupt

The function [MU\\_GetStatusFlags\(\)](#) returns all MU status flags. Use the `_mu_status_flags` to check for specific flags, for example, to check RX0 and RX1 register full, use the following code:

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/mu. The receive full flags are cleared automatically after messages are read out. The transmit empty flags are cleared automatically after new messages are written to the transmit register. The general purpose interrupt flags must be cleared manually using the function [MU\\_ClearStatusFlags\(\)](#).

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/mu. To enable or disable a specific interrupt, use [MU\\_EnableInterrupts\(\)](#) and [MU\\_DisableInterrupts\(\)](#) functions. The interrupts to enable or disable should be passed in as a bit mask of the `_mu_interrupt_enable`.

The [MU\\_TriggerInterrupts\(\)](#) function triggers general purpose interrupts and NMI to the other core. The interrupts to trigger are passed in as a bit mask of the `_mu_interrupt_trigger`. If previously triggered interrupts have not been processed by the other side, this function returns an error.

### 19.2.5 MU misc functions

The [MU\\_BootCoreB\(\)](#) and [MU\\_HoldCoreBReset\(\)](#) functions should only be used from A side. They are used to boot the core B or to hold core B in reset.

The [MU\\_ResetBothSides\(\)](#) function resets MU at both A and B sides. However, only the A side can call this function.

If a core enters stop mode, the platform clock of this core is disabled by default. The function [MU\\_SetClockOnOtherCoreEnable\(\)](#) forces the other core's platform clock to remain enabled even after that core has entered a stop mode. In this case, the other core's platform clock keeps running until the current core enters stop mode too.

Function [MU\\_GetOtherCorePowerMode\(\)](#) gets the power mode of the other core.

## Typedefs

- **typedef enum \_mu\_msg\_reg\_index mu\_msg\_reg\_index\_t**  
*MU message register.*

## Enumerations

- **enum \_mu\_status\_flags {**  
 kMU\_Tx0EmptyFlag = (1U << (MU\_SR\_TEn\_SHIFT + 3U)),  
 kMU\_Tx1EmptyFlag = (1U << (MU\_SR\_TEn\_SHIFT + 2U)),  
 kMU\_Tx2EmptyFlag = (1U << (MU\_SR\_TEn\_SHIFT + 1U)),  
 kMU\_Tx3EmptyFlag = (1U << (MU\_SR\_TEn\_SHIFT + 0U)),  
 kMU\_Rx0FullFlag = (1U << (MU\_SR\_RFn\_SHIFT + 3U)),  
 kMU\_Rx1FullFlag = (1U << (MU\_SR\_RFn\_SHIFT + 2U)),  
 kMU\_Rx2FullFlag = (1U << (MU\_SR\_RFn\_SHIFT + 1U)),  
 kMU\_Rx3FullFlag = (1U << (MU\_SR\_RFn\_SHIFT + 0U)),  
 kMU\_GenInt0Flag = (1U << (MU\_SR\_GIPn\_SHIFT + 3U)),  
 kMU\_GenInt1Flag = (1U << (MU\_SR\_GIPn\_SHIFT + 2U)),  
 kMU\_GenInt2Flag = (1U << (MU\_SR\_GIPn\_SHIFT + 1U)),  
 kMU\_GenInt3Flag = (1U << (MU\_SR\_GIPn\_SHIFT + 0U)),  
 kMU\_EventPendingFlag = MU\_SR\_EP\_MASK,  
 kMU\_FlagsUpdatingFlag = MU\_SR\_FUP\_MASK,  
 kMU\_OtherSideInResetFlag = MU\_SR\_RS\_MASK }
- MU status flags.
- **enum \_mu\_interrupt\_enable {**  
 kMU\_Tx0EmptyInterruptEnable = (1U << (MU\_CR\_TIEn\_SHIFT + 3U)),  
 kMU\_Tx1EmptyInterruptEnable = (1U << (MU\_CR\_TIEn\_SHIFT + 2U)),  
 kMU\_Tx2EmptyInterruptEnable = (1U << (MU\_CR\_TIEn\_SHIFT + 1U)),  
 kMU\_Tx3EmptyInterruptEnable = (1U << (MU\_CR\_TIEn\_SHIFT + 0U)),  
 kMU\_Rx0FullInterruptEnable = (1U << (MU\_CR\_RIEn\_SHIFT + 3U)),  
 kMU\_Rx1FullInterruptEnable = (1U << (MU\_CR\_RIEn\_SHIFT + 2U)),  
 kMU\_Rx2FullInterruptEnable = (1U << (MU\_CR\_RIEn\_SHIFT + 1U)),  
 kMU\_Rx3FullInterruptEnable = (1U << (MU\_CR\_RIEn\_SHIFT + 0U)),  
 kMU\_GenInt0InterruptEnable = (int)(1U << (MU\_CR\_GIEn\_SHIFT + 3U)),  
 kMU\_GenInt1InterruptEnable = (1U << (MU\_CR\_GIEn\_SHIFT + 2U)),  
 kMU\_GenInt2InterruptEnable = (1U << (MU\_CR\_GIEn\_SHIFT + 1U)),  
 kMU\_GenInt3InterruptEnable = (1U << (MU\_CR\_GIEn\_SHIFT + 0U)) }
- MU interrupt source to enable.
- **enum \_mu\_interrupt\_trigger {**  
 kMU\_GenInt0InterruptTrigger = (1U << (MU\_CR\_GIRn\_SHIFT + 3U)),  
 kMU\_GenInt1InterruptTrigger = (1U << (MU\_CR\_GIRn\_SHIFT + 2U)),  
 kMU\_GenInt2InterruptTrigger = (1U << (MU\_CR\_GIRn\_SHIFT + 1U)),  
 kMU\_GenInt3InterruptTrigger = (1U << (MU\_CR\_GIRn\_SHIFT + 0U)) }
- MU interrupt that could be triggered to the other core.
- **enum \_mu\_msg\_reg\_index**  
*MU message register.*

## Driver version

- #define **FSL\_MU\_DRIVER\_VERSION** (MAKE\_VERSION(2, 1, 3))  
*MU driver version.*

## MU initialization.

- void **MU\_Init** (MU\_Type \*base)  
*Initializes the MU module.*
- void **MU\_Deinit** (MU\_Type \*base)  
*De-initializes the MU module.*

## MU Message

- static void **MU\_SendMsgNonBlocking** (MU\_Type \*base, uint32\_t regIndex, uint32\_t msg)  
*Writes a message to the TX register.*
- void **MU\_SendMsg** (MU\_Type \*base, uint32\_t regIndex, uint32\_t msg)  
*Blocks to send a message.*
- static uint32\_t **MU\_ReceiveMsgNonBlocking** (MU\_Type \*base, uint32\_t regIndex)  
*Reads a message from the RX register.*
- uint32\_t **MU\_ReceiveMsg** (MU\_Type \*base, uint32\_t regIndex)  
*Blocks to receive a message.*

## MU Flags

- static void **MU\_SetFlagsNonBlocking** (MU\_Type \*base, uint32\_t flags)  
*Sets the 3-bit MU flags reflect on the other MU side.*
- void **MU\_SetFlags** (MU\_Type \*base, uint32\_t flags)  
*Blocks setting the 3-bit MU flags reflect on the other MU side.*
- static uint32\_t **MU\_GetFlags** (MU\_Type \*base)  
*Gets the current value of the 3-bit MU flags set by the other side.*

## Status and Interrupt.

- static uint32\_t **MU\_GetStatusFlags** (MU\_Type \*base)  
*Gets the MU status flags.*
- static uint32\_t **MU\_GetInterruptsPending** (MU\_Type \*base)  
*Gets the MU IRQ pending status.*
- static void **MU\_ClearStatusFlags** (MU\_Type \*base, uint32\_t mask)  
*Clears the specific MU status flags.*
- static void **MU\_EnableInterrupts** (MU\_Type \*base, uint32\_t mask)  
*Enables the specific MU interrupts.*
- static void **MU\_DisableInterrupts** (MU\_Type \*base, uint32\_t mask)  
*Disables the specific MU interrupts.*
- **status\_t MU\_TriggerInterrupts** (MU\_Type \*base, uint32\_t mask)  
*Triggers interrupts to the other core.*

## MU misc functions

- static void **MU\_MaskHardwareReset** (MU\_Type \*base, bool mask)  
*Mask hardware reset by the other core.*

- static mu\_power\_mode\_t [MU\\_GetOtherCorePowerMode](#) (MU\_Type \*base)  
*Gets the power mode of the other core.*

## 19.3 Macro Definition Documentation

### 19.3.1 #define FSL\_MU\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 3))

## 19.4 Enumeration Type Documentation

### 19.4.1 enum \_mu\_status\_flags

Enumerator

*kMU\_Tx0EmptyFlag* TX0 empty.  
*kMU\_Tx1EmptyFlag* TX1 empty.  
*kMU\_Tx2EmptyFlag* TX2 empty.  
*kMU\_Tx3EmptyFlag* TX3 empty.  
*kMU\_Rx0FullFlag* RX0 full.  
*kMU\_Rx1FullFlag* RX1 full.  
*kMU\_Rx2FullFlag* RX2 full.  
*kMU\_Rx3FullFlag* RX3 full.  
*kMU\_GenInt0Flag* General purpose interrupt 0 pending.  
*kMU\_GenInt1Flag* General purpose interrupt 1 pending.  
*kMU\_GenInt2Flag* General purpose interrupt 2 pending.  
*kMU\_GenInt3Flag* General purpose interrupt 3 pending.  
*kMU\_EventPendingFlag* MU event pending.  
*kMU\_FlagsUpdatingFlag* MU flags update is on-going.  
*kMU\_OtherSideInResetFlag* The other side is in reset.

### 19.4.2 enum \_mu\_interrupt\_enable

Enumerator

*kMU\_Tx0EmptyInterruptEnable* TX0 empty.  
*kMU\_Tx1EmptyInterruptEnable* TX1 empty.  
*kMU\_Tx2EmptyInterruptEnable* TX2 empty.  
*kMU\_Tx3EmptyInterruptEnable* TX3 empty.  
*kMU\_Rx0FullInterruptEnable* RX0 full.  
*kMU\_Rx1FullInterruptEnable* RX1 full.  
*kMU\_Rx2FullInterruptEnable* RX2 full.  
*kMU\_Rx3FullInterruptEnable* RX3 full.  
*kMU\_GenInt0InterruptEnable* General purpose interrupt 0.  
*kMU\_GenInt1InterruptEnable* General purpose interrupt 1.  
*kMU\_GenInt2InterruptEnable* General purpose interrupt 2.  
*kMU\_GenInt3InterruptEnable* General purpose interrupt 3.

### 19.4.3 enum \_mu\_interrupt\_trigger

Enumerator

|                                    |                              |
|------------------------------------|------------------------------|
| <i>kMU_GenInt0InterruptTrigger</i> | General purpose interrupt 0. |
| <i>kMU_GenInt1InterruptTrigger</i> | General purpose interrupt 1. |
| <i>kMU_GenInt2InterruptTrigger</i> | General purpose interrupt 2. |
| <i>kMU_GenInt3InterruptTrigger</i> | General purpose interrupt 3. |

## 19.5 Function Documentation

### 19.5.1 void MU\_Init( MU\_Type \* *base* )

This function enables the MU clock only.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

### 19.5.2 void MU\_Deinit( MU\_Type \* *base* )

This function disables the MU clock only.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

### 19.5.3 static void MU\_SendMsgNonBlocking( MU\_Type \* *base*, uint32\_t *regIndex*, uint32\_t *msg* ) [inline], [static]

This function writes a message to the specific TX register. It does not check whether the TX register is empty or not. The upper layer should make sure the TX register is empty before calling this function. This function can be used in ISR for better performance.

```
* while (!(kMU_Tx0EmptyFlag & MU_GetStatusFlags(base))) { } Wait for TX0
register empty.
* MU_SendMsgNonBlocking(base, kMU_MsgReg0, MSG_VAL); Write message to the TX0
register.
*
```

## Parameters

|                 |                                                             |
|-----------------|-------------------------------------------------------------|
| <i>base</i>     | MU peripheral base address.                                 |
| <i>regIndex</i> | TX register index, see <a href="#">mu_msg_reg_index_t</a> . |
| <i>msg</i>      | Message to send.                                            |

**19.5.4 void MU\_SendMsg ( MU\_Type \* *base*, uint32\_t *regIndex*, uint32\_t *msg* )**

This function waits until the TX register is empty and sends the message.

## Parameters

|                 |                                                               |
|-----------------|---------------------------------------------------------------|
| <i>base</i>     | MU peripheral base address.                                   |
| <i>regIndex</i> | MU message register, see <a href="#">mu_msg_reg_index_t</a> . |
| <i>msg</i>      | Message to send.                                              |

**19.5.5 static uint32\_t MU\_ReceiveMsgNonBlocking ( MU\_Type \* *base*, uint32\_t *regIndex* ) [inline], [static]**

This function reads a message from the specific RX register. It does not check whether the RX register is full or not. The upper layer should make sure the RX register is full before calling this function. This function can be used in ISR for better performance.

```
* uint32_t msg;
* while (!(kMU_Rx0FullFlag & MU_GetStatusFlags(base)))
* {
* } Wait for the RX0 register full.
*
* msg = MU_ReceiveMsgNonBlocking(base, kMU_MsgReg0); Read message from RX0
* register.
*
```

## Parameters

|                 |                                                             |
|-----------------|-------------------------------------------------------------|
| <i>base</i>     | MU peripheral base address.                                 |
| <i>regIndex</i> | RX register index, see <a href="#">mu_msg_reg_index_t</a> . |

## Returns

The received message.

### 19.5.6 `uint32_t MU_ReceiveMsg ( MU_Type * base, uint32_t regIndex )`

This function waits until the RX register is full and receives the message.

## Parameters

|                 |                                                             |
|-----------------|-------------------------------------------------------------|
| <i>base</i>     | MU peripheral base address.                                 |
| <i>regIndex</i> | MU message register, see <a href="#">mu_msg_reg_index_t</a> |

## Returns

The received message.

### 19.5.7 static void MU\_SetFlagsNonBlocking ( MU\_Type \* *base*, uint32\_t *flags* ) [inline], [static]

This function sets the 3-bit MU flags directly. Every time the 3-bit MU flags are changed, the status flag kMU\_FlagsUpdatingFlag asserts indicating the 3-bit MU flags are updating to the other side. After the 3-bit MU flags are updated, the status flag kMU\_FlagsUpdatingFlag is cleared by hardware. During the flags updating period, the flags cannot be changed. The upper layer should make sure the status flag kMU\_FlagsUpdatingFlag is cleared before calling this function.

```
* while (kMU_FlagsUpdatingFlag & MU_GetStatusFlags(base))
{
} Wait for previous MU flags updating.
*
* MU_SetFlagsNonBlocking(base, 0U); Set the mU flags.
*
```

## Parameters

|              |                             |
|--------------|-----------------------------|
| <i>base</i>  | MU peripheral base address. |
| <i>flags</i> | The 3-bit MU flags to set.  |

### 19.5.8 void MU\_SetFlags ( MU\_Type \* *base*, uint32\_t *flags* )

This function blocks setting the 3-bit MU flags. Every time the 3-bit MU flags are changed, the status flag kMU\_FlagsUpdatingFlag asserts indicating the 3-bit MU flags are updating to the other side. After the 3-bit MU flags are updated, the status flag kMU\_FlagsUpdatingFlag is cleared by hardware. During the flags updating period, the flags cannot be changed. This function waits for the MU status flag kMU\_FlagsUpdatingFlag cleared and sets the 3-bit MU flags.

## Parameters

|              |                             |
|--------------|-----------------------------|
| <i>base</i>  | MU peripheral base address. |
| <i>flags</i> | The 3-bit MU flags to set.  |

**19.5.9 static uint32\_t MU\_GetFlags( MU\_Type \* *base* ) [inline], [static]**

This function gets the current 3-bit MU flags on the current side.

## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

## Returns

*flags* Current value of the 3-bit flags.

**19.5.10 static uint32\_t MU\_GetStatusFlags( MU\_Type \* *base* ) [inline], [static]**

This function returns the bit mask of the MU status flags. See `_mu_status_flags`.

```
* uint32_t flags;
* flags = MU_GetStatusFlags(base); Get all status flags.
* if (kMU_Tx0EmptyFlag & flags)
* {
* The TX0 register is empty. Message can be sent.
* MU_SendMsgNonBlocking(base, kMU_MsgReg0, MSG0_VAL);
* }
* if (kMU_Tx1EmptyFlag & flags)
* {
* The TX1 register is empty. Message can be sent.
* MU_SendMsgNonBlocking(base, kMU_MsgReg1, MSG1_VAL);
* }
```

## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

## Returns

Bit mask of the MU status flags, see `_mu_status_flags`.

**19.5.11 static uint32\_t MU\_GetInterruptsPending ( MU\_Type \* *base* ) [inline],  
[static]**

This function returns the bit mask of the pending MU IRQs.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

Returns

Bit mask of the MU IRQs pending.

### 19.5.12 static void MU\_ClearStatusFlags ( MU\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function clears the specific MU status flags. The flags to clear should be passed in as bit mask. See `_mu_status_flags`.

```
* Clear general interrupt 0 and general interrupt 1 pending flags.
* MU_ClearStatusFlags(base, kMU_GenInt0Flag |
 kMU_GenInt1Flag);
*
```

Parameters

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | MU peripheral base address.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <i>mask</i> | <p>Bit mask of the MU status flags. See <code>_mu_status_flags</code>. The following flags are cleared by hardware, this function could not clear them.</p> <ul style="list-style-type: none"> <li>• kMU_Tx0EmptyFlag</li> <li>• kMU_Tx1EmptyFlag</li> <li>• kMU_Tx2EmptyFlag</li> <li>• kMU_Tx3EmptyFlag</li> <li>• kMU_Rx0FullFlag</li> <li>• kMU_Rx1FullFlag</li> <li>• kMU_Rx2FullFlag</li> <li>• kMU_Rx3FullFlag</li> <li>• kMU_EventPendingFlag</li> <li>• kMU_FlagsUpdatingFlag</li> <li>• kMU_OtherSideInResetFlag</li> </ul> |

### 19.5.13 static void MU\_EnableInterrupts ( MU\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function enables the specific MU interrupts. The interrupts to enable should be passed in as bit mask. See `_mu_interrupt_enable`.

```
* Enable general interrupt 0 and TX0 empty interrupt.
* MU_EnableInterrupts(base, kMU_GenInt0InterruptEnable |
* kMU_Tx0EmptyInterruptEnable);
*
```

## Parameters

|             |                                                                        |
|-------------|------------------------------------------------------------------------|
| <i>base</i> | MU peripheral base address.                                            |
| <i>mask</i> | Bit mask of the MU interrupts. See <code>_mu_interrupt_enable</code> . |

#### 19.5.14 static void MU\_DisableInterrupts ( MU\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function disables the specific MU interrupts. The interrupts to disable should be passed in as bit mask. See `_mu_interrupt_enable`.

```
* Disable general interrupt 0 and TX0 empty interrupt.
* MU_DisableInterrupts(base, kMU_GenInt0InterruptEnable |
* kMU_Tx0EmptyInterruptEnable);
*
```

## Parameters

|             |                                                                        |
|-------------|------------------------------------------------------------------------|
| <i>base</i> | MU peripheral base address.                                            |
| <i>mask</i> | Bit mask of the MU interrupts. See <code>_mu_interrupt_enable</code> . |

#### 19.5.15 status\_t MU\_TriggerInterrupts ( MU\_Type \* *base*, uint32\_t *mask* )

This function triggers the specific interrupts to the other core. The interrupts to trigger are passed in as bit mask. See `_mu_interrupt_trigger`. The MU should not trigger an interrupt to the other core when the previous interrupt has not been processed by the other core. This function checks whether the previous interrupts have been processed. If not, it returns an error.

```
* if (kStatus_Success != MU_TriggerInterrupts(base,
* kMU_GenInt0InterruptTrigger |
* kMU_GenInt2InterruptTrigger))
* {
* Previous general purpose interrupt 0 or general purpose interrupt 2
* has not been processed by the other core.
* }
*
```

Parameters

|             |                                                                                 |
|-------------|---------------------------------------------------------------------------------|
| <i>base</i> | MU peripheral base address.                                                     |
| <i>mask</i> | Bit mask of the interrupts to trigger. See <code>_mu_interrupt_trigger</code> . |

Return values

|                        |                                              |
|------------------------|----------------------------------------------|
| <i>kStatus_Success</i> | Interrupts have been triggered successfully. |
| <i>kStatus_Fail</i>    | Previous interrupts have not been accepted.  |

### 19.5.16 static void MU\_MaskHardwareReset ( MU\_Type \* *base*, bool *mask* ) [inline], [static]

The other core could call `MU_HardwareResetOtherCore()` to reset current core. To mask the reset, call this function and pass in true.

Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | MU peripheral base address.                                    |
| <i>mask</i> | Pass true to mask the hardware reset, pass false to unmask it. |

### 19.5.17 static mu\_power\_mode\_t MU\_GetOtherCorePowerMode ( MU\_Type \* *base* ) [inline], [static]

This function gets the power mode of the other core.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

Returns

Power mode of the other core.

# Chapter 20

## PDM: Microphone Interface

### 20.1 Overview

#### Modules

- PDM Driver
- PDM SDMA Driver

### 20.2 *Typical use case*

## 20.3 PDM Driver

### 20.3.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Microphone Interface (PDM) module of MCUXpresso SDK devices.

PDM driver includes functional APIs and transactional APIs.

Functional APIs target low-level APIs. Functional APIs can be used for PDM initialization, configuration, and operation for the optimization and customization purpose. Using the functional API requires the knowledge of the PDM peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. PDM functional operation groups provide the functional API set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. Initialize the handle by calling the [PDM\\_TransferCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions [PDM\\_TransferReceive-NonBlocking\(\)](#) set up the interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with kStatus\_PDM\_Idle status.

### 20.3.2 Typical use case

#### 20.3.2.1 PDM receive using an interrupt method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pdm\_interrupt

#### 20.3.2.2 PDM receive using a SDMA method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pdm/pdm\_sdma\_transfer

#### 20.3.2.3 PDM receive using a EDMA method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pdm/pdm\_edma\_transfer Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pdm/pdm\_sai\_edma Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pdm/pdm\_sai\_multi\_channel\_edma

### 20.3.2.4 PDM receive using a transactional method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pdm/pdm\_interrupt\_transfer

## Data Structures

- struct [\\_pdm\\_channel\\_config](#)  
*PDM channel configurations.* [More...](#)
- struct [\\_pdm\\_config](#)  
*PDM user configuration structure.* [More...](#)
- struct [\\_pdm\\_hwvad\\_config](#)  
*PDM voice activity detector user configuration structure.* [More...](#)
- struct [\\_pdm\\_hwvad\\_noise\\_filter](#)  
*PDM voice activity detector noise filter user configuration structure.* [More...](#)
- struct [\\_pdm\\_hwvad\\_zero\\_cross\\_detector](#)  
*PDM voice activity detector zero cross detector configuration structure.* [More...](#)
- struct [\\_pdm\\_transfer](#)  
*PDM SDMA transfer structure.* [More...](#)
- struct [\\_pdm\\_hwvad\\_notification](#)  
*PDM HWVAD notification structure.* [More...](#)
- struct [\\_pdm\\_handle](#)  
*PDM handle structure.* [More...](#)

## Macros

- #define [PDM\\_XFER\\_QUEUE\\_SIZE](#) (4U)  
*PDM XFER QUEUE SIZE.*

## Typedefs

- typedef enum [\\_pdm\\_dc\\_remover](#) pdm\_dc\_remover\_t  
*PDM DC remover configurations.*
- typedef enum [\\_pdm\\_df\\_quality\\_mode](#) pdm\_df\_quality\_mode\_t  
*PDM decimation filter quality mode.*
- typedef enum [\\_pdm\\_df\\_output\\_gain](#) pdm\_df\_output\_gain\_t  
*PDM decimation filter output gain.*
- typedef struct [\\_pdm\\_channel\\_config](#) pdm\_channel\_config\_t  
*PDM channel configurations.*
- typedef struct [\\_pdm\\_config](#) pdm\_config\_t  
*PDM user configuration structure.*
- typedef enum [\\_pdm\\_hwvad\\_hpf\\_config](#) pdm\_hwvad\_hpf\_config\_t  
*High pass filter configure cut-off frequency.*
- typedef enum [\\_pdm\\_hwvad\\_filter\\_status](#) pdm\_hwvad\_filter\_status\_t  
*HWVAD internal filter status.*
- typedef struct [\\_pdm\\_hwvad\\_config](#) pdm\_hwvad\_config\_t

- *PDM voice activity detector user configuration structure.*
- **typedef struct**  
`_pdm_hwvad_noise_filter pdm_hwvad_noise_filter_t`  
*PDM voice activity detector noise filter user configuration structure.*
- **typedef enum** `_pdm_hwvad_zcd_result pdm_hwvad_zcd_result_t`  
*PDM voice activity detector zero cross detector result.*
- **typedef struct**  
`_pdm_hwvad_zero_cross_detector pdm_hwvad_zero_cross_detector_t`  
*PDM voice activity detector zero cross detector configuration structure.*
- **typedef struct** `_pdm_transfer pdm_transfer_t`  
*PDM SDMA transfer structure.*
- **typedef struct** `_pdm_handle pdm_handle_t`  
*PDM handle.*
- **typedef void(\* pdm\_transfer\_callback\_t)(PDM\_Type \*base, pdm\_handle\_t \*handle, status\_t status, void \*userData)**  
*PDM transfer callback prototype.*
- **typedef void(\* pdm\_hwvad\_callback\_t )(status\_t status, void \*userData)**  
*PDM HWVAD callback prototype.*
- **typedef struct**  
`_pdm_hwvad_notification pdm_hwvad_notification_t`  
*PDM HWVAD notification structure.*

## Enumerations

- **enum {**  
`kStatus_PDM_Busy = MAKE_STATUS(kStatusGroup_PDM, 0),`  
`kStatus_PDM_CLK_LOW = MAKE_STATUS(kStatusGroup_PDM, 1),`  
`kStatus_PDM_FIFO_ERROR = MAKE_STATUS(kStatusGroup_PDM, 2),`  
`kStatus_PDM_QueueFull = MAKE_STATUS(kStatusGroup_PDM, 3),`  
`kStatus_PDM_Idle = MAKE_STATUS(kStatusGroup_PDM, 4),`  
`kStatus_PDM_Output_ERROR = MAKE_STATUS(kStatusGroup_PDM, 5),`  
`kStatus_PDM_ChannelConfig_Failed = MAKE_STATUS(kStatusGroup_PDM, 6),`  
`kStatus_PDM_HWVAD_VoiceDetected = MAKE_STATUS(kStatusGroup_PDM, 7),`  
`kStatus_PDM_HWVAD_Error = MAKE_STATUS(kStatusGroup_PDM, 8) }`  
*PDM return status.*
- **enum \_pdm\_interrupt\_enable {**  
`kPDM_ErrorInterruptEnable = PDM_CTRL_1_ERREN_MASK,`  
`kPDM_FIFOInterruptEnable = PDM_CTRL_1_DISEL(2U) }`  
*The PDM interrupt enable flag.*
- **enum \_pdm\_internal\_status {**

```
kPDM_StatusDfBusyFlag = (int)PDM_STAT_BSY_FIL_MASK,
kPDM_StatusFrequencyLow = PDM_STAT_LOWFREQF_MASK,
kPDM_StatusCh0FifoDataAvailable = PDM_STAT_CH0F_MASK,
kPDM_StatusCh1FifoDataAvailable = PDM_STAT_CH1F_MASK,
kPDM_StatusCh2FifoDataAvailable = PDM_STAT_CH2F_MASK,
kPDM_StatusCh3FifoDataAvailable = PDM_STAT_CH3F_MASK,
kPDM_StatusCh4FifoDataAvailable = PDM_STAT_CH4F_MASK,
kPDM_StatusCh5FifoDataAvailable = PDM_STAT_CH5F_MASK,
kPDM_StatusCh6FifoDataAvailable = PDM_STAT_CH6F_MASK,
kPDM_StatusCh7FifoDataAvailable = PDM_STAT_CH7F_MASK }
```

*The PDM status.*

- enum `_pdm_channel_enable_mask` {
 

```
kPDM_EnableChannel0 = PDM_STAT_CH0F_MASK,
kPDM_EnableChannel1 = PDM_STAT_CH1F_MASK,
kPDM_EnableChannel2 = PDM_STAT_CH2F_MASK,
kPDM_EnableChannel3 = PDM_STAT_CH3F_MASK,
kPDM_EnableChannel4 = PDM_STAT_CH4F_MASK,
kPDM_EnableChannel5 = PDM_STAT_CH5F_MASK,
kPDM_EnableChannel6 = PDM_STAT_CH6F_MASK,
kPDM_EnableChannel7 = PDM_STAT_CH7F_MASK }
```

*PDM channel enable mask.*

- enum `_pdm_fifo_status` {
 

```
kPDM_FifoStatusUnderflowCh0 = PDM_FIFO_STAT_FIFOUND0_MASK,
kPDM_FifoStatusUnderflowCh1 = PDM_FIFO_STAT_FIFOUND1_MASK,
kPDM_FifoStatusUnderflowCh2 = PDM_FIFO_STAT_FIFOUND2_MASK,
kPDM_FifoStatusUnderflowCh3 = PDM_FIFO_STAT_FIFOUND3_MASK,
kPDM_FifoStatusUnderflowCh4 = PDM_FIFO_STAT_FIFOUND4_MASK,
kPDM_FifoStatusUnderflowCh5 = PDM_FIFO_STAT_FIFOUND5_MASK,
kPDM_FifoStatusUnderflowCh6 = PDM_FIFO_STAT_FIFOUND6_MASK,
kPDM_FifoStatusUnderflowCh7 = PDM_FIFO_STAT_FIFOUND6_MASK,
kPDM_FifoStatusOverflowCh0 = PDM_FIFO_STAT_FIFOOVF0_MASK,
kPDM_FifoStatusOverflowCh1 = PDM_FIFO_STAT_FIFOOVF1_MASK,
kPDM_FifoStatusOverflowCh2 = PDM_FIFO_STAT_FIFOOVF2_MASK,
kPDM_FifoStatusOverflowCh3 = PDM_FIFO_STAT_FIFOOVF3_MASK,
kPDM_FifoStatusOverflowCh4 = PDM_FIFO_STAT_FIFOOVF4_MASK,
kPDM_FifoStatusOverflowCh5 = PDM_FIFO_STAT_FIFOOVF5_MASK,
kPDM_FifoStatusOverflowCh6 = PDM_FIFO_STAT_FIFOOVF6_MASK,
kPDM_FifoStatusOverflowCh7 = PDM_FIFO_STAT_FIFOOVF7_MASK }
```

*The PDM fifo status.*

- enum `_pdm_range_status` {

```

kPDM_RangeStatusUnderFlowCh0 = PDM_RANGE_STAT_RANGEUNF0_MASK,
kPDM_RangeStatusUnderFlowCh1 = PDM_RANGE_STAT_RANGEUNF1_MASK,
kPDM_RangeStatusUnderFlowCh2 = PDM_RANGE_STAT_RANGEUNF2_MASK,
kPDM_RangeStatusUnderFlowCh3 = PDM_RANGE_STAT_RANGEUNF3_MASK,
kPDM_RangeStatusUnderFlowCh4 = PDM_RANGE_STAT_RANGEUNF4_MASK,
kPDM_RangeStatusUnderFlowCh5 = PDM_RANGE_STAT_RANGEUNF5_MASK,
kPDM_RangeStatusUnderFlowCh6 = PDM_RANGE_STAT_RANGEUNF6_MASK,
kPDM_RangeStatusUnderFlowCh7 = PDM_RANGE_STAT_RANGEUNF7_MASK,
kPDM_RangeStatusOverFlowCh0 = PDM_RANGE_STAT_RANGEOVF0_MASK,
kPDM_RangeStatusOverFlowCh1 = PDM_RANGE_STAT_RANGEOVF1_MASK,
kPDM_RangeStatusOverFlowCh2 = PDM_RANGE_STAT_RANGEOVF2_MASK,
kPDM_RangeStatusOverFlowCh3 = PDM_RANGE_STAT_RANGEOVF3_MASK,
kPDM_RangeStatusOverFlowCh4 = PDM_RANGE_STAT_RANGEOVF4_MASK,
kPDM_RangeStatusOverFlowCh5 = PDM_RANGE_STAT_RANGEOVF5_MASK,
kPDM_RangeStatusOverFlowCh6 = PDM_RANGE_STAT_RANGEOVF6_MASK,
kPDM_RangeStatusOverFlowCh7 = PDM_RANGE_STAT_RANGEOVF7_MASK }

```

*The PDM output status.*

- enum `_pdm_dc_remover` {
   
kPDM\_DcRemoverCutOff21Hz = 0U,
   
kPDM\_DcRemoverCutOff83Hz = 1U,
   
kPDM\_DcRemoverCutOff152Hz = 2U,
   
kPDM\_DcRemoverBypass = 3U }

*PDM DC remover configurations.*

- enum `_pdm_df_quality_mode` {
   
kPDM\_QualityModeMedium = 0U,
   
kPDM\_QualityModeHigh = 1U,
   
kPDM\_QualityModeLow = 7U,
   
kPDM\_QualityModeVeryLow0 = 6U,
   
kPDM\_QualityModeVeryLow1 = 5U,
   
kPDM\_QualityModeVeryLow2 = 4U }

*PDM decimation filter quality mode.*

- enum `_pdm_qulaity_mode_k_factor` {
   
kPDM\_QualityModeHighKFactor = 1U,
   
kPDM\_QualityModeMediumKFactor = 2U,
   
kPDM\_QualityModeLowKFactor = 4U,
   
kPDM\_QualityModeVeryLow2KFactor = 8U }

*PDM quality mode K factor.*

- enum `_pdm_df_output_gain` {

```

kPDM_DfOutputGain0 = 0U,
kPDM_DfOutputGain1 = 1U,
kPDM_DfOutputGain2 = 2U,
kPDM_DfOutputGain3 = 3U,
kPDM_DfOutputGain4 = 4U,
kPDM_DfOutputGain5 = 5U,
kPDM_DfOutputGain6 = 6U,
kPDM_DfOutputGain7 = 7U,
kPDM_DfOutputGain8 = 8U,
kPDM_DfOutputGain9 = 9U,
kPDM_DfOutputGain10 = 0xAU,
kPDM_DfOutputGain11 = 0xBU,
kPDM_DfOutputGain12 = 0xCU,
kPDM_DfOutputGain13 = 0xDU,
kPDM_DfOutputGain14 = 0xEU,
kPDM_DfOutputGain15 = 0xFU }

```

*PDM decimation filter output gain.*

- enum `_pdm_data_width` {
   
kPDM\_DataWidth24 = 3U,
   
kPDM\_DataWidth32 = 4U }

*PDM data width.*

- enum `_pdm_hwvad_interrupt_enable` {
   
kPDM\_HwvadErrorInterruptEnable = PDM\_VAD0\_CTRL\_1\_VADERIE\_MASK,
   
kPDM\_HwvadInterruptEnable = PDM\_VAD0\_CTRL\_1\_VADIE\_MASK }
- PDM voice activity detector interrupt type.*

- enum `_pdm_hwvad_int_status` {
   
kPDM\_HwvadStatusInputSaturation = PDM\_VAD0\_STAT\_VADINSATF\_MASK,
   
kPDM\_HwvadStatusVoiceDetectFlag = PDM\_VAD0\_STAT\_VADIF\_MASK }

*The PDM hwvad interrupt status flag.*

- enum `_pdm_hwvad_hpf_config` {
   
kPDM\_HwvadHpfBypassed = 0x0U,
   
kPDM\_HwvadHpfCutOffFreq1750Hz = 0x1U,
   
kPDM\_HwvadHpfCutOffFreq215Hz = 0x2U,
   
kPDM\_HwvadHpfCutOffFreq102Hz = 0x3U }

*High pass filter configure cut-off frequency.*

- enum `_pdm_hwvad_filter_status` {
   
kPDM\_HwvadInternalFilterNormalOperation = 0U,
   
kPDM\_HwvadInternalFilterInitial = PDM\_VAD0\_CTRL\_1\_VADST10\_MASK }

*HWVAD internal filter status.*

- enum `_pdm_hwvad_zcd_result` {
   
kPDM\_HwvadResultOREnergyBasedDetection,
   
kPDM\_HwvadResultANDEnergyBasedDetection }

*PDM voice activity detector zero cross detector result.*

## Driver version

- #define **FSL\_PDM\_DRIVER\_VERSION** (MAKE\_VERSION(2, 9, 1))  
*Version 2.9.1.*

## Initialization and deinitialization

- void **PDM\_Init** (PDM\_Type \*base, const **pdm\_config\_t** \*config)  
*Initializes the PDM peripheral.*
- void **PDM\_Deinit** (PDM\_Type \*base)  
*De-initializes the PDM peripheral.*
- static void **PDM\_Reset** (PDM\_Type \*base)  
*Resets the PDM module.*
- static void **PDM\_Enable** (PDM\_Type \*base, bool enable)  
*Enables/disables PDM interface.*
- static void **PDM\_EnableDoze** (PDM\_Type \*base, bool enable)  
*Enables/disables DOZE.*
- static void **PDM\_EnableDebugMode** (PDM\_Type \*base, bool enable)  
*Enables/disables debug mode for PDM.*
- static void **PDM\_EnableInDebugMode** (PDM\_Type \*base, bool enable)  
*Enables/disables PDM interface in debug mode.*
- static void **PDM\_EnterLowLeakageMode** (PDM\_Type \*base, bool enable)  
*Enables/disables PDM interface disable/Low Leakage mode.*
- static void **PDM\_EnableChannel** (PDM\_Type \*base, uint8\_t channel, bool enable)  
*Enables/disables the PDM channel.*
- void **PDM\_SetChannelConfig** (PDM\_Type \*base, uint32\_t channel, const **pdm\_channel\_config\_t** \*config)  
*PDM one channel configurations.*
- status\_t **PDM\_SetSampleRateConfig** (PDM\_Type \*base, uint32\_t sourceClock\_HZ, uint32\_t sampleRate\_HZ)  
*PDM set sample rate.*
- status\_t **PDM\_SetSampleRate** (PDM\_Type \*base, uint32\_t enableChannelMask, **pdm\_df\_quality\_mode\_t** qualityMode, uint8\_t osr, uint32\_t clkDiv)  
*PDM set sample rate.*
- uint32\_t **PDMGetInstance** (PDM\_Type \*base)  
*Get the instance number for PDM.*

## Status

- static uint32\_t **PDM\_GetStatus** (PDM\_Type \*base)  
*Gets the PDM internal status flag.*
- static uint32\_t **PDM\_GetFifoStatus** (PDM\_Type \*base)  
*Gets the PDM FIFO status flag.*
- static uint32\_t **PDM\_GetRangeStatus** (PDM\_Type \*base)  
*Gets the PDM Range status flag.*
- static void **PDM\_ClearStatus** (PDM\_Type \*base, uint32\_t mask)  
*Clears the PDM Tx status.*
- static void **PDM\_ClearFIFOStatus** (PDM\_Type \*base, uint32\_t mask)

- Clears the PDM Tx status.
- static void [PDM\\_ClearRangeStatus](#) (PDM\_Type \*base, uint32\_t mask)  
*Clears the PDM range status.*

## Interrupts

- void [PDM\\_EnableInterrupts](#) (PDM\_Type \*base, uint32\_t mask)  
*Enables the PDM interrupt requests.*
- static void [PDM\\_DisableInterrupts](#) (PDM\_Type \*base, uint32\_t mask)  
*Disables the PDM interrupt requests.*

## DMA Control

- static void [PDM\\_EnableDMA](#) (PDM\_Type \*base, bool enable)  
*Enables/disables the PDM DMA requests.*
- static uint32\_t [PDM\\_GetDataRegisterAddress](#) (PDM\_Type \*base, uint32\_t channel)  
*Gets the PDM data register address.*

## Bus Operations

- void [PDM\\_ReadFifo](#) (PDM\_Type \*base, uint32\_t startChannel, uint32\_t channelNums, void \*buffer, size\_t size, uint32\_t dataWidth)  
*PDM read fifo.*
- static uint32\_t [PDM\\_ReadData](#) (PDM\_Type \*base, uint32\_t channel)  
*Reads data from the PDM FIFO.*
- void [PDM\\_SetChannelGain](#) (PDM\_Type \*base, uint32\_t channel, [pdm\\_df\\_output\\_gain\\_t](#) gain)  
*Set the PDM channel gain.*

## Voice Activity Detector

- void [PDM\\_SetHwvadConfig](#) (PDM\_Type \*base, const [pdm\\_hwvad\\_config\\_t](#) \*config)  
*Configure voice activity detector.*
- static void [PDM\\_ForceHwvadOutputDisable](#) (PDM\_Type \*base, bool enable)  
*PDM hwvad force output disable.*
- static void [PDM\\_ResetHwvad](#) (PDM\_Type \*base)  
*PDM hwvad reset.*
- static void [PDM\\_EnableHwvad](#) (PDM\_Type \*base, bool enable)  
*Enable/Disable Voice activity detector.*
- static void [PDM\\_EnableHwvadInterrupts](#) (PDM\_Type \*base, uint32\_t mask)  
*Enables the PDM Voice Detector interrupt requests.*
- static void [PDM\\_DisableHwvadInterrupts](#) (PDM\_Type \*base, uint32\_t mask)  
*Disables the PDM Voice Detector interrupt requests.*
- static void [PDM\\_ClearHwvadInterruptStatusFlags](#) (PDM\_Type \*base, uint32\_t mask)  
*Clears the PDM voice activity detector status flags.*
- static uint32\_t [PDM\\_GetHwvadInterruptStatusFlags](#) (PDM\_Type \*base)  
*Clears the PDM voice activity detector status flags.*

- static uint32\_t **PDM\_GetHvvadInitialFlag** (PDM\_Type \*base)  
*Get the PDM voice activity detector initial flags.*
- static uint32\_t **PDM\_GetHvvadVoiceDetectedFlag** (PDM\_Type \*base)  
*Get the PDM voice activity detector voice detected flags.*
- static void **PDM\_EnableHvvadSignalFilter** (PDM\_Type \*base, bool enable)  
*Enables/disables voice activity detector signal filter.*
- void **PDM\_SetHvvadSignalFilterConfig** (PDM\_Type \*base, bool enableMaxBlock, uint32\_t signalGain)  
*Configure voice activity detector signal filter.*
- void **PDM\_SetHvvadNoiseFilterConfig** (PDM\_Type \*base, const pdm\_hwvad\_noise\_filter\_t \*config)  
*Configure voice activity detector noise filter.*
- static void **PDM\_EnableHvvadZeroCrossDetector** (PDM\_Type \*base, bool enable)  
*Enables/disables voice activity detector zero cross detector.*
- void **PDM\_SetHvvadZeroCrossDetectorConfig** (PDM\_Type \*base, const pdm\_hwvad\_zero\_cross\_detector\_t \*config)  
*Configure voice activity detector zero cross detector.*
- static uint16\_t **PDM\_GetNoiseData** (PDM\_Type \*base)  
*Reads noise data.*
- static void **PDM\_SetHvvadInternalFilterStatus** (PDM\_Type \*base, pdm\_hwvad\_filter\_status\_t status)  
*set hwvad internal filter status .*
- void **PDM\_SetHvvadInEnvelopeBasedMode** (PDM\_Type \*base, const pdm\_hwvad\_config\_t \*hwvadConfig, const pdm\_hwvad\_noise\_filter\_t \*noiseConfig, const pdm\_hwvad\_zero\_cross\_detector\_t \*zcdConfig, uint32\_t signalGain)  
*set HWVAD in envelope based mode .*
- void **PDM\_SetHvvadInEnergyBasedMode** (PDM\_Type \*base, const pdm\_hwvad\_config\_t \*hwvadConfig, const pdm\_hwvad\_noise\_filter\_t \*noiseConfig, const pdm\_hwvad\_zero\_cross\_detector\_t \*zcdConfig, uint32\_t signalGain)  
*brief set HWVAD in energy based mode .*
- void **PDM\_EnableHvvadInterruptCallback** (PDM\_Type \*base, pdm\_hwvad\_callback\_t vadCallback, void \*userData, bool enable)  
*Enable/Disable hwvad callback.*

## Transactional

- void **PDM\_TransferCreateHandle** (PDM\_Type \*base, pdm\_handle\_t \*handle, pdm\_transfer\_callback\_t callback, void \*userData)  
*Initializes the PDM handle.*
- status\_t **PDM\_TransferSetChannelConfig** (PDM\_Type \*base, pdm\_handle\_t \*handle, uint32\_t channel, const pdm\_channel\_config\_t \*config, uint32\_t format)  
*PDM set channel transfer config.*
- status\_t **PDM\_TransferReceiveNonBlocking** (PDM\_Type \*base, pdm\_handle\_t \*handle, pdm\_transfer\_t \*xfer)  
*Performs an interrupt non-blocking receive transfer on PDM.*
- void **PDM\_TransferAbortReceive** (PDM\_Type \*base, pdm\_handle\_t \*handle)  
*Aborts the current IRQ receive.*
- void **PDM\_TransferHandleIRQ** (PDM\_Type \*base, pdm\_handle\_t \*handle)

*Tx interrupt handler.*

### 20.3.3 Data Structure Documentation

#### 20.3.3.1 struct \_pdm\_channel\_config

##### Data Fields

- `pdm_dc_remover_t cutOffFreq`  
*DC remover cut off frequency.*
- `pdm_df_output_gain_t gain`  
*Decimation Filter Output Gain.*

#### 20.3.3.2 struct \_pdm\_config

##### Data Fields

- `bool enableDoze`  
*This module will enter disable/low leakage mode if DOZEN is active with ipg\_doze is asserted.*
- `uint8_t fifoWatermark`  
*Watermark value for FIFO.*
- `pdm_df_quality_mode_t qualityMode`  
*Quality mode.*
- `uint8_t cicOverSampleRate`  
*CIC filter over sampling rate.*

#### 20.3.3.3 struct \_pdm\_hwvad\_config

##### Data Fields

- `uint8_t channel`  
*Which channel uses voice activity detector.*
- `uint8_t initializeTime`  
*Number of frames or samples to initialize voice activity detector.*
- `uint8_t cicOverSampleRate`  
*CIC filter over sampling rate.*
- `uint8_t inputGain`  
*Voice activity detector input gain.*
- `uint32_t frameTime`  
*Voice activity frame time.*
- `pdm_hwvad_hpf_config_t cutOffFreq`  
*High pass filter cut off frequency.*
- `bool enableFrameEnergy`  
*If frame energy enabled, true means enable.*
- `bool enablePreFilter`  
*If pre-filter enabled.*

## Field Documentation

(1) `uint8_t _pdm_hwvad_config::initializeTime`

### 20.3.3.4 struct \_pdm\_hwvad\_noise\_filter

#### Data Fields

- `bool enableAutoNoiseFilter`  
*If noise filterer automatically activated, true means enable.*
- `bool enableNoiseMin`  
*If Noise minimum block enabled, true means enabled.*
- `bool enableNoiseDecimation`  
*If enable noise input decimation.*
- `bool enableNoiseDetectOR`  
*Enables a OR logic in the output of minimum noise estimator block.*
- `uint32_t noiseFilterAdjustment`  
*The adjustment value of the noise filter.*
- `uint32_t noiseGain`  
*Gain value for the noise energy or envelope estimated.*

### 20.3.3.5 struct \_pdm\_hwvad\_zero\_cross\_detector

#### Data Fields

- `bool enableAutoThreshold`  
*If ZCD auto-threshold enabled, true means enabled.*
- `pdm_hwvad_zcd_result_t zcdAnd`  
*Is ZCD result is AND'ed with energy-based detection, false means OR'ed.*
- `uint32_t threshold`  
*The adjustment value of the noise filter.*
- `uint32_t adjustmentThreshold`  
*Gain value for the noise energy or envelope estimated.*

## Field Documentation

(1) `bool _pdm_hwvad_zero_cross_detector::enableAutoThreshold`

### 20.3.3.6 struct \_pdm\_transfer

#### Data Fields

- `volatile uint8_t * data`  
*Data start address to transfer.*
- `volatile size_t dataSize`  
*Total Transfer bytes size.*

## Field Documentation

- (1) volatile uint8\_t\* \_pdm\_transfer::data
- (2) volatile size\_t \_pdm\_transfer::dataSize

### 20.3.3.7 struct \_pdm\_hwvad\_notification

### 20.3.3.8 struct \_pdm\_handle

## Data Fields

- uint32\_t state  
*Transfer status.*
- pdm\_transfer\_callback\_t callback  
*Callback function called at transfer event.*
- void \* userData  
*Callback parameter passed to callback function.*
- pdm\_transfer\_t pdmQueue [PDM\_XFER\_QUEUE\_SIZE]  
*Transfer queue storing queued transfer.*
- size\_t transferSize [PDM\_XFER\_QUEUE\_SIZE]  
*Data bytes need to transfer.*
- volatile uint8\_t queueUser  
*Index for user to queue transfer.*
- volatile uint8\_t queueDriver  
*Index for driver to get the transfer data and size.*
- uint32\_t format  
*data format*
- uint8\_t watermark  
*Watermark value.*
- uint8\_t startChannel  
*end channel*
- uint8\_t channelNums  
*Enabled channel number.*

### 20.3.4 Enumeration Type Documentation

#### 20.3.4.1 anonymous enum

Enumerator

- kStatus\_PDM\_Busy* PDM is busy.
- kStatus\_PDM\_CLK\_LOW* PDM clock frequency low.
- kStatus\_PDM\_FIFO\_ERROR* PDM FIFO underrun or overflow.
- kStatus\_PDM\_QueueFull* PDM FIFO underrun or overflow.
- kStatus\_PDM\_Idle* PDM is idle.
- kStatus\_PDM\_Output\_ERROR* PDM is output error.
- kStatus\_PDM\_ChannelConfig\_Failed* PDM channel config failed.

*kStatus\_PDM\_HWVAD\_VoiceDetected* PDM hwvad voice detected.

*kStatus\_PDM\_HWVAD\_Error* PDM hwvad error.

#### 20.3.4.2 enum \_pdm\_interrupt\_enable

Enumerator

*kPDM\_ErrorInterruptEnable* PDM channel error interrupt enable.

*kPDM\_FIFOInterruptEnable* PDM channel FIFO interrupt.

#### 20.3.4.3 enum \_pdm\_internal\_status

Enumerator

*kPDM\_StatusDfBusyFlag* Decimation filter is busy processing data.

*kPDM\_StatusFrequencyLow* Mic app clock frequency not high enough.

*kPDM\_StatusCh0FifoDataAvailable* channel 0 fifo data reached watermark level

*kPDM\_StatusCh1FifoDataAvailable* channel 1 fifo data reached watermark level

*kPDM\_StatusCh2FifoDataAvailable* channel 2 fifo data reached watermark level

*kPDM\_StatusCh3FifoDataAvailable* channel 3 fifo data reached watermark level

*kPDM\_StatusCh4FifoDataAvailable* channel 4 fifo data reached watermark level

*kPDM\_StatusCh5FifoDataAvailable* channel 5 fifo data reached watermark level

*kPDM\_StatusCh6FifoDataAvailable* channel 6 fifo data reached watermark level

*kPDM\_StatusCh7FifoDataAvailable* channel 7 fifo data reached watermark level

#### 20.3.4.4 enum \_pdm\_channel\_enable\_mask

Enumerator

*kPDM\_EnableChannel0* channge1 0 enable mask

*kPDM\_EnableChannel1* channge1 1 enable mask

*kPDM\_EnableChannel2* channge1 2 enable mask

*kPDM\_EnableChannel3* channge1 3 enable mask

*kPDM\_EnableChannel4* channge1 4 enable mask

*kPDM\_EnableChannel5* channge1 5 enable mask

*kPDM\_EnableChannel6* channge1 6 enable mask

*kPDM\_EnableChannel7* channge1 7 enable mask

#### 20.3.4.5 enum \_pdm\_fifo\_status

Enumerator

*kPDM\_FifoStatusUnderflowCh0* channel0 fifo status underflow

|                                    |                                |
|------------------------------------|--------------------------------|
| <i>kPDM_FifoStatusUnderflowCh1</i> | channel1 fifo status underflow |
| <i>kPDM_FifoStatusUnderflowCh2</i> | channel2 fifo status underflow |
| <i>kPDM_FifoStatusUnderflowCh3</i> | channel3 fifo status underflow |
| <i>kPDM_FifoStatusUnderflowCh4</i> | channel4 fifo status underflow |
| <i>kPDM_FifoStatusUnderflowCh5</i> | channel5 fifo status underflow |
| <i>kPDM_FifoStatusUnderflowCh6</i> | channel6 fifo status underflow |
| <i>kPDM_FifoStatusUnderflowCh7</i> | channel7 fifo status underflow |
| <i>kPDM_FifoStatusOverflowCh0</i>  | channel0 fifo status overflow  |
| <i>kPDM_FifoStatusOverflowCh1</i>  | channel1 fifo status overflow  |
| <i>kPDM_FifoStatusOverflowCh2</i>  | channel2 fifo status overflow  |
| <i>kPDM_FifoStatusOverflowCh3</i>  | channel3 fifo status overflow  |
| <i>kPDM_FifoStatusOverflowCh4</i>  | channel4 fifo status overflow  |
| <i>kPDM_FifoStatusOverflowCh5</i>  | channel5 fifo status overflow  |
| <i>kPDM_FifoStatusOverflowCh6</i>  | channel6 fifo status overflow  |
| <i>kPDM_FifoStatusOverflowCh7</i>  | channel7 fifo status overflow  |

#### 20.3.4.6 enum \_pdm\_range\_status

Enumerator

|                                     |                                 |
|-------------------------------------|---------------------------------|
| <i>kPDM_RangeStatusUnderFlowCh0</i> | channel0 range status underflow |
| <i>kPDM_RangeStatusUnderFlowCh1</i> | channel1 range status underflow |
| <i>kPDM_RangeStatusUnderFlowCh2</i> | channel2 range status underflow |
| <i>kPDM_RangeStatusUnderFlowCh3</i> | channel3 range status underflow |
| <i>kPDM_RangeStatusUnderFlowCh4</i> | channel4 range status underflow |
| <i>kPDM_RangeStatusUnderFlowCh5</i> | channel5 range status underflow |
| <i>kPDM_RangeStatusUnderFlowCh6</i> | channel6 range status underflow |
| <i>kPDM_RangeStatusUnderFlowCh7</i> | channel7 range status underflow |
| <i>kPDM_RangeStatusOverFlowCh0</i>  | channel0 range status overflow  |
| <i>kPDM_RangeStatusOverFlowCh1</i>  | channel1 range status overflow  |
| <i>kPDM_RangeStatusOverFlowCh2</i>  | channel2 range status overflow  |
| <i>kPDM_RangeStatusOverFlowCh3</i>  | channel3 range status overflow  |
| <i>kPDM_RangeStatusOverFlowCh4</i>  | channel4 range status overflow  |
| <i>kPDM_RangeStatusOverFlowCh5</i>  | channel5 range status overflow  |
| <i>kPDM_RangeStatusOverFlowCh6</i>  | channel6 range status overflow  |
| <i>kPDM_RangeStatusOverFlowCh7</i>  | channel7 range status overflow  |

#### 20.3.4.7 enum \_pdm\_dc\_remover

Enumerator

|                                 |                          |
|---------------------------------|--------------------------|
| <i>kPDM_DcRemoverCutOff21Hz</i> | DC remover cut off 21HZ. |
| <i>kPDM_DcRemoverCutOff83Hz</i> | DC remover cut off 83HZ. |

***kPDM\_DcRemoverCutOff152Hz*** DC remover cut off 152HZ.

***kPDM\_DcRemoverBypass*** DC remover bypass.

#### 20.3.4.8 enum \_pdm\_df\_quality\_mode

Enumerator

***kPDM\_QualityModeMedium*** quality mode memdium

***kPDM\_QualityModeHigh*** quality mode high

***kPDM\_QualityModeLow*** quality mode low

***kPDM\_QualityModeVeryLow0*** quality mode very low0

***kPDM\_QualityModeVeryLow1*** quality mode very low1

***kPDM\_QualityModeVeryLow2*** quality mode very low2

#### 20.3.4.9 enum \_pdm\_qulaity\_mode\_k\_factor

Enumerator

***kPDM\_QualityModeHighKFactor*** high quality mode K factor = 1 / 2

***kPDM\_QualityModeMediumKFactor*** medium/very low0 quality mode K factor = 2 / 2

***kPDM\_QualityModeLowKFactor*** low/very low1 quality mode K factor = 4 / 2

***kPDM\_QualityModeVeryLow2KFactor*** very low2 quality mode K factor = 8 / 2

#### 20.3.4.10 enum \_pdm\_df\_output\_gain

Enumerator

***kPDM\_DfOutputGain0*** Decimation filter output gain 0.

***kPDM\_DfOutputGain1*** Decimation filter output gain 1.

***kPDM\_DfOutputGain2*** Decimation filter output gain 2.

***kPDM\_DfOutputGain3*** Decimation filter output gain 3.

***kPDM\_DfOutputGain4*** Decimation filter output gain 4.

***kPDM\_DfOutputGain5*** Decimation filter output gain 5.

***kPDM\_DfOutputGain6*** Decimation filter output gain 6.

***kPDM\_DfOutputGain7*** Decimation filter output gain 7.

***kPDM\_DfOutputGain8*** Decimation filter output gain 8.

***kPDM\_DfOutputGain9*** Decimation filter output gain 9.

***kPDM\_DfOutputGain10*** Decimation filter output gain 10.

***kPDM\_DfOutputGain11*** Decimation filter output gain 11.

***kPDM\_DfOutputGain12*** Decimation filter output gain 12.

***kPDM\_DfOutputGain13*** Decimation filter output gain 13.

***kPDM\_DfOutputGain14*** Decimation filter output gain 14.

***kPDM\_DfOutputGain15*** Decimation filter output gain 15.

#### 20.3.4.11 enum \_pdm\_data\_width

Enumerator

***kPDM\_DataWidth24*** PDM data width 24bit.

***kPDM\_DataWidth32*** PDM data width 32bit.

#### 20.3.4.12 enum \_pdm\_hwvad\_interrupt\_enable

Enumerator

***kPDM\_HwvadErrorInterruptEnable*** PDM channel HWVAD error interrupt enable.

***kPDM\_HwvadInterruptEnable*** PDM channel HWVAD interrupt.

#### 20.3.4.13 enum \_pdm\_hwvad\_int\_status

Enumerator

***kPDM\_HwvadStatusInputSaturation*** HWVAD saturation condition.

***kPDM\_HwvadStatusVoiceDetectFlag*** HWVAD voice detect interrupt triggered.

#### 20.3.4.14 enum \_pdm\_hwvad\_hpf\_config

Enumerator

***kPDM\_HwvadHpfBypassed*** High-pass filter bypass.

***kPDM\_HwvadHpfCutOffFreq1750Hz*** High-pass filter cut off frequency 1750HZ.

***kPDM\_HwvadHpfCutOffFreq215Hz*** High-pass filter cut off frequency 215HZ.

***kPDM\_HwvadHpfCutOffFreq102Hz*** High-pass filter cut off frequency 102HZ.

#### 20.3.4.15 enum \_pdm\_hwvad\_filter\_status

Enumerator

***kPDM\_HwvadInternalFilterNormalOperation*** internal filter ready for normal operation

***kPDM\_HwvadInternalFilterInitial*** interla filter are initial

#### 20.3.4.16 enum \_pdm\_hwvad\_zcd\_result

Enumerator

***kPDM\_HwvadResultOREnergyBasedDetection*** zero cross detector result will be OR with energy based detection

***kPDM\_HwvadResultANDEnergyBasedDetection*** zero cross detector result will be AND with energy based detection

### 20.3.5 Function Documentation

#### 20.3.5.1 void PDM\_Init ( **PDM\_Type** \* *base*, **const pdm\_config\_t** \* *config* )

Ungates the PDM clock, resets the module, and configures PDM with a configuration structure. The configuration structure can be custom filled or set with default values by PDM\_GetDefaultConfig().

##### Note

This API should be called at the beginning of the application to use the PDM driver. Otherwise, accessing the PDM module can cause a hard fault because the clock is not enabled.

##### Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | PDM base pointer             |
| <i>config</i> | PDM configuration structure. |

#### 20.3.5.2 void PDM\_Deinit ( **PDM\_Type** \* *base* )

This API gates the PDM clock. The PDM module can't operate unless PDM\_Init is called to enable the clock.

##### Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | PDM base pointer |
|-------------|------------------|

#### 20.3.5.3 static void PDM\_Reset ( **PDM\_Type** \* *base* ) [inline], [static]

##### Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | PDM base pointer |
|-------------|------------------|

#### 20.3.5.4 static void PDM\_Enable ( **PDM\_Type** \* *base*, **bool enable** ) [inline], [static]

Parameters

|               |                                                                             |
|---------------|-----------------------------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                                            |
| <i>enable</i> | True means PDM interface is enabled, false means PDM interface is disabled. |

#### 20.3.5.5 static void PDM\_EnableDoze ( PDM\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                                                                                                                                                |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                                                                                                                                               |
| <i>enable</i> | True means the module will enter Disable/Low Leakage mode when ipg_doze is asserted, false means the module will not enter Disable/Low Leakage mode when ipg_doze is asserted. |

#### 20.3.5.6 static void PDM\_EnableDebugMode ( PDM\_Type \* *base*, bool *enable* ) [inline], [static]

The PDM interface cannot enter debug mode once in Disable/Low Leakage or Low Power mode.

Parameters

|               |                                                                                      |
|---------------|--------------------------------------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                                                     |
| <i>enable</i> | True means PDM interface enter debug mode, false means PDM interface in normal mode. |

#### 20.3.5.7 static void PDM\_EnableInDebugMode ( PDM\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                                                                                                               |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                                                                                                              |
| <i>enable</i> | True means PDM interface is enabled debug mode, false means PDM interface is disabled after after completing the current frame in debug mode. |

#### 20.3.5.8 static void PDM\_EnterLowLeakageMode ( PDM\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                                                                       |
|---------------|-------------------------------------------------------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                                                                      |
| <i>enable</i> | True means PDM interface is in disable/low leakage mode, False means PDM interface is in normal mode. |

### 20.3.5.9 static void PDM\_EnableChannel ( PDM\_Type \* *base*, uint8\_t *channel*, bool *enable* ) [inline], [static]

Parameters

|                |                                                     |
|----------------|-----------------------------------------------------|
| <i>base</i>    | PDM base pointer                                    |
| <i>channel</i> | PDM channel number need to enable or disable.       |
| <i>enable</i>  | True means enable PDM channel, false means disable. |

### 20.3.5.10 void PDM\_SetChannelConfig ( PDM\_Type \* *base*, uint32\_t *channel*, const pdm\_channel\_config\_t \* *config* )

Parameters

|                |                                                                   |
|----------------|-------------------------------------------------------------------|
| <i>base</i>    | PDM base pointer                                                  |
| <i>config</i>  | PDM channel configurations.                                       |
| <i>channel</i> | channel number. after completing the current frame in debug mode. |

### 20.3.5.11 status\_t PDM\_SetSampleRateConfig ( PDM\_Type \* *base*, uint32\_t *sourceClock\_HZ*, uint32\_t *sampleRate\_HZ* )

Note

This function is depend on the configuration of the PDM and PDM channel, so the correct call sequence is

```
* PDM_Init(base, pdmConfig)
* PDM_SetChannelConfig(base, channel, &channelConfig)
* PDM_SetSampleRateConfig(base, source, sampleRate)
*
```

Parameters

|                       |                             |
|-----------------------|-----------------------------|
| <i>base</i>           | PDM base pointer            |
| <i>sourceClock_HZ</i> | PDM source clock frequency. |
| <i>sampleRate_HZ</i>  | PDM sample rate.            |

**20.3.5.12 status\_t PDM\_SetSampleRate ( PDM\_Type \* *base*, uint32\_t *enableChannelMask*, pdm\_df\_quality\_mode\_t *qualityMode*, uint8\_t *osr*, uint32\_t *clkDiv* )**

**Deprecated** Do not use this function. It has been superceded by [PDM\\_SetSampleRateConfig](#)

Parameters

|                           |                          |
|---------------------------|--------------------------|
| <i>base</i>               | PDM base pointer         |
| <i>enable-ChannelMask</i> | PDM channel enable mask. |
| <i>qualityMode</i>        | quality mode.            |
| <i>osr</i>                | cic oversample rate      |
| <i>clkDiv</i>             | clock divider            |

**20.3.5.13 uint32\_t PDMGetInstance ( PDM\_Type \* *base* )**

Parameters

|             |                   |
|-------------|-------------------|
| <i>base</i> | PDM base pointer. |
|-------------|-------------------|

**20.3.5.14 static uint32\_t PDM\_GetStatus ( PDM\_Type \* *base* ) [inline], [static]**

Use the Status Mask in \_pdm\_internal\_status to get the status value needed

Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | PDM base pointer |
|-------------|------------------|

Returns

PDM status flag value.

#### **20.3.5.15 static uint32\_t PDM\_GetFifoStatus ( PDM\_Type \* *base* ) [inline], [static]**

Use the Status Mask in \_pdm\_fifo\_status to get the status value needed

Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | PDM base pointer |
|-------------|------------------|

Returns

FIFO status.

#### **20.3.5.16 static uint32\_t PDM\_GetRangeStatus ( PDM\_Type \* *base* ) [inline], [static]**

Use the Status Mask in \_pdm\_range\_status to get the status value needed

Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | PDM base pointer |
|-------------|------------------|

Returns

output status.

#### **20.3.5.17 static void PDM\_ClearStatus ( PDM\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

Parameters

|             |                                                                                                                        |
|-------------|------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | PDM base pointer                                                                                                       |
| <i>mask</i> | State mask. It can be a combination of the status between kPDM_StatusFrequencyLow and kPDM_StatusCh7FifoDataAvailable. |

**20.3.5.18 static void PDM\_ClearFIFOStatus ( PDM\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

|             |                                                                        |
|-------------|------------------------------------------------------------------------|
| <i>base</i> | PDM base pointer                                                       |
| <i>mask</i> | State mask. It can be a combination of the status in _pdm_fifo_status. |

**20.3.5.19 static void PDM\_ClearRangeStatus ( PDM\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

|             |                                                                         |
|-------------|-------------------------------------------------------------------------|
| <i>base</i> | PDM base pointer                                                        |
| <i>mask</i> | State mask. It can be a combination of the status in _pdm_range_status. |

**20.3.5.20 void PDM\_EnableInterrupts ( PDM\_Type \* *base*, uint32\_t *mask* )**

Parameters

|             |                                                                                                                                                                                                            |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | PDM base pointer                                                                                                                                                                                           |
| <i>mask</i> | interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> <li>• kPDM_ErrorInterruptEnable</li> <li>• kPDM_FIFOInterruptEnable</li> </ul> |

**20.3.5.21 static void PDM\_DisableInterrupts ( PDM\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

|             |                                                                                                                                                                                                            |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | PDM base pointer                                                                                                                                                                                           |
| <i>mask</i> | interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> <li>• kPDM_ErrorInterruptEnable</li> <li>• kPDM_FIFOInterruptEnable</li> </ul> |

#### 20.3.5.22 static void PDM\_EnableDMA ( PDM\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                 |
|---------------|-------------------------------------------------|
| <i>base</i>   | PDM base pointer                                |
| <i>enable</i> | True means enable DMA, false means disable DMA. |

#### 20.3.5.23 static uint32\_t PDM\_GetDataRegisterAddress ( PDM\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This API is used to provide a transfer address for the PDM DMA transfer configuration.

Parameters

|                |                          |
|----------------|--------------------------|
| <i>base</i>    | PDM base pointer.        |
| <i>channel</i> | Which data channel used. |

Returns

data register address.

#### 20.3.5.24 void PDM\_ReadFifo ( PDM\_Type \* *base*, uint32\_t *startChannel*, uint32\_t *channelNums*, void \* *buffer*, size\_t *size*, uint32\_t *dataWidth* )

Note

: This function support 16 bit only for IP version that only supports 16bit.

Parameters

|                     |                            |
|---------------------|----------------------------|
| <i>base</i>         | PDM base pointer.          |
| <i>startChannel</i> | start channel number.      |
| <i>channelNums</i>  | total enabled channelnums. |
| <i>buffer</i>       | received buffer address.   |
| <i>size</i>         | number of samples to read. |
| <i>dataWidth</i>    | sample width.              |

**20.3.5.25 static uint32\_t PDM\_ReadData ( PDM\_Type \* *base*, uint32\_t *channel* )  
[inline], [static]**

Parameters

|                |                    |
|----------------|--------------------|
| <i>base</i>    | PDM base pointer.  |
| <i>channel</i> | Data channel used. |

Returns

Data in PDM FIFO.

**20.3.5.26 void PDM\_SetChannelGain ( PDM\_Type \* *base*, uint32\_t *channel*,  
pdm\_df\_output\_gain\_t *gain* )**

Please note for different quality mode, the valid gain value is different, reference RM for detail.

Parameters

|                |                                                        |
|----------------|--------------------------------------------------------|
| <i>base</i>    | PDM base pointer.                                      |
| <i>channel</i> | PDM channel index.                                     |
| <i>gain</i>    | channel gain, the register gain value range is 0 - 15. |

**20.3.5.27 void PDM\_SetHwvadConfig ( PDM\_Type \* *base*, const pdm\_hwvad\_config\_t \*  
*config* )**

Parameters

|               |                                                       |
|---------------|-------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                      |
| <i>config</i> | Voice activity detector configure structure pointer . |

### 20.3.5.28 static void PDM\_ForceHvvadOutputDisable ( PDM\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                          |
|---------------|----------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                         |
| <i>enable</i> | true is output force disable, false is output not force. |

### 20.3.5.29 static void PDM\_ResetHvvad ( PDM\_Type \* *base* ) [inline], [static]

It will reset VADNDATA register and will clean all internal buffers, should be called when the PDM isn't running.

Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | PDM base pointer |
|-------------|------------------|

### 20.3.5.30 static void PDM\_EnableHvvad ( PDM\_Type \* *base*, bool *enable* ) [inline], [static]

Should be called when the PDM isn't running.

Parameters

|               |                                                                 |
|---------------|-----------------------------------------------------------------|
| <i>base</i>   | PDM base pointer.                                               |
| <i>enable</i> | True means enable voice activity detector, false means disable. |

### 20.3.5.31 static void PDM\_EnableHvvadInterrupts ( PDM\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                                                                                                                                                                                                          |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | PDM base pointer                                                                                                                                                                                                         |
| <i>mask</i> | <p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> <li>• kPDM_HWVADErrorInterruptEnable</li> <li>• kPDM_HWVADIInterruptEnable</li> </ul> |

### 20.3.5.32 static void PDM\_DisableHwvadInterrupts ( PDM\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                                                                                                                                                                                                          |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | PDM base pointer                                                                                                                                                                                                         |
| <i>mask</i> | <p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> <li>• kPDM_HWVADErrorInterruptEnable</li> <li>• kPDM_HWVADIInterruptEnable</li> </ul> |

### 20.3.5.33 static void PDM\_ClearHwvadInterruptStatusFlags ( PDM\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                             |
|-------------|---------------------------------------------|
| <i>base</i> | PDM base pointer                            |
| <i>mask</i> | State mask,reference _pdm_hwvad_int_status. |

### 20.3.5.34 static uint32\_t PDM\_GetHwvadInterruptStatusFlags ( PDM\_Type \* *base* ) [inline], [static]

Parameters

---

|             |                  |
|-------------|------------------|
| <i>base</i> | PDM base pointer |
|-------------|------------------|

Returns

status, reference \_pdm\_hwvad\_int\_status

### 20.3.5.35 static uint32\_t PDM\_GetHwvadInitialFlag ( PDM\_Type \* *base* ) [inline], [static]

Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | PDM base pointer |
|-------------|------------------|

Returns

initial flag.

### 20.3.5.36 static uint32\_t PDM\_GetHwvadVoiceDetectedFlag ( PDM\_Type \* *base* ) [inline], [static]

NOte: this flag is auto cleared when voice gone.

Parameters

|             |                  |
|-------------|------------------|
| <i>base</i> | PDM base pointer |
|-------------|------------------|

Returns

voice detected flag.

### 20.3.5.37 static void PDM\_EnableHwvadSignalFilter ( PDM\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                       |
|---------------|-------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                      |
| <i>enable</i> | True means enable signal filter, false means disable. |

### 20.3.5.38 void PDM\_SetHwvadSignalFilterConfig ( PDM\_Type \* *base*, bool *enableMaxBlock*, uint32\_t *signalGain* )

Parameters

|                        |                                   |
|------------------------|-----------------------------------|
| <i>base</i>            | PDM base pointer                  |
| <i>enableMax-Block</i> | If signal maximum block enabled.  |
| <i>signalGain</i>      | Gain value for the signal energy. |

**20.3.5.39 void PDM\_SetHwvadNoiseFilterConfig ( PDM\_Type \* *base*, const pdm\_hwvad\_noise\_filter\_t \* *config* )**

Parameters

|               |                                                                    |
|---------------|--------------------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                                   |
| <i>config</i> | Voice activity detector noise filter configure structure pointer . |

**20.3.5.40 static void PDM\_EnableHwvadZeroCrossDetector ( PDM\_Type \* *base*, bool *enable* ) [inline], [static]**

Parameters

|               |                                                             |
|---------------|-------------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                            |
| <i>enable</i> | True means enable zero cross detector, false means disable. |

**20.3.5.41 void PDM\_SetHwvadZeroCrossDetectorConfig ( PDM\_Type \* *base*, const pdm\_hwvad\_zero\_cross\_detector\_t \* *config* )**

Parameters

|               |                                                                           |
|---------------|---------------------------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                                          |
| <i>config</i> | Voice activity detector zero cross detector configure structure pointer . |

**20.3.5.42 static uint16\_t PDM\_GetNoiseData ( PDM\_Type \* *base* ) [inline], [static]**

Parameters

|             |                   |
|-------------|-------------------|
| <i>base</i> | PDM base pointer. |
|-------------|-------------------|

Returns

Data in PDM noise data register.

#### 20.3.5.43 static void PDM\_SetHwvadInternalFilterStatus ( PDM\_Type \* *base*, pdm\_hwvad\_filter\_status\_t *status* ) [inline], [static]

Note: filter initial status should be asserted for two more cycles, then set it to normal operation.

Parameters

|               |                         |
|---------------|-------------------------|
| <i>base</i>   | PDM base pointer.       |
| <i>status</i> | internal filter status. |

#### 20.3.5.44 void PDM\_SetHwvadInEnvelopeBasedMode ( PDM\_Type \* *base*, const pdm\_hwvad\_config\_t \* *hwvadConfig*, const pdm\_hwvad\_noise\_filter\_t \* *noiseConfig*, const pdm\_hwvad\_zero\_cross\_detector\_t \* *zcdConfig*, uint32\_t *signalGain* )

Recommand configurations,

```
* static const pdm_hwvad_config_t hwvadConfig = {
* .channel = 0,
* .initializeTime = 10U,
* .cicOverSampleRate = 0U,
* .inputGain = 0U,
* .frameTime = 10U,
* .cutOffFreq = kPDM_HwvadHpfBypassed,
* .enableFrameEnergy = false,
* .enablePreFilter = true,
};

* static const pdm_hwvad_noise_filter_t noiseFilterConfig = {
* .enableAutoNoiseFilter = false,
* .enableNoiseMin = true,
* .enableNoiseDecimation = true,
* .noiseFilterAdjustment = 0U,
* .noiseGain = 7U,
* .enableNoiseDetectOR = true,
* };
*
```

Parameters

|                    |                                                                           |
|--------------------|---------------------------------------------------------------------------|
| <i>base</i>        | PDM base pointer.                                                         |
| <i>hwvadConfig</i> | internal filter status.                                                   |
| <i>noiseConfig</i> | Voice activity detector noise filter configure structure pointer.         |
| <i>zcdConfig</i>   | Voice activity detector zero cross detector configure structure pointer . |
| <i>signalGain</i>  | signal gain value.                                                        |

**20.3.5.45 void PDM\_SetHwvadInEnergyBasedMode ( PDM\_Type \* *base*, const pdm\_hwvad\_config\_t \* *hwvadConfig*, const pdm\_hwvad\_noise\_filter\_t \* *noiseConfig*, const pdm\_hwvad\_zero\_cross\_detector\_t \* *zcdConfig*, uint32\_t *signalGain* )**

Recommand configurations, code static const pdm\_hwvad\_config\_t hwvadConfig = { .channel = 0, .initializeTime = 10U, .cicOverSampleRate = 0U, .inputGain = 0U, .frameTime = 10U, .cutOffFreq = kPDM\_HwvadHpfBypassed, .enableFrameEnergy = true, .enablePreFilter = true, };

static const pdm\_hwvad\_noise\_filter\_t noiseFilterConfig = { .enableAutoNoiseFilter = true, .enableNoiseMin = false, .enableNoiseDecimation = false, .noiseFilterAdjustment = 0U, .noiseGain = 7U, .enableNoiseDetectOR = false, }; code param base PDM base pointer. param hwvadConfig internal filter status. param noiseConfig Voice activity detector noise filter configure structure pointer. param zcdConfig Voice activity detector zero cross detector configure structure pointer . param signalGain signal gain value, signal gain value should be properly according to application.

**20.3.5.46 void PDM\_EnableHwvadInterruptCallback ( PDM\_Type \* *base*, pdm\_hwvad\_callback\_t *vadCallback*, void \* *userData*, bool *enable* )**

This function enable/disable the hwvad interrupt for the selected PDM peripheral.

Parameters

|                    |                                                                           |
|--------------------|---------------------------------------------------------------------------|
| <i>base</i>        | Base address of the PDM peripheral.                                       |
| <i>vadCallback</i> | callback Pointer to store callback function, should be NULL when disable. |
| <i>userData</i>    | user data.                                                                |
| <i>enable</i>      | true is enable, false is disable.                                         |

Return values

|              |
|--------------|
| <i>None.</i> |
|--------------|

#### 20.3.5.47 void PDM\_TransferCreateHandle ( **PDM\_Type** \* *base*, **pdm\_handle\_t** \* *handle*, **pdm\_transfer\_callback\_t** *callback*, **void** \* *userData* )

This function initializes the handle for the PDM transactional APIs. Call this function once to get the handle initialized.

Parameters

|                 |                                                 |
|-----------------|-------------------------------------------------|
| <i>base</i>     | PDM base pointer.                               |
| <i>handle</i>   | PDM handle pointer.                             |
| <i>callback</i> | Pointer to the user callback function.          |
| <i>userData</i> | User parameter passed to the callback function. |

#### 20.3.5.48 status\_t PDM\_TransferSetChannelConfig ( **PDM\_Type** \* *base*, **pdm\_handle\_t** \* *handle*, **uint32\_t** *channel*, **const pdm\_channel\_config\_t** \* *config*, **uint32\_t** *format* )

Parameters

|                |                                                                 |
|----------------|-----------------------------------------------------------------|
| <i>base</i>    | PDM base pointer.                                               |
| <i>handle</i>  | PDM handle pointer.                                             |
| <i>channel</i> | PDM channel.                                                    |
| <i>config</i>  | channel config.                                                 |
| <i>format</i>  | data format, support data width configurations,_pdm_data_width. |

Return values

|                                          |                     |
|------------------------------------------|---------------------|
| <i>kStatus_PDM_Channel-Config_Failed</i> | or kStatus_Success. |
|------------------------------------------|---------------------|

#### 20.3.5.49 status\_t PDM\_TransferReceiveNonBlocking ( **PDM\_Type** \* *base*, **pdm\_handle\_t** \* *handle*, **pdm\_transfer\_t** \* *xfer* )

## Note

This API returns immediately after the transfer initiates. Call the PDM\_RxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not kStatus\_PDM\_Busy, the transfer is finished.

## Parameters

|               |                                                                        |
|---------------|------------------------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                                       |
| <i>handle</i> | Pointer to the pdm_handle_t structure which stores the transfer state. |
| <i>xfer</i>   | Pointer to the pdm_transfer_t structure.                               |

## Return values

|                         |                                        |
|-------------------------|----------------------------------------|
| <i>kStatus_Success</i>  | Successfully started the data receive. |
| <i>kStatus_PDM_Busy</i> | Previous receive still not finished.   |

**20.3.5.50 void PDM\_TransferAbortReceive ( PDM\_Type \* *base*, pdm\_handle\_t \* *handle* )**

## Note

This API can be called when an interrupt non-blocking transfer initiates to abort the transfer early.

## Parameters

|               |                                                                        |
|---------------|------------------------------------------------------------------------|
| <i>base</i>   | PDM base pointer                                                       |
| <i>handle</i> | Pointer to the pdm_handle_t structure which stores the transfer state. |

**20.3.5.51 void PDM\_TransferHandleIRQ ( PDM\_Type \* *base*, pdm\_handle\_t \* *handle* )**

## Parameters

|               |                                        |
|---------------|----------------------------------------|
| <i>base</i>   | PDM base pointer.                      |
| <i>handle</i> | Pointer to the pdm_handle_t structure. |

## 20.4 PDM SDMA Driver

### 20.4.1 Typical use case

### 20.4.2 Overview

The SDMA multi fifo script support transfer data between multi peripheral fifos and memory, a typical user case is that receiving multi PDM channel data and put it into memory as

| channel 0 | channel 1 | channel 2 | channel 3 | channel 4 | ..... |

Multi fifo script is target to implement above feature, it can supports 1.configurable fifo watermark range from 1~(2^12-1), it is a value of fifo\_watermark \* channel\_numbers 2.configurable fifo numbers, support up to 15 continuous fifos 3.configurable fifo address offset, support address offset up to 64

```
/* load sdma script */
SDMA_LoadScript()
/* pdm multi channel configurations */
PDM_SetChannelConfigSDMA()
PDM_SetChannelConfigSDMA()
PDM_SetChannelConfigSDMA()
PDM_SetChannelConfigSDMA()
.....
PDM_TransferReceiveSDMA
```

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pdm/pdm\_sai\_sdma

## Data Structures

- struct [\\_pdm\\_sdma\\_handle](#)  
*PDM DMA transfer handle, users should not touch the content of the handle.* [More...](#)

## TypeDefs

- [typedef void\(\\* pdm\\_sdma\\_callback\\_t \)](#)(PDM\_Type \*base, [pdm\\_sdma\\_handle\\_t](#) \*handle, [status\\_t](#) status, void \*userData)  
*PDM eDMA transfer callback function for finish and error.*

## Driver version

- #define [FSL\\_PDM\\_SDMA\\_DRIVER\\_VERSION](#) ([MAKE\\_VERSION](#)(2, 7, 0))  
*Version 2.7.0.*

## eDMA Transactional

- void **PDM\_TransferCreateHandleSDMA** (PDM\_Type \*base, pdm\_sdma\_handle\_t \*handle, pdm\_sdma\_callback\_t callback, void \*userData, sdma\_handle\_t \*dmaHandle, uint32\_t eventSource)  
*Initializes the PDM eDMA handle.*
- status\_t **PDM\_TransferReceiveSDMA** (PDM\_Type \*base, pdm\_sdma\_handle\_t \*handle, pdm\_transfer\_t \*xfer)  
*Performs a non-blocking PDM receive using eDMA.*
- void **PDM\_TransferAbortReceiveSDMA** (PDM\_Type \*base, pdm\_sdma\_handle\_t \*handle)  
*Aborts a PDM receive using eDMA.*
- void **PDM\_SetChannelConfigSDMA** (PDM\_Type \*base, pdm\_sdma\_handle\_t \*handle, uint32\_t channel, const pdm\_channel\_config\_t \*config)  
*PDM channel configurations.*
- void **PDM\_TransferTerminateReceiveSDMA** (PDM\_Type \*base, pdm\_sdma\_handle\_t \*handle)  
*Terminate all the PDM sdma receive transfer.*

### 20.4.3 Data Structure Documentation

#### 20.4.3.1 struct \_pdm\_sdma\_handle

##### Data Fields

- **sdma\_handle\_t \* dmaHandle**  
*DMA handler for PDM send.*
- **uint8\_t nbytes**  
*eDMA minor byte transfer count initially configured.*
- **uint8\_t fifoWidth**  
*fifo width*
- **uint8\_t endChannel**  
*The last enabled channel.*
- **uint8\_t channelNums**  
*total channel numbers*
- **uint32\_t count**  
*The transfer data count in a DMA request.*
- **uint32\_t state**  
*Internal state for PDM eDMA transfer.*
- **uint32\_t eventSource**  
*PDM event source number.*
- **pdm\_sdma\_callback\_t callback**  
*Callback for users while transfer finish or error occurs.*
- **void \* userData**  
*User callback parameter.*
- **sdma\_buffer\_descriptor\_t bdPool [PDM\_XFER\_QUEUE\_SIZE]**  
*BD pool for SDMA transfer.*
- **pdm\_transfer\_t pdmQueue [PDM\_XFER\_QUEUE\_SIZE]**  
*Transfer queue storing queued transfer.*
- **size\_t transferSize [PDM\_XFER\_QUEUE\_SIZE]**  
*Data bytes need to transfer.*
- **volatile uint8\_t queueUser**

- **volatile uint8\_t queueDriver**  
*Index for user to queue transfer.*
- **Index for driver to get the transfer data and size.**

## Field Documentation

- (1) **uint8\_t \_pdm\_sdma\_handle::nbytes**
- (2) **sdma\_buffer\_descriptor\_t \_pdm\_sdma\_handle::bdPool[PDM\_XFER\_QUEUE\_SIZE]**
- (3) **pdm\_transfer\_t \_pdm\_sdma\_handle::pdmQueue[PDM\_XFER\_QUEUE\_SIZE]**
- (4) **volatile uint8\_t \_pdm\_sdma\_handle::queueUser**

## 20.4.4 Function Documentation

### 20.4.4.1 void PDM\_TransferCreateHandleSDMA ( **PDM\_Type \* base**, **pdm\_sdma\_handle\_t \* handle**, **pdm\_sdma\_callback\_t callback**, **void \* userData**, **sdma\_handle\_t \* dmaHandle**, **uint32\_t eventSource** )

This function initializes the PDM DMA handle, which can be used for other PDM master transactional APIs. Usually, for a specified PDM instance, call this API once to get the initialized handle.

#### Parameters

|                    |                                                                      |
|--------------------|----------------------------------------------------------------------|
| <i>base</i>        | PDM base pointer.                                                    |
| <i>handle</i>      | PDM eDMA handle pointer.                                             |
| <i>callback</i>    | Pointer to user callback function.                                   |
| <i>userData</i>    | User parameter passed to the callback function.                      |
| <i>dmaHandle</i>   | eDMA handle pointer, this handle shall be static allocated by users. |
| <i>eventSource</i> | PDM event source number.                                             |

### 20.4.4.2 status\_t PDM\_TransferReceiveSDMA ( **PDM\_Type \* base**, **pdm\_sdma\_handle\_t \* handle**, **pdm\_transfer\_t \* xfer** )

#### Note

This interface returns immediately after the transfer initiates. Call the PDM\_GetReceiveRemaining-Bytes to poll the transfer status and check whether the PDM transfer is finished.

Parameters

|               |                                    |
|---------------|------------------------------------|
| <i>base</i>   | PDM base pointer                   |
| <i>handle</i> | PDM eDMA handle pointer.           |
| <i>xfer</i>   | Pointer to DMA transfer structure. |

Return values

|                                |                                        |
|--------------------------------|----------------------------------------|
| <i>kStatus_Success</i>         | Start a PDM eDMA receive successfully. |
| <i>kStatus_InvalidArgument</i> | The input argument is invalid.         |
| <i>kStatus_RxBusy</i>          | PDM is busy receiving data.            |

#### 20.4.4.3 void PDM\_TransferAbortReceiveSDMA ( PDM\_Type \* *base*, pdm\_sdma\_handle\_t \* *handle* )

Parameters

|               |                          |
|---------------|--------------------------|
| <i>base</i>   | PDM base pointer         |
| <i>handle</i> | PDM eDMA handle pointer. |

#### 20.4.4.4 void PDM\_SetChannelConfigSDMA ( PDM\_Type \* *base*, pdm\_sdma\_handle\_t \* *handle*, uint32\_t *channel*, const pdm\_channel\_config\_t \* *config* )

Parameters

|                |                          |
|----------------|--------------------------|
| <i>base</i>    | PDM base pointer.        |
| <i>handle</i>  | PDM eDMA handle pointer. |
| <i>channel</i> | channel number.          |
| <i>config</i>  | channel configurations.  |

#### 20.4.4.5 void PDM\_TransferTerminateReceiveSDMA ( PDM\_Type \* *base*, pdm\_sdma\_handle\_t \* *handle* )

## Parameters

|               |                          |
|---------------|--------------------------|
| <i>base</i>   | PDM base pointer.        |
| <i>handle</i> | PDM SDMA handle pointer. |

# Chapter 21

## RDC: Resource Domain Controller

### 21.1 Overview

The MCUXpresso SDK provides a driver for the RDC module of MCUXpresso SDK devices.

The Resource Domain Controller (RDC) provides robust support for the isolation of destination memory mapped locations such as peripherals and memory to a single core, a bus master, or set of cores and bus masters.

The RDC driver should be used together with the RDC\_SEMA42 driver.

### Data Structures

- struct `_rdc_hardware_config`  
*RDC hardware configuration.* [More...](#)
- struct `_rdc_domain_assignment`  
*Master domain assignment.* [More...](#)
- struct `_rdc_periph_access_config`  
*Peripheral domain access permission configuration.* [More...](#)
- struct `_rdc_mem_access_config`  
*Memory region domain access control configuration.* [More...](#)
- struct `_rdc_mem_status`  
*Memory region access violation status.* [More...](#)

### Typedefs

- typedef struct `_rdc_hardware_config` `rdc_hardware_config_t`  
*RDC hardware configuration.*
- typedef struct `_rdc_domain_assignment` `rdc_domain_assignment_t`  
*Master domain assignment.*
- typedef struct `_rdc_periph_access_config` `rdc_periph_access_config_t`  
*Peripheral domain access permission configuration.*
- typedef struct `_rdc_mem_access_config` `rdc_mem_access_config_t`  
*Memory region domain access control configuration.*
- typedef struct `_rdc_mem_status` `rdc_mem_status_t`  
*Memory region access violation status.*

### Enumerations

- enum `_rdc_interrupts` { `kRDC_RestoreCompleteInterrupt` = `RDC_INTCTRL_RCI_EN_MASK` }  
*RDC interrupts.*
- enum `_rdc_flags` { `kRDC_PowerDownDomainOn` = `RDC_STAT_PDS_MASK` }

- enum `_rdc_access_policy` {
   
    `kRDC_NoAccess` = 0,  
     `kRDC_WriteOnly` = 1,  
     `kRDC_ReadOnly` = 2,  
     `kRDC_ReadWrite` = 3 }
   
    *Access permission policy.*

## Functions

- void `RDC_Init` (`RDC_Type` \*base)
   
    *Initializes the RDC module.*
- void `RDC_Deinit` (`RDC_Type` \*base)
   
    *De-initializes the RDC module.*
- void `RDC_GetHardwareConfig` (`RDC_Type` \*base, `rdc_hardware_config_t` \*config)
   
    *Gets the RDC hardware configuration.*
- static void `RDC_EnableInterrupts` (`RDC_Type` \*base, `uint32_t` mask)
   
    *Enable interrupts.*
- static void `RDC_DisableInterrupts` (`RDC_Type` \*base, `uint32_t` mask)
   
    *Disable interrupts.*
- static `uint32_t` `RDC_GetInterruptStatus` (`RDC_Type` \*base)
   
    *Get the interrupt pending status.*
- static void `RDC_ClearInterruptStatus` (`RDC_Type` \*base, `uint32_t` mask)
   
    *Clear interrupt pending status.*
- static `uint32_t` `RDC_GetStatus` (`RDC_Type` \*base)
   
    *Get RDC status.*
- static void `RDC_ClearStatus` (`RDC_Type` \*base, `uint32_t` mask)
   
    *Clear RDC status.*
- void `RDC_SetMasterDomainAssignment` (`RDC_Type` \*base, `rdc_master_t` master, const `rdc_domain_assignment_t` \*domainAssignment)
   
    *Set master domain assignment.*
- void `RDC_GetDefaultMasterDomainAssignment` (`rdc_domain_assignment_t` \*domainAssignment)
   
    *Get default master domain assignment.*
- static void `RDC_LockMasterDomainAssignment` (`RDC_Type` \*base, `rdc_master_t` master)
   
    *Lock master domain assignment.*
- void `RDC_SetPeriphAccessConfig` (`RDC_Type` \*base, const `rdc_periph_access_config_t` \*config)
   
    *Set peripheral access policy.*
- void `RDC_GetDefaultPeriphAccessConfig` (`rdc_periph_access_config_t` \*config)
   
    *Get default peripheral access policy.*
- static void `RDC_LockPeriphAccessConfig` (`RDC_Type` \*base, `rdc_periph_t` periph)
   
    *Lock peripheral access policy configuration.*
- static `uint8_t` `RDC_GetPeriphAccessPolicy` (`RDC_Type` \*base, `rdc_periph_t` periph, `uint8_t` domainId)
   
    *Get the peripheral access policy for specific domain.*
- void `RDC_SetMemAccessConfig` (`RDC_Type` \*base, const `rdc_mem_access_config_t` \*config)
   
    *Set memory region access policy.*
- void `RDC_GetDefaultMemAccessConfig` (`rdc_mem_access_config_t` \*config)
   
    *Get default memory region access policy.*
- static void `RDC_LockMemAccessConfig` (`RDC_Type` \*base, `rdc_mem_t` mem)
   
    *Lock memory access policy configuration.*
- static void `RDC_SetMemAccessValid` (`RDC_Type` \*base, `rdc_mem_t` mem, `bool` valid)

- void [RDC\\_GetMemViolationStatus](#) (RDC\_Type \*base, rdc\_mem\_t mem, rdc\_mem\_status\_t \*status)  
*Enable or disable memory access policy configuration.*
- static void [RDC\\_ClearMemViolationFlag](#) (RDC\_Type \*base, rdc\_mem\_t mem)  
*Get the memory region violation status.*
- static uint8\_t [RDC\\_GetMemAccessPolicy](#) (RDC\_Type \*base, rdc\_mem\_t mem, uint8\_t domainId)  
*Clear the memory region violation flag.*
- static uint8\_t [RDC\\_GetCurrentMasterDomainId](#) (RDC\_Type \*base)  
*Get the memory region access policy for specific domain.*
- static uint8\_t [RDC\\_GetCurrentMasterDomainId](#) (RDC\_Type \*base)  
*Gets the domain ID of the current bus master.*

## 21.2 Data Structure Documentation

### 21.2.1 struct \_rdc\_hardware\_config

#### Data Fields

- uint32\_t **domainNumber**: 4  
*Number of domains.*
- uint32\_t **masterNumber**: 8  
*Number of bus masters.*
- uint32\_t **periphNumber**: 8  
*Number of peripherals.*
- uint32\_t **memNumber**: 8  
*Number of memory regions.*

#### Field Documentation

- (1) **uint32\_t \_rdc\_hardware\_config::domainNumber**
- (2) **uint32\_t \_rdc\_hardware\_config::masterNumber**
- (3) **uint32\_t \_rdc\_hardware\_config::periphNumber**
- (4) **uint32\_t \_rdc\_hardware\_config::memNumber**

### 21.2.2 struct \_rdc\_domain\_assignment

#### Data Fields

- uint32\_t **domainId**: 2U  
*Domain ID.*
- uint32\_t **pad0**: 29U  
*Reserved.*
- uint32\_t **lock**: 1U  
*Lock the domain assignment.*

**Field Documentation**

- (1) `uint32_t _rdc_domain_assignment::domainId`
- (2) `uint32_t _rdc_domain_assignment::__pad0__`
- (3) `uint32_t _rdc_domain_assignment::lock`

**21.2.3 struct \_rdc\_periph\_access\_config****Data Fields**

- `rdc_periph_t periph`  
*Peripheral name.*
- `bool lock`  
*Lock the permission until reset.*
- `bool enableSema`  
*Enable semaphore or not, when enabled, master should call [RDC\\_SEMA42\\_Lock](#) to lock the semaphore gate accordingly before access the peripheral.*
- `uint16_t policy`  
*Access policy.*

**Field Documentation**

- (1) `rdc_periph_t _rdc_periph_access_config::periph`
- (2) `bool _rdc_periph_access_config::lock`
- (3) `bool _rdc_periph_access_config::enableSema`
- (4) `uint16_t _rdc_periph_access_config::policy`

**21.2.4 struct \_rdc\_mem\_access\_config**

Note that when setting the `rdc_mem_access_config_t::baseAddress` and `rdc_mem_access_config_t::endAddress`, should be aligned to the region resolution, see `rdc_mem_t` definitions.

**Data Fields**

- `rdc_mem_t mem`  
*Memory region descriptor name.*
- `bool lock`  
*Lock the configuration.*
- `uint64_t baseAddress`  
*Start address of the memory region.*
- `uint64_t endAddress`  
*End address of the memory region.*
- `uint16_t policy`

*Access policy.*

#### Field Documentation

- (1) `rdc_mem_t_rdc_mem_access_config::mem`
- (2) `bool _rdc_mem_access_config::lock`
- (3) `uint64_t _rdc_mem_access_config::baseAddress`
- (4) `uint64_t _rdc_mem_access_config::endAddress`
- (5) `uint16_t _rdc_mem_access_config::policy`

### 21.2.5 struct \_rdc\_mem\_status

#### Data Fields

- `bool hasViolation`  
*Violating happens or not.*
- `uint8_t domainID`  
*Violating Domain ID.*
- `uint64_t address`  
*Violating Address.*

#### Field Documentation

- (1) `bool _rdc_mem_status::hasViolation`
- (2) `uint8_t _rdc_mem_status::domainID`
- (3) `uint64_t _rdc_mem_status::address`

### 21.3 Typedef Documentation

#### 21.3.1 typedef struct \_rdc\_mem\_access\_config rdc\_mem\_access\_config\_t

Note that when setting the `rdc_mem_access_config_t::baseAddress` and `rdc_mem_access_config_t::endAddress`, should be aligned to the region resolution, see `rdc_mem_t` definitions.

### 21.4 Enumeration Type Documentation

#### 21.4.1 enum \_rdc\_interrupts

Enumerator

**kRDC\_RestoreCompleteInterrupt** Interrupt generated when the RDC has completed restoring state to a recently re-powered memory regions.

## 21.4.2 enum \_rdc\_flags

Enumerator

*kRDC\_PowerDownDomainOn* Power down domain is ON.

## 21.4.3 enum \_rdc\_access\_policy

Enumerator

*kRDC\_NoAccess* Could not read or write.

*kRDC\_WriteOnly* Write only.

*kRDC\_ReadOnly* Read only.

*kRDC\_ReadWrite* Read and write.

## 21.5 Function Documentation

### 21.5.1 void RDC\_Init ( RDC\_Type \* *base* )

This function enables the RDC clock.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | RDC peripheral base address. |
|-------------|------------------------------|

### 21.5.2 void RDC\_Deinit ( RDC\_Type \* *base* )

This function disables the RDC clock.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | RDC peripheral base address. |
|-------------|------------------------------|

### 21.5.3 void RDC\_GetHardwareConfig ( RDC\_Type \* *base*, rdc\_hardware\_config\_t \* *config* )

This function gets the RDC hardware configurations, including number of bus masters, number of domains, number of memory regions and number of peripherals.

Parameters

|               |                                                    |
|---------------|----------------------------------------------------|
| <i>base</i>   | RDC peripheral base address.                       |
| <i>config</i> | Pointer to the structure to get the configuration. |

**21.5.4 static void RDC\_EnableInterrupts ( RDC\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

|             |                                                                                   |
|-------------|-----------------------------------------------------------------------------------|
| <i>base</i> | RDC peripheral base address.                                                      |
| <i>mask</i> | Interrupts to enable, it is OR'ed value of enum <a href="#">_rdc_interrupts</a> . |

**21.5.5 static void RDC\_DisableInterrupts ( RDC\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

|             |                                                                                    |
|-------------|------------------------------------------------------------------------------------|
| <i>base</i> | RDC peripheral base address.                                                       |
| <i>mask</i> | Interrupts to disable, it is OR'ed value of enum <a href="#">_rdc_interrupts</a> . |

**21.5.6 static uint32\_t RDC\_GetInterruptStatus ( RDC\_Type \* *base* ) [inline],  
[static]**

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | RDC peripheral base address. |
|-------------|------------------------------|

Returns

Interrupts pending status, it is OR'ed value of enum [\\_rdc\\_interrupts](#).

**21.5.7 static void RDC\_ClearInterruptStatus ( RDC\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

Parameters

|             |                                                                              |
|-------------|------------------------------------------------------------------------------|
| <i>base</i> | RDC peripheral base address.                                                 |
| <i>mask</i> | Status to clear, it is OR'ed value of enum <a href="#">_rdc_interrupts</a> . |

### 21.5.8 static uint32\_t RDC\_GetStatus ( RDC\_Type \* *base* ) [inline], [static]

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | RDC peripheral base address. |
|-------------|------------------------------|

Returns

mask RDC status, it is OR'ed value of enum [\\_rdc\\_flags](#).

### 21.5.9 static void RDC\_ClearStatus ( RDC\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                                                             |
|-------------|-----------------------------------------------------------------------------|
| <i>base</i> | RDC peripheral base address.                                                |
| <i>mask</i> | RDC status to clear, it is OR'ed value of enum <a href="#">_rdc_flags</a> . |

### 21.5.10 void RDC\_SetMasterDomainAssignment ( RDC\_Type \* *base*, rdc\_master\_t *master*, const rdc\_domain\_assignment\_t \* *domainAssignment* )

Parameters

|                         |                              |
|-------------------------|------------------------------|
| <i>base</i>             | RDC peripheral base address. |
| <i>master</i>           | Which master to set.         |
| <i>domainAssignment</i> | Pointer to the assignment.   |

### 21.5.11 void RDC\_GetDefaultMasterDomainAssignment ( rdc\_domain\_assignment\_t \* *domainAssignment* )

The default configuration is:

```
assignment->domainId = 0U;
assignment->lock = 0U;
```

Parameters

|                         |                            |
|-------------------------|----------------------------|
| <i>domainAssignment</i> | Pointer to the assignment. |
|-------------------------|----------------------------|

### 21.5.12 static void RDC\_LockMasterDomainAssignment ( RDC\_Type \* *base*, rdc\_master\_t *master* ) [inline], [static]

Once locked, it could not be unlocked until next reset.

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | RDC peripheral base address. |
| <i>master</i> | Which master to lock.        |

### 21.5.13 void RDC\_SetPeriphAccessConfig ( RDC\_Type \* *base*, const rdc\_periph\_access\_config\_t \* *config* )

Parameters

|               |                                      |
|---------------|--------------------------------------|
| <i>base</i>   | RDC peripheral base address.         |
| <i>config</i> | Pointer to the policy configuration. |

### 21.5.14 void RDC\_GetDefaultPeriphAccessConfig ( rdc\_periph\_access\_config\_t \* *config* )

The default configuration is:

```
config->lock = false;
config->enableSema = false;
config->policy = RDC_ACCESS_POLICY(0, kRDC_ReadWrite) |
 RDC_ACCESS_POLICY(1, kRDC_ReadWrite) |
 RDC_ACCESS_POLICY(2, kRDC_ReadWrite) |
 RDC_ACCESS_POLICY(3, kRDC_ReadWrite);
```

Parameters

|               |                                      |
|---------------|--------------------------------------|
| <i>config</i> | Pointer to the policy configuration. |
|---------------|--------------------------------------|

### 21.5.15 static void RDC\_LockPeriphAccessConfig ( **RDC\_Type** \* *base*, **rdc\_periph\_t** *periph* ) [inline], [static]

Once locked, it could not be unlocked until reset.

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | RDC peripheral base address. |
| <i>periph</i> | Which peripheral to lock.    |

### 21.5.16 static uint8\_t RDC\_GetPeriphAccessPolicy ( **RDC\_Type** \* *base*, **rdc\_periph\_t** *periph*, **uint8\_t** *domainId* ) [inline], [static]

Parameters

|                 |                              |
|-----------------|------------------------------|
| <i>base</i>     | RDC peripheral base address. |
| <i>periph</i>   | Which peripheral to get.     |
| <i>domainId</i> | Get policy for which domain. |

Returns

Access policy, see [\\_rdc\\_access\\_policy](#).

### 21.5.17 void RDC\_SetMemAccessConfig ( **RDC\_Type** \* *base*, **const rdc\_mem\_access\_config\_t** \* *config* )

Note that when setting the `baseAddress` and `endAddress` in `config`, should be aligned to the region resolution, see `rdc_mem_t` definitions.

Parameters

|               |                                      |
|---------------|--------------------------------------|
| <i>base</i>   | RDC peripheral base address.         |
| <i>config</i> | Pointer to the policy configuration. |

### 21.5.18 void RDC\_GetDefaultMemAccessConfig ( rdc\_mem\_access\_config\_t \* *config* )

The default configuration is:

```
config->lock = false;
config->baseAddress = 0;
config->endAddress = 0;
config->policy = RDC_ACCESS_POLICY(0, kRDC_ReadWrite) |
 RDC_ACCESS_POLICY(1, kRDC_ReadWrite) |
 RDC_ACCESS_POLICY(2, kRDC_ReadWrite) |
 RDC_ACCESS_POLICY(3, kRDC_ReadWrite);
```

Parameters

|               |                                      |
|---------------|--------------------------------------|
| <i>config</i> | Pointer to the policy configuration. |
|---------------|--------------------------------------|

### 21.5.19 static void RDC\_LockMemAccessConfig ( RDC\_Type \* *base*, rdc\_mem\_t *mem* ) [inline], [static]

Once locked, it could not be unlocked until reset. After locked, you can only call [RDC\\_SetMemAccessValid](#) to enable the configuration, but can not disable it or change other settings.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | RDC peripheral base address. |
| <i>mem</i>  | Which memory region to lock. |

### 21.5.20 static void RDC\_SetMemAccessValid ( RDC\_Type \* *base*, rdc\_mem\_t *mem*, bool *valid* ) [inline], [static]

Parameters

|              |                                          |
|--------------|------------------------------------------|
| <i>base</i>  | RDC peripheral base address.             |
| <i>mem</i>   | Which memory region to operate.          |
| <i>valid</i> | Pass in true to valid, false to invalid. |

### 21.5.21 void RDC\_GetMemViolationStatus ( RDC\_Type \* *base*, rdc\_mem\_t *mem*, rdc\_mem\_status\_t \* *status* )

The first access violation is captured. Subsequent violations are ignored until the status register is cleared. Contents are cleared upon reading the register. Clearing of contents occurs only when the status is read by the memory region's associated domain ID(s).

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | RDC peripheral base address. |
| <i>mem</i>    | Which memory region to get.  |
| <i>status</i> | The returned status.         |

### 21.5.22 static void RDC\_ClearMemViolationFlag ( RDC\_Type \* *base*, rdc\_mem\_t *mem* ) [inline], [static]

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | RDC peripheral base address.  |
| <i>mem</i>  | Which memory region to clear. |

### 21.5.23 static uint8\_t RDC\_GetMemAccessPolicy ( RDC\_Type \* *base*, rdc\_mem\_t *mem*, uint8\_t *domainId* ) [inline], [static]

Parameters

|                 |                              |
|-----------------|------------------------------|
| <i>base</i>     | RDC peripheral base address. |
| <i>mem</i>      | Which memory region to get.  |
| <i>domainId</i> | Get policy for which domain. |

Returns

Access policy, see [\\_rdc\\_access\\_policy](#).

### 21.5.24 static uint8\_t RDC\_GetCurrentMasterDomainId ( RDC\_Type \* *base* ) [inline], [static]

This function returns the domain ID of the current bus master.

### Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | RDC peripheral base address. |
|-------------|------------------------------|

### Returns

Domain ID of current bus master.

# Chapter 22

## RDC\_SEMA42: Hardware Semaphores Driver

### 22.1 Overview

The MCUXpresso SDK provides a driver for the RDC\_SEMA42 module of MCUXpresso SDK devices.

The RDC\_SEMA42 driver should be used together with RDC driver.

Before using the RDC\_SEMA42, call the [RDC\\_SEMA42\\_Init\(\)](#) function to initialize the module. Note that this function only enables the clock but does not reset the gates because the module might be used by other processors at the same time. To reset the gates, call either the [RDC\\_SEMA42\\_ResetGate\(\)](#) or [RDC\\_SEMA42\\_ResetAllGates\(\)](#) functions. The function [RDC\\_SEMA42\\_Deinit\(\)](#) deinitializes the RD-C\_SEMA42.

The RDC\_SEMA42 provides two functions to lock the RDC\_SEMA42 gate. The function [RDC\\_SEMA42\\_TryLock\(\)](#) tries to lock the gate. If the gate has been locked by another processor, this function returns an error immediately. The function [RDC\\_SEMA42\\_Lock\(\)](#) is a blocking method, which waits until the gate is free and locks it.

The [RDC\\_SEMA42\\_Unlock\(\)](#) unlocks the RDC\_SEMA42 gate. The gate can only be unlocked by the processor which locked it. If the gate is not locked by the current processor, this function takes no effect. The function [RDC\\_SEMA42\\_GetGateStatus\(\)](#) returns a status whether the gate is unlocked and which processor locks the gate. The function [RDC\\_SEMA42\\_GetLockDomainID\(\)](#) returns the ID of the domain which has locked the gate.

The RDC\_SEMA42 gate can be reset to unlock forcefully. The function [RDC\\_SEMA42\\_ResetGate\(\)](#) resets a specific gate. The function [RDC\\_SEMA42\\_ResetAllGates\(\)](#) resets all gates.

### Macros

- #define [RDC\\_SEMA42\\_GATE\\_NUM\\_RESET\\_ALL](#) (64U)  
*The number to reset all RDC\_SEMA42 gates.*
- #define [RDC\\_SEMA42\\_GATEn](#)(base, n) (((volatile uint8\_t \*)(&((base)->GATE0)))[(n)])  
*RDC\_SEMA42 gate n register address.*
- #define [RDC\\_SEMA42\\_GATE\\_COUNT](#) (64U)  
*RDC\_SEMA42 gate count.*

### Functions

- void [RDC\\_SEMA42\\_Init](#) (RDC\_SEMAPHORE\_Type \*base)  
*Initializes the RDC\_SEMA42 module.*
- void [RDC\\_SEMA42\\_Deinit](#) (RDC\_SEMAPHORE\_Type \*base)  
*De-initializes the RDC\_SEMA42 module.*
- status\_t [RDC\\_SEMA42\\_TryLock](#) (RDC\_SEMAPHORE\_Type \*base, uint8\_t gateNum, uint8\_t masterIndex, uint8\_t domainId)  
*Tries to lock the RDC\_SEMA42 gate.*

- void [RDC\\_SEMA42\\_Lock](#) (RDC\_SEMAPHORE\_Type \*base, uint8\_t gateNum, uint8\_t masterIndex, uint8\_t domainId)  
*Locks the RDC\_SEMA42 gate.*
- static void [RDC\\_SEMA42\\_Unlock](#) (RDC\_SEMAPHORE\_Type \*base, uint8\_t gateNum)  
*Unlocks the RDC\_SEMA42 gate.*
- static int32\_t [RDC\\_SEMA42\\_GetLockMasterIndex](#) (RDC\_SEMAPHORE\_Type \*base, uint8\_t gateNum)  
*Gets which master has currently locked the gate.*
- int32\_t [RDC\\_SEMA42\\_GetLockDomainID](#) (RDC\_SEMAPHORE\_Type \*base, uint8\_t gateNum)  
*Gets which domain has currently locked the gate.*
- status\_t [RDC\\_SEMA42\\_ResetGate](#) (RDC\_SEMAPHORE\_Type \*base, uint8\_t gateNum)  
*Resets the RDC\_SEMA42 gate to an unlocked status.*
- static status\_t [RDC\\_SEMA42\\_ResetAllGates](#) (RDC\_SEMAPHORE\_Type \*base)  
*Resets all RDC\_SEMA42 gates to an unlocked status.*

## Driver version

- #define [FSL\\_RDC\\_SEMA42\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 0, 4))  
*RDC\_SEMA42 driver version.*

## 22.2 Macro Definition Documentation

### 22.2.1 #define RDC\_SEMA42\_GATE\_NUM\_RESET\_ALL (64U)

### 22.2.2 #define RDC\_SEMA42\_GATEn( *base*, *n* ) (((volatile uint8\_t \*)(&(*base*)->GATE0))[(*n*)])

### 22.2.3 #define RDC\_SEMA42\_GATE\_COUNT (64U)

## 22.3 Function Documentation

### 22.3.1 void RDC\_SEMA42\_Init ( RDC\_SEMAPHORE\_Type \* *base* )

This function initializes the RDC\_SEMA42 module. It only enables the clock but does not reset the gates because the module might be used by other processors at the same time. To reset the gates, call either RDC\_SEMA42\_ResetGate or RDC\_SEMA42\_ResetAllGates function.

Parameters

|             |                                     |
|-------------|-------------------------------------|
| <i>base</i> | RDC_SEMA42 peripheral base address. |
|-------------|-------------------------------------|

### 22.3.2 void RDC\_SEMA42\_Deinit ( RDC\_SEMAPHORE\_Type \* *base* )

This function de-initializes the RDC\_SEMA42 module. It only disables the clock.

Parameters

|             |                                     |
|-------------|-------------------------------------|
| <i>base</i> | RDC_SEMA42 peripheral base address. |
|-------------|-------------------------------------|

### 22.3.3 **status\_t RDC\_SEMA42\_TryLock ( RDC\_SEMAPHORE\_Type \* *base*, uint8\_t *gateNum*, uint8\_t *masterIndex*, uint8\_t *domainId* )**

This function tries to lock the specific RDC\_SEMA42 gate. If the gate has been locked by another processor, this function returns an error code.

Parameters

|                    |                                     |
|--------------------|-------------------------------------|
| <i>base</i>        | RDC_SEMA42 peripheral base address. |
| <i>gateNum</i>     | Gate number to lock.                |
| <i>masterIndex</i> | Current processor master index.     |
| <i>domainId</i>    | Current processor domain ID.        |

Return values

|                        |                                                   |
|------------------------|---------------------------------------------------|
| <i>kStatus_Success</i> | Lock the sema42 gate successfully.                |
| <i>kStatus_Failed</i>  | Sema42 gate has been locked by another processor. |

### 22.3.4 **void RDC\_SEMA42\_Lock ( RDC\_SEMAPHORE\_Type \* *base*, uint8\_t *gateNum*, uint8\_t *masterIndex*, uint8\_t *domainId* )**

This function locks the specific RDC\_SEMA42 gate. If the gate has been locked by other processors, this function waits until it is unlocked and then lock it.

Parameters

|                    |                                     |
|--------------------|-------------------------------------|
| <i>base</i>        | RDC_SEMA42 peripheral base address. |
| <i>gateNum</i>     | Gate number to lock.                |
| <i>masterIndex</i> | Current processor master index.     |
| <i>domainId</i>    | Current processor domain ID.        |

### 22.3.5 static void RDC\_SEMA42\_Unlock( RDC\_SEMAPHORE\_Type \* *base*, uint8\_t *gateNum* ) [inline], [static]

This function unlocks the specific RDC\_SEMA42 gate. It only writes unlock value to the RDC\_SEMA42 gate register. However, it does not check whether the RDC\_SEMA42 gate is locked by the current processor or not. As a result, if the RDC\_SEMA42 gate is not locked by the current processor, this function has no effect.

Parameters

|                |                                     |
|----------------|-------------------------------------|
| <i>base</i>    | RDC_SEMA42 peripheral base address. |
| <i>gateNum</i> | Gate number to unlock.              |

### 22.3.6 static int32\_t RDC\_SEMA42\_GetLockMasterIndex( RDC\_SEMAPHORE\_Type \* *base*, uint8\_t *gateNum* ) [inline], [static]

Parameters

|                |                                     |
|----------------|-------------------------------------|
| <i>base</i>    | RDC_SEMA42 peripheral base address. |
| <i>gateNum</i> | Gate number.                        |

Returns

Return -1 if the gate is not locked by any master, otherwise return the master index.

### 22.3.7 int32\_t RDC\_SEMA42\_GetLockDomainID( RDC\_SEMAPHORE\_Type \* *base*, uint8\_t *gateNum* )

Parameters

|                |                                     |
|----------------|-------------------------------------|
| <i>base</i>    | RDC_SEMA42 peripheral base address. |
| <i>gateNum</i> | Gate number.                        |

Returns

Return -1 if the gate is not locked by any domain, otherwise return the domain ID.

### 22.3.8 status\_t RDC\_SEMA42\_ResetGate ( RDC\_SEMAPHORE\_Type \* *base*,                   uint8\_t *gateNum* )

This function resets a RDC\_SEMA42 gate to an unlocked status.

Parameters

|                |                                     |
|----------------|-------------------------------------|
| <i>base</i>    | RDC_SEMA42 peripheral base address. |
| <i>gateNum</i> | Gate number.                        |

Return values

|                        |                                        |
|------------------------|----------------------------------------|
| <i>kStatus_Success</i> | RDC_SEMA42 gate is reset successfully. |
| <i>kStatus_Failed</i>  | Some other reset process is ongoing.   |

### 22.3.9 static status\_t RDC\_SEMA42\_ResetAllGates ( RDC\_SEMAPHORE\_Type \* *base* ) [inline], [static]

This function resets all RDC\_SEMA42 gate to an unlocked status.

Parameters

|             |                                     |
|-------------|-------------------------------------|
| <i>base</i> | RDC_SEMA42 peripheral base address. |
|-------------|-------------------------------------|

Return values

|                                    |                                      |
|------------------------------------|--------------------------------------|
| <i>kStatus_Success</i>             | RDC_SEMA42 is reset successfully.    |
| <i>kStatus_RDC_SEMA42_Reseting</i> | Some other reset process is ongoing. |

# Chapter 23

## SAI: Serial Audio Interface

### 23.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Serial Audio Interface (SAI) module of MCUXpresso SDK devices.

SAI driver includes functional APIs and transactional APIs.

Functional APIs target low-level APIs. Functional APIs can be used for SAI initialization, configuration and operation, and for optimization and customization purposes. Using the functional API requires the knowledge of the SAI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. SAI functional operation groups provide the functional API set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. All transactional APIs use the `sai_handle_t` as the first parameter. Initialize the handle by calling the [SAI\\_TransferTxCreateHandle\(\)](#) or [SAI\\_TransferRxCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions [SAI\\_TransferSendNonBlocking\(\)](#) and [SAI\\_TransferReceiveNonBlocking\(\)](#) set up the interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_SAI_TxIdle` and `kStatus_SAI_RxIdle` status.

### 23.2 Typical configurations

#### Bit width configuration

SAI driver support 8/16/24/32bits stereo/mono raw audio data transfer. SAI EDMA driver support 8/16/32bits stereo/mono raw audio data transfer, since the EDMA doesn't support 24bit data width, so application should pre-convert the 24bit data to 32bit. SAI DMA driver support 8/16/32bits stereo/mono raw audio data transfer, since the EDMA doesn't support 24bit data width, so application should pre-convert the 24bit data to 32bit. SAI SDMA driver support 8/16/24/32bits stereo/mono raw audio data transfer.

#### Frame configuration

SAI driver support I2S, DSP, Left justified, Right justified, TDM mode. Application can call the api directly: `SAI_GetClassicI2SConfig` `SAI_GetLeftJustifiedConfig` `SAI_GetRightJustifiedConfig` `SAI_GetTDMConfig` `SAI_GetDSPConfig`

### 23.3 Typical use case

#### 23.3.1 SAI Send/receive using an interrupt method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/sai

#### 23.3.2 SAI Send/receive using a DMA method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/sai

### Modules

- [SAI Driver](#)
- [SAI SDMA Driver](#)

### 23.4 *Typical use case*

## 23.5 SAI Driver

### 23.5.1 Overview

#### Data Structures

- struct `_sai_config`  
`SAI user configuration structure.` [More...](#)
- struct `_sai_transfer_format`  
`sai transfer format` [More...](#)
- struct `_sai_master_clock`  
`master clock configurations` [More...](#)
- struct `_sai_fifo`  
`sai fifo configurations` [More...](#)
- struct `_sai_bit_clock`  
`sai bit clock configurations` [More...](#)
- struct `_sai_frame_sync`  
`sai frame sync configurations` [More...](#)
- struct `_sai_serial_data`  
`sai serial data configurations` [More...](#)
- struct `_sai_transceiver`  
`sai transceiver configurations` [More...](#)
- struct `_sai_transfer`  
`SAI transfer structure.` [More...](#)
- struct `_sai_handle`  
`SAI handle structure.` [More...](#)

#### Macros

- #define `SAI_XFER_QUEUE_SIZE` (4U)  
`SAI transfer queue size, user can refine it according to use case.`
- #define `FSL_SAI_HAS_FIFO_EXTEND_FEATURE` 1  
`sai fifo feature`

#### Typedefs

- typedef enum `_sai_protocol` `sai_protocol_t`  
`Define the SAI bus type.`
- typedef enum `_sai_master_slave` `sai_master_slave_t`  
`Master or slave mode.`
- typedef enum `_sai_mono_stereo` `sai_mono_stereo_t`  
`Mono or stereo audio format.`
- typedef enum `_sai_data_order` `sai_data_order_t`  
`SAI data order, MSB or LSB.`
- typedef enum `_sai_clock_polarity` `sai_clock_polarity_t`  
`SAI clock polarity, active high or low.`
- typedef enum `_sai_sync_mode` `sai_sync_mode_t`  
`Synchronous or asynchronous mode.`

- `typedef enum _sai_bclk_source sai_bclk_source_t`  
*Bit clock source.*
- `typedef enum _sai_reset_type sai_reset_type_t`  
*The reset type.*
- `typedef enum _sai_fifo_packing sai_fifo_packing_t`  
*The SAI packing mode The mode includes 8 bit and 16 bit packing.*
- `typedef struct _sai_config sai_config_t`  
*SAI user configuration structure.*
- `typedef enum _sai_sample_rate sai_sample_rate_t`  
*Audio sample rate.*
- `typedef enum _sai_word_width sai_word_width_t`  
*Audio word width.*
- `typedef enum _sai_data_pin_state sai_data_pin_state_t`  
*sai data pin state definition*
- `typedef enum _sai_fifo_combine sai_fifo_combine_t`  
*sai fifo combine mode definition*
- `typedef enum _sai_transceiver_type sai_transceiver_type_t`  
*sai transceiver type*
- `typedef enum _sai_frame_sync_len sai_frame_sync_len_t`  
*sai frame sync len*
- `typedef struct _sai_transfer_format sai_transfer_format_t`  
*sai transfer format*
- `typedef struct _sai_master_clock sai_master_clock_t`  
*master clock configurations*
- `typedef struct _sai_fifo sai_fifo_t`  
*sai fifo configurations*
- `typedef struct _sai_bit_clock sai_bit_clock_t`  
*sai bit clock configurations*
- `typedef struct _sai_frame_sync sai_frame_sync_t`  
*sai frame sync configurations*
- `typedef struct _sai_serial_data sai_serial_data_t`  
*sai serial data configurations*
- `typedef struct _sai_transceiver sai_transceiver_t`  
*sai transceiver configurations*
- `typedef struct _sai_transfer sai_transfer_t`  
*SAI transfer structure.*
- `typedef void(* sai_transfer_callback_t )(I2S_Type *base, sai_handle_t *handle, status_t status, void *userData)`  
*SAI transfer callback prototype.*

## Enumerations

- `enum {`
- `kStatus_SAI_TxBusy = MAKE_STATUS(kStatusGroup_SAI, 0),`
- `kStatus_SAI_RxBusy = MAKE_STATUS(kStatusGroup_SAI, 1),`
- `kStatus_SAI_TxError = MAKE_STATUS(kStatusGroup_SAI, 2),`
- `kStatus_SAI_RxError = MAKE_STATUS(kStatusGroup_SAI, 3),`
- `kStatus_SAI_QueueFull = MAKE_STATUS(kStatusGroup_SAI, 4),`
- `kStatus_SAI_TxIdle = MAKE_STATUS(kStatusGroup_SAI, 5),`

- ```

kStatus_SAI_RxIdle = MAKE_STATUS(kStatusGroup_SAI, 6) }

    _sai_status_t, SAI return status.

• enum {
    kSAI_Channel0Mask = 1 << 0U,
    kSAI_Channel1Mask = 1 << 1U,
    kSAI_Channel2Mask = 1 << 2U,
    kSAI_Channel3Mask = 1 << 3U,
    kSAI_Channel4Mask = 1 << 4U,
    kSAI_Channel5Mask = 1 << 5U,
    kSAI_Channel6Mask = 1 << 6U,
    kSAI_Channel7Mask = 1 << 7U }

    _sai_channel_mask,.sai channel mask value, actual channel numbers is depend soc specific

• enum _sai_protocol {
    kSAI_BusLeftJustified = 0x0U,
    kSAI_BusRightJustified,
    kSAI_BusI2S,
    kSAI_BusPCMA,
    kSAI_BusPCMB }

    Define the SAI bus type.

• enum _sai_master_slave {
    kSAI_Master = 0x0U,
    kSAI_Slave = 0x1U,
    kSAI_Bclk_Master_FrameSync_Slave = 0x2U,
    kSAI_Bclk_Slave_FrameSync_Master = 0x3U }

    Master or slave mode.

• enum _sai_mono_stereo {
    kSAI_Stereo = 0x0U,
    kSAI_MonoRight,
    kSAI_MonoLeft }

    Mono or stereo audio format.

• enum _sai_data_order {
    kSAI_DataLSB = 0x0U,
    kSAI_DataMSB }

    SAI data order, MSB or LSB.

• enum _sai_clock_polarity {
    kSAI_PolarityActiveHigh = 0x0U,
    kSAI_PolarityActiveLow = 0x1U,
    kSAI_SampleOnFallingEdge = 0x0U,
    kSAI_SampleOnRisingEdge = 0x1U }

    SAI clock polarity, active high or low.

• enum _sai_sync_mode {
    kSAI_ModeAsync = 0x0U,
    kSAI_ModeSync }

    Synchronous or asynchronous mode.

• enum _sai_bclk_source {

```

```
kSAI_BclkSourceBusclk = 0x0U,
kSAI_BclkSourceMclkOption1 = 0x1U,
kSAI_BclkSourceMclkOption2 = 0x2U,
kSAI_BclkSourceMclkOption3 = 0x3U,
kSAI_BclkSourceMclkDiv = 0x1U,
kSAI_BclkSourceOtherSai0 = 0x2U,
kSAI_BclkSourceOtherSai1 = 0x3U }
```

Bit clock source.

- enum {

kSAI_WordStartInterruptEnable,
 kSAI_SyncErrorInterruptEnable = I2S_TCSR_SEIE_MASK,
 kSAI_FIFOWarningInterruptEnable = I2S_TCSR_FWIE_MASK,
 kSAI_FIFOErrorInterruptEnable = I2S_TCSR_FEIE_MASK,
 kSAI_FIFORequestInterruptEnable = I2S_TCSR_FRIE_MASK }

_sai_interrupt_enable_t, The SAI interrupt enable flag
- enum {

kSAI_FIFOWarningDMAEnable = I2S_TCSR_FWDE_MASK,
 kSAI_FIFORequestDMAEnable = I2S_TCSR_FRDE_MASK }

_sai_dma_enable_t, The DMA request sources
- enum {

kSAI_WordStartFlag = I2S_TCSR_WSF_MASK,
 kSAI_SyncErrorFlag = I2S_TCSR_SEF_MASK,
 kSAI_FIFOErrorFlag = I2S_TCSR_FEF_MASK,
 kSAI_FIFORequestFlag = I2S_TCSR_FRF_MASK,
 kSAI_FIFOWarningFlag = I2S_TCSR_FWF_MASK }

_sai_flags, The SAI status flag
- enum *_sai_reset_type* {

kSAI_ResetTypeSoftware = I2S_TCSR_SR_MASK,
 kSAI_ResetTypeFIFO = I2S_TCSR_FR_MASK,
 kSAI_ResetAll = I2S_TCSR_SR_MASK | I2S_TCSR_FR_MASK }

The reset type.
- enum *_sai_fifo_packing* {

kSAI_FifoPackingDisabled = 0x0U,
 kSAI_FifoPacking8bit = 0x2U,
 kSAI_FifoPacking16bit = 0x3U }

The SAI packing mode The mode includes 8 bit and 16 bit packing.
- enum *_sai_sample_rate* {

```

kSAI_SampleRate8KHz = 8000U,
kSAI_SampleRate11025Hz = 11025U,
kSAI_SampleRate12KHz = 12000U,
kSAI_SampleRate16KHz = 16000U,
kSAI_SampleRate22050Hz = 22050U,
kSAI_SampleRate24KHz = 24000U,
kSAI_SampleRate32KHz = 32000U,
kSAI_SampleRate44100Hz = 44100U,
kSAI_SampleRate48KHz = 48000U,
kSAI_SampleRate96KHz = 96000U,
kSAI_SampleRate192KHz = 192000U,
kSAI_SampleRate384KHz = 384000U }

```

Audio sample rate.

- enum `_sai_word_width` {

kSAI_WordWidth8bits = 8U,

kSAI_WordWidth16bits = 16U,

kSAI_WordWidth24bits = 24U,

kSAI_WordWidth32bits = 32U }

Audio word width.

- enum `_sai_data_pin_state` {

kSAI_DataPinStateTriState,

kSAI_DataPinStateOutputZero = 1U }
- sai data pin state definition*
- enum `_sai_fifo_combine` {

kSAI_FifoCombineDisabled = 0U,

kSAI_FifoCombineModeEnabledOnRead,

kSAI_FifoCombineModeEnabledOnWrite,

kSAI_FifoCombineModeEnabledReadWrite }
- sai fifo combine mode definition*

- enum `_sai_transceiver_type` {

kSAI_Transmitter = 0U,

kSAI_Receiver = 1U }
- sai transceiver type*
- enum `_sai_frame_sync_len` {

kSAI_FrameSyncLenOneBitClk = 0U,

kSAI_FrameSyncLenPerWordWidth = 1U }
- sai frame sync len*

Driver version

- #define `FSL_SAI_DRIVER_VERSION` (`MAKE_VERSION(2, 4, 2)`)
- Version 2.4.2.*

Initialization and deinitialization

- void **SAI_Init** (I2S_Type *base)
Initializes the SAI peripheral.
- void **SAI_Deinit** (I2S_Type *base)
De-initializes the SAI peripheral.
- void **SAI_TxReset** (I2S_Type *base)
Resets the SAI Tx.
- void **SAI_RxReset** (I2S_Type *base)
Resets the SAI Rx.
- void **SAI_TxEnable** (I2S_Type *base, bool enable)
Enables/disables the SAI Tx.
- void **SAI_RxEnable** (I2S_Type *base, bool enable)
Enables/disables the SAI Rx.
- static void **SAI_TxSetBitClockDirection** (I2S_Type *base, **sai_master_slave_t** masterSlave)
Set Rx bit clock direction.
- static void **SAI_RxSetBitClockDirection** (I2S_Type *base, **sai_master_slave_t** masterSlave)
Set Rx bit clock direction.
- static void **SAI_RxSetFrameSyncDirection** (I2S_Type *base, **sai_master_slave_t** masterSlave)
Set Rx frame sync direction.
- static void **SAI_TxSetFrameSyncDirection** (I2S_Type *base, **sai_master_slave_t** masterSlave)
Set Tx frame sync direction.
- void **SAI_TxSetBitClockRate** (I2S_Type *base, uint32_t sourceClockHz, uint32_t sampleRate, uint32_t bitWidth, uint32_t channelNumbers)
Transmitter bit clock rate configurations.
- void **SAI_RxSetBitClockRate** (I2S_Type *base, uint32_t sourceClockHz, uint32_t sampleRate, uint32_t bitWidth, uint32_t channelNumbers)
Receiver bit clock rate configurations.
- void **SAI_TxSetBitclockConfig** (I2S_Type *base, **sai_master_slave_t** masterSlave, **sai_bit_clock_t** *config)
Transmitter Bit clock configurations.
- void **SAI_RxSetBitclockConfig** (I2S_Type *base, **sai_master_slave_t** masterSlave, **sai_bit_clock_t** *config)
Receiver Bit clock configurations.
- void **SAI_SetMasterClockConfig** (I2S_Type *base, **sai_master_clock_t** *config)
Master clock configurations.
- void **SAI_TxSetFifoConfig** (I2S_Type *base, **sai_fifo_t** *config)
SAI transmitter fifo configurations.
- void **SAI_RxSetFifoConfig** (I2S_Type *base, **sai_fifo_t** *config)
SAI receiver fifo configurations.
- void **SAI_TxSetFrameSyncConfig** (I2S_Type *base, **sai_master_slave_t** masterSlave, **sai_frame_sync_t** *config)
SAI transmitter Frame sync configurations.
- void **SAI_RxSetFrameSyncConfig** (I2S_Type *base, **sai_master_slave_t** masterSlave, **sai_frame_sync_t** *config)
SAI receiver Frame sync configurations.
- void **SAI_TxSetSerialDataConfig** (I2S_Type *base, **sai_serial_data_t** *config)
SAI transmitter Serial data configurations.
- void **SAI_RxSetSerialDataConfig** (I2S_Type *base, **sai_serial_data_t** *config)
SAI receiver Serial data configurations.

- void **SAI_TxSetConfig** (I2S_Type *base, **sai_transceiver_t** *config)
SAI transmitter configurations.
- void **SAI_RxSetConfig** (I2S_Type *base, **sai_transceiver_t** *config)
SAI receiver configurations.
- void **SAI_GetClassicI2SConfig** (**sai_transceiver_t** *config, **sai_word_width_t** bitWidth, **sai_mono_stereo_t** mode, uint32_t saiChannelMask)
Get classic I2S mode configurations.
- void **SAI_GetLeftJustifiedConfig** (**sai_transceiver_t** *config, **sai_word_width_t** bitWidth, **sai_mono_stereo_t** mode, uint32_t saiChannelMask)
Get left justified mode configurations.
- void **SAI_GetRightJustifiedConfig** (**sai_transceiver_t** *config, **sai_word_width_t** bitWidth, **sai_mono_stereo_t** mode, uint32_t saiChannelMask)
Get right justified mode configurations.
- void **SAI_GetTDMConfig** (**sai_transceiver_t** *config, **sai_frame_sync_len_t** frameSyncWidth, **sai_word_width_t** bitWidth, uint32_t dataWordNum, uint32_t saiChannelMask)
Get TDM mode configurations.
- void **SAI_GetDSPConfig** (**sai_transceiver_t** *config, **sai_frame_sync_len_t** frameSyncWidth, **sai_word_width_t** bitWidth, **sai_mono_stereo_t** mode, uint32_t saiChannelMask)
Get DSP mode configurations.

Status

- static uint32_t **SAI_TxGetStatusFlag** (I2S_Type *base)
Gets the SAI Tx status flag state.
- static void **SAI_TxClearStatusFlags** (I2S_Type *base, uint32_t mask)
Clears the SAI Tx status flag state.
- static uint32_t **SAI_RxGetStatusFlag** (I2S_Type *base)
Gets the SAI Rx status flag state.
- static void **SAI_RxClearStatusFlags** (I2S_Type *base, uint32_t mask)
Clears the SAI Rx status flag state.
- void **SAI_TxSoftwareReset** (I2S_Type *base, **sai_reset_type_t** resetType)
Do software reset or FIFO reset .
- void **SAI_RxSoftwareReset** (I2S_Type *base, **sai_reset_type_t** resetType)
Do software reset or FIFO reset .
- void **SAI_TxSetChannelFIFOMask** (I2S_Type *base, uint8_t mask)
Set the Tx channel FIFO enable mask.
- void **SAI_RxSetChannelFIFOMask** (I2S_Type *base, uint8_t mask)
Set the Rx channel FIFO enable mask.
- void **SAI_TxSetDataOrder** (I2S_Type *base, **sai_data_order_t** order)
Set the Tx data order.
- void **SAI_RxSetDataOrder** (I2S_Type *base, **sai_data_order_t** order)
Set the Rx data order.
- void **SAI_TxSetBitClockPolarity** (I2S_Type *base, **sai_clock_polarity_t** polarity)
Set the Tx data order.
- void **SAI_RxSetBitClockPolarity** (I2S_Type *base, **sai_clock_polarity_t** polarity)
Set the Rx data order.
- void **SAI_TxSetFrameSyncPolarity** (I2S_Type *base, **sai_clock_polarity_t** polarity)
Set the Tx data order.
- void **SAI_RxSetFrameSyncPolarity** (I2S_Type *base, **sai_clock_polarity_t** polarity)

Set the Rx data order.

- void [SAI_TxSetFIFOPacking](#) (I2S_Type *base, sai_fifo_packing_t pack)
Set Tx FIFO packing feature.
- void [SAI_RxSetFIFOPacking](#) (I2S_Type *base, sai_fifo_packing_t pack)
Set Rx FIFO packing feature.
- static void [SAI_TxSetFIFOErrorContinue](#) (I2S_Type *base, bool isEnabled)
Set Tx FIFO error continue.
- static void [SAI_RxSetFIFOErrorContinue](#) (I2S_Type *base, bool isEnabled)
Set Rx FIFO error continue.

Interrupts

- static void [SAI_TxEnableInterrupts](#) (I2S_Type *base, uint32_t mask)
Enables the SAI Tx interrupt requests.
- static void [SAI_RxEnableInterrupts](#) (I2S_Type *base, uint32_t mask)
Enables the SAI Rx interrupt requests.
- static void [SAI_TxDisableInterrupts](#) (I2S_Type *base, uint32_t mask)
Disables the SAI Tx interrupt requests.
- static void [SAI_RxDisableInterrupts](#) (I2S_Type *base, uint32_t mask)
Disables the SAI Rx interrupt requests.

DMA Control

- static void [SAI_TxEnableDMA](#) (I2S_Type *base, uint32_t mask, bool enable)
Enables/disables the SAI Tx DMA requests.
- static void [SAI_RxEnableDMA](#) (I2S_Type *base, uint32_t mask, bool enable)
Enables/disables the SAI Rx DMA requests.
- static uintptr_t [SAI_TxGetDataRegisterAddress](#) (I2S_Type *base, uint32_t channel)
Gets the SAI Tx data register address.
- static uintptr_t [SAI_RxGetDataRegisterAddress](#) (I2S_Type *base, uint32_t channel)
Gets the SAI Rx data register address.

Bus Operations

- void [SAI_WriteBlocking](#) (I2S_Type *base, uint32_t channel, uint32_t bitWidth, uint8_t *buffer, uint32_t size)
Sends data using a blocking method.
- void [SAI_WriteMultiChannelBlocking](#) (I2S_Type *base, uint32_t channel, uint32_t channelMask, uint32_t bitWidth, uint8_t *buffer, uint32_t size)
Sends data to multi channel using a blocking method.
- static void [SAI_WriteData](#) (I2S_Type *base, uint32_t channel, uint32_t data)
Writes data into SAI FIFO.
- void [SAI_ReadBlocking](#) (I2S_Type *base, uint32_t channel, uint32_t bitWidth, uint8_t *buffer, uint32_t size)
Receives data using a blocking method.
- void [SAI_ReadMultiChannelBlocking](#) (I2S_Type *base, uint32_t channel, uint32_t channelMask, uint32_t bitWidth, uint8_t *buffer, uint32_t size)

- Receives multi channel data using a blocking method.
- static uint32_t **SAI_ReadData** (I2S_Type *base, uint32_t channel)
Reads data from the SAI FIFO.

Transactional

- void **SAI_TransferTxCreateHandle** (I2S_Type *base, sai_handle_t *handle, sai_transfer_callback_t callback, void *userData)
Initializes the SAI Tx handle.
- void **SAI_TransferRxCreateHandle** (I2S_Type *base, sai_handle_t *handle, sai_transfer_callback_t callback, void *userData)
Initializes the SAI Rx handle.
- void **SAI_TransferTxSetConfig** (I2S_Type *base, sai_handle_t *handle, sai_transceiver_t *config)
SAI transmitter transfer configurations.
- void **SAI_TransferRxSetConfig** (I2S_Type *base, sai_handle_t *handle, sai_transceiver_t *config)
SAI receiver transfer configurations.
- status_t **SAI_TransferSendNonBlocking** (I2S_Type *base, sai_handle_t *handle, sai_transfer_t *xfer)
Performs an interrupt non-blocking send transfer on SAI.
- status_t **SAI_TransferReceiveNonBlocking** (I2S_Type *base, sai_handle_t *handle, sai_transfer_t *xfer)
Performs an interrupt non-blocking receive transfer on SAI.
- status_t **SAI_TransferGetSendCount** (I2S_Type *base, sai_handle_t *handle, size_t *count)
Gets a set byte count.
- status_t **SAI_TransferGetReceiveCount** (I2S_Type *base, sai_handle_t *handle, size_t *count)
Gets a received byte count.
- void **SAI_TransferAbortSend** (I2S_Type *base, sai_handle_t *handle)
Aborts the current send.
- void **SAI_TransferAbortReceive** (I2S_Type *base, sai_handle_t *handle)
Aborts the current IRQ receive.
- void **SAI_TransferTerminateSend** (I2S_Type *base, sai_handle_t *handle)
Terminate all SAI send.
- void **SAI_TransferTerminateReceive** (I2S_Type *base, sai_handle_t *handle)
Terminate all SAI receive.
- void **SAI_TransferTxHandleIRQ** (I2S_Type *base, sai_handle_t *handle)
Tx interrupt handler.
- void **SAI_TransferRxHandleIRQ** (I2S_Type *base, sai_handle_t *handle)
Rx interrupt handler.

23.5.2 Data Structure Documentation

23.5.2.1 struct _sai_config

Data Fields

- sai_protocol_t protocol
Audio bus protocol in SAI.

- **sai_sync_mode_t syncMode**
SAI sync mode, control Tx/Rx clock sync.
- **bool mclkOutputEnable**
Master clock output enable, true means master clock divider enabled.
- **sai_bclk_source_t bclkSource**
Bit Clock source.
- **sai_master_slave_t masterSlave**
Master or slave.

23.5.2.2 struct _sai_transfer_format

Data Fields

- **uint32_t sampleRate_Hz**
Sample rate of audio data.
- **uint32_t bitWidth**
Data length of audio data, usually 8/16/24/32 bits.
- **sai_mono_stereo_t stereo**
Mono or stereo.
- **uint8_t watermark**
Watermark value.
- **uint8_t channel**
Transfer start channel.
- **uint8_t channelMask**
enabled channel mask value, reference _sai_channel_mask
- **uint8_t endChannel**
end channel number
- **uint8_t channelNums**
Total enabled channel numbers.
- **sai_protocol_t protocol**
Which audio protocol used.
- **bool isFrameSyncCompact**
True means Frame sync length is configurable according to bitWidth, false means frame sync length is 64 times of bit clock.

Field Documentation

(1) **bool _sai_transfer_format::isFrameSyncCompact**

23.5.2.3 struct _sai_master_clock

Data Fields

- **bool mclkOutputEnable**
master clock output enable
- **uint32_t mclkHz**
target mclk frequency
- **uint32_t mclkSourceClkHz**
mclk source frequency

23.5.2.4 struct _sai_fifo

Data Fields

- bool `fifoContinueOneError`
fifo continues when error occur
- `sai_fifo_combine_t fifoCombine`
fifo combine mode
- `sai_fifo_packing_t fifoPacking`
fifo packing mode
- uint8_t `fifoWatermark`
fifo watermark

23.5.2.5 struct _sai_bit_clock

Data Fields

- bool `bclkSrcSwap`
bit clock source swap
- bool `bclkInputDelay`
bit clock actually used by the transmitter is delayed by the pad output delay, this has effect of decreasing the data input setup time, but increasing the data output valid time .
- `sai_clock_polarity_t bclkPolarity`
bit clock polarity
- `sai_bclk_source_t bclkSource`
bit Clock source

Field Documentation

(1) `bool _sai_bit_clock::bclkInputDelay`

23.5.2.6 struct _sai_frame_sync

Data Fields

- uint8_t `frameSyncWidth`
frame sync width in number of bit clocks
- bool `frameSyncEarly`
TRUE is frame sync assert one bit before the first bit of frame FALSE is frame sync assert with the first bit of the frame.
- bool `frameSyncGenerateOnDemand`
internal frame sync is generated when FIFO waring flag is clear
- `sai_clock_polarity_t frameSyncPolarity`
frame sync polarity

23.5.2.7 struct _sai_serial_data

Data Fields

- **sai_data_pin_state_t dataMode**
sai data pin state when slots masked or channel disabled
- **sai_data_order_t dataOrder**
configure whether the LSB or MSB is transmitted first
- **uint8_t dataWord0Length**
configure the number of bits in the first word in each frame
- **uint8_t dataWordNLength**
configure the number of bits in the each word in each frame, except the first word
- **uint8_t dataWordLength**
used to record the data length for dma transfer
- **uint8_t dataFirstBitShifted**
Configure the bit index for the first bit transmitted for each word in the frame.
- **uint8_t dataWordNum**
configure the number of words in each frame
- **uint32_t dataMaskedWord**
configure whether the transmit word is masked

23.5.2.8 struct _sai_transceiver

Data Fields

- **sai_serial_data_t serialData**
serial data configurations
- **sai_frame_sync_t frameSync**
ws configurations
- **sai_bit_clock_t bitClock**
bit clock configurations
- **sai_fifo_t fifo**
fifo configurations
- **sai_master_slave_t masterSlave**
transceiver is master or slave
- **sai_sync_mode_t syncMode**
transceiver sync mode
- **uint8_t startChannel**
Transfer start channel.
- **uint8_t channelMask**
enabled channel mask value, reference _sai_channel_mask
- **uint8_t endChannel**
end channel number
- **uint8_t channelNums**
Total enabled channel numbers.

23.5.2.9 struct _sai_transfer

Data Fields

- `uint8_t * data`
Data start address to transfer.
- `size_t dataSize`
Transfer size.

Field Documentation

- (1) `uint8_t* _sai_transfer::data`
- (2) `size_t _sai_transfer::dataSize`

23.5.2.10 struct _sai_handle

Data Fields

- `I2S_Type * base`
base address
- `uint32_t state`
Transfer status.
- `sai_transfer_callback_t callback`
Callback function called at transfer event.
- `void * userData`
Callback parameter passed to callback function.
- `uint8_t bitWidth`
Bit width for transfer, 8/16/24/32 bits.
- `uint8_t channel`
Transfer start channel.
- `uint8_t channelMask`
enabled channel mask value, refernece _sai_channel_mask
- `uint8_t endChannel`
end channel number
- `uint8_t channelNums`
Total enabled channel numbers.
- `sai_transfer_t saiQueue [SAI_XFER_QUEUE_SIZE]`
Transfer queue storing queued transfer.
- `size_t transferSize [SAI_XFER_QUEUE_SIZE]`
Data bytes need to transfer.
- `volatile uint8_t queueUser`
Index for user to queue transfer.
- `volatile uint8_t queueDriver`
Index for driver to get the transfer data and size.
- `uint8_t watermark`
Watermark value.

23.5.3 Macro Definition Documentation

23.5.3.1 #define SAI_XFER_QUEUE_SIZE (4U)

23.5.4 Enumeration Type Documentation

23.5.4.1 anonymous enum

Enumerator

kStatus_SAI_TxBusy SAI Tx is busy.
kStatus_SAI_RxBusy SAI Rx is busy.
kStatus_SAI_TxError SAI Tx FIFO error.
kStatus_SAI_RxError SAI Rx FIFO error.
kStatus_SAI_QueueFull SAI transfer queue is full.
kStatus_SAI_TxIdle SAI Tx is idle.
kStatus_SAI_RxIdle SAI Rx is idle.

23.5.4.2 anonymous enum

Enumerator

kSAI_Channel0Mask channel 0 mask value
kSAI_Channel1Mask channel 1 mask value
kSAI_Channel2Mask channel 2 mask value
kSAI_Channel3Mask channel 3 mask value
kSAI_Channel4Mask channel 4 mask value
kSAI_Channel5Mask channel 5 mask value
kSAI_Channel6Mask channel 6 mask value
kSAI_Channel7Mask channel 7 mask value

23.5.4.3 enum _sai_protocol

Enumerator

kSAI_BusLeftJustified Uses left justified format.
kSAI_BusRightJustified Uses right justified format.
kSAI_BusI2S Uses I2S format.
kSAI_BusPCMA Uses I2S PCM A format.
kSAI_BusPCMB Uses I2S PCM B format.

23.5.4.4 enum _sai_master_slave

Enumerator

kSAI_Master Master mode include bclk and frame sync.

kSAI_Slave Slave mode include bclk and frame sync.

kSAI_Bclk_Master_FrameSync_Slave bclk in master mode, frame sync in slave mode

kSAI_Bclk_Slave_FrameSync_Master bclk in slave mode, frame sync in master mode

23.5.4.5 enum _sai_mono_stereo

Enumerator

kSAI_Stereo Stereo sound.

kSAI_MonoRight Only Right channel have sound.

kSAI_MonoLeft Only left channel have sound.

23.5.4.6 enum _sai_data_order

Enumerator

kSAI_DataLSB LSB bit transferred first.

kSAI_DataMSB MSB bit transferred first.

23.5.4.7 enum _sai_clock_polarity

Enumerator

kSAI_PolarityActiveHigh Drive outputs on rising edge.

kSAI_PolarityActiveLow Drive outputs on falling edge.

kSAI_SampleOnFallingEdge Sample inputs on falling edge.

kSAI_SampleOnRisingEdge Sample inputs on rising edge.

23.5.4.8 enum _sai_sync_mode

Enumerator

kSAI_ModeAsync Asynchronous mode.

kSAI_ModeSync Synchronous mode (with receiver or transmit)

23.5.4.9 enum _sai_bclk_source

Enumerator

- kSAI_BclkSourceBusclk* Bit clock using bus clock.
- kSAI_BclkSourceMclkOption1* Bit clock MCLK option 1.
- kSAI_BclkSourceMclkOption2* Bit clock MCLK option2.
- kSAI_BclkSourceMclkOption3* Bit clock MCLK option3.
- kSAI_BclkSourceMclkDiv* Bit clock using master clock divider.
- kSAI_BclkSourceOtherSai0* Bit clock from other SAI device.
- kSAI_BclkSourceOtherSai1* Bit clock from other SAI device.

23.5.4.10 anonymous enum

Enumerator

- kSAI_WordStartInterruptEnable* Word start flag, means the first word in a frame detected.
- kSAI_SyncErrorInterruptEnable* Sync error flag, means the sync error is detected.
- kSAI_FIFOWarningInterruptEnable* FIFO warning flag, means the FIFO is empty.
- kSAI_FIFOErrorInterruptEnable* FIFO error flag.
- kSAI_FIFORequestInterruptEnable* FIFO request, means reached watermark.

23.5.4.11 anonymous enum

Enumerator

- kSAI_FIFOWarningDMAEnable* FIFO warning caused by the DMA request.
- kSAI_FIFORequestDMAEnable* FIFO request caused by the DMA request.

23.5.4.12 anonymous enum

Enumerator

- kSAI_WordStartFlag* Word start flag, means the first word in a frame detected.
- kSAI_SyncErrorFlag* Sync error flag, means the sync error is detected.
- kSAI_FIFOErrorFlag* FIFO error flag.
- kSAI_FIFORequestFlag* FIFO request flag.
- kSAI_FIFOWarningFlag* FIFO warning flag.

23.5.4.13 enum _sai_reset_type

Enumerator

- kSAI_ResetTypeSoftware* Software reset, reset the logic state.
- kSAI_ResetTypeFIFO* FIFO reset, reset the FIFO read and write pointer.

kSAI_ResetAll All reset.

23.5.4.14 enum _sai_fifo_packing

Enumerator

kSAI_FifoPackingDisabled Packing disabled.

kSAI_FifoPacking8bit 8 bit packing enabled

kSAI_FifoPacking16bit 16bit packing enabled

23.5.4.15 enum _sai_sample_rate

Enumerator

kSAI_SampleRate8KHz Sample rate 8000 Hz.

kSAI_SampleRate11025Hz Sample rate 11025 Hz.

kSAI_SampleRate12KHz Sample rate 12000 Hz.

kSAI_SampleRate16KHz Sample rate 16000 Hz.

kSAI_SampleRate22050Hz Sample rate 22050 Hz.

kSAI_SampleRate24KHz Sample rate 24000 Hz.

kSAI_SampleRate32KHz Sample rate 32000 Hz.

kSAI_SampleRate44100Hz Sample rate 44100 Hz.

kSAI_SampleRate48KHz Sample rate 48000 Hz.

kSAI_SampleRate96KHz Sample rate 96000 Hz.

kSAI_SampleRate192KHz Sample rate 192000 Hz.

kSAI_SampleRate384KHz Sample rate 384000 Hz.

23.5.4.16 enum _sai_word_width

Enumerator

kSAI_WordWidth8bits Audio data width 8 bits.

kSAI_WordWidth16bits Audio data width 16 bits.

kSAI_WordWidth24bits Audio data width 24 bits.

kSAI_WordWidth32bits Audio data width 32 bits.

23.5.4.17 enum _sai_data_pin_state

Enumerator

kSAI_DataPinStateTriState transmit data pins are tri-stated when slots are masked or channels are disabled

kSAI_DataPinStateOutputZero transmit data pins are never tri-stated and will output zero when slots are masked or channel disabled

23.5.4.18 enum _sai_fifo_combine

Enumerator

kSAI_FifoCombineDisabled sai fifo combine mode disabled
kSAI_FifoCombineModeEnabledOnRead sai fifo combine mode enabled on FIFO reads
kSAI_FifoCombineModeEnabledOnWrite sai fifo combine mode enabled on FIFO write
kSAI_FifoCombineModeEnabledOnReadWrite sai fifo combined mode enabled on FIFO read/writes

23.5.4.19 enum _sai_transceiver_type

Enumerator

kSAI_Transmitter sai transmitter
kSAI_Receiver sai receiver

23.5.4.20 enum _sai_frame_sync_len

Enumerator

kSAI_FrameSyncLenOneBitClk 1 bit clock frame sync len for DSP mode
kSAI_FrameSyncLenPerWordWidth Frame sync length decided by word width.

23.5.5 Function Documentation

23.5.5.1 void SAI_Init (I2S_Type * *base*)

This API gates the SAI clock. The SAI module can't operate unless SAI_Init is called to enable the clock.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

23.5.5.2 void SAI_Deinit (I2S_Type * *base*)

This API gates the SAI clock. The SAI module can't operate unless SAI_TxInit or SAI_RxInit is called to enable the clock.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

23.5.5.3 void SAI_TxReset (I2S_Type * *base*)

This function enables the software reset and FIFO reset of SAI Tx. After reset, clear the reset bit.

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

23.5.5.4 void SAI_RxReset (I2S_Type * *base*)

This function enables the software reset and FIFO reset of SAI Rx. After reset, clear the reset bit.

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

23.5.5.5 void SAI_TxEnable (I2S_Type * *base*, bool *enable*)

Parameters

<i>base</i>	SAI base pointer.
<i>enable</i>	True means enable SAI Tx, false means disable.

23.5.5.6 void SAI_RxEnable (I2S_Type * *base*, bool *enable*)

Parameters

<i>base</i>	SAI base pointer.
<i>enable</i>	True means enable SAI Rx, false means disable.

23.5.5.7 static void SAI_TxSetBitClockDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select bit clock direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

23.5.5.8 static void SAI_RxSetBitClockDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select bit clock direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

23.5.5.9 static void SAI_RxSetFrameSyncDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select frame sync direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

23.5.5.10 static void SAI_TxSetFrameSyncDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select frame sync direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

23.5.5.11 void SAI_TxSetBitClockRate (I2S_Type * *base*, uint32_t *sourceClockHz*, uint32_t *sampleRate*, uint32_t *bitWidth*, uint32_t *channelNumbers*)

Parameters

<i>base</i>	SAI base pointer.
<i>sourceClockHz</i>	Bit clock source frequency.
<i>sampleRate</i>	Audio data sample rate.
<i>bitWidth</i>	Audio data bitWidth.
<i>channel-Numbers</i>	Audio channel numbers.

23.5.5.12 void SAI_RxSetBitClockRate (I2S_Type * *base*, uint32_t *sourceClockHz*, uint32_t *sampleRate*, uint32_t *bitWidth*, uint32_t *channelNumbers*)

Parameters

<i>base</i>	SAI base pointer.
<i>sourceClockHz</i>	Bit clock source frequency.
<i>sampleRate</i>	Audio data sample rate.
<i>bitWidth</i>	Audio data bitWidth.
<i>channel-Numbers</i>	Audio channel numbers.

23.5.5.13 void SAI_TxSetBitclockConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_bit_clock_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	bit clock other configurations, can be NULL in slave mode.

23.5.5.14 void SAI_RxSetBitclockConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_bit_clock_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	bit clock other configurations, can be NULL in slave mode.

23.5.5.15 void SAI_SetMasterClockConfig (I2S_Type * *base*, sai_master_clock_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	master clock configurations.

23.5.5.16 void SAI_TxSetFifoConfig (I2S_Type * *base*, sai_fifo_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	fifo configurations.

23.5.5.17 void SAI_RxSetFifoConfig (I2S_Type * *base*, sai_fifo_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	fifo configurations.

23.5.5.18 void SAI_TxSetFrameSyncConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_frame_sync_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	frame sync configurations, can be NULL in slave mode.

23.5.5.19 void SAI_RxSetFrameSyncConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_frame_sync_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	frame sync configurations, can be NULL in slave mode.

23.5.5.20 void SAI_TxSetSerialDataConfig (I2S_Type * *base*, sai_serial_data_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	serial data configurations.

23.5.5.21 void SAI_RxSetSerialDataConfig (I2S_Type * *base*, sai_serial_data_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	serial data configurations.

23.5.5.22 void SAI_TxSetConfig (I2S_Type * *base*, sai_transceiver_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	transmitter configurations.

23.5.5.23 void SAI_RxSetConfig (I2S_Type * *base*, sai_transceiver_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	receiver configurations.

23.5.5.24 void SAI_GetClassicI2SConfig (sai_transceiver_t * *config*, sai_word_width_t *bitWidth*, sai_mono_stereo_t *mode*, uint32_t *saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel- Mask</i>	mask value of the channel to be enable.

23.5.5.25 void SAI_GetLeftJustifiedConfig (sai_transceiver_t * *config*, sai_word_width_t *bitWidth*, sai_mono_stereo_t *mode*, uint32_t *saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel- Mask</i>	mask value of the channel to be enable.

23.5.5.26 void SAI_GetRightJustifiedConfig (sai_transceiver_t * *config*, sai_word_width_t *bitWidth*, sai_mono_stereo_t *mode*, uint32_t *saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

23.5.5.27 void SAI_GetTDMConfig (sai_transceiver_t * *config*, sai_frame_sync_len_t *frameSyncWidth*, sai_word_width_t *bitWidth*, uint32_t *dataWordNum*, uint32_t *saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>frameSync-Width</i>	length of frame sync.
<i>bitWidth</i>	audio data word width.
<i>dataWordNum</i>	word number in one frame.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

23.5.5.28 void SAI_GetDSPConfig (sai_transceiver_t * *config*, sai_frame_sync_len_t *frameSyncWidth*, sai_word_width_t *bitWidth*, sai_mono_stereo_t *mode*, uint32_t *saiChannelMask*)

Note

DSP mode is also called PCM mode which support MODE A and MODE B, DSP/PCM MODE A configuration flow. RX is similiar but uses SAI_RxSetConfig instead of SAI_TxSetConfig:

```
* SAI_GetDSPConfig(config, kSAI_FrameSyncLenOneBitClk, bitWidth,
    kSAI_Stereo, channelMask)
* config->frameSync.frameSyncEarly      = true;
* SAI_TxSetConfig(base, config)
*
```

DSP/PCM MODE B configuration flow for TX. RX is similiar but uses SAI_RxSetConfig instead of SAI_TxSetConfig:

```
* SAI_GetDSPConfig(config, kSAI_FrameSyncLenOneBitClk, bitWidth,
    kSAI_Stereo, channelMask)
* SAI_TxSetConfig(base, config)
*
```

Parameters

<i>config</i>	transceiver configurations.
<i>frameSyncWidth</i>	length of frame sync.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannelMask</i>	mask value of the channel to enable.

23.5.5.29 static uint32_t SAI_TxGetStatusFlag (I2S_Type * *base*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

Returns

SAI Tx status flag value. Use the Status Mask to get the status value needed.

23.5.5.30 static void SAI_TxClearStatusFlags (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	State mask. It can be a combination of the following source if defined: <ul style="list-style-type: none"> • kSAI_WordStartFlag • kSAI_SyncErrorFlag • kSAI_FIFOErrorFlag

23.5.5.31 static uint32_t SAI_RxGetStatusFlag (I2S_Type * *base*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

Returns

SAI Rx status flag value. Use the Status Mask to get the status value needed.

23.5.5.32 static void SAI_RxClearStatusFlags (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>State mask. It can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_WordStartFlag • kSAI_SyncErrorFlag • kSAI_FIFOErrorFlag

23.5.5.33 void SAI_TxSoftwareReset (I2S_Type * *base*, sai_reset_type_t *resetType*)

FIFO reset means clear all the data in the FIFO, and make the FIFO pointer both to 0. Software reset means clear the Tx internal logic, including the bit clock, frame count etc. But software reset will not clear any configuration registers like TCR1~TCR5. This function will also clear all the error flags such as FIFO error, sync error etc.

Parameters

<i>base</i>	SAI base pointer
<i>resetType</i>	Reset type, FIFO reset or software reset

23.5.5.34 void SAI_RxSoftwareReset (I2S_Type * *base*, sai_reset_type_t *resetType*)

FIFO reset means clear all the data in the FIFO, and make the FIFO pointer both to 0. Software reset means clear the Rx internal logic, including the bit clock, frame count etc. But software reset will not clear any configuration registers like RCR1~RCR5. This function will also clear all the error flags such as FIFO error, sync error etc.

Parameters

<i>base</i>	SAI base pointer
<i>resetType</i>	Reset type, FIFO reset or software reset

23.5.5.35 void SAI_TxSetChannelFIFOMask (I2S_Type * *base*, uint8_t *mask*)

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	Channel enable mask, 0 means all channel FIFO disabled, 1 means channel 0 enabled, 3 means both channel 0 and channel 1 enabled.

23.5.5.36 void SAI_RxSetChannelFIFOMask (I2S_Type * *base*, uint8_t *mask*)

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	Channel enable mask, 0 means all channel FIFO disabled, 1 means channel 0 enabled, 3 means both channel 0 and channel 1 enabled.

23.5.5.37 void SAI_TxSetDataOrder (I2S_Type * *base*, sai_data_order_t *order*)

Parameters

<i>base</i>	SAI base pointer
<i>order</i>	Data order MSB or LSB

23.5.5.38 void SAI_RxSetDataOrder (I2S_Type * *base*, sai_data_order_t *order*)

Parameters

<i>base</i>	SAI base pointer
<i>order</i>	Data order MSB or LSB

```
23.5.5.39 void SAI_TxSetBitClockPolarity ( I2S_Type * base, sai_clock_polarity_t polarity )
```

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

23.5.5.40 void SAI_RxSetBitClockPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

23.5.5.41 void SAI_TxSetFrameSyncPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

23.5.5.42 void SAI_RxSetFrameSyncPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

23.5.5.43 void SAI_TxSetFIFOPacking (I2S_Type * *base*, sai_fifo_packing_t *pack*)

Parameters

<i>base</i>	SAI base pointer.
<i>pack</i>	FIFO pack type. It is element of sai_fifo_packing_t.

23.5.5.44 void SAI_RxSetFIFOPacking (I2S_Type * *base*, sai_fifo_packing_t *pack*)

Parameters

<i>base</i>	SAI base pointer.
<i>pack</i>	FIFO pack type. It is element of sai_fifo_packing_t.

23.5.5.45 static void SAI_TxSetFIFOErrorContinue (I2S_Type * *base*, bool *isEnabled*) [inline], [static]

FIFO error continue mode means SAI will keep running while FIFO error occurred. If this feature not enabled, SAI will hang and users need to clear FEF flag in TCSR register.

Parameters

<i>base</i>	SAI base pointer.
<i>isEnabled</i>	Is FIFO error continue enabled, true means enable, false means disable.

23.5.5.46 static void SAI_RxSetFIFOErrorContinue (I2S_Type * *base*, bool *isEnabled*) [inline], [static]

FIFO error continue mode means SAI will keep running while FIFO error occurred. If this feature not enabled, SAI will hang and users need to clear FEF flag in RCSR register.

Parameters

<i>base</i>	SAI base pointer.
<i>isEnabled</i>	Is FIFO error continue enabled, true means enable, false means disable.

23.5.5.47 static void SAI_TxEnableInterrupts (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	interrupt source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

**23.5.5.48 static void SAI_RxEnableInterrupts (I2S_Type * *base*, uint32_t *mask*)
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

**23.5.5.49 static void SAI_TxDisableInterrupts (I2S_Type * *base*, uint32_t *mask*)
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

**23.5.5.50 static void SAI_RxDisableInterrupts (I2S_Type * *base*, uint32_t *mask*)
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

23.5.5.51 static void SAI_TxEnableDMA (I2S_Type * *base*, uint32_t *mask*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>DMA source The parameter can be combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_FIFOWarningDMAEnable • kSAI_FIFORequestDMAEnable
<i>enable</i>	True means enable DMA, false means disable DMA.

23.5.5.52 static void SAI_RxEnableDMA (I2S_Type * *base*, uint32_t *mask*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>DMA source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_FIFOWarningDMAEnable • kSAI_FIFORequestDMAEnable

<i>enable</i>	True means enable DMA, false means disable DMA.
---------------	---

23.5.5.53 static uintptr_t SAI_TxGetDataRegisterAddress (I2S_Type * *base*, uint32_t *channel*) [inline], [static]

This API is used to provide a transfer address for the SAI DMA transfer configuration.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Which data channel used.

Returns

data register address.

23.5.5.54 static uintptr_t SAI_RxGetDataRegisterAddress (I2S_Type * *base*, uint32_t *channel*) [inline], [static]

This API is used to provide a transfer address for the SAI DMA transfer configuration.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Which data channel used.

Returns

data register address.

23.5.5.55 void SAI_WriteBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

23.5.5.56 void SAI_WriteMultiChannelBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *channelMask*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>channelMask</i>	channel mask.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

23.5.5.57 static void SAI_WriteData (I2S_Type * *base*, uint32_t *channel*, uint32_t *data*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>data</i>	Data needs to be written.

23.5.5.58 void SAI_ReadBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

23.5.5.59 void SAI_ReadMultiChannelBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *channelMask*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>channelMask</i>	channel mask.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

23.5.5.60 static uint32_t SAI_ReadData (I2S_Type * *base*, uint32_t *channel*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

<i>channel</i>	Data channel used.
----------------	--------------------

Returns

Data in SAI FIFO.

23.5.5.61 void SAI_TransferTxCreateHandle (*I2S_Type * base*, *sai_handle_t * handle*, *sai_transfer_callback_t callback*, *void * userData*)

This function initializes the Tx handle for the SAI Tx transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function

23.5.5.62 void SAI_TransferRxCreateHandle (*I2S_Type * base*, *sai_handle_t * handle*, *sai_transfer_callback_t callback*, *void * userData*)

This function initializes the Rx handle for the SAI Rx transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function.

23.5.5.63 void SAI_TransferTxSetConfig (*I2S_Type * base*, *sai_handle_t * handle*, *sai_transceiver_t * config*)

This function initializes the Tx, include bit clock, frame sync, master clock, serial data and fifo configurations.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>config</i>	transmitter configurations.

23.5.5.64 void SAI_TransferRxSetConfig (I2S_Type * *base*, sai_handle_t * *handle*, sai_transceiver_t * *config*)

This function initializes the Rx, include bit clock, frame sync, master clock, serial data and fifo configurations.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>config</i>	receiver configurations.

23.5.5.65 status_t SAI_TransferSendNonBlocking (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_t * *xfer*)

Note

This API returns immediately after the transfer initiates. Call the SAI_TxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not kStatus_SAI_Busy, the transfer is finished.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>xfer</i>	Pointer to the sai_transfer_t structure.

Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_SAI_TxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

23.5.5.66 status_t SAI_TransferReceiveNonBlocking (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_t * *xfer*)

Note

This API returns immediately after the transfer initiates. Call the SAI_RxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not kStatus_SAI_Busy, the transfer is finished.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>xfer</i>	Pointer to the sai_transfer_t structure.

Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_SAI_RxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

23.5.5.67 status_t SAI_TransferGetSendCount (I2S_Type * *base*, sai_handle_t * *handle*, size_t * *count*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>count</i>	Bytes count sent.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

23.5.5.68 status_t SAI_TransferGetReceiveCount (I2S_Type * *base*, sai_handle_t * *handle*, size_t * *count*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>count</i>	Bytes count received.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

23.5.5.69 void SAI_TransferAbortSend (I2S_Type * *base*, sai_handle_t * *handle*)

Note

This API can be called any time when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.

23.5.5.70 void SAI_TransferAbortReceive (I2S_Type * *base*, sai_handle_t * *handle*)

Note

This API can be called when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.

23.5.5.71 void SAI_TransferTerminateSend (I2S_Type * *base*, sai_handle_t * *handle*)

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI_TransferAbortSend.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

23.5.5.72 void SAI_TransferTerminateReceive (I2S_Type * *base*, sai_handle_t * *handle*)

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI_TransferAbortReceive.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

23.5.5.73 void SAI_TransferTxHandleIRQ (I2S_Type * *base*, sai_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure.

23.5.5.74 void SAI_TransferRxHandleIRQ (I2S_Type * *base*, sai_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure.

23.6 SAI SDMA Driver

23.6.1 Typical use case

23.6.2 Overview

Multi fifo transfer use sai sdma driver

The SDMA multi fifo script support transfer data between multi peripheral fifos and memory, a typical user case is that receiving multi sai channel data and put it into memory as

| channel 0 | channel 1 | channel 2 | channel 3 | channel 4 | |

Multi fifo script is target to implement above feature, it can supports 1.configurable fifo watermark range from 1~(2^12-1), it is a value of fifo_watermark * channel_numbers 2.configurable fifo numbers, support up to 15 continuous fifos 3.configurable fifo address offset, support address offset up to 64

```
/* load sdma script */
SDMA_LoadScript()
/* sai multi channel configurations */
SAI_GetClassicI2SConfig(&config, DEMO_AUDIO_BIT_WIDTH, kSAI_Stereo,
    kSAI_Channel0Mask | kSAI_Channel1Mask |
    kSAI_Channel2Mask| kSAI_Channel3Mask | kSAI_Channel4Mask);
SAI_TransferRxSetConfigSDMA(SAI, handle, &config);
SAI_TransferReceiveSDMA(SAI, handle, &config);
```

Transmitting data using multi fifo is same as above.

Data Structures

- struct `_sai_sdma_handle`
SAI DMA transfer handle, users should not touch the content of the handle. [More...](#)

Typedefs

- `typedef void(* sai_sdma_callback_t)(I2S_Type *base, sai_sdma_handle_t *handle, status_t status, void *userData)`
SAI SDMA transfer callback function for finish and error.

Driver version

- `#define FSL_SAI_SDMA_DRIVER_VERSION (MAKE_VERSION(2, 6, 0))`
Version 2.6.0.

SDMA Transactional

- void **SAI_TransferTxCreateHandleSDMA** (I2S_Type *base, sai_sdma_handle_t *handle, sai_sdma_callback_t callback, void *userData, sdma_handle_t *dmaHandle, uint32_t eventSource)
Initializes the SAI SDMA handle.
- void **SAI_TransferRxCreateHandleSDMA** (I2S_Type *base, sai_sdma_handle_t *handle, sai_sdma_callback_t callback, void *userData, sdma_handle_t *dmaHandle, uint32_t eventSource)
Initializes the SAI Rx SDMA handle.
- status_t **SAI_TransferSendSDMA** (I2S_Type *base, sai_sdma_handle_t *handle, sai_transfer_t *xfer)
Performs a non-blocking SAI transfer using DMA.
- status_t **SAI_TransferReceiveSDMA** (I2S_Type *base, sai_sdma_handle_t *handle, sai_transfer_t *xfer)
Performs a non-blocking SAI receive using SDMA.
- void **SAI_TransferAbortSendSDMA** (I2S_Type *base, sai_sdma_handle_t *handle)
Aborts a SAI transfer using SDMA.
- void **SAI_TransferAbortReceiveSDMA** (I2S_Type *base, sai_sdma_handle_t *handle)
Aborts a SAI receive using SDMA.
- void **SAI_TransferTerminateReceiveSDMA** (I2S_Type *base, sai_sdma_handle_t *handle)
Terminate all the SAI sdma receive transfer.
- void **SAI_TransferTerminateSendSDMA** (I2S_Type *base, sai_sdma_handle_t *handle)
Terminate all the SAI sdma send transfer.
- void **SAI_TransferRxSetConfigSDMA** (I2S_Type *base, sai_sdma_handle_t *handle, sai_transceiver_t *saiConfig)
brief Configures the SAI RX.
- void **SAI_TransferTxSetConfigSDMA** (I2S_Type *base, sai_sdma_handle_t *handle, sai_transceiver_t *saiConfig)
brief Configures the SAI Tx.

23.6.3 Data Structure Documentation

23.6.3.1 struct _sai_sdma_handle

Data Fields

- **sdma_handle_t * dmaHandle**
DMA handler for SAI send.
- **uint8_t bytesPerFrame**
Bytes in a frame.
- **uint8_t channel**
start data channel
- **uint8_t channelNums**
total transfer channel numbers, used for multifo
- **uint8_t channelMask**
enabled channel mask value, refernece _sai_channel_mask
- **uint8_t fifoOffset**
fifo address offset between multifo
- **uint32_t count**

- *The transfer data count in a DMA request.*
- `uint32_t state`
Internal state for SAI SDMA transfer.
- `uint32_t eventSource`
SAI event source number.
- `sai_sdma_callback_t callback`
Callback for users while transfer finish or error occurs.
- `void *userData`
User callback parameter.
- `sdma_buffer_descriptor_t bdPool [SAI_XFER_QUEUE_SIZE]`
BD pool for SDMA transfer.
- `sai_transfer_t saiQueue [SAI_XFER_QUEUE_SIZE]`
Transfer queue storing queued transfer.
- `size_t transferSize [SAI_XFER_QUEUE_SIZE]`
Data bytes need to transfer.
- `volatile uint8_t queueUser`
Index for user to queue transfer.
- `volatile uint8_t queueDriver`
Index for driver to get the transfer data and size.

Field Documentation

- (1) `sdma_buffer_descriptor_t _sai_sdma_handle::bdPool[SAI_XFER_QUEUE_SIZE]`
- (2) `sai_transfer_t _sai_sdma_handle::saiQueue[SAI_XFER_QUEUE_SIZE]`
- (3) `volatile uint8_t _sai_sdma_handle::queueUser`

23.6.4 Function Documentation

23.6.4.1 void SAI_TransferTxCreateHandleSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_sdma_callback_t *callback*, void * *userData*, sdma_handle_t * *dmaHandle*, uint32_t *eventSource*)

This function initializes the SAI master DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI SDMA handle pointer.
<i>base</i>	SAI peripheral base address.

<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User parameter passed to the callback function.
<i>dmaHandle</i>	SDMA handle pointer, this handle shall be static allocated by users.
<i>eventSource</i>	SAI event source number.

23.6.4.2 void SAI_TransferRxCreateHandleSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_sdma_callback_t *callback*, void * *userData*, sdma_handle_t * *dmaHandle*, uint32_t *eventSource*)

This function initializes the SAI slave DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI SDMA handle pointer.
<i>base</i>	SAI peripheral base address.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User parameter passed to the callback function.
<i>dmaHandle</i>	SDMA handle pointer, this handle shall be static allocated by users.
<i>eventSource</i>	SAI event source number.

23.6.4.3 status_t SAI_TransferSendSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_transfer_t * *xfer*)

Note

This interface returns immediately after the transfer initiates. Call SAI_GetTransferStatus to poll the transfer status and check whether the SAI transfer is finished.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI SDMA handle pointer.

<i>xfer</i>	Pointer to the DMA transfer structure.
-------------	--

Return values

<i>kStatus_Success</i>	Start a SAI SDMA send successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.
<i>kStatus_TxBusy</i>	SAI is busy sending data.

23.6.4.4 status_t SAI_TransferReceiveSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_transfer_t * *xfer*)

Note

This interface returns immediately after the transfer initiates. Call the SAI_GetReceiveRemainingBytes to poll the transfer status and check whether the SAI transfer is finished.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI SDMA handle pointer.
<i>xfer</i>	Pointer to DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a SAI SDMA receive successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.
<i>kStatus_RxBusy</i>	SAI is busy receiving data.

23.6.4.5 void SAI_TransferAbortSendSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

<i>handle</i>	SAI SDMA handle pointer.
---------------	--------------------------

23.6.4.6 void SAI_TransferAbortReceiveSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI SDMA handle pointer.

23.6.4.7 void SAI_TransferTerminateReceiveSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI SDMA handle pointer.

23.6.4.8 void SAI_TransferTerminateSendSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI SDMA handle pointer.

23.6.4.9 void SAI_TransferRxSetConfigSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_transceiver_t * *saiConfig*)

param base SAI base pointer. param handle SAI SDMA handle pointer. param saiConig sai configurations.

23.6.4.10 void SAI_TransferTxSetConfigSDMA (I2S_Type * *base*, sai_sdma_handle_t * *handle*, sai_transceiver_t * *saiConfig*)

param base SAI base pointer. param handle SAI SDMA handle pointer. param saiConig sai configurations.

Chapter 24

SDMA: Smart Direct Memory Access (SDMA) Controller Driver

24.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Smart Direct Memory Access (SDMA) of devices.

24.2 Typical use case

24.2.1 SDMA Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/sdma

Data Structures

- struct `_sdma_config`
SDMA global configuration structure. [More...](#)
- struct `_sdma_multi_fifo_config`
SDMA multi fifo configurations. [More...](#)
- struct `_sdma_sw_done_config`
SDMA sw done configurations. [More...](#)
- struct `_sdma_p2p_config`
SDMA peripheral to peripheral R7 config. [More...](#)
- struct `_sdma_transfer_config`
SDMA transfer configuration. [More...](#)
- struct `_sdma_buffer_descriptor`
SDMA buffer descriptor structure. [More...](#)
- struct `_sdma_channel_control`
SDMA channel control descriptor structure. [More...](#)
- struct `_sdma_context_data`
SDMA context structure for each channel. [More...](#)
- struct `_sdma_handle`
SDMA transfer handle structure. [More...](#)

Typedefs

- typedef enum `_sdma_transfer_size` `sdma_transfer_size_t`
SDMA transfer configuration.
- typedef enum `_sdma_bd_status` `sdma_bd_status_t`
SDMA buffer descriptor status.
- typedef enum `_sdma_bd_command` `sdma_bd_command_t`
SDMA buffer descriptor command.
- typedef enum
 `_sdma_context_switch_mode` `sdma_context_switch_mode_t`

- *SDMA context switch mode.*
- `typedef enum _sdma_clock_ratio sdma_clock_ratio_t`
SDMA core clock frequency ratio to the ARM DMA interface.
- `typedef enum _sdma_transfer_type sdma_transfer_type_t`
SDMA transfer type.
- `typedef enum sdma_peripheral sdma_peripheral_t`
Peripheral type use SDMA.
- `typedef enum _sdma_done_src sdma_done_src_t`
SDMA done source.
- `typedef struct _sdma_config sdma_config_t`
SDMA global configuration structure.
- `typedef struct _sdma_multi_fifo_config sdma_multi_fifo_config_t`
SDMA multi fifo configurations.
- `typedef struct _sdma_sw_done_config sdma_sw_done_config_t`
SDMA sw done configurations.
- `typedef struct _sdma_p2p_config sdma_p2p_config_t`
SDMA peripheral to peripheral R7 config.
- `typedef struct _sdma_transfer_config sdma_transfer_config_t`
SDMA transfer configuration.
- `typedef struct _sdma_buffer_descriptor sdma_buffer_descriptor_t`
SDMA buffer descriptor structure.
- `typedef struct _sdma_channel_control sdma_channel_control_t`
SDMA channel control descriptor structure.
- `typedef struct _sdma_context_data sdma_context_data_t`
SDMA context structure for each channel.
- `typedef void(* sdma_callback)(struct _sdma_handle *handle, void *userData, bool transferDone, uint32_t bdIndex)`
Define callback function for SDMA.
- `typedef struct _sdma_handle sdma_handle_t`
SDMA transfer handle structure.

Enumerations

- `enum _sdma_transfer_size {`
 `kSDMA_TransferSize1Bytes = 0x1U,`
 `kSDMA_TransferSize2Bytes = 0x2U,`
 `kSDMA_TransferSize3Bytes = 0x3U,`
 `kSDMA_TransferSize4Bytes = 0x0U }`
SDMA transfer configuration.
- `enum _sdma_bd_status {`

```

kSDMA_BDStatusDone = 0x1U,
kSDMA_BDStatusWrap = 0x2U,
kSDMA_BDStatusContinuous = 0x4U,
kSDMA_BDStatusInterrupt = 0x8U,
kSDMA_BDStatusError = 0x10U,
kSDMA_BDStatusLast,
kSDMA_BDStatusExtend = 0x80U }

```

SDMA buffer descriptor status.

- enum `_sdma_bd_command` {

```

kSDMA_BDCommandSETDM = 0x1U,
kSDMA_BDCommandGETDM = 0x2U,
kSDMA_BDCommandSETPM = 0x4U,
kSDMA_BDCommandGETPM = 0x6U,
kSDMA_BDCommandSETCTX = 0x7U,
kSDMA_BDCommandGETCTX = 0x3U }

```

SDMA buffer descriptor command.

- enum `_sdma_context_switch_mode` {

```

kSDMA_ContextSwitchModeStatic = 0x0U,
kSDMA_ContextSwitchModeDynamicLowPower,
kSDMA_ContextSwitchModeDynamicWithNoLoop,
kSDMA_ContextSwitchModeDynamic }

```

SDMA context switch mode.

- enum `_sdma_clock_ratio` {

```

kSDMA_HalfARMClockFreq = 0x0U,
kSDMA_ARMClockFreq }

```

SDMA core clock frequency ratio to the ARM DMA interface.

- enum `_sdma_transfer_type` {

```

kSDMA_MemoryToMemory = 0x0U,
kSDMA_PeripheralToMemory,
kSDMA_MemoryToPeripheral,
kSDMA_PeripheralToPeripheral }

```

SDMA transfer type.

- enum `sdma_peripheral` {

```

kSDMA_PeripheralTypeMemory = 0x0,
kSDMA_PeripheralTypeUART,
kSDMA_PeripheralTypeUART_SP,
kSDMA_PeripheralTypeSPDIF,
kSDMA_PeripheralNormal,
kSDMA_PeripheralNormal_SP,
kSDMA_PeripheralMultiFifoPDM,
kSDMA_PeripheralMultiFifoSaiRX,
kSDMA_PeripheralMultiFifoSaiTX,
kSDMA_PeripheralASRCM2P,
kSDMA_PeripheralASRCP2M,
kSDMA_PeripheralASRCP2P }

```

Peripheral type use SDMA.

- enum {
 kStatus_SDMA_ERROR = MAKE_STATUS(kStatusGroup_SDMA, 0),
 kStatus_SDMA_Busy = MAKE_STATUS(kStatusGroup_SDMA, 1) }
 _sdma_transfer_status SDMA transfer status
- enum {
 kSDMA_MultiFifoWatermarkLevelMask = 0xFFFF,
 kSDMA_MultiFifoNumsMask = 0xFU,
 kSDMA_MultiFifoOffsetMask = 0xFU,
 kSDMA_MultiFifoSwDoneMask = 0x1U,
 kSDMA_MultiFifoSwDoneSelectorMask = 0xFU }
 _sdma_multi_fifo_mask SDMA multi fifo mask
- enum {
 kSDMA_MultiFifoWatermarkLevelShift = 0U,
 kSDMA_MultiFifoNumsShift = 12U,
 kSDMA_MultiFifoOffsetShift = 16U,
 kSDMA_MultiFifoSwDoneShift = 23U,
 kSDMA_MultiFifoSwDoneSelectorShift = 24U }
 _sdma_multi_fifo_shift SDMA multi fifo shift
- enum {
 kSDMA_DoneChannel0 = 0U,
 kSDMA_DoneChannel1 = 1U,
 kSDMA_DoneChannel2 = 2U,
 kSDMA_DoneChannel3 = 3U,
 kSDMA_DoneChannel4 = 4U,
 kSDMA_DoneChannel5 = 5U,
 kSDMA_DoneChannel6 = 6U,
 kSDMA_DoneChannel7 = 7U }
 _sdma_done_channel SDMA done channel
- enum _sdma_done_src {

```

kSDMA_DoneSrcSW = 0U,
kSDMA_DoneSrcHwEvent0U = 1U,
kSDMA_DoneSrcHwEvent1U = 2U,
kSDMA_DoneSrcHwEvent2U = 3U,
kSDMA_DoneSrcHwEvent3U = 4U,
kSDMA_DoneSrcHwEvent4U = 5U,
kSDMA_DoneSrcHwEvent5U = 6U,
kSDMA_DoneSrcHwEvent6U = 7U,
kSDMA_DoneSrcHwEvent7U = 8U,
kSDMA_DoneSrcHwEvent8U = 9U,
kSDMA_DoneSrcHwEvent9U = 10U,
kSDMA_DoneSrcHwEvent10U = 11U,
kSDMA_DoneSrcHwEvent11U = 12U,
kSDMA_DoneSrcHwEvent12U = 13U,
kSDMA_DoneSrcHwEvent13U = 14U,
kSDMA_DoneSrcHwEvent14U = 15U,
kSDMA_DoneSrcHwEvent15U = 16U,
kSDMA_DoneSrcHwEvent16U = 17U,
kSDMA_DoneSrcHwEvent17U = 18U,
kSDMA_DoneSrcHwEvent18U = 19U,
kSDMA_DoneSrcHwEvent19U = 20U,
kSDMA_DoneSrcHwEvent20U = 21U,
kSDMA_DoneSrcHwEvent21U = 22U,
kSDMA_DoneSrcHwEvent22U = 23U,
kSDMA_DoneSrcHwEvent23U = 24U,
kSDMA_DoneSrcHwEvent24U = 25U,
kSDMA_DoneSrcHwEvent25U = 26U,
kSDMA_DoneSrcHwEvent26U = 27U,
kSDMA_DoneSrcHwEvent27U = 28U,
kSDMA_DoneSrcHwEvent28U = 29U,
kSDMA_DoneSrcHwEvent29U = 30U,
kSDMA_DoneSrcHwEvent30U = 31U,
kSDMA_DoneSrcHwEvent31U = 32U }

```

SDMA done source.

Driver version

- #define **FSL_SDMA_DRIVER_VERSION** (MAKE_VERSION(2, 4, 2))
SDMA driver version.

SDMA initialization and de-initialization

- void **SDMA_Init** (SDMAARM_Type *base, const **sdma_config_t** *config)
Initializes the SDMA peripheral.
- void **SDMA_Deinit** (SDMAARM_Type *base)
Deinitializes the SDMA peripheral.

- void **SDMA_GetDefaultConfig** (sdma_config_t *config)
Gets the SDMA default configuration structure.
- void **SDMA_ResetModule** (SDMAARM_Type *base)
Sets all SDMA core register to reset status.

SDMA Channel Operation

- static void **SDMA_EnableChannelErrorInterrupts** (SDMAARM_Type *base, uint32_t channel)
Enables the interrupt source for the SDMA error.
- static void **SDMA_DisableChannelErrorInterrupts** (SDMAARM_Type *base, uint32_t channel)
Disables the interrupt source for the SDMA error.

SDMA Buffer Descriptor Operation

- void **SDMA_ConfigBufferDescriptor** (sdma_buffer_descriptor_t *bd, uint32_t srcAddr, uint32_t destAddr, sdma_transfer_size_t busWidth, size_t bufferSize, bool isLast, bool enableInterrupt, bool isWrap, sdma_transfer_type_t type)
Sets buffer descriptor contents.

SDMA Channel Transfer Operation

- static void **SDMA_SetChannelPriority** (SDMAARM_Type *base, uint32_t channel, uint8_t priority)
Set SDMA channel priority.
- static void **SDMA_SetSourceChannel** (SDMAARM_Type *base, uint32_t source, uint32_t channelMask)
Set SDMA request source mapping channel.
- static void **SDMA_StartChannelSoftware** (SDMAARM_Type *base, uint32_t channel)
Start a SDMA channel by software trigger.
- static void **SDMA_StartChannelEvents** (SDMAARM_Type *base, uint32_t channel)
Start a SDMA channel by hardware events.
- static void **SDMA_StopChannel** (SDMAARM_Type *base, uint32_t channel)
Stop a SDMA channel.
- void **SDMA_SetContextSwitchMode** (SDMAARM_Type *base, sdma_context_switch_mode_t mode)
Set the SDMA context switch mode.

SDMA Channel Status Operation

- static uint32_t **SDMA_GetChannelInterruptStatus** (SDMAARM_Type *base)
Gets the SDMA interrupt status of all channels.
- static void **SDMA_ClearChannelInterruptStatus** (SDMAARM_Type *base, uint32_t mask)
Clear the SDMA channel interrupt status of specific channels.
- static uint32_t **SDMA_GetChannelStopStatus** (SDMAARM_Type *base)
Gets the SDMA stop status of all channels.
- static void **SDMA_ClearChannelStopStatus** (SDMAARM_Type *base, uint32_t mask)
Clear the SDMA channel stop status of specific channels.
- static uint32_t **SDMA_GetChannelPendStatus** (SDMAARM_Type *base)
Gets the SDMA channel pending status of all channels.
- static void **SDMA_ClearChannelPendStatus** (SDMAARM_Type *base, uint32_t mask)

Clear the SDMA channel pending status of specific channels.

- static uint32_t **SDMA_GetErrorStatus** (SDMAARM_Type *base)
Gets the SDMA channel error status.
- bool **SDMA_GetRequestSourceStatus** (SDMAARM_Type *base, uint32_t source)
Gets the SDMA request source pending status.

SDMA Transactional Operation

- void **SDMA_CreateHandle** (sdma_handle_t *handle, SDMAARM_Type *base, uint32_t channel, sdma_context_data_t *context)
Creates the SDMA handle.
- void **SDMA_InstallBDMemory** (sdma_handle_t *handle, sdma_buffer_descriptor_t *BDPool, uint32_t BDCount)
Installs the BDs memory pool into the SDMA handle.
- void **SDMA_SetCallback** (sdma_handle_t *handle, sdma_callback callback, void *userData)
Installs a callback function for the SDMA transfer.
- void **SDMA_SetMultiFifoConfig** (sdma_transfer_config_t *config, uint32_t fifoNums, uint32_t fifoOffset)
multi fifo configurations.
- void **SDMA_EnableSwDone** (SDMAARM_Type *base, sdma_transfer_config_t *config, uint8_t sel, sdma_peripheral_t type)
enable sdma sw done feature.
- void **SDMA_SetDoneConfig** (SDMAARM_Type *base, sdma_transfer_config_t *config, sdma_peripheral_t type, sdma_done_src_t doneSrc)
sdma channel done configurations.
- void **SDMA_LoadScript** (SDMAARM_Type *base, uint32_t destAddr, void *srcAddr, size_t bufferSizeBytes)
load script to sdma program memory.
- void **SDMA_DumpScript** (SDMAARM_Type *base, uint32_t srcAddr, void *destAddr, size_t bufferSizeBytes)
dump script from sdma program memory.
- static const char * **SDMA_GetRamScriptVersion** (SDMAARM_Type *base)
Get RAM script version.
- void **SDMA_PrepTransfer** (sdma_transfer_config_t *config, uint32_t srcAddr, uint32_t destAddr, uint32_t srcWidth, uint32_t destWidth, uint32_t bytesEachRequest, uint32_t transferSize, uint32_t eventSource, sdma_peripheral_t peripheral, sdma_transfer_type_t type)
Prepares the SDMA transfer structure.
- void **SDMA_PrepP2PTransfer** (sdma_transfer_config_t *config, uint32_t srcAddr, uint32_t destAddr, uint32_t srcWidth, uint32_t destWidth, uint32_t bytesEachRequest, uint32_t transferSize, uint32_t eventSource, uint32_t eventSource1, sdma_peripheral_t peripheral, sdma_p2p_config_t *p2p)
Prepares the SDMA P2P transfer structure.
- void **SDMA_SubmitTransfer** (sdma_handle_t *handle, const sdma_transfer_config_t *config)
Submits the SDMA transfer request.
- void **SDMA_StartTransfer** (sdma_handle_t *handle)
SDMA starts transfer.
- void **SDMA_StopTransfer** (sdma_handle_t *handle)
SDMA stops transfer.
- void **SDMA_AbortTransfer** (sdma_handle_t *handle)
SDMA aborts transfer.

- `uint32_t SDMA_GetTransferredBytes (sdma_handle_t *handle)`
Get transferred bytes while not using BD pools.
- `bool SDMA_IsPeripheralInSPBA (uint32_t addr)`
Judge if address located in SPBA.
- `void SDMA_HandleIRQ (sdma_handle_t *handle)`
SDMA IRQ handler for complete a buffer descriptor transfer.

24.3 Data Structure Documentation

24.3.1 struct _sdma_config

Data Fields

- `bool enableRealTimeDebugPin`
If enable real-time debug pin, default is closed to reduce power consumption.
- `bool isSoftwareResetClearLock`
If software reset clears the LOCK bit which prevent writing SDMA scripts into SDMA.
- `sdma_clock_ratio_t ratio`
SDMA core clock ratio to ARM platform DMA interface.

Field Documentation

- (1) `bool _sdma_config::enableRealTimeDebugPin`
- (2) `bool _sdma_config::isSoftwareResetClearLock`

24.3.2 struct _sdma_multi_fifo_config

Data Fields

- `uint8_t fifoNums`
fifo numbers
- `uint8_t fifoOffset`
offset between multi fifo data register address

24.3.3 struct _sdma_sw_done_config

Data Fields

- `bool enableSwDone`
true is enable sw done, false is disable
- `uint8_t swDoneSel`
sw done channel number per peripheral type

24.3.4 struct _sdma_p2p_config

Data Fields

- uint8_t **sourceWatermark**
lower watermark value
- uint8_t **destWatermark**
higher watermark value
- bool **continuousTransfer**
0: the amount of samples to be transferred is equal to the cont field of mode word 1: the amount of samples to be transferred is unknown and script will keep on transferring as long as both events are detected and script must be stopped by application.

Field Documentation

(1) **bool _sdma_p2p_config::continuousTransfer**

24.3.5 struct _sdma_transfer_config

This structure configures the source/destination transfer attribute.

Data Fields

- uint32_t **srcAddr**
Source address of the transfer.
- uint32_t **destAddr**
Destination address of the transfer.
- **sdma_transfer_size_t srcTransferSize**
Source data transfer size.
- **sdma_transfer_size_t destTransferSize**
Destination data transfer size.
- uint32_t **bytesPerRequest**
Bytes to transfer in a minor loop.
- uint32_t **transferSzie**
Bytes to transfer for this descriptor.
- uint32_t **scriptAddr**
SDMA script address located in SDMA ROM.
- uint32_t **eventSource**
Event source number for the channel.
- uint32_t **eventSource1**
event source 1
- bool **isEventIgnore**
True means software trigger, false means hardware trigger.
- bool **isSoftTriggerIgnore**
If ignore the HE bit, 1 means use hardware events trigger, 0 means software trigger.
- **sdma_transfer_type_t type**
Transfer type, transfer type used to decide the SDMA script.
- **sdma_multi_fifo_config_t multiFifo**

- *multi fifo configurations*
- **sdma_sw_done_config_t swDone**
sw done selector
- **uint32_t watermarkLevel**
watermark level
- **uint32_t eventMask0**
event mask 0
- **uint32_t eventMask1**
event mask 1

Field Documentation

- (1) **sdma_transfer_size_t _sdma_transfer_config::srcTransferSize**
- (2) **sdma_transfer_size_t _sdma_transfer_config::destTransferSize**
- (3) **uint32_t _sdma_transfer_config::scriptAddr**
- (4) **uint32_t _sdma_transfer_config::eventSource**
0 means no event, use software trigger
- (5) **sdma_transfer_type_t _sdma_transfer_config::type**

24.3.6 struct _sdma_buffer_descriptor

This structure is a buffer descriptor, this structure describes the buffer start address and other options

Data Fields

- **uint32_t count:** 16
Bytes of the buffer length for this buffer descriptor.
- **uint32_t status:** 8
E,R,I,C,W,D status bits stored here.
- **uint32_t command:** 8
command mostly used for channel 0
- **uint32_t bufferAddr**
Buffer start address for this descriptor.
- **uint32_t extendBufferAddr**
External buffer start address, this is an optional for a transfer.

Field Documentation

- (1) `uint32_t _sdma_buffer_descriptor::count`
- (2) `uint32_t _sdma_buffer_descriptor::bufferAddr`
- (3) `uint32_t _sdma_buffer_descriptor::extendBufferAddr`

24.3.7 struct _sdma_channel_control**Data Fields**

- `uint32_t currentBDAddr`
Address of current buffer descriptor processed.
- `uint32_t baseBDAddr`
The start address of the buffer descriptor array.
- `uint32_t channelDesc`
Optional for transfer.
- `uint32_t status`
Channel status.

24.3.8 struct _sdma_context_data

This structure can be load into SDMA core, with this structure, SDMA scripts can start work.

Data Fields

- `uint32_t GeneralReg [8]`
8 general registers used for SDMA RISC core

24.3.9 struct _sdma_handle**Data Fields**

- `sdma_callback callback`
Callback function for major count exhausted.
- `void * userData`
Callback function parameter.
- `SDMAARM_Type * base`
SDMA peripheral base address.
- `sdma_buffer_descriptor_t * BDPool`
Pointer to memory stored BD arrays.
- `uint32_t bdCount`
How many buffer descriptor.
- `uint32_t bdIndex`

- `uint32_t eventSource`
How many buffer descriptor.
- `uint32_t eventSource1`
Event source count for the channel.
- `sdma_context_data_t * context`
Channel context to execute in SDMA.
- `uint8_t channel`
SDMA channel number.
- `uint8_t priority`
SDMA channel priority.
- `uint8_t flags`
The status of the current channel.

Field Documentation

- (1) `sdma_callback _sdma_handle::callback`
- (2) `void* _sdma_handle::userData`
- (3) `SDMAARM_Type* _sdma_handle::base`
- (4) `sdma_buffer_descriptor_t* _sdma_handle::BDPool`
- (5) `uint8_t _sdma_handle::channel`
- (6) `uint8_t _sdma_handle::flags`

24.4 Macro Definition Documentation

24.4.1 `#define FSL_SDMA_DRIVER_VERSION (MAKE_VERSION(2, 4, 2))`

Version 2.4.2.

24.5 Typedef Documentation

24.5.1 `typedef enum _sdma_clock_ratio sdma_clock_ratio_t`

24.5.2 `typedef struct _sdma_config sdma_config_t`

24.5.3 `typedef struct _sdma_multi_fifo_config sdma_multi_fifo_config_t`

24.5.4 `typedef struct _sdma_sw_done_config sdma_sw_done_config_t`

24.5.5 `typedef struct _sdma_transfer_config sdma_transfer_config_t`

This structure configures the source/destination transfer attribute.

24.5.6 `typedef struct _sdma_buffer_descriptor sdma_buffer_descriptor_t`

This structure is a buffer descriptor, this structure describes the buffer start address and other options

24.5.7 `typedef struct _sdma_context_data sdma_context_data_t`

This structure can be load into SDMA core, with this structure, SDMA scripts can start work.

24.5.8 `typedef void(* sdma_callback)(struct _sdma_handle *handle, void *userData, bool transferDone, uint32_t bdlIndex)`**24.6 Enumeration Type Documentation****24.6.1 `enum _sdma_transfer_size`**

Enumerator

kSDMA_TransferSize1Bytes Source/Destination data transfer size is 1 byte every time.

kSDMA_TransferSize2Bytes Source/Destination data transfer size is 2 bytes every time.

kSDMA_TransferSize3Bytes Source/Destination data transfer size is 3 bytes every time.

kSDMA_TransferSize4Bytes Source/Destination data transfer size is 4 bytes every time.

24.6.2 `enum _sdma_bd_status`

Enumerator

kSDMA_BDStatusDone BD ownership, 0 means ARM core owns the BD, while 1 means SDMA owns BD.

kSDMA_BDStatusWrap While this BD is last one, the next BD will be the first one.

kSDMA_BDStatusContinuous Buffer is allowed to transfer/receive to/from multiple buffers.

kSDMA_BDStatusInterrupt While this BD finished, send an interrupt.

kSDMA_BDStatusError Error occurred on buffer descriptor command.

kSDMA_BDStatusLast This BD is the last BD in this array. It means the transfer ended after this buffer

kSDMA_BDStatusExtend Buffer descriptor extend status for SDMA scripts.

24.6.3 `enum _sdma_bd_command`

Enumerator

kSDMA_BDCommandSETDM Load SDMA data memory from ARM core memory buffer.

kSDMA_BDCommandGETDM Copy SDMA data memory to ARM core memory buffer.
kSDMA_BDCommandSETPM Load SDMA program memory from ARM core memory buffer.
kSDMA_BDCommandGETPM Copy SDMA program memory to ARM core memory buffer.
kSDMA_BDCommandSETCTX Load context for one channel into SDMA RAM from ARM platform memory buffer.
kSDMA_BDCommandGETCTX Copy context for one channel from SDMA RAM to ARM platform memory buffer.

24.6.4 enum _sdma_context_switch_mode

Enumerator

kSDMA_ContextSwitchModeStatic SDMA context switch mode static.
kSDMA_ContextSwitchModeDynamicLowPower SDMA context switch mode dynamic with low power.
kSDMA_ContextSwitchModeDynamicWithNoLoop SDMA context switch mode dynamic with no loop.
kSDMA_ContextSwitchModeDynamic SDMA context switch mode dynamic.

24.6.5 enum _sdma_clock_ratio

Enumerator

kSDMA_HalfARMClockFreq SDMA core clock frequency half of ARM platform.
kSDMA_ARMClockFreq SDMA core clock frequency equals to ARM platform.

24.6.6 enum _sdma_transfer_type

Enumerator

kSDMA_MemoryToMemory Transfer from memory to memory.
kSDMA_PeripheralToMemory Transfer from peripheral to memory.
kSDMA_MemoryToPeripheral Transfer from memory to peripheral.
kSDMA_PeripheralToPeripheral Transfer from peripheral to peripheral.

24.6.7 enum sdma_peripheral

Enumerator

kSDMA_PeripheralTypeMemory Peripheral DDR memory.

kSDMA_PeripheralTypeUART UART use SDMA.
kSDMA_PeripheralTypeUART_SP UART instance in SPBA use SDMA.
kSDMA_PeripheralTypeSPDIF SPDIF use SDMA.
kSDMA_PeripheralNormal Normal peripheral use SDMA.
kSDMA_PeripheralNormal_SP Normal peripheral in SPBA use SDMA.
kSDMA_PeripheralMultiFifoPDM multi fifo PDM
kSDMA_PeripheralMultiFifoSaiRX multi fifo sai rx use SDMA
kSDMA_PeripheralMultiFifoSaiTX multi fifo sai tx use SDMA
kSDMA_PeripheralASRCM2P asrc m2p
kSDMA_PeripheralASRCP2M asrc p2m
kSDMA_PeripheralASRCP2P asrc p2p

24.6.8 anonymous enum

Enumerator

kStatus_SDMA_ERROR SDMA context error.
kStatus_SDMA_Busy Channel is busy and can't handle the transfer request.

24.6.9 anonymous enum

Enumerator

kSDMA_MultiFifoWatermarkLevelMask multi fifo watermark level mask
kSDMA_MultiFifoNumsMask multi fifo nums mask
kSDMA_MultiFifoOffsetMask multi fifo offset mask
kSDMA_MultiFifoSwDoneMask multi fifo sw done mask
kSDMA_MultiFifoSwDoneSelectorMask multi fifo sw done selector mask

24.6.10 anonymous enum

Enumerator

kSDMA_MultiFifoWatermarkLevelShift multi fifo watermark level shift
kSDMA_MultiFifoNumsShift multi fifo nums shift
kSDMA_MultiFifoOffsetShift multi fifo offset shift
kSDMA_MultiFifoSwDoneShift multi fifo sw done shift
kSDMA_MultiFifoSwDoneSelectorShift multi fifo sw done selector shift

24.6.11 anonymous enum

Enumerator

<i>kSDMA_DoneChannel0</i>	SDMA done channel 0.
<i>kSDMA_DoneChannel1</i>	SDMA done channel 1.
<i>kSDMA_DoneChannel2</i>	SDMA done channel 2.
<i>kSDMA_DoneChannel3</i>	SDMA done channel 3.
<i>kSDMA_DoneChannel4</i>	SDMA done channel 4.
<i>kSDMA_DoneChannel5</i>	SDMA done channel 5.
<i>kSDMA_DoneChannel6</i>	SDMA done channel 6.
<i>kSDMA_DoneChannel7</i>	SDMA done channel 7.

24.6.12 enum _sdma_done_src

Enumerator

<i>kSDMA_DoneSrcSW</i>	software done
<i>kSDMA_DoneSrcHwEvent0U</i>	HW event 0 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent1U</i>	HW event 1 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent2U</i>	HW event 2 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent3U</i>	HW event 3 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent4U</i>	HW event 4 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent5U</i>	HW event 5 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent6U</i>	HW event 6 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent7U</i>	HW event 7 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent8U</i>	HW event 8 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent9U</i>	HW event 9 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent10U</i>	HW event 10 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent11U</i>	HW event 11 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent12U</i>	HW event 12 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent13U</i>	HW event 13 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent14U</i>	HW event 14 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent15U</i>	HW event 15 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent16U</i>	HW event 16 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent17U</i>	HW event 17 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent18U</i>	HW event 18 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent19U</i>	HW event 19 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent20U</i>	HW event 20 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent21U</i>	HW event 21 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent22U</i>	HW event 22 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent23U</i>	HW event 23 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent24U</i>	HW event 24 is used for DONE event.
<i>kSDMA_DoneSrcHwEvent25U</i>	HW event 25 is used for DONE event.

- kSDMA_DoneSrcHwEvent26U* HW event 26 is used for DONE event.
- kSDMA_DoneSrcHwEvent27U* HW event 27 is used for DONE event.
- kSDMA_DoneSrcHwEvent28U* HW event 28 is used for DONE event.
- kSDMA_DoneSrcHwEvent29U* HW event 29 is used for DONE event.
- kSDMA_DoneSrcHwEvent30U* HW event 30 is used for DONE event.
- kSDMA_DoneSrcHwEvent31U* HW event 31 is used for DONE event.

24.7 Function Documentation

24.7.1 void SDMA_Init (**SDMAARM_Type** * *base*, **const sdma_config_t** * *config*)

This function ungates the SDMA clock and configures the SDMA peripheral according to the configuration structure.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>config</i>	A pointer to the configuration structure, see "sdma_config_t".

Note

This function enables the minor loop map feature.

24.7.2 void SDMA_Deinit (**SDMAARM_Type** * *base*)

This function gates the SDMA clock.

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

24.7.3 void SDMA_GetDefaultConfig (**sdma_config_t** * *config*)

This function sets the configuration structure to default values. The default configuration is set to the following values.

```
*   config.enableRealTimeDebugPin = false;
*   config.isSoftwareResetClearLock = true;
*   config.ratio = kSDMA_HalfARMClockFreq;
*
```

Parameters

<i>config</i>	A pointer to the SDMA configuration structure.
---------------	--

24.7.4 void SDMA_ResetModule (SDMAARM_Type * *base*)

If only reset ARM core, SDMA register cannot return to reset value, shall call this function to reset all SDMA register to reset value. But the internal status cannot be reset.

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

24.7.5 static void SDMA_EnableChannelErrorInterrupts (SDMAARM_Type * *base*, uint32_t *channel*) [inline], [static]

Enable this will trigger an interrupt while SDMA occurs error while executing scripts.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.

24.7.6 static void SDMA_DisableChannelErrorInterrupts (SDMAARM_Type * *base*, uint32_t *channel*) [inline], [static]

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.

24.7.7 void SDMA_ConfigBufferDescriptor (sdma_buffer_descriptor_t * *bd*, uint32_t *srcAddr*, uint32_t *destAddr*, sdma_transfer_size_t *busWidth*, size_t *bufferSize*, bool *isLast*, bool *enableInterrupt*, bool *isWrap*, sdma_transfer_type_t *type*)

This function sets the descriptor contents such as source, dest address and status bits.

Parameters

<i>bd</i>	Pointer to the buffer descriptor structure.
<i>srcAddr</i>	Source address for the buffer descriptor.
<i>destAddr</i>	Destination address for the buffer descriptor.
<i>busWidth</i>	The transfer width, it only can be a member of sdma_transfer_size_t.
<i>bufferSize</i>	Buffer size for this descriptor, this number shall less than 0xFFFF. If need to transfer a big size, shall divide into several buffer descriptors.
<i>isLast</i>	Is the buffer descriptor the last one for the channel to transfer. If only one descriptor used for the channel, this bit shall set to TRUE.
<i>enableInterrupt</i>	If trigger an interrupt while this buffer descriptor transfer finished.
<i>isWrap</i>	Is the buffer descriptor need to be wrapped. While this bit set to true, it will automatically wrap to the first buffer descriptor to do transfer.
<i>type</i>	Transfer type, memory to memory, peripheral to memory or memory to peripheral.

24.7.8 static void SDMA_SetChannelPriority (SDMAARM_Type * *base*, uint32_t *channel*, uint8_t *priority*) [inline], [static]

This function sets the channel priority. The default value is 0 for all channels, priority 0 will prevent channel from starting, so the priority must be set before start a channel.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.
<i>priority</i>	SDMA channel priority.

24.7.9 static void SDMA_SetSourceChannel (SDMAARM_Type * *base*, uint32_t *source*, uint32_t *channelMask*) [inline], [static]

This function sets which channel will be triggered by the dma request source.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>source</i>	SDMA dma request source number.
<i>channelMask</i>	SDMA channel mask. 1 means channel 0, 2 means channel 1, 4 means channel 3. SDMA supports an event trigger multi-channel. A channel can also be triggered by several source events.

24.7.10 static void SDMA_StartChannelSoftware (**SDMAARM_Type** * *base*, **uint32_t** *channel*) [inline], [static]

This function start a channel.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.

24.7.11 static void SDMA_StartChannelEvents (**SDMAARM_Type** * *base*, **uint32_t** *channel*) [inline], [static]

This function start a channel.

Parameters

<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.

24.7.12 static void SDMA_StopChannel (**SDMAARM_Type** * *base*, **uint32_t** *channel*) [inline], [static]

This function stops a channel.

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

<i>channel</i>	SDMA channel number.
----------------	----------------------

24.7.13 void SDMA_SetContextSwitchMode (SDMAARM_Type * *base*, sdma_context_switch_mode_t *mode*)

Parameters

<i>base</i>	SDMA peripheral base address.
<i>mode</i>	SDMA context switch mode.

24.7.14 static uint32_t SDMA_GetChannelInterruptStatus (SDMAARM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

Returns

The interrupt status for all channels. Check the relevant bits for specific channel.

24.7.15 static void SDMA_ClearChannelInterruptStatus (SDMAARM_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SDMA peripheral base address.
<i>mask</i>	The interrupt status need to be cleared.

24.7.16 static uint32_t SDMA_GetChannelStopStatus (SDMAARM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

Returns

The stop status for all channels. Check the relevant bits for specific channel.

24.7.17 static void SDMA_ClearChannelStopStatus (SDMAARM_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SDMA peripheral base address.
<i>mask</i>	The stop status need to be cleared.

24.7.18 static uint32_t SDMA_GetChannelPendStatus (SDMAARM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

Returns

The pending status for all channels. Check the relevant bits for specific channel.

24.7.19 static void SDMA_ClearChannelPendStatus (SDMAARM_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

<i>mask</i>	The pending status need to be cleared.
-------------	--

24.7.20 static uint32_t SDMA_GetErrorStatus (**SDMAARM_Type** * *base*) [**inline**], [**static**]

SDMA channel error flag is asserted while an incoming DMA request was detected and it triggers a channel that is already pending or being serviced. This probably means there is an overflow of data for that channel.

Parameters

<i>base</i>	SDMA peripheral base address.
-------------	-------------------------------

Returns

The error status for all channels. Check the relevant bits for specific channel.

24.7.21 bool SDMA_GetRequestSourceStatus (**SDMAARM_Type** * *base*, **uint32_t** *source*)

Parameters

<i>base</i>	SDMA peripheral base address.
<i>source</i>	DMA request source number.

Returns

True means the request source is pending, otherwise not pending.

24.7.22 void SDMA_CreateHandle (**sdma_handle_t** * *handle*, **SDMAARM_Type** * *base*, **uint32_t** *channel*, **sdma_context_data_t** * *context*)

This function is called if using the transactional API for SDMA. This function initializes the internal state of the SDMA handle.

Parameters

<i>handle</i>	SDMA handle pointer. The SDMA handle stores callback function and parameters.
<i>base</i>	SDMA peripheral base address.
<i>channel</i>	SDMA channel number.
<i>context</i>	Context structure for the channel to download into SDMA. Users shall make sure the context located in a non-cacheable memory, or it will cause SDMA run fail. Users shall not touch the context contents, it only be filled by SDMA driver in SDMA--SubmitTransfer function.

24.7.23 void SDMA_InstallIBDMemory (*sdma_handle_t * handle*, *sdma_buffer_descriptor_t * BDPool*, *uint32_t BDCount*)

This function is called after the SDMA_CreateHandle to use multi-buffer feature.

Parameters

<i>handle</i>	SDMA handle pointer.
<i>BDPool</i>	A memory pool to store BDs. It must be located in non-cacheable address.
<i>BDCount</i>	The number of BD slots.

24.7.24 void SDMA_SetCallback (*sdma_handle_t * handle*, *sdma_callback callback*, *void * userData*)

This callback is called in the SDMA IRQ handler. Use the callback to do something after the current major loop transfer completes.

Parameters

<i>handle</i>	SDMA handle pointer.
<i>callback</i>	SDMA callback function pointer.
<i>userData</i>	A parameter for the callback function.

24.7.25 void SDMA_SetMultiFifoConfig (*sdma_transfer_config_t * config*, *uint32_t fifoNums*, *uint32_t fifoOffset*)

This api is used to support multi fifo for SDMA, if user want to get multi fifo data, then this api shoule be called before submit transfer.

Parameters

<i>config</i>	transfer configurations.
<i>fifoNums</i>	fifo numbers that multi fifo operation perform, support up to 15 fifo numbers.
<i>fifoOffset</i>	<i>fifoOffset</i> = fifo address offset / sizeof(uint32_t) - 1.

24.7.26 void SDMA_EnableSwDone (SDMAARM_Type * *base*, sdma_transfer_config_t * *config*, uint8_t *sel*, sdma_peripheral_t *type*)

Deprecated Do not use this function. It has been superceded by [SDMA_SetDoneConfig](#).

Parameters

<i>base</i>	SDMA base.
<i>config</i>	transfer configurations.
<i>sel</i>	sw done selector.
<i>type</i>	peripheral type is used to determine the corresponding peripheral sw done selector bit.

24.7.27 void SDMA_SetDoneConfig (SDMAARM_Type * *base*, sdma_transfer_config_t * *config*, sdma_peripheral_t *type*, sdma_done_src_t *doneSrc*)

Parameters

<i>base</i>	SDMA base.
<i>config</i>	transfer configurations.
<i>type</i>	peripheral type.
<i>doneSrc</i>	reference sdma_done_src_t.

24.7.28 void SDMA_LoadScript (SDMAARM_Type * *base*, uint32_t *destAddr*, void * *srcAddr*, size_t *bufferSizeBytes*)

Parameters

<i>base</i>	SDMA base.
<i>destAddr</i>	dest script address, should be SDMA program memory address.
<i>srcAddr</i>	source address of target script.
<i>bufferSizeBytes</i>	bytes size of script.

24.7.29 void SDMA_DumpScript (SDMAARM_Type * *base*, uint32_t *srcAddr*, void * *destAddr*, size_t *bufferSizeBytes*)

Parameters

<i>base</i>	SDMA base.
<i>srcAddr</i>	should be SDMA program memory address.
<i>destAddr</i>	address to store scripts.
<i>bufferSizeBytes</i>	bytes size of script.

24.7.30 static const char* SDMA_GetRamScriptVersion (SDMAARM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	SDMA base.
-------------	------------

Returns

The script version of RAM.

24.7.31 void SDMA_PrepTransfer (sdma_transfer_config_t * *config*, uint32_t *srcAddr*, uint32_t *destAddr*, uint32_t *srcWidth*, uint32_t *destWidth*, uint32_t *bytesEachRequest*, uint32_t *transferSize*, uint32_t *eventSource*, sdma_peripheral_t *peripheral*, sdma_transfer_type_t *type*)

This function prepares the transfer configuration structure according to the user input.

Parameters

<i>config</i>	The user configuration structure of type sdma_transfer_t.
<i>srcAddr</i>	SDMA transfer source address.
<i>destAddr</i>	SDMA transfer destination address.
<i>srcWidth</i>	SDMA transfer source address width(bytes).
<i>destWidth</i>	SDMA transfer destination address width(bytes).
<i>bytesEachRequest</i>	SDMA transfer bytes per channel request.
<i>transferSize</i>	SDMA transfer bytes to be transferred.
<i>eventSource</i>	Event source number for the transfer, if use software trigger, just write 0.
<i>peripheral</i>	Peripheral type, used to decide if need to use some special scripts.
<i>type</i>	SDMA transfer type. Used to decide the correct SDMA script address in SDMA ROM.

Note

The data address and the data width must be consistent. For example, if the SRC is 4 bytes, the source address must be 4 bytes aligned, or it results in source address error.

**24.7.32 void SDMA_PreparesP2PTransfer (sdma_transfer_config_t * *config*,
 uint32_t *srcAddr*, uint32_t *destAddr*, uint32_t *srcWidth*, uint32_t
destWidth, uint32_t *bytesEachRequest*, uint32_t *transferSize*, uint32_t
eventSource, uint32_t *eventSource1*, sdma_peripheral_t *peripheral*,
 sdma_p2p_config_t * *p2p*)**

This function prepares the transfer configuration structure according to the user input.

Parameters

<i>config</i>	The user configuration structure of type sdma_transfer_t.
<i>srcAddr</i>	SDMA transfer source address.
<i>destAddr</i>	SDMA transfer destination address.

<i>srcWidth</i>	SDMA transfer source address width(bytes).
<i>destWidth</i>	SDMA transfer destination address width(bytes).
<i>bytesEachRequest</i>	SDMA transfer bytes per channel request.
<i>transferSize</i>	SDMA transfer bytes to be transferred.
<i>eventSource</i>	Event source number for the transfer.
<i>eventSource1</i>	Event source1 number for the transfer.
<i>peripheral</i>	Peripheral type, used to decide if need to use some special scripts.
<i>p2p</i>	sdma p2p configuration pointer.

Note

The data address and the data width must be consistent. For example, if the SRC is 4 bytes, the source address must be 4 bytes aligned, or it results in source address error.

24.7.33 void SDMA_SubmitTransfer (*sdma_handle_t * handle*, *const sdma_transfer_config_t * config*)

This function submits the SDMA transfer request according to the transfer configuration structure.

Parameters

<i>handle</i>	SDMA handle pointer.
<i>config</i>	Pointer to SDMA transfer configuration structure.

24.7.34 void SDMA_StartTransfer (*sdma_handle_t * handle*)

This function enables the channel request. Users can call this function after submitting the transfer request or before submitting the transfer request.

Parameters

<i>handle</i>	SDMA handle pointer.
---------------	----------------------

24.7.35 void SDMA_StopTransfer (*sdma_handle_t * handle*)

This function disables the channel request to pause the transfer. Users can call [SDMA_StartTransfer\(\)](#) again to resume the transfer.

Parameters

<i>handle</i>	SDMA handle pointer.
---------------	----------------------

24.7.36 void SDMA_AbortTransfer (**sdma_handle_t * handle**)

This function disables the channel request and clear transfer status bits. Users can submit another transfer after calling this API.

Parameters

<i>handle</i>	DMA handle pointer.
---------------	---------------------

24.7.37 uint32_t SDMA_GetTransferredBytes (**sdma_handle_t * handle**)

This function returns the buffer descriptor count value if not using buffer descriptor. While do a simple transfer, which only uses one descriptor, the SDMA driver inside handle the buffer descriptor. In uart receive case, it can tell users how many data already received, also it can tells users how many data transferred while error occurred. Notice, the count would not change while transfer is on-going using default SDMA script.

Parameters

<i>handle</i>	DMA handle pointer.
---------------	---------------------

Returns

Transferred bytes.

24.7.38 bool SDMA_IsPeripheralInSPBA (**uint32_t addr**)

Parameters

<i>addr</i>	Address which need to judge.
-------------	------------------------------

Return values

<i>True</i>	means located in SPBA, false means not.
-------------	---

24.7.39 void SDMA_HandleIRQ (*sdma_handle_t* * *handle*)

This function clears the interrupt flags and also handle the CCB for the channel.

Parameters

<i>handle</i>	SDMA handle pointer.
---------------	----------------------

Chapter 25

SEMA4: Hardware Semaphores Driver

25.1 Overview

The MCUXpresso SDK provides a driver for the SEMA4 module of MCUXpresso SDK devices.

Macros

- `#define SEMA4_GATE_NUM_RESET_ALL (64U)`
The number to reset all SEMA4 gates.
- `#define SEMA4_GATEn(base, n) (((volatile uint8_t *)(&((base)->Gate00)))[(n)])`
SEMA4 gate n register address.

Functions

- `void SEMA4_Init (SEMA4_Type *base)`
Initializes the SEMA4 module.
- `void SEMA4_Deinit (SEMA4_Type *base)`
De-initializes the SEMA4 module.
- `status_t SEMA4_TryLock (SEMA4_Type *base, uint8_t gateNum, uint8_t procNum)`
Tries to lock the SEMA4 gate.
- `void SEMA4_Lock (SEMA4_Type *base, uint8_t gateNum, uint8_t procNum)`
Locks the SEMA4 gate.
- `static void SEMA4_Unlock (SEMA4_Type *base, uint8_t gateNum)`
Unlocks the SEMA4 gate.
- `static int32_t SEMA4_GetLockProc (SEMA4_Type *base, uint8_t gateNum)`
Gets the status of the SEMA4 gate.
- `status_t SEMA4_ResetGate (SEMA4_Type *base, uint8_t gateNum)`
Resets the SEMA4 gate to an unlocked status.
- `static status_t SEMA4_ResetAllGates (SEMA4_Type *base)`
Resets all SEMA4 gates to an unlocked status.
- `static void SEMA4_EnableGateNotifyInterrupt (SEMA4_Type *base, uint8_t procNum, uint32_t mask)`
Enable the gate notification interrupt.
- `static void SEMA4_DisableGateNotifyInterrupt (SEMA4_Type *base, uint8_t procNum, uint32_t mask)`
Disable the gate notification interrupt.
- `static uint32_t SEMA4_GetGateNotifyStatus (SEMA4_Type *base, uint8_t procNum)`
Get the gate notification flags.
- `status_t SEMA4_ResetGateNotify (SEMA4_Type *base, uint8_t gateNum)`
Resets the SEMA4 gate IRQ notification.
- `static status_t SEMA4_ResetAllGateNotify (SEMA4_Type *base)`
Resets all SEMA4 gates IRQ notification.

Driver version

- #define **FSL_SEMA4_DRIVER_VERSION** (**MAKE_VERSION**(2, 0, 3))
SEMA4 driver version.

25.2 Macro Definition Documentation

25.2.1 #define SEMA4_GATE_NUM_RESET_ALL (64U)

25.3 Function Documentation

25.3.1 void SEMA4_Init (**SEMA4_Type** * *base*)

This function initializes the SEMA4 module. It only enables the clock but does not reset the gates because the module might be used by other processors at the same time. To reset the gates, call either SEMA4_ResetGate or SEMA4_ResetAllGates function.

Parameters

<i>base</i>	SEMA4 peripheral base address.
-------------	--------------------------------

25.3.2 void SEMA4_Deinit (**SEMA4_Type** * *base*)

This function de-initializes the SEMA4 module. It only disables the clock.

Parameters

<i>base</i>	SEMA4 peripheral base address.
-------------	--------------------------------

25.3.3 status_t SEMA4_TryLock (**SEMA4_Type** * *base*, **uint8_t** *gateNum*, **uint8_t** *procNum*)

This function tries to lock the specific SEMA4 gate. If the gate has been locked by another processor, this function returns an error code.

Parameters

<i>base</i>	SEMA4 peripheral base address.
-------------	--------------------------------

<i>gateNum</i>	Gate number to lock.
<i>procNum</i>	Current processor number.

Return values

<i>kStatus_Success</i>	Lock the sema4 gate successfully.
<i>kStatus_Fail</i>	Sema4 gate has been locked by another processor.

25.3.4 void SEMA4_Lock (SEMA4_Type * *base*, uint8_t *gateNum*, uint8_t *procNum*)

This function locks the specific SEMA4 gate. If the gate has been locked by other processors, this function waits until it is unlocked and then lock it.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>gateNum</i>	Gate number to lock.
<i>procNum</i>	Current processor number.

25.3.5 static void SEMA4_Unlock (SEMA4_Type * *base*, uint8_t *gateNum*) [inline], [static]

This function unlocks the specific SEMA4 gate. It only writes unlock value to the SEMA4 gate register. However, it does not check whether the SEMA4 gate is locked by the current processor or not. As a result, if the SEMA4 gate is not locked by the current processor, this function has no effect.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>gateNum</i>	Gate number to unlock.

25.3.6 static int32_t SEMA4_GetLockProc (SEMA4_Type * *base*, uint8_t *gateNum*) [inline], [static]

This function checks the lock status of a specific SEMA4 gate.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>gateNum</i>	Gate number.

Returns

Return -1 if the gate is unlocked, otherwise return the processor number which has locked the gate.

25.3.7 **status_t SEMA4_ResetGate (SEMA4_Type * *base*, uint8_t *gateNum*)**

This function resets a SEMA4 gate to an unlocked status.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>gateNum</i>	Gate number.

Return values

<i>kStatus_Success</i>	SEMA4 gate is reset successfully.
<i>kStatus_Fail</i>	Some other reset process is ongoing.

25.3.8 **static status_t SEMA4_ResetAllGates (SEMA4_Type * *base*) [inline], [static]**

This function resets all SEMA4 gate to an unlocked status.

Parameters

<i>base</i>	SEMA4 peripheral base address.
-------------	--------------------------------

Return values

<i>kStatus_Success</i>	SEMA4 is reset successfully.
------------------------	------------------------------

<i>kStatus_Fail</i>	Some other reset process is ongoing.
---------------------	--------------------------------------

25.3.9 static void SEMA4_EnableGateNotifyInterrupt (SEMA4_Type * *base*, uint8_t *procNum*, uint32_t *mask*) [inline], [static]

Gate notification provides such feature, when core tried to lock the gate and failed, it could get notification when the gate is idle.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>procNum</i>	Current processor number.
<i>mask</i>	OR'ed value of the gate index, for example: (1<<0) (1<<1) means gate 0 and gate 1.

25.3.10 static void SEMA4_DisableGateNotifyInterrupt (SEMA4_Type * *base*, uint8_t *procNum*, uint32_t *mask*) [inline], [static]

Gate notification provides such feature, when core tried to lock the gate and failed, it could get notification when the gate is idle.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>procNum</i>	Current processor number.
<i>mask</i>	OR'ed value of the gate index, for example: (1<<0) (1<<1) means gate 0 and gate 1.

25.3.11 static uint32_t SEMA4_GetGateNotifyStatus (SEMA4_Type * *base*, uint8_t *procNum*) [inline], [static]

Gate notification provides such feature, when core tried to lock the gate and failed, it could get notification when the gate is idle. The status flags are cleared automatically when the gate is locked by current core or locked again before the other core.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>procNum</i>	Current processor number.

Returns

OR'ed value of the gate index, for example: $(1 << 0) | (1 << 1)$ means gate 0 and gate 1 flags are pending.

25.3.12 status_t SEMA4_ResetGateNotify (SEMA4_Type * *base*, uint8_t *gateNum*)

This function resets a SEMA4 gate IRQ notification.

Parameters

<i>base</i>	SEMA4 peripheral base address.
<i>gateNum</i>	Gate number.

Return values

<i>kStatus_Success</i>	Reset successfully.
<i>kStatus_Fail</i>	Some other reset process is ongoing.

25.3.13 static status_t SEMA4_ResetAllGateNotify (SEMA4_Type * *base*) [inline], [static]

This function resets all SEMA4 gate IRQ notifications.

Parameters

<i>base</i>	SEMA4 peripheral base address.
-------------	--------------------------------

Return values

<i>kStatus_Success</i>	Reset successfully.
<i>kStatus_Fail</i>	Some other reset process is ongoing.

Chapter 26

TMU: Thermal Management Unit Driver

26.1 Overview

The MCUXpresso SDK provides a peripheral driver for the thermal management unit (TMU) module of MCUXpresso SDK devices.

26.2 Typical use case

26.2.1 Monitor and report Configuration

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/tmu

Data Structures

- struct `_tmu_threshold_config`
configuration for TMU threshold. [More...](#)
- struct `_tmu_config`
Configuration for TMU module. [More...](#)

Macros

- `#define FSL_TMU_DRIVER_VERSION (MAKE_VERSION(2, 0, 0))`
TMU driver version.

Typedefs

- `typedef struct _tmu_threshold_config tmu_threshold_config_t`
configuration for TMU threshold.
- `typedef enum _tmu_probe_select tmu_probe_select_t`
Probe selection.
- `typedef enum _tmu_average_low_pass_filter tmu_average_low_pass_filter_t`
Average low pass filter setting.
- `typedef struct _tmu_config tmu_config_t`
Configuration for TMU module.

Enumerations

- enum {

kTMU_ImmediateTemperature0InterruptEnable,
 kTMU_AverageTemperature0InterruptEnable,
 kTMU_AverageTemperature0CriticalInterruptEnable,
 kTMU_ImmediateTemperature1Interrupt1Enable,
 kTMU_AverageTemperature1Interrupt1Enable,
 kTMU_AverageTemperature1CriticalInterrupt1Enable }

TMU interrupt enable, _tmu_interrupt_enable.
- enum {

kTMU_ImmediateTemperature0InterruptStausFlags,
 kTMU_AverageTemperature0InterruptStausFlags,
 kTMU_AverageTemperature0CriticalInterruptStausFlags,
 kTMU_ImmediateTemperature1Interrupt1StausFlags,
 kTMU_AverageTemperature1Interrupt1StausFlags,
 kTMU_AverageTemperature1CriticalInterrupt1StausFlags }

TMU interrupt enable, _tmu_interrupt_status_flags.
- enum _tmu_probe_select {

kTMU_ProbeSelectMainProbe = 1U << 0U,
 kTMU_ProbeSelectRemoteProbe = 1U << 1U,
 kTMU_ProbeSelectBothProbes = (1U << 0U) | (1U << 1U) }

Probe selection.
- enum _tmu_average_low_pass_filter {

kTMU_AverageLowPassFilter1_0 = 0U,
 kTMU_AverageLowPassFilter0_5 = 1U,
 kTMU_AverageLowPassFilter0_25 = 2U,
 kTMU_AverageLowPassFilter0_125 = 3U }

Average low pass filter setting.

Functions

- void **TMU_Init** (TMU_Type *base, const **tmu_config_t** *config)

Enable the access to TMU registers and Initialize TMU module.
- void **TMU_Deinit** (TMU_Type *base)

De-initialize TMU module and Disable the access to DCDC registers.
- void **TMU_Enable** (TMU_Type *base, bool enable)

Enable/disable TMU module.
- void **TMU_GetDefaultConfig** (**tmu_config_t** *config)

Gets the default configuration for TMU.
- static void **TMU_EnableInterrupts** (TMU_Type *base, uint32_t mask)

Enable the TMU interrupts.
- static void **TMU_DisableInterrupts** (TMU_Type *base, uint32_t mask)

Disable the TMU interrupts.
- static uint32_t **TMU_GetInterruptStatusFlags** (TMU_Type *base)

Get interrupt status flags.
- static void **TMU_ClearInterruptStatusFlags** (TMU_Type *base, uint32_t mask)

Clear interrupt status flags.

- `status_t TMU_GetImmediateTemperature` (`TMU_Type *base, tmu_probe_select_t probe, int8_t *temperature)`
Get the last immediate temperature at site.
- `status_t TMU_GetAverageTemperature` (`TMU_Type *base, tmu_probe_select_t probe, int8_t *temperature)`
Get the last average temperature at site.
- `void TMU_UpdateHighTemperatureThreshold` (`TMU_Type *base, tmu_probe_select_t probe, const tmu_threshold_config_t *thresholdConfig)`
Update the high temperature threshold value.

26.3 Data Structure Documentation

26.3.1 struct _tmu_threshold_config

Data Fields

- `bool immediateThresholdEnable`
Enable high temperature immediate threshold.
- `bool AverageThresholdEnable`
Enable high temperature average threshold.
- `bool AverageCriticalThresholdEnable`
Enable high temperature average critical threshold.
- `uint8_t immediateThresholdValueOfMainProbe`
Range:-40~125.
- `uint8_t averageThresholdValueOfMainProbe`
Range:-40~125.
- `uint8_t averageCriticalThresholdValueOfMainProbe`
Range:-40~125.
- `uint8_t immediateThresholdValueOfRemoteProbe`
Range:-40~125.
- `uint8_t averageThresholdValueOfRemoteProbe`
Range:-40~125.
- `uint8_t averageCriticalThresholdValueOfRemoteProbe`
Range:-40~125.

Field Documentation

- (1) `bool _tmu_threshold_config::immediateThresholdEnable`
- (2) `bool _tmu_threshold_config::AverageThresholdEnable`
- (3) `bool _tmu_threshold_config::AverageCriticalThresholdEnable`
- (4) `uint8_t _tmu_threshold_config::immediateThresholdValueOfMainProbe`

Valid when corresponding threshold is enabled. High temperature immediate threshold value of main probe. Besides, bit-8 is sign bit: 1 means negative and 0 means positive.

(5) uint8_t _tmu_threshold_config::averageThresholdValueOfMainProbe

Valid when corresponding threshold is enabled. High temperature average threshold value of main probe. Besides, bit-8 is sign bit: 1 means nagetive and 0 means positive.

(6) uint8_t _tmu_threshold_config::averageCriticalThresholdValueOfMainProbe

Valid when corresponding threshold is enabled. High temperature average critical threshold value of main probe. Besides, bit-8 is sign bit: 1 means nagetive and 0 means positive.

(7) uint8_t _tmu_threshold_config::immediateThresholdValueOfRemoteProbe

Valid when corresponding threshold is enabled. High temperature immediate threshold value of remote probe. Besides, bit-8 is sign bit: 1 means nagetive and 0 means positive.

(8) uint8_t _tmu_threshold_config::averageThresholdValueOfRemoteProbe

Valid when corresponding threshold is enabled. High temperature average threshold value of remote probe. Besides, bit-8 is sign bit: 1 means nagetive and 0 means positive.

(9) uint8_t _tmu_threshold_config::averageCriticalThresholdValueOfRemoteProbe

Valid when corresponding threshold is enabled. High temperature average critical threshold value of remote probe. Besides, bit-8 is sign bit: 1 means nagetive and 0 means positive.

26.3.2 struct _tmu_config

Data Fields

- [tmu_probe_select_t probeSelect](#)
The temperature monitor probe select.
- [tmu_average_low_pass_filter_t averageLPF](#)
The average temperature is calculated as: ALPF x Current_Temp + (1 - ALPF) x Average_Temp.
- [tmu_threshold_config_t thresholdConfig](#)
The high temperature threshold configuration.

Field Documentation

(1) tmu_probe_select_t _tmu_config::probeSelect**(2) tmu_average_low_pass_filter_t _tmu_config::averageLPF**

For proper operation, this field should only change when monitoring is disabled.

(3) tmu_threshold_config_t _tmu_config::thresholdConfig

26.4 Macro Definition Documentation

26.4.1 #define FSL_TMU_DRIVER_VERSION (MAKE_VERSION(2, 0, 0))

Version 2.0.0.

26.5 Enumeration Type Documentation

26.5.1 anonymous enum

Enumerator

kTMU_ImmediateTemperature0InterruptEnable Immediate temperature threshold exceeded interrupt enable of probe0.

kTMU_AverageTemperature0InterruptEnable Average temperature threshold exceeded interrupt enable of probe0.

kTMU_AverageTemperature0CriticalInterruptEnable Average temperature critical threshold exceeded interrupt enable of probe0.

kTMU_ImmediateTemperature1Interrupt1Enable Immediate temperature threshold exceeded interrupt enable of probe1.

kTMU_AverageTemperature1Interrupt1Enable Average temperature threshold exceeded interrupt enable of probe1.

kTMU_AverageTemperature1CriticalInterrupt1Enable Average temperature critical threshold exceeded interrupt enable of probe1.

26.5.2 anonymous enum

Enumerator

kTMU_ImmediateTemperature0InterruptStatusFlags Immediate temperature threshold exceeded interrupt status of probe0.

kTMU_AverageTemperature0InterruptStatusFlags Average temperature threshold exceeded interrupt status of probe0.

kTMU_AverageTemperature0CriticalInterruptStatusFlags Average temperature critical threshold exceeded interrupt status of probe0.

kTMU_ImmediateTemperature1Interrupt1StatusFlags Immediate temperature threshold exceeded interrupt status of probe1.

kTMU_AverageTemperature1Interrupt1StatusFlags Average temperature threshold exceeded interrupt status of probe1.

kTMU_AverageTemperature1CriticalInterrupt1StatusFlags Average temperature critical threshold exceeded interrupt status of probe1.

26.5.3 enum _tmu_probe_select

Enumerator

kTMU_ProbeSelectMainProbe Select the main probe only.

kTMU_ProbeSelectRemoteProbe Select the remote probe(near A53) only.

kTMU_ProbeSelectBothProbes Select both 2 probes.

26.5.4 enum _tmu_average_low_pass_filter

Enumerator

kTMU_AverageLowPassFilter1_0 Average low pass filter = 1.

kTMU_AverageLowPassFilter0_5 Average low pass filter = 0.5.

kTMU_AverageLowPassFilter0_25 Average low pass filter = 0.25.

kTMU_AverageLowPassFilter0_125 Average low pass filter = 0.125.

26.6 Function Documentation

26.6.1 void TMU_Init (TMU_Type * *base*, const tmu_config_t * *config*)

Parameters

<i>base</i>	TMU peripheral base address.
<i>config</i>	Pointer to configuration structure. Refer to "tmu_config_t" structure.

26.6.2 void TMU_Deinit (TMU_Type * *base*)

Parameters

<i>base</i>	TMU peripheral base address.
-------------	------------------------------

26.6.3 void TMU_Enable (TMU_Type * *base*, bool *enable*)

Parameters

<i>base</i>	TMU peripheral base address.
<i>enable</i>	enable or disable TMU.

26.6.4 void TMU_GetDefaultConfig (tmu_config_t * *config*)

This function initializes the user configuration structure to default value. The default value are:

Example:

```
config.averageLPF = kTMU_AverageLowPassFilter0_5;
config.probeSelect = kTMU_ProbeSelectMainProbe;
config.thresholdConfig.immediateThresholdEnable = false;
config.thresholdConfig.immediateThresholdValue = DEMO_TMU_IMMEDIATE_THRESHOLD;
config.thresholdConfig.AverageThresholdEnable = true;
config.thresholdConfig.averageThresholdValue = DEMO_TMU_AVERAGE_THRESHOLD;
config.thresholdConfig.AverageCriticalThresholdEnable = false;
config.thresholdConfig.averageCriticalThresholdValue = DEMO_TMU_AVERAGE_CRITICAL_THRESHOLD;
```

Parameters

<i>config</i>	Pointer to TMU configuration structure.
---------------	---

26.6.5 static void TMU_EnableInterrupts (TMU_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	TMU peripheral base address.
<i>mask</i>	The interrupt mask. Refer to "_tmu_interrupt_enable" enumeration.

26.6.6 static void TMU_DisableInterrupts (TMU_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	TMU peripheral base address.
<i>mask</i>	The interrupt mask. Refer to "_tmu_interrupt_enable" enumeration.

26.6.7 static uint32_t TMU_GetInterruptStatusFlags (TMU_Type * *base*) [inline], [static]

Parameters

<i>base</i>	TMU peripheral base address.
-------------	------------------------------

Return values

<i>The</i>	current interrupt status.
------------	---------------------------

26.6.8 static void TMU_ClearInterruptStatusFlags (TMU_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	TMU peripheral base address.
<i>mask</i>	The mask of interrupt status flags. Refer to "_tmu_interrupt_status_flags" enumeration.

26.6.9 status_t TMU_GetImmediateTemperature (TMU_Type * *base*, tmu_probe_select_t *probe*, int8_t * *temperature*)

Parameters

<i>base</i>	TMU peripheral base address.
<i>probe</i>	probe selection, if select both 2 probes, return main probe temeperature by default. Refer to "tmu_probe_select_t" structure.

<i>temperature</i>	Last immediate temperature reading at site when V=1. besides, Bit-8 is sign bit: 1 means negative and 0 means positive.
--------------------	---

Return values

<i>get</i>	immediate temperature status.
------------	-------------------------------

26.6.10 **status_t TMU_GetAverageTemperature (TMU_Type * *base*, tmu_probe_select_t *probe*, int8_t * *temperature*)**

Parameters

<i>base</i>	TMU peripheral base address.
<i>probe</i>	probe selection, if select both 2 probes, return main probe temperature by default. Refer to "tmu_probe_select_t" structure.
<i>temperature</i>	Last average temperature reading at site; besides, Bit-8 is sign bit: 1 means negative and 0 means positive.

Return values

<i>get</i>	average temperature status.
------------	-----------------------------

26.6.11 **void TMU_UpdateHighTemperatureThreshold (TMU_Type * *base*, tmu_probe_select_t *probe*, const tmu_threshold_config_t * *thresholdConfig*)**

Parameters

<i>base</i>	TMU peripheral base address.
<i>probe</i>	probe selection, if select both 2 probes, set main probe path by default. Refer to "tmu_probe_select_t" structure.
<i>threshold-Config</i>	threshold configuration. Refer to "tmu_threshold_config_t" structure.

Chapter 27

WDOG: Watchdog Timer Driver

27.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Watchdog module (WDOG) of MCUXpresso SDK devices.

27.2 Typical use case

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/wdog

Data Structures

- struct `_wdog_work_mode`
Defines WDOG work mode. [More...](#)
- struct `_wdog_config`
Describes WDOG configuration structure. [More...](#)

Typedefs

- typedef struct `_wdog_work_mode` `wdog_work_mode_t`
Defines WDOG work mode.
- typedef struct `_wdog_config` `wdog_config_t`
Describes WDOG configuration structure.

Enumerations

- enum `_wdog_interrupt_enable` { `kWDOG_InterruptEnable` = `WDOG_WICR_WIE_MASK` }
WDOG interrupt configuration structure, default settings all disabled.
- enum `_wdog_status_flags` {
 `kWDOG_RunningFlag` = `WDOG_WCR_WDE_MASK`,
 `kWDOG_PowerOnResetFlag` = `WDOG_WRSR_POR_MASK`,
 `kWDOG_TimeoutResetFlag` = `WDOG_WRSR_TOUT_MASK`,
 `kWDOG_SoftwareResetFlag` = `WDOG_WRSR_SFTW_MASK`,
 `kWDOG_InterruptFlag` = `WDOG_WICR_WTIS_MASK` }
WDOG status flags.

Driver version

- #define `FSL_WDOG_DRIVER_VERSION` (`MAKE_VERSION(2, 2, 0)`)
Defines WDOG driver version.

Refresh sequence

- #define `WDOG_REFRESH_KEY` (0xAAAA5555U)

WDOG Initialization and De-initialization.

- void [WDOG_GetDefaultConfig](#) (wdog_config_t *config)
Initializes the WDOG configuration structure.
- void [WDOG_Init](#) (WDOG_Type *base, const wdog_config_t *config)
Initializes the WDOG.
- void [WDOG_Deinit](#) (WDOG_Type *base)
Shuts down the WDOG.
- static void [WDOG_Enable](#) (WDOG_Type *base)
Enables the WDOG module.
- static void [WDOG_Disable](#) (WDOG_Type *base)
Disables the WDOG module.
- static void [WDOG_TriggerSystemSoftwareReset](#) (WDOG_Type *base)
Trigger the system software reset.
- static void [WDOG_TriggerSoftwareSignal](#) (WDOG_Type *base)
Trigger an output assertion.
- static void [WDOG_EnableInterrupts](#) (WDOG_Type *base, uint16_t mask)
Enables the WDOG interrupt.
- uint16_t [WDOG_GetStatusFlags](#) (WDOG_Type *base)
Gets the WDOG all reset status flags.
- void [WDOG_ClearInterruptStatus](#) (WDOG_Type *base, uint16_t mask)
Clears the WDOG flag.
- static void [WDOG_SetTimeoutValue](#) (WDOG_Type *base, uint16_t timeoutCount)
Sets the WDOG timeout value.
- static void [WDOG_SetInterruptTimeoutValue](#) (WDOG_Type *base, uint16_t timeoutCount)
Sets the WDOG interrupt count timeout value.
- static void [WDOG_DisablePowerDownEnable](#) (WDOG_Type *base)
Disable the WDOG power down enable bit.
- void [WDOG_Refresh](#) (WDOG_Type *base)
Refreshes the WDOG timer.

27.3 Data Structure Documentation

27.3.1 struct _wdog_work_mode

Data Fields

- bool [enableWait](#)
If set to true, WDOG continues in wait mode.
- bool [enableStop](#)
If set to true, WDOG continues in stop mode.
- bool [enableDebug](#)
If set to true, WDOG continues in debug mode.

27.3.2 struct _wdog_config

Data Fields

- bool [enableWdog](#)

- Enables or disables WDOG.
- **wdog_work_mode_t workMode**
Configures WDOG work mode in debug stop and wait mode.
- bool **enableInterrupt**
Enables or disables WDOG interrupt.
- uint16_t **timeoutValue**
Timeout value.
- uint16_t **interruptTimeValue**
Interrupt count timeout value.
- bool **softwareResetExtension**
software reset extension
- bool **enablePowerDown**
power down enable bit
- bool **enableTimeOutAssert**
Enable WDOG_B timeout assertion.

Field Documentation

(1) **bool _wdog_config::enableTimeOutAssert**

27.4 Typedef Documentation

27.4.1 **typedef struct _wdog_work_mode wdog_work_mode_t**

27.4.2 **typedef struct _wdog_config wdog_config_t**

27.5 Enumeration Type Documentation

27.5.1 **enum _wdog_interrupt_enable**

This structure contains the settings for all of the WDOG interrupt configurations.

Enumerator

kWDOG_InterruptEnable WDOG timeout generates an interrupt before reset.

27.5.2 **enum _wdog_status_flags**

This structure contains the WDOG status flags for use in the WDOG functions.

Enumerator

kWDOG_RunningFlag Running flag, set when WDOG is enabled.

kWDOG_PowerOnResetFlag Power On flag, set when reset is the result of a powerOnReset.

kWDOG_TimeoutResetFlag Timeout flag, set when reset is the result of a timeout.

kWDOG_SoftwareResetFlag Software flag, set when reset is the result of a software.

kWDOG_InterruptFlag interrupt flag, whether interrupt has occurred or not

27.6 Function Documentation

27.6.1 void WDOG_GetDefaultConfig (wdog_config_t * *config*)

This function initializes the WDOG configuration structure to default values. The default values are as follows.

```
*     wdogConfig->enableWdog = true;
*     wdogConfig->workMode.enableWait = true;
*     wdogConfig->workMode.enableStop = true;
*     wdogConfig->workMode.enableDebug = true;
*     wdogConfig->enableInterrupt = false;
*     wdogConfig->enablePowerdown = false;
*     wdogConfig->resetExtension = flase;
*     wdogConfig->timeoutValue = 0xFFU;
*     wdogConfig->interruptTimeValue = 0x04u;
*
```

Parameters

<i>config</i>	Pointer to the WDOG configuration structure.
---------------	--

See Also

[wdog_config_t](#)

27.6.2 void WDOG_Init (WDOG_Type * *base*, const wdog_config_t * *config*)

This function initializes the WDOG. When called, the WDOG runs according to the configuration.
This is an example.

```
*     wdog_config_t config;
*     WDOG_GetDefaultConfig(&config);
*     config.timeoutValue = 0xffU;
*     config->interruptTimeValue = 0x04u;
*     WDOG_Init(wdog_base,&config);
*
```

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

<i>config</i>	The configuration of WDOG
---------------	---------------------------

27.6.3 void WDOG_Deinit (WDOG_Type * *base*)

This function shuts down the WDOG. Watchdog Enable bit is a write one once only bit. It is not possible to clear this bit by a software write, once the bit is set. This bit(WDE) can be set/reset only in debug mode(exception).

27.6.4 static void WDOG_Enable (WDOG_Type * *base*) [inline], [static]

This function writes a value into the WDOG_WCR register to enable the WDOG. This is a write one once only bit. It is not possible to clear this bit by a software write, once the bit is set. only debug mode exception.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

27.6.5 static void WDOG_Disable (WDOG_Type * *base*) [inline], [static]

This function writes a value into the WDOG_WCR register to disable the WDOG. This is a write one once only bit. It is not possible to clear this bit by a software write,once the bit is set. only debug mode exception

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

27.6.6 static void WDOG_TriggerSystemSoftwareReset (WDOG_Type * *base*) [inline], [static]

This function will write to the WCR[SRS] bit to trigger a software system reset. This bit will automatically resets to "1" after it has been asserted to "0". Note: Calling this API will reset the system right now, please using it with more attention.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

27.6.7 static void WDOG_TriggerSoftwareSignal (**WDOG_Type** * *base*) [inline], [static]

This function will write to the WCR[WDA] bit to trigger WDOG_B signal assertion. The WDOG_B signal can be routed to external pin of the chip, the output pin will turn to assertion along with WDOG_B signal. Note: The WDOG_B signal will remain assert until a power on reset occurred, so, please take more attention while calling it.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

27.6.8 static void WDOG_EnableInterrupts (**WDOG_Type** * *base*, **uint16_t** *mask*) [inline], [static]

This bit is a write once only bit. Once the software does a write access to this bit, it will get locked and cannot be reprogrammed until the next system reset assertion

Parameters

<i>base</i>	WDOG peripheral base address
<i>mask</i>	The interrupts to enable The parameter can be combination of the following source if defined. <ul style="list-style-type: none">• kWDOG_InterruptEnable

27.6.9 **uint16_t** WDOG_GetStatusFlags (**WDOG_Type** * *base*)

This function gets all reset status flags.

```
* uint16_t status;
* status = WDOG\_GetStatusFlags (wdog_base);
*
```

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

Returns

State of the status flag: asserted (true) or not-asserted (false).

See Also

[_wdog_status_flags](#)

- true: a related status flag has been set.
- false: a related status flag is not set.

27.6.10 void WDOG_ClearInterruptStatus (**WDOG_Type** * *base*, **uint16_t** *mask*)

This function clears the WDOG status flag.

This is an example for clearing the interrupt flag.

```
*     WDOG_ClearStatusFlags (wdog_base, KWDOG_InterruptFlag);
*
```

Parameters

<i>base</i>	WDOG peripheral base address
<i>mask</i>	The status flags to clear. The parameter could be any combination of the following values. kWDOG_TimeoutFlag

27.6.11 static void WDOG_SetTimeoutValue (**WDOG_Type** * *base*, **uint16_t** *timeoutCount*) [inline], [static]

This function sets the timeout value. This function writes a value into WCR registers. The time-out value can be written at any point of time but it is loaded to the counter at the time when WDOG is enabled or after the service routine has been performed.

Parameters

<i>base</i>	WDOG peripheral base address
<i>timeoutCount</i>	WDOG timeout value; count of WDOG clock tick.

27.6.12 static void WDOG_SetInterruptTimeoutValue (WDOG_Type * *base*, uint16_t *timeoutCount*) [inline], [static]

This function sets the interrupt count timeout value. This function writes a value into WIC registers which are write-once. This field is write once only. Once the software does a write access to this field, it will get locked and cannot be reprogrammed until the next system reset assertion.

Parameters

<i>base</i>	WDOG peripheral base address
<i>timeoutCount</i>	WDOG timeout value; count of WDOG clock tick.

27.6.13 static void WDOG_DisablePowerDownEnable (WDOG_Type * *base*) [inline], [static]

This function disable the WDOG power down enable(PDE). This function writes a value into WMCR registers which are write-once. This field is write once only. Once software sets this bit it cannot be reset until the next system reset.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

27.6.14 void WDOG_Refresh (WDOG_Type * *base*)

This function feeds the WDOG. This function should be called before the WDOG timer is in timeout. Otherwise, a reset is asserted.

Parameters

<i>base</i>	WDOG peripheral base address
-------------	------------------------------

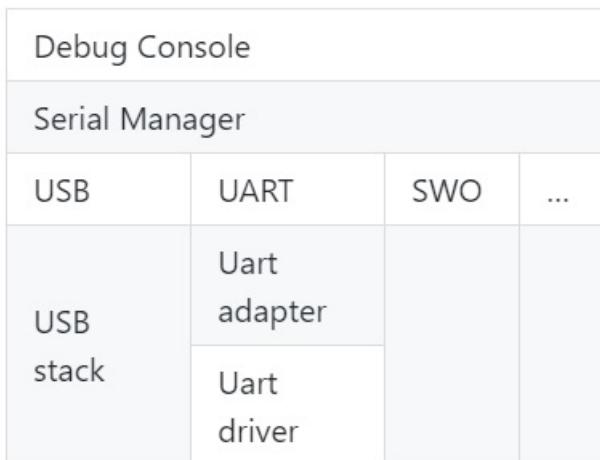
Chapter 28

Debug Console

28.1 Overview

This chapter describes the programming interface of the debug console driver.

The debug console enables debug log messages to be output via the specified peripheral with frequency of the peripheral source clock and base address at the specified baud rate. Additionally, it provides input and output functions to scan and print formatted data. The below picture shows the layout of debug console.



Debug console overview

28.2 Function groups

28.2.1 Initialization

To initialize the debug console, call the [DbgConsole_Init\(\)](#) function with these parameters. This function automatically enables the module and the clock.

```
status_t DbgConsole_Init(uint8_t instance, uint32_t baudRate,  
                         serial_port_type_t device, uint32_t clkSrcFreq);
```

Select the supported debug console hardware device type, such as

```
typedef enum _serial_port_type  
{  
    kSerialPort_Uart = 1U,  
    kSerialPort_UsbCdc,  
    kSerialPort_Swo,  
} serial_port_type_t;
```

After the initialization is successful, stdout and stdin are connected to the selected peripheral. This example shows how to call the [DbgConsole_Init\(\)](#) given the user configuration structure.

```
DbgConsole_Init(BOARD_DEBUG_UART_INSTANCE, BOARD_DEBUG_UART_BAUDRATE, BOARD_DEBUG_UART_TYPE,
                 BOARD_DEBUG_UART_CLK_FREQ);
```

28.2.2 Advanced Feature

The debug console provides input and output functions to scan and print formatted data.

- Support a format specifier for PRINTF following this prototype " %[flags][width][.precision][length]specifier", which is explained below

flags	Description
-	Left-justified within the given field width. Right-justified is the default.
+	Forces to precede the result with a plus or minus sign (+ or -) even for positive numbers. By default, only negative numbers are preceded with a - sign.
(space)	If no sign is written, a blank space is inserted before the value.
#	Used with o, x, or X specifiers the value is preceded with 0, 0x, or 0X respectively for values other than zero. Used with e, E and f, it forces the written output to contain a decimal point even if no digits would follow. By default, if no digits follow, no decimal point is written. Used with g or G the result is the same as with e or E but trailing zeros are not removed.
0	Left-pads the number with zeroes (0) instead of spaces, where padding is specified (see width sub-specifier).

Width	Description
(number)	A minimum number of characters to be printed. If the value to be printed is shorter than this number, the result is padded with blank spaces. The value is not truncated even if the result is larger.
*	The width is not specified in the format string, but as an additional integer value argument preceding the argument that has to be formatted.

.precision	Description
.number	For integer specifiers (d, i, o, u, x, X) precision specifies the minimum number of digits to be written. If the value to be written is shorter than this number, the result is padded with leading zeros. The value is not truncated even if the result is longer. A precision of 0 means that no character is written for the value 0. For e, E, and f specifiers this is the number of digits to be printed after the decimal point. For g and G specifiers This is the maximum number of significant digits to be printed. For s this is the maximum number of characters to be printed. By default, all characters are printed until the ending null character is encountered. For c type it has no effect. When no precision is specified, the default is 1. If the period is specified without an explicit value for precision, 0 is assumed.
.*	The precision is not specified in the format string, but as an additional integer value argument preceding the argument that has to be formatted.

length	Description
Do not support	

specifier	Description
d or i	Signed decimal integer
f	Decimal floating point
F	Decimal floating point capital letters
x	Unsigned hexadecimal integer
X	Unsigned hexadecimal integer capital letters
o	Signed octal
b	Binary value
p	Pointer address
u	Unsigned decimal integer
c	Character
s	String of characters
n	Nothing printed

specifier	Description
-----------	-------------

- Support a format specifier for SCANF following this prototype " %[*][width][length]specifier", which is explained below

*	Description
	An optional starting asterisk indicates that the data is to be read from the stream but ignored. In other words, it is not stored in the corresponding argument.

width	Description
	This specifies the maximum number of characters to be read in the current reading operation.

length	Description
hh	The argument is interpreted as a signed character or unsigned character (only applies to integer specifiers: i, d, o, u, x, and X).
h	The argument is interpreted as a short integer or unsigned short integer (only applies to integer specifiers: i, d, o, u, x, and X).
l	The argument is interpreted as a long integer or unsigned long integer for integer specifiers (i, d, o, u, x, and X) and as a wide character or wide character string for specifiers c and s.
ll	The argument is interpreted as a long long integer or unsigned long long integer for integer specifiers (i, d, o, u, x, and X) and as a wide character or wide character string for specifiers c and s.
L	The argument is interpreted as a long double (only applies to floating point specifiers: e, E, f, g, and G).
j or z or t	Not supported

specifier	Qualifying Input	Type of argument
c	Single character: Reads the next character. If a width different from 1 is specified, the function reads width characters and stores them in the successive locations of the array passed as argument. No null character is appended at the end.	char *
i	Integer: : Number optionally preceded with a + or - sign	int *
d	Decimal integer: Number optionally preceded with a + or - sign	int *
a, A, e, E, f, F, g, G	Floating point: Decimal number containing a decimal point, optionally preceded by a + or - sign and optionally followed by the e or E character and a decimal number. Two examples of valid entries are -732.103 and 7.12e4	float *
o	Octal Integer:	int *
s	String of characters. This reads subsequent characters until a white space is found (white space characters are considered to be blank, newline, and tab).	char *
u	Unsigned decimal integer.	unsigned int *

The debug console has its own printf/scanf/putchar/getchar functions which are defined in the header file.

```
int DbgConsole_Printf(const char *fmt_s, ...);
int DbgConsole_Putchar(int ch);
int DbgConsole_Scanf(char *fmt_ptr, ...);
int DbgConsole_Getchar(void);
```

This utility supports selecting toolchain's printf/scanf or the MCUXpresso SDK printf/scanf.

```
#if SDK_DEBUGCONSOLE == DEBUGCONSOLE_DISABLE /* Disable debug console */
#define PRINTF
#define SCANF
#define PUTCHAR
#define GETCHAR
#elif SDK_DEBUGCONSOLE == DEBUGCONSOLE_REDIRECT_TO_SDK /* Select printf, scanf, putchar, getchar of SDK
```

```

version. */
#define PRINTF DbgConsole_Printf
#define SCANF DbgConsole_Scanf
#define PUTCHAR DbgConsole_Putchar
#define GETCHAR DbgConsole_Getchar
#elif SDK_DEBUGCONSOLE == DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN /* Select printf, scanf, putchar, getchar of
toolchain. */
#define PRINTF printf
#define SCANF scanf
#define PUTCHAR putchar
#define GETCHAR getchar
#endif /* SDK_DEBUGCONSOLE */

```

28.2.3 SDK_DEBUGCONSOLE and SDK_DEBUGCONSOLE_UART

There are two macros `SDK_DEBUGCONSOLE` and `SDK_DEBUGCONSOLE_UART` added to configure `PRINTF` and low level output peripheral.

- The macro `SDK_DEBUGCONSOLE` is used for frontend. Whether debug console redirect to toolchain or SDK or disabled, it decides which is the frontend of the debug console, Tool chain or SDK. The function can be set by the macro `SDK_DEBUGCONSOLE`.
- The macro `SDK_DEBUGCONSOLE_UART` is used for backend. It is used to decide whether provide low level IO implementation to toolchain printf and scanf. For example, within MCUXpresso, if the macro `SDK_DEBUGCONSOLE_UART` is defined, `_sys_write` and `_sys_read` will be used when `_REDLIB_` is defined; `_write` and `_read` will be used in other cases. The macro does not specifically refer to the peripheral "UART". It refers to the external peripheral similar to UART, like as USB CDC, UART, SWO, etc. So if the macro `SDK_DEBUGCONSOLE_UART` is not defined when tool-chain printf is calling, the semihosting will be used.

The following matrix show the effects of `SDK_DEBUGCONSOLE` and `SDK_DEBUGCONSOLE_UART` on `PRINTF` and `printf`. The green mark is the default setting of the debug console.

<code>SDK_DEBUGCONSOLE</code>	<code>SDK_DEBUGCONSOLE_UART</code>	<code>PRINTF</code>	<code>printf</code>
<code>DEBUGCONSOLE_- REDIRECT_TO_SDK</code>	defined	Low level peripheral*	Low level peripheral
<code>DEBUGCONSOLE_- REDIRECT_TO_SDK</code>	undefined	Low level peripheral*	semihost
<code>DEBUGCONSOLE_- REDIRECT_TO_TO- OLCHAIN</code>	defined	Low level peripheral*	Low level peripheral
<code>DEBUGCONSOLE_- REDIRECT_TO_TO- OLCHAIN</code>	undefined	semihost	semihost
<code>DEBUGCONSOLE_- DISABLE</code>	defined	No output	Low level peripheral
<code>DEBUGCONSOLE_- DISABLE</code>	undefined	No output	semihost

SDK_DEBUGCONSOLE	SDK_DEBUGCONSOLE_UART	PRINTF	printf
-------------------------	------------------------------	---------------	---------------

* the **low level peripheral** could be USB CDC, UART, or SWO, and so on.

28.3 Typical use case

Some examples use the PUTCHAR & GETCHAR function

```
ch = GETCHAR();
PUTCHAR(ch);
```

Some examples use the PRINTF function

Statement prints the string format.

```
PRINTF("%s %s\r\n", "Hello", "world!");
```

Statement prints the hexadecimal format/

```
PRINTF("0x%02X hexadecimal number equivalents 255", 255);
```

Statement prints the decimal floating point and unsigned decimal.

```
PRINTF("Execution timer: %s\n\rTime: %u ticks %2.5f milliseconds\n\rDONE\n\r", "1 day", 86400, 86.4);
```

Some examples use the SCANF function

```
PRINTF("Enter a decimal number: ");
SCANF("%d", &i);
PRINTF("\r\nYou have entered %d.\r\n", i, i);
PRINTF("Enter a hexadecimal number: ");
SCANF("%x", &i);
PRINTF("\r\nYou have entered 0x%X (%d).\r\n", i, i);
```

Print out failure messages using MCUXpresso SDK __assert_func:

```
void __assert_func(const char *file, int line, const char *func, const char *failedExpr)
{
    PRINTF("ASSERT ERROR \" %s \": file \"%s\" Line \"%d\" function name \"%s\" \n", failedExpr, file
           , line, func);
    for (;;) {
    }
}
```

Note:

To use 'printf' and 'scanf' for GNUMC Base, add file '**fsl_sbrk.c**' in path: ..\{package}\devices\{subset}\utilities\fsl_sbrk.c to your project.

Modules

- [SWO](#)
- [Semihosting](#)
- [debug console configuration](#)

The configuration is used for debug console only.

Macros

- #define [DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN](#) 0U
Definition select redirect toolchain printf, scanf to uart or not.
- #define [DEBUGCONSOLE_REDIRECT_TO_SDK](#) 1U
Select SDK version printf, scanf.
- #define [DEBUGCONSOLE_DISABLE](#) 2U
Disable debugconsole function.
- #define [SDK_DEBUGCONSOLE DEBUGCONSOLE_REDIRECT_TO_SDK](#)
Definition to select sdk or toolchain printf, scanf.
- #define [PRINTF DbgConsole_Printf](#)
Definition to select redirect toolchain printf, scanf to uart or not.

Variables

- [serial_handle_t g_serialHandle](#)
serial manager handle

Initialization

- [status_t DbgConsole_Init](#) (uint8_t instance, uint32_t baudRate, [serial_port_type_t](#) device, uint32_t clkSrcFreq)
Initializes the peripheral used for debug messages.
- [status_t DbgConsole_Deinit](#) (void)
De-initializes the peripheral used for debug messages.
- [status_t DbgConsole_EnterLowpower](#) (void)
Prepares to enter low power consumption.
- [status_t DbgConsole_ExitLowpower](#) (void)
Restores from low power consumption.
- int [DbgConsole_Printf](#) (const char *fmt_s,...)
Writes formatted output to the standard output stream.
- int [DbgConsole_Vprintf](#) (const char *fmt_s, va_list formatStringArg)
Writes formatted output to the standard output stream.
- int [DbgConsole_Putchar](#) (int ch)
Writes a character to stdout.
- int [DbgConsole_Scanf](#) (char *fmt_s,...)
Reads formatted data from the standard input stream.
- int [DbgConsole_Getchar](#) (void)

- *Reads a character from standard input.*
• int [DbgConsole_BlockingPrintf](#) (const char *fmt_s,...)
Writes formatted output to the standard output stream with the blocking mode.
- int [DbgConsole_BlockingVprintf](#) (const char *fmt_s, va_list formatStringArg)
Writes formatted output to the standard output stream with the blocking mode.
- status_t [DbgConsole_Flush](#) (void)
Debug console flush.
- status_t [DbgConsole_TryGetchar](#) (char *ch)
Debug console try to get char This function provides a API which will not block current task, if character is available return it, otherwise return fail.

28.4 Macro Definition Documentation

28.4.1 #define DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN 0U

Select toolchain printf and scanf.

28.4.2 #define DEBUGCONSOLE_REDIRECT_TO_SDK 1U

28.4.3 #define DEBUGCONSOLE_DISABLE 2U

28.4.4 #define SDK_DEBUGCONSOLE DEBUGCONSOLE_REDIRECT_TO_SDK

The macro only support to be redefined in project setting.

28.4.5 #define PRINTF DbgConsole_Printf

if SDK_DEBUGCONSOLE defined to 0,it represents select toolchain printf, scanf. if SDK_DEBUGCONSOLE defined to 1,it represents select SDK version printf, scanf. if SDK_DEBUGCONSOLE defined to 2,it represents disable debugconsole function.

28.5 Function Documentation

28.5.1 status_t DbgConsole_Init (uint8_t instance, uint32_t baudRate, serial_port_type_t device, uint32_t clkSrcFreq)

Call this function to enable debug log messages to be output via the specified peripheral initialized by the serial manager module. After this function has returned, stdout and stdin are connected to the selected peripheral.

Parameters

<i>instance</i>	The instance of the module. If the device is kSerialPort_Uart, the instance is UART peripheral instance. The UART hardware peripheral type is determined by UART adapter. For example, if the instance is 1, if the lpuart_adapter.c is added to the current project, the UART peripheral is LPUART1. If the uart_adapter.c is added to the current project, the UART peripheral is UART1.
<i>baudRate</i>	The desired baud rate in bits per second.
<i>device</i>	Low level device type for the debug console, can be one of the following. <ul style="list-style-type: none"> • kSerialPort_Uart, • kSerialPort_UsbCdc
<i>clkSrcFreq</i>	Frequency of peripheral source clock.

Returns

Indicates whether initialization was successful or not.

Return values

<i>kStatus_Success</i>	Execution successfully
------------------------	------------------------

28.5.2 status_t DbgConsole_Deinit (void)

Call this function to disable debug log messages to be output via the specified peripheral initialized by the serial manager module.

Returns

Indicates whether de-initialization was successful or not.

28.5.3 status_t DbgConsole_EnterLowpower (void)

This function is used to prepare to enter low power consumption.

Returns

Indicates whether de-initialization was successful or not.

28.5.4 status_t DbgConsole_ExitLowpower (void)

This function is used to restore from low power consumption.

Returns

Indicates whether de-initialization was successful or not.

28.5.5 int DbgConsole_Printf (const char * *fmt_s*, ...)

Call this function to write a formatted output to the standard output stream.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of characters printed or a negative value if an error occurs.

28.5.6 int DbgConsole_Vprintf (const char * *fmt_s*, va_list *formatStringArg*)

Call this function to write a formatted output to the standard output stream.

Parameters

<i>fmt_s</i>	Format control string.
<i>formatString-Arg</i>	Format arguments.

Returns

Returns the number of characters printed or a negative value if an error occurs.

28.5.7 int DbgConsole_Putchar (int *ch*)

Call this function to write a character to stdout.

Parameters

<i>ch</i>	Character to be written.
-----------	--------------------------

Returns

Returns the character written.

28.5.8 int DbgConsole_Scanf (char * *fmt_s*, ...)

Call this function to read formatted data from the standard input stream.

Note

Due the limitation in the BM OSA environment (CPU is blocked in the function, other tasks will not be scheduled), the function cannot be used when the DEBUG_CONSOLE_TRANSFER_NON_B-LOCKING is set in the BM OSA environment. And an error is returned when the function called in this case. The suggestion is that polling the non-blocking function DbgConsole_TryGetchar to get the input char.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of fields successfully converted and assigned.

28.5.9 int DbgConsole_Getchar (void)

Call this function to read a character from standard input.

Note

Due the limitation in the BM OSA environment (CPU is blocked in the function, other tasks will not be scheduled), the function cannot be used when the DEBUG_CONSOLE_TRANSFER_NON_B-LOCKING is set in the BM OSA environment. And an error is returned when the function called in this case. The suggestion is that polling the non-blocking function DbgConsole_TryGetchar to get the input char.

Returns

Returns the character read.

28.5.10 int DbgConsole_BlockingPrintf (const char * *fmt_s*, ...)

Call this function to write a formatted output to the standard output stream with the blocking mode. The function will send data with blocking mode no matter the DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set or not. The function could be used in system ISR mode with DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of characters printed or a negative value if an error occurs.

28.5.11 int DbgConsole_BlockingVprintf (const char * *fmt_s*, va_list *formatStringArg*)

Call this function to write a formatted output to the standard output stream with the blocking mode. The function will send data with blocking mode no matter the DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set or not. The function could be used in system ISR mode with DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set.

Parameters

<i>fmt_s</i>	Format control string.
<i>formatString-Arg</i>	Format arguments.

Returns

Returns the number of characters printed or a negative value if an error occurs.

28.5.12 status_t DbgConsole_Flush (void)

Call this function to wait the tx buffer empty. If interrupt transfer is using, make sure the global IRQ is enable before call this function This function should be called when 1, before enter power down mode 2, log is required to print to terminal immediately

Returns

Indicates whether wait idle was successful or not.

28.5.13 **status_t DbgConsole_TryGetchar (char * *ch*)**

Parameters

<i>ch</i>	the address of char to receive
-----------	--------------------------------

Returns

Indicates get char was successful or not.

28.6 debug console configuration

The configuration is used for debug console only.

28.6.1 Overview

Please note, it is not sued for debug console lite.

Macros

- `#define DEBUG_CONSOLE_TRANSMIT_BUFFER_LEN (512U)`
If Non-blocking mode is needed, please define it at project setting, otherwise blocking mode is the default transfer mode.
- `#define DEBUG_CONSOLE_RECEIVE_BUFFER_LEN (1024U)`
define the receive buffer length which is used to store the user input, buffer is enabled automatically when non-blocking transfer is using, This value will affect the RAM's ultilization, should be set per paltform's capability and software requirement.
- `#define DEBUG_CONSOLE_TX_RELIABLE_ENABLE (1U)`
Whether enable the reliable TX function If the macro is zero, the reliable TX function of the debug console is disabled.
- `#define DEBUG_CONSOLE_RX_ENABLE (1U)`
Whether enable the RX function If the macro is zero, the receive function of the debug console is disabled.
- `#define DEBUG_CONSOLE_PRINTF_MAX_LOG_LEN (128U)`
define the MAX log length debug console support , that is when you call printf("log", x);, the log length can not bigger than this value.
- `#define DEBUG_CONSOLE_SCANF_MAX_LOG_LEN (20U)`
define the buffer support buffer scanf log length, that is when you call scanf("log", &x);, the log length can not bigger than this value.
- `#define DEBUG_CONSOLE_SYNCHRONIZATION_BM 0`
Debug console synchronization User should not change these macro for synchronization mode, but add the corresponding synchronization mechanism per different software environment.
- `#define DEBUG_CONSOLE_SYNCHRONIZATION_FREERTOS 1`
synchronization for freertos software
- `#define DEBUG_CONSOLE_SYNCHRONIZATION_MODE DEBUG_CONSOLE_SYNCHRONIZATION_BM`
RTOS synchronization mechanism disable If not defined, default is enable, to avoid multitask log print mess.
- `#define DEBUG_CONSOLE_ENABLE_ECHO_FUNCTION 0`
echo function support If you want to use the echo function,please define DEBUG_CONSOLE_ENABLE_ECHO at your project setting.
- `#define BOARD_USE_VIRTUALCOM 0U`
Definition to select virtual com(USB CDC) as the debug console.

28.6.2 Macro Definition Documentation

28.6.2.1 #define DEBUG_CONSOLE_TRANSMIT_BUFFER_LEN (512U)

Warning: If you want to use non-blocking transfer, please make sure the corresponding IO interrupt is enable, otherwise there is no output. And non-blocking is combine with buffer, no matter bare-metal or rtos. Below shows how to configure in your project if you want to use non-blocking mode. For IAR, right click project and select "Options", define it in "C/C++ Compiler->Preprocessor->Defined symbols". For KEIL, click "Options for Target...", define it in "C/C++->Preprocessor Symbols->Define". For ARM-GCC, open CmakeLists.txt and add the following lines, "SET(CMAKE_C_FLAGS_DEBUG "\${CMAKE_C_FLAGS_DEBUG} -DDEBUG_CONSOLE_TRANSFER_NON_BLOCKING")" for debug target. "SET(CMAKE_C_FLAGS_RELEASE "\${CMAKE_C_FLAGS_RELEASE} -DDEBUG_CONSOLE_TRANSFER_NON_BLOCKING")" for release target. For MCUXpresso, right click project and select "Properties", define it in "C/C++ Build->Settings->MCU C Complier->Preprocessor".

define the transmit buffer length which is used to store the multi task log, buffer is enabled automatically when non-blocking transfer is using, This value will affect the RAM's utilization, should be set per platform's capability and software requirement. If it is configured too small, log maybe missed , because the log will not be buffered if the buffer is full, and the print will return immediately with -1. And this value should be multiple of 4 to meet memory alignment.

28.6.2.2 #define DEBUG_CONSOLE_RECEIVE_BUFFER_LEN (1024U)

If it is configured too small, log maybe missed, because buffer will be overwritten if buffer is too small. And this value should be multiple of 4 to meet memory alignment.

28.6.2.3 #define DEBUG_CONSOLE_TX_RELIABLE_ENABLE (1U)

When the macro is zero, the string of PRINTF will be thrown away after the transmit buffer is full.

28.6.2.4 #define DEBUG_CONSOLE_PRINTF_MAX_LOG_LEN (128U)

This macro decide the local log buffer length, the buffer locate at stack, the stack maybe overflow if the buffer is too big and current task stack size not big enough.

28.6.2.5 #define DEBUG_CONSOLE_SCANF_MAX_LOG_LEN (20U)

As same as the DEBUG_CONSOLE_BUFFER_PRINTF_MAX_LOG_LEN.

28.6.2.6 #define DEBUG_CONSOLE_SYNCHRONIZATION_BM 0

Such as, if another RTOS is used, add: #define DEBUG_CONSOLE_SYNCHRONIZATION_XXXX 3 in this configuration file and implement the synchronization in fsl.log.c.

synchronization for baremetal software

28.6.2.7 #define DEBUG_CONSOLE_SYNCHRONIZATION_MODE DEBUG_CONSOLE_SYNCHRONIZATION_BM

If other RTOS is used, you can implement the RTOS's specific synchronization mechanism in fsl.log.c If synchronization is disabled, log maybe messed on terminal.

28.6.2.8 #define BOARD_USE_VIRTUALCOM 0U

28.7 Semihosting

Semihosting is a mechanism for ARM targets to communicate input/output requests from application code to a host computer running a debugger. This mechanism can be used, for example, to enable functions in the C library, such as printf() and scanf(), to use the screen and keyboard of the host rather than having a screen and keyboard on the target system.

28.7.1 Guide Semihosting for IAR

NOTE: After the setting both "printf" and "scanf" are available for debugging, if you want use PRINTF with semihosting, please make sure the SDK_DEBUGCONSOLE is DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN.

Step 1: Setting up the environment

1. To set debugger options, choose Project>Options. In the Debugger category, click the Setup tab.
2. Select Run to main and click OK. This ensures that the debug session starts by running the main function.
3. The project is now ready to be built.

Step 2: Building the project

1. Compile and link the project by choosing Project>Make or F7.
2. Alternatively, click the Make button on the tool bar. The Make command compiles and links those files that have been modified.

Step 3: Starting semihosting

1. Choose "Semihosting_IAR" project -> "Options" -> "Debugger" -> "J-Link/J-Trace".
2. Choose tab "J-Link/J-Trace" -> "Connection" tab -> "SWD".
3. Choose tab "General Options" -> "Library Configurations", select Semihosted, select Via semihosting. Please Make sure the SDK_DEBUGCONSOLE_UART is not defined in project settings.
4. Start the project by choosing Project>Download and Debug.
5. Choose View>Terminal I/O to display the output from the I/O operations.

28.7.2 Guide Semihosting for Keil µVision

NOTE: Semihosting is not support by MDK-ARM, use the retargeting functionality of MDK-ARM instead.

28.7.3 Guide Semihosting for MCUXpresso IDE

Step 1: Setting up the environment

1. To set debugger options, choose Project>Properties. select the setting category.
2. Select Tool Settings, unfold MCU C Compile.
3. Select Preprocessor item.
4. Set SDK_DEBUGCONSOLE=0, if set SDK_DEBUGCONSOLE=1, the log will be redirect to the UART.

Step 2: Building the project

1. Compile and link the project.

Step 3: Starting semihosting

1. Download and debug the project.
2. When the project runs successfully, the result can be seen in the Console window.

Semihosting can also be selected through the "Quick settings" menu in the left bottom window, Quick settings->SDK Debug Console->Semihost console.

28.7.4 Guide Semihosting for ARMGCC

Step 1: Setting up the environment

1. Turn on "J-LINK GDB Server" -> Select suitable "Target device" -> "OK".
2. Turn on "PuTTY". Set up as follows.
 - "Host Name (or IP address)" : localhost
 - "Port" :2333
 - "Connection type" : Telet.
 - Click "Open".
3. Increase "Heap/Stack" for GCC to 0x2000:

Add to "CMakeLists.txt"

```
SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE} --defsym=__stack_size__=0x2000")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --defsym=__stack_size__=0x2000")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --defsym=__heap_size__=0x2000")
SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE} --defsym=__heap_size__=0x2000")
```

Step 2: Building the project

1. Change "CMakeLists.txt":

```
Change "SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE} -specs=nano.specs")"
to "SET(CMAKE_EXE_LINKER_FLAGS_RELEASE "${CMAKE_EXE_LINKER_FLAGS_RELEASE} -specs=rdimon.specs")"
```

Replace paragraph

```
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -fno-common")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -ffunction-sections")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -fdata-sections")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -ffreestanding")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -fno-builtin")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -mthumb")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -mapcs")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --gc-sections")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -static")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -z")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} -Xlinker")
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} muldefs")
```

To

```
SET(CMAKE_EXE_LINKER_FLAGS_DEBUG "${CMAKE_EXE_LINKER_FLAGS_DEBUG} --specs=rdimon.specs ")
```

Remove

```
target_link_libraries(semihosting_ARMGCC.elf debug nosys)
```

2. Run "build_debug.bat" to build project

Step 3: Starting semihosting

1. Download the image and set as follows.

```
cd D:\mcu-sdk-2.0-origin\boards\twrk64f120m\driver_examples\semihosting\armgcc\debug
d:
C:\PROGRA~2\GNUTOO~1\4BD65~1.920\bin\arm-none-eabi-gdb.exe
target remote localhost:2331
monitor reset
monitor semihosting enable
monitor semihosting thumbSWI 0xAB
monitor semihosting IOClient 1
monitor flash device = MK64FN1M0xxxx12
load semihosting_ARMGCC.elf
monitor reg pc = (0x00000004)
monitor reg sp = (0x00000000)
continue
```

2. After the setting, press "enter". The PuTTY window now shows the printf() output.

28.8 SWO

Serial wire output is a mechanism for ARM targets to output signal from core through a single pin. Some IDEs also support SWO, such IAR and KEIL, both input and output are supported, see below for details.

28.8.1 Guide SWO for SDK

NOTE: After the setting both "printf" and "PRINTF" are available for debugging, JlinkSWOViewer can be used to capture the output log.

Step 1: Setting up the environment

1. Define SERIAL_PORT_TYPE_SWO in your project settings.
2. Prepare code, the port and baudrate can be decided by application, clkSrcFreq should be mcu core clock frequency:

```
DbgConsole_Init(instance, baudRate, kSerialPort_Swo, clkSrcFreq);
```

3. Use PRINTF or printf to print some thing in application.

Step 2: Building the project

Step 3: Download and run project

28.8.1.1 Guide SWO for IAR

NOTE: After the setting both "printf" and "scanf" are available for debugging.

Step 1: Setting up the environment

1. Choose project -> "Options" -> "Debugger" -> "J-Link/J-Trace".
2. Choose tab "J-Link/J-Trace" -> "Connection" tab -> "SWD".
3. Choose tab "General Options" -> "Library Configurations", select Semihosted, select Via SWO.
4. To configure the hardware's generation of trace data, click the SWO Configuration button available in the SWO Configuration dialog box. The value of the CPU clock option must reflect the frequency of the CPU clock speed at which the application executes. Note also that the settings you make are preserved between debug sessions. To decrease the amount of transmissions on the communication channel, you can disable the Timestamp option. Alternatively, set a lower rate for PC Sampling or use a higher SWO clock frequency.
5. Open the SWO Trace window from J-LINK, and click the Activate button to enable trace data collection.
6. There are three cases for this SDK_DEBUGCONSOLE_UART whether or not defined. a: if use uppercase PRINTF to output log, The SDK_DEBUGCONSOLE_UART defined or not defined will not effect debug function. b: if use lowercase printf to output log and defined SDK_DEBUGCONSOLE_UART to zero, then debug function ok. c: if use lowercase printf to output log and defined SDK_DEBUGCONSOLE_UART to one, then debug function ok.

NOTE: Case a or c only apply at example which enable swo function, the SDK_DEBUGCONSOLE_UART definition in fsl_debug_console.h. For case a and c, Do and not do the above third step will be not affect function.

1. Start the project by choosing Project>Download and Debug.

Step 2: Building the project

Step 3: Starting swo

1. Download and debug application.
2. Choose View -> Terminal I/O to display the output from the I/O operations.
3. Run application.

28.8.2 Guide SWO for Keil µVision

NOTE: After the setting both "printf" and "scanf" are available for debugging.

Step 1: Setting up the environment

1. There are three cases for this SDK_DEBUGCONSOLE_UART whether or not defined. a: if use uppercase PRINTF to output log, the SDK_DEBUGCONSOLE_UART definition does not affect the functionality and skip the second step directly. b: if use lowercase printf to output log and defined SDK_DEBUGCONSOLE_UART to zero, then start the second step. c: if use lowercase printf to output log and defined SDK_DEBUGCONSOLE_UART to one, then skip the second step directly.

NOTE: Case a or c only apply at example which enable swo function, the SDK_DEBUGCONSOLE_UART definition in fsl_debug_console.h.

1. In menu bar, click Management Run-Time Environment icon, select Compiler, unfold I/O, enable STDERR/STDIN/STDOUT and set the variant to ITM.
2. Open Project>Options for target or using Alt+F7 or click.
3. Select “Debug” tab, select “J-Link/J-Trace Cortex” and click “Setting button”.
4. Select “Debug” tab and choose Port:SW, then select “Trace” tab, choose “Enable” and click OK, please make sure the Core clock is set correctly, enable autodetect max SWO clk, enable ITM Stimulus Ports 0.

Step 3: Building the project

1. Compile and link the project by choosing Project>Build Target or using F7.

Step 4: Run the project

1. Choose “Debug” on menu bar or Ctrl F5.
2. In menu bar, choose “Serial Window” and click to “Debug (printf) Viewer”.
3. Run line by line to see result in Console Window.

28.8.3 Guide SWO for MCUXpresso IDE

NOTE: MCUX support SWO for LPC-Link2 debug probe only.

28.8.4 Guide SWO for ARMGCC

NOTE: ARMGCC has no library support SWO.

Chapter 29

CODEC Driver

29.1 Overview

The MCUXpresso SDK provides a codec abstraction driver interface to access codec register.

Modules

- [CODEC Common Driver](#)
- [CODEC I2C Driver](#)
- [WM8960 Driver](#)

29.2 CODEC Common Driver

29.2.1 Overview

The codec common driver provides a codec control abstraction interface.

Modules

- [CODEC Adapter](#)
- [WM8960 Adapter](#)

Data Structures

- [struct _codec_config](#)
Initialize structure of the codec. [More...](#)
- [struct _codec_capability](#)
codec capability [More...](#)
- [struct _codec_handle](#)
Codec handle definition. [More...](#)

Macros

- [#define CODEC_VOLUME_MAX_VALUE \(100U\)](#)
codec maximum volume range

Typedefs

- [typedef enum _codec_audio_protocol codec_audio_protocol_t](#)
AUDIO format definition.
- [typedef enum _codec_module codec_module_t](#)
audio codec module
- [typedef enum _codec_module_ctrl_cmd codec_module_ctrl_cmd_t](#)
audio codec module control cmd
- [typedef struct _codec_handle codec_handle_t](#)
codec handle declaration
- [typedef struct _codec_config codec_config_t](#)
Initialize structure of the codec.
- [typedef struct _codec_capability codec_capability_t](#)
codec capability

Enumerations

- enum {

kStatus_CODEC_NotSupport = MAKE_STATUS(kStatusGroup_CODEC, 0U),

kStatus_CODEC_DeviceNotRegistered = MAKE_STATUS(kStatusGroup_CODEC, 1U),

kStatus_CODEC_I2CBusInitialFailed,

kStatus_CODEC_I2CCommandTransferFailed }

CODEC status.
- enum _codec_audio_protocol {

kCODEC_BusI2S = 0U,

kCODEC_BusLeftJustified = 1U,

kCODEC_BusRightJustified = 2U,

kCODEC_BusPCMA = 3U,

kCODEC_BusPCMB = 4U,

kCODEC_BusTDM = 5U }

AUDIO format definition.
- enum {

kCODEC_AudioSampleRate8KHz = 8000U,

kCODEC_AudioSampleRate11025Hz = 11025U,

kCODEC_AudioSampleRate12KHz = 12000U,

kCODEC_AudioSampleRate16KHz = 16000U,

kCODEC_AudioSampleRate22050Hz = 22050U,

kCODEC_AudioSampleRate24KHz = 24000U,

kCODEC_AudioSampleRate32KHz = 32000U,

kCODEC_AudioSampleRate44100Hz = 44100U,

kCODEC_AudioSampleRate48KHz = 48000U,

kCODEC_AudioSampleRate96KHz = 96000U,

kCODEC_AudioSampleRate192KHz = 192000U,

kCODEC_AudioSampleRate384KHz = 384000U }

audio sample rate definition
- enum {

kCODEC_AudioBitWidth16bit = 16U,

kCODEC_AudioBitWidth20bit = 20U,

kCODEC_AudioBitWidth24bit = 24U,

kCODEC_AudioBitWidth32bit = 32U }

audio bit width
- enum _codec_module {

```

kCODEC_ModuleADC = 0U,
kCODEC_ModuleDAC = 1U,
kCODEC_ModulePGA = 2U,
kCODEC_ModuleHeadphone = 3U,
kCODEC_ModuleSpeaker = 4U,
kCODEC_ModuleLinein = 5U,
kCODEC_ModuleLineout = 6U,
kCODEC_ModuleVref = 7U,
kCODEC_ModuleMicbias = 8U,
kCODEC_ModuleMic = 9U,
kCODEC_ModuleI2SIn = 10U,
kCODEC_ModuleI2SOut = 11U,
kCODEC_ModuleMixer = 12U }

    audio codec module
• enum _codec_module_ctrl_cmd { kCODEC_ModuleSwitchI2SInInterface = 0U }

    audio codec module control cmd
• enum {

    kCODEC_ModuleI2SInInterfacePCM = 0U,
    kCODEC_ModuleI2SInInterfaceDSD = 1U }

    audio codec module digital interface
• enum {

    kCODEC_RecordSourceDifferentialLine = 1U,
    kCODEC_RecordSourceLineInput = 2U,
    kCODEC_RecordSourceDifferentialMic = 4U,
    kCODEC_RecordSourceDigitalMic = 8U,
    kCODEC_RecordSourceSingleEndMic = 16U }

    audio codec module record source value
• enum {

    kCODEC_RecordChannelLeft1 = 1U,
    kCODEC_RecordChannelLeft2 = 2U,
    kCODEC_RecordChannelLeft3 = 4U,
    kCODEC_RecordChannelRight1 = 1U,
    kCODEC_RecordChannelRight2 = 2U,
    kCODEC_RecordChannelRight3 = 4U,
    kCODEC_RecordChannelDifferentialPositive1 = 1U,
    kCODEC_RecordChannelDifferentialPositive2 = 2U,
    kCODEC_RecordChannelDifferentialPositive3 = 4U,
    kCODEC_RecordChannelDifferentialNegative1 = 8U,
    kCODEC_RecordChannelDifferentialNegative2 = 16U,
    kCODEC_RecordChannelDifferentialNegative3 = 32U }

    audio codec record channel
• enum {

```

```

kCODEC_PlaySourcePGA = 1U,
kCODEC_PlaySourceInput = 2U,
kCODEC_PlaySourceDAC = 4U,
kCODEC_PlaySourceMixerIn = 1U,
kCODEC_PlaySourceMixerInLeft = 2U,
kCODEC_PlaySourceMixerInRight = 4U,
kCODEC_PlaySourceAux = 8U }

```

audio codec module play source value

- enum {

```

kCODEC_PlayChannelHeadphoneLeft = 1U,
kCODEC_PlayChannelHeadphoneRight = 2U,
kCODEC_PlayChannelSpeakerLeft = 4U,
kCODEC_PlayChannelSpeakerRight = 8U,
kCODEC_PlayChannelLineOutLeft = 16U,
kCODEC_PlayChannelLineOutRight = 32U,
kCODEC_PlayChannelLeft0 = 1U,
kCODEC_PlayChannelRight0 = 2U,
kCODEC_PlayChannelLeft1 = 4U,
kCODEC_PlayChannelRight1 = 8U,
kCODEC_PlayChannelLeft2 = 16U,
kCODEC_PlayChannelRight2 = 32U,
kCODEC_PlayChannelLeft3 = 64U,
kCODEC_PlayChannelRight3 = 128U }

```

codec play channel

- enum {

```

kCODEC_VolumeHeadphoneLeft = 1U,
kCODEC_VolumeHeadphoneRight = 2U,
kCODEC_VolumeSpeakerLeft = 4U,
kCODEC_VolumeSpeakerRight = 8U,
kCODEC_VolumeLineOutLeft = 16U,
kCODEC_VolumeLineOutRight = 32U,
kCODEC_VolumeLeft0 = 1UL << 0U,
kCODEC_VolumeRight0 = 1UL << 1U,
kCODEC_VolumeLeft1 = 1UL << 2U,
kCODEC_VolumeRight1 = 1UL << 3U,
kCODEC_VolumeLeft2 = 1UL << 4U,
kCODEC_VolumeRight2 = 1UL << 5U,
kCODEC_VolumeLeft3 = 1UL << 6U,
kCODEC_VolumeRight3 = 1UL << 7U,
kCODEC_VolumeDAC = 1UL << 8U }

```

codec volume setting

- enum {

```

kCODEC_SupportModuleADC = 1U << 0U,
kCODEC_SupportModuleDAC = 1U << 1U,
kCODEC_SupportModulePGA = 1U << 2U,
kCODEC_SupportModuleHeadphone = 1U << 3U,
kCODEC_SupportModuleSpeaker = 1U << 4U,
kCODEC_SupportModuleLinein = 1U << 5U,
kCODEC_SupportModuleLineout = 1U << 6U,
kCODEC_SupportModuleVref = 1U << 7U,
kCODEC_SupportModuleMicbias = 1U << 8U,
kCODEC_SupportModuleMic = 1U << 9U,
kCODEC_SupportModuleI2SIn = 1U << 10U,
kCODEC_SupportModuleI2SOut = 1U << 11U,
kCODEC_SupportModuleMixer = 1U << 12U,
kCODEC_SupportModuleI2SInSwitchInterface = 1U << 13U,
kCODEC_SupportPlayChannelLeft0 = 1U << 0U,
kCODEC_SupportPlayChannelRight0 = 1U << 1U,
kCODEC_SupportPlayChannelLeft1 = 1U << 2U,
kCODEC_SupportPlayChannelRight1 = 1U << 3U,
kCODEC_SupportPlayChannelLeft2 = 1U << 4U,
kCODEC_SupportPlayChannelRight2 = 1U << 5U,
kCODEC_SupportPlayChannelLeft3 = 1U << 6U,
kCODEC_SupportPlayChannelRight3 = 1U << 7U,
kCODEC_SupportPlaySourcePGA = 1U << 8U,
kCODEC_SupportPlaySourceInput = 1U << 9U,
kCODEC_SupportPlaySourceDAC = 1U << 10U,
kCODEC_SupportPlaySourceMixerIn = 1U << 11U,
kCODEC_SupportPlaySourceMixerInLeft = 1U << 12U,
kCODEC_SupportPlaySourceMixerInRight = 1U << 13U,
kCODEC_SupportPlaySourceAux = 1U << 14U,
kCODEC_SupportRecordSourceDifferentialLine = 1U << 0U,
kCODEC_SupportRecordSourceLineInput = 1U << 1U,
kCODEC_SupportRecordSourceDifferentialMic = 1U << 2U,
kCODEC_SupportRecordSourceDigitalMic = 1U << 3U,
kCODEC_SupportRecordSourceSingleEndMic = 1U << 4U,
kCODEC_SupportRecordChannelLeft1 = 1U << 6U,
kCODEC_SupportRecordChannelLeft2 = 1U << 7U,
kCODEC_SupportRecordChannelLeft3 = 1U << 8U,
kCODEC_SupportRecordChannelRight1 = 1U << 9U,
kCODEC_SupportRecordChannelRight2 = 1U << 10U,
kCODEC_SupportRecordChannelRight3 = 1U << 11U }

```

audio codec capability

Functions

- `status_t CODEC_Init (codec_handle_t *handle, codec_config_t *config)`
Codec initialization.
- `status_t CODEC_Deinit (codec_handle_t *handle)`
Codec de-initilization.
- `status_t CODEC_SetFormat (codec_handle_t *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`
set audio data format.
- `status_t CODEC_ModuleControl (codec_handle_t *handle, codec_module_ctrl_cmd_t cmd, uint32_t data)`
codec module control.
- `status_t CODEC_SetVolume (codec_handle_t *handle, uint32_t channel, uint32_t volume)`
set audio codec pl volume.
- `status_t CODEC_SetMute (codec_handle_t *handle, uint32_t channel, bool mute)`
set audio codec module mute.
- `status_t CODEC_SetPower (codec_handle_t *handle, codec_module_t module, bool powerOn)`
set audio codec power.
- `status_t CODEC_SetRecord (codec_handle_t *handle, uint32_t recordSource)`
codec set record source.
- `status_t CODEC_SetRecordChannel (codec_handle_t *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)`
codec set record channel.
- `status_t CODEC_SetPlay (codec_handle_t *handle, uint32_t playSource)`
codec set play source.

Driver version

- `#define FSL_CODEC_DRIVER_VERSION (MAKE_VERSION(2, 3, 1))`
CLOCK driver version 2.3.1.

29.2.2 Data Structure Documentation

29.2.2.1 struct _codec_config

Data Fields

- `uint32_t codecDevType`
codec type
- `void *codecDevConfig`
Codec device specific configuration.

29.2.2.2 struct _codec_capability

Data Fields

- `uint32_t codecModuleCapability`
codec module capability
- `uint32_t codecPlayCapability`
codec play capability
- `uint32_t codecRecordCapability`
codec record capability
- `uint32_t codecVolumeCapability`
codec volume capability

29.2.2.3 struct _codec_handle

- Application should allocate a buffer with CODEC_HANDLE_SIZE for handle definition, such as `uint8_t codecHandleBuffer[CODEC_HANDLE_SIZE]; codec_handle_t *codecHandle = codecHandleBuffer;`;

Data Fields

- `codec_config_t * codecConfig`
codec configuration function pointer
- `const codec_capability_t * codecCapability`
codec capability
- `uint8_t codecDevHandle [HAL_CODEC_HANDLER_SIZE]`
codec device handle

29.2.3 Macro Definition Documentation

29.2.3.1 #define FSL_CODEC_DRIVER_VERSION (MAKE_VERSION(2, 3, 1))

29.2.4 Typedef Documentation

29.2.4.1 typedef enum _codec_audio_protocol codec_audio_protocol_t

29.2.5 Enumeration Type Documentation

29.2.5.1 anonymous enum

Enumerator

kStatus_CODEC_NotSupport CODEC not support status.

kStatus_CODEC_DeviceNotRegistered CODEC device register failed status.

kStatus_CODEC_I2CBusInitialFailed CODEC i2c bus initialization failed status.

kStatus_CODEC_I2CCommandTransferFailed CODEC i2c bus command transfer failed status.

29.2.5.2 enum _codec_audio_protocol

Enumerator

kCODEC_BusI2S I2S type.

kCODEC_BusLeftJustified Left justified mode.

kCODEC_BusRightJustified Right justified mode.

kCODEC_BusPCMA DSP/PCM A mode.

kCODEC_BusPCMB DSP/PCM B mode.

kCODEC_BusTDM TDM mode.

29.2.5.3 anonymous enum

Enumerator

kCODEC_AudioSampleRate8KHz Sample rate 8000 Hz.

kCODEC_AudioSampleRate11025Hz Sample rate 11025 Hz.

kCODEC_AudioSampleRate12KHz Sample rate 12000 Hz.

kCODEC_AudioSampleRate16KHz Sample rate 16000 Hz.

kCODEC_AudioSampleRate22050Hz Sample rate 22050 Hz.

kCODEC_AudioSampleRate24KHz Sample rate 24000 Hz.

kCODEC_AudioSampleRate32KHz Sample rate 32000 Hz.

kCODEC_AudioSampleRate44100Hz Sample rate 44100 Hz.

kCODEC_AudioSampleRate48KHz Sample rate 48000 Hz.

kCODEC_AudioSampleRate96KHz Sample rate 96000 Hz.

kCODEC_AudioSampleRate192KHz Sample rate 192000 Hz.

kCODEC_AudioSampleRate384KHz Sample rate 384000 Hz.

29.2.5.4 anonymous enum

Enumerator

kCODEC_AudioBitWidth16bit audio bit width 16

kCODEC_AudioBitWidth20bit audio bit width 20

kCODEC_AudioBitWidth24bit audio bit width 24

kCODEC_AudioBitWidth32bit audio bit width 32

29.2.5.5 enum _codec_module

Enumerator

kCODEC_ModuleADC codec module ADC

kCODEC_ModuleDAC codec module DAC
kCODEC_ModulePGA codec module PGA
kCODEC_ModuleHeadphone codec module headphone
kCODEC_ModuleSpeaker codec module speaker
kCODEC_ModuleLinein codec module linein
kCODEC_ModuleLineout codec module lineout
kCODEC_ModuleVref codec module VREF
kCODEC_ModuleMicbias codec module MIC BIAS
kCODEC_ModuleMic codec module MIC
kCODEC_ModuleI2SIn codec module I2S in
kCODEC_ModuleI2SOut codec module I2S out
kCODEC_ModuleMixer codec module mixer

29.2.5.6 enum _codec_module_ctrl_cmd

Enumerator

kCODEC_ModuleSwitchI2SInInterface module digital interface siwtch.

29.2.5.7 anonymous enum

Enumerator

kCODEC_ModuleI2SInInterfacePCM Pcm interface.
kCODEC_ModuleI2SInInterfaceDSD DSD interface.

29.2.5.8 anonymous enum

Enumerator

kCODEC_RecordSourceDifferentialLine record source from differential line
kCODEC_RecordSourceLineInput record source from line input
kCODEC_RecordSourceDifferentialMic record source from differential mic
kCODEC_RecordSourceDigitalMic record source from digital microphone
kCODEC_RecordSourceSingleEndMic record source from single microphone

29.2.5.9 anonymous enum

Enumerator

kCODEC_RecordChannelLeft1 left record channel 1
kCODEC_RecordChannelLeft2 left record channel 2
kCODEC_RecordChannelLeft3 left record channel 3
kCODEC_RecordChannelRight1 right record channel 1

kCODEC_RecordChannelRight2 right record channel 2
kCODEC_RecordChannelRight3 right record channel 3
kCODEC_RecordChannelDifferentialPositive1 differential positive record channel 1
kCODEC_RecordChannelDifferentialPositive2 differential positive record channel 2
kCODEC_RecordChannelDifferentialPositive3 differential positive record channel 3
kCODEC_RecordChannelDifferentialNegative1 differential negative record channel 1
kCODEC_RecordChannelDifferentialNegative2 differential negative record channel 2
kCODEC_RecordChannelDifferentialNegative3 differential negative record channel 3

29.2.5.10 anonymous enum

Enumerator

kCODEC_PlaySourcePGA play source PGA, bypass ADC
kCODEC_PlaySourceInput play source Input3
kCODEC_PlaySourceDAC play source DAC
kCODEC_PlaySourceMixerIn play source mixer in
kCODEC_PlaySourceMixerInLeft play source mixer in left
kCODEC_PlaySourceMixerInRight play source mixer in right
kCODEC_PlaySourceAux play source mixer in AUX

29.2.5.11 anonymous enum

Enumerator

kCODEC_PlayChannelHeadphoneLeft play channel headphone left
kCODEC_PlayChannelHeadphoneRight play channel headphone right
kCODEC_PlayChannelSpeakerLeft play channel speaker left
kCODEC_PlayChannelSpeakerRight play channel speaker right
kCODEC_PlayChannelLineOutLeft play channel lineout left
kCODEC_PlayChannelLineOutRight play channel lineout right
kCODEC_PlayChannelLeft0 play channel left0
kCODEC_PlayChannelRight0 play channel right0
kCODEC_PlayChannelLeft1 play channel left1
kCODEC_PlayChannelRight1 play channel right1
kCODEC_PlayChannelLeft2 play channel left2
kCODEC_PlayChannelRight2 play channel right2
kCODEC_PlayChannelLeft3 play channel left3
kCODEC_PlayChannelRight3 play channel right3

29.2.5.12 anonymous enum

Enumerator

kCODEC_VolumeHeadphoneLeft headphone left volume

kCODEC_VolumeHeadphoneRight headphone right volume
kCODEC_VolumeSpeakerLeft speaker left volume
kCODEC_VolumeSpeakerRight speaker right volume
kCODEC_VolumeLineOutLeft lineout left volume
kCODEC_VolumeLineOutRight lineout right volume
kCODEC_VolumeLeft0 left0 volume
kCODEC_VolumeRight0 right0 volume
kCODEC_VolumeLeft1 left1 volume
kCODEC_VolumeRight1 right1 volume
kCODEC_VolumeLeft2 left2 volume
kCODEC_VolumeRight2 right2 volume
kCODEC_VolumeLeft3 left3 volume
kCODEC_VolumeRight3 right3 volume
kCODEC_VolumeDAC dac volume

29.2.5.13 anonymous enum

Enumerator

kCODEC_SupportModuleADC codec capability of module ADC
kCODEC_SupportModuleDAC codec capability of module DAC
kCODEC_SupportModulePGA codec capability of module PGA
kCODEC_SupportModuleHeadphone codec capability of module headphone
kCODEC_SupportModuleSpeaker codec capability of module speaker
kCODEC_SupportModuleLinein codec capability of module linein
kCODEC_SupportModuleLineout codec capability of module lineout
kCODEC_SupportModuleVref codec capability of module vref
kCODEC_SupportModuleMicbias codec capability of module mic bias
kCODEC_SupportModuleMic codec capability of module mic bias
kCODEC_SupportModuleI2SIn codec capability of module I2S in
kCODEC_SupportModuleI2SOut codec capability of module I2S out
kCODEC_SupportModuleMixer codec capability of module mixer
kCODEC_SupportModuleI2SInSwitchInterface codec capability of module I2S in switch interface

kCODEC_SupportPlayChannelLeft0 codec capability of play channel left 0
kCODEC_SupportPlayChannelRight0 codec capability of play channel right 0
kCODEC_SupportPlayChannelLeft1 codec capability of play channel left 1
kCODEC_SupportPlayChannelRight1 codec capability of play channel right 1
kCODEC_SupportPlayChannelLeft2 codec capability of play channel left 2
kCODEC_SupportPlayChannelRight2 codec capability of play channel right 2
kCODEC_SupportPlayChannelLeft3 codec capability of play channel left 3
kCODEC_SupportPlayChannelRight3 codec capability of play channel right 3
kCODEC_SupportPlaySourcePGA codec capability of set playback source PGA
kCODEC_SupportPlaySourceInput codec capability of set playback source INPUT
kCODEC_SupportPlaySourceDAC codec capability of set playback source DAC

kCODEC_SupportPlaySourceMixerIn codec capability of set play source Mixer in
kCODEC_SupportPlaySourceMixerInLeft codec capability of set play source Mixer in left
kCODEC_SupportPlaySourceMixerInRight codec capability of set play source Mixer in right
kCODEC_SupportPlaySourceAux codec capability of set play source aux
kCODEC_SupportRecordSourceDifferentialLine codec capability of record source differential line

kCODEC_SupportRecordSourceLineInput codec capability of record source line input
kCODEC_SupportRecordSourceDifferentialMic codec capability of record source differential mic

kCODEC_SupportRecordSourceDigitalMic codec capability of record digital mic
kCODEC_SupportRecordSourceSingleEndMic codec capability of single end mic
kCODEC_SupportRecordChannelLeft1 left record channel 1
kCODEC_SupportRecordChannelLeft2 left record channel 2
kCODEC_SupportRecordChannelLeft3 left record channel 3
kCODEC_SupportRecordChannelRight1 right record channel 1
kCODEC_SupportRecordChannelRight2 right record channel 2
kCODEC_SupportRecordChannelRight3 right record channel 3

29.2.6 Function Documentation

29.2.6.1 status_t CODEC_Init (*codec_handle_t * handle*, *codec_config_t * config*)

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configurations.

Returns

kStatus_Success is success, else de-initial failed.

29.2.6.2 status_t CODEC_Deinit (*codec_handle_t * handle*)

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus_Success is success, else de-initial failed.

29.2.6.3 status_t CODEC_SetFormat (*codec_handle_t * handle*, *uint32_t mclk*, *uint32_t sampleRate*, *uint32_t bitWidth*)

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

29.2.6.4 status_t CODEC_ModuleControl (*codec_handle_t * handle*, *codec_module_ctrl_cmd_t cmd*, *uint32_t data*)

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature.

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

29.2.6.5 status_t CODEC_SetVolume (*codec_handle_t * handle*, *uint32_t channel*, *uint32_t volume*)

Parameters

<i>handle</i>	codec handle.
<i>channel</i>	audio codec volume channel, can be a value or combine value of _codec_volume_-capability or _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

29.2.6.6 status_t CODEC_SetMute (*codec_handle_t * handle*, *uint32_t channel*, *bool mute*)

Parameters

<i>handle</i>	codec handle.
<i>channel</i>	audio codec volume channel, can be a value or combine value of _codec_volume_-capability or _codec_play_channel.
<i>mute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

29.2.6.7 status_t CODEC_SetPower (*codec_handle_t * handle*, *codec_module_t module*, *bool powerOn*)

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

29.2.6.8 status_t CODEC_SetRecord (*codec_handle_t * handle*, *uint32_t recordSource*)

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

29.2.6.9 status_t CODEC_SetRecordChannel (*codec_handle_t * handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel*)

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

29.2.6.10 status_t CODEC_SetPlay (*codec_handle_t * handle, uint32_t playSource*)

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus_Success is success, else configure failed.

29.3 CODEC I2C Driver

The codec common driver provides a codec control abstraction interface.

29.4 WM8960 Driver

29.4.1 Overview

The wm8960 driver provides a codec control interface.

Data Structures

- struct `_wm8960_audio_format`
wm8960 audio format [More...](#)
- struct `_wm8960_master_sysclk_config`
wm8960 master system clock configuration [More...](#)
- struct `wm8960_config`
Initialize structure of WM8960. [More...](#)
- struct `_wm8960_handle`
wm8960 codec handler [More...](#)

Macros

- #define `WM8960_I2C_HANDLER_SIZE` CODEC_I2C_MASTER_HANDLER_SIZE
wm8960 handle size
- #define `WM8960_LINVOL` 0x0U
Define the register address of WM8960.
- #define `WM8960_CACHEREGNUM` 56U
Cache register number.
- #define `WM8960_CLOCK2_BCLK_DIV_MASK` 0xFU
WM8960 CLOCK2 bits.
- #define `WM8960_IFACE1_FORMAT_MASK` 0x03U
WM8960_IFACE1 FORMAT bits.
- #define `WM8960_IFACE1_WL_MASK` 0x0CU
WM8960_IFACE1 WL bits.
- #define `WM8960_IFACE1_LRP_MASK` 0x10U
WM8960_IFACE1 LRP bit.
- #define `WM8960_IFACE1_DLRSWAP_MASK` 0x20U
WM8960_IFACE1 DLRSWAP bit.
- #define `WM8960_IFACE1_MS_MASK` 0x40U
WM8960_IFACE1 MS bit.
- #define `WM8960_IFACE1_BCLKINV_MASK` 0x80U
WM8960_IFACE1 BCLKINV bit.
- #define `WM8960_IFACE1_ALRSWAP_MASK` 0x100U
WM8960_IFACE1 ALRSWAP bit.
- #define `WM8960_POWER1_VREF_MASK` 0x40U
WM8960_POWER1.
- #define `WM8960_POWER2_DACL_MASK` 0x100U
WM8960_POWER2.
- #define `WM8960_I2C_ADDR` 0x1A
WM8960 I2C address.
- #define `WM8960_I2C_BAUDRATE` (100000U)

- `#define WM8960_ADC_MAX_VOLUME_vVALUE 0xFFU`
WM8960 maximum volume value.

Typedefs

- `typedef enum _wm8960_module wm8960_module_t`
Modules in WM8960 board.
- `typedef enum _wm8960_play_source wm8960_play_source_t`
wm8960 play source
- `typedef enum _wm8960_route wm8960_route_t`
WM8960 data route.
- `typedef enum _wm8960_protocol wm8960_protocol_t`
The audio data transfer protocol choice.
- `typedef enum _wm8960_input wm8960_input_t`
wm8960 input source
- `typedef enum _wm8960_sysclk_source wm8960_sysclk_source_t`
wm8960 sysclk source
- `typedef struct _wm8960_audio_format wm8960_audio_format_t`
wm8960 audio format
- `typedef struct _wm8960_master_sysclk_config wm8960_master_sysclk_config_t`
wm8960 master system clock configuration
- `typedef struct wm8960_config wm8960_config_t`
Initialize structure of WM8960.
- `typedef struct _wm8960_handle wm8960_handle_t`
wm8960 codec handler

Enumerations

- `enum _wm8960_module {`
`kWM8960_ModuleADC = 0,`
`kWM8960_ModuleDAC = 1,`
`kWM8960_ModuleVREF = 2,`
`kWM8960_ModuleHP = 3,`
`kWM8960_ModuleMICB = 4,`
`kWM8960_ModuleMIC = 5,`
`kWM8960_ModuleLineIn = 6,`
`kWM8960_ModuleLineOut = 7,`
`kWM8960_ModuleSpeaker = 8,`
`kWM8960_ModuleOMIX = 9 }`
Modules in WM8960 board.
- `enum {`
`kWM8960_HeadphoneLeft = 1,`
`kWM8960_HeadphoneRight = 2,`
`kWM8960_SpeakerLeft = 4,`

```

kWM8960_SpeakerRight = 8 }

wm8960 play channel
• enum _wm8960_play_source {
  kWM8960_PlaySourcePGA = 1,
  kWM8960_PlaySourceInput = 2,
  kWM8960_PlaySourceDAC = 4 }

wm8960 play source
• enum _wm8960_route {
  kWM8960_RouteBypass = 0,
  kWM8960_RoutePlayback = 1,
  kWM8960_RoutePlaybackandRecord = 2,
  kWM8960_RouteRecord = 5 }

WM8960 data route.

• enum _wm8960_protocol {
  kWM8960_BusI2S = 2,
  kWM8960_BusLeftJustified = 1,
  kWM8960_BusRightJustified = 0,
  kWM8960_BusPCMA = 3,
  kWM8960_BusPCMB = 3 | (1 << 4) }

The audio data transfer protocol choice.

• enum _wm8960_input {
  kWM8960_InputClosed = 0,
  kWM8960_InputSingleEndedMic = 1,
  kWM8960_InputDifferentialMicInput2 = 2,
  kWM8960_InputDifferentialMicInput3 = 3,
  kWM8960_InputLineINPUT2 = 4,
  kWM8960_InputLineINPUT3 = 5 }

wm8960 input source

• enum {
  kWM8960_AudioSampleRate8KHz = 8000U,
  kWM8960_AudioSampleRate11025Hz = 11025U,
  kWM8960_AudioSampleRate12KHz = 12000U,
  kWM8960_AudioSampleRate16KHz = 16000U,
  kWM8960_AudioSampleRate22050Hz = 22050U,
  kWM8960_AudioSampleRate24KHz = 24000U,
  kWM8960_AudioSampleRate32KHz = 32000U,
  kWM8960_AudioSampleRate44100Hz = 44100U,
  kWM8960_AudioSampleRate48KHz = 48000U,
  kWM8960_AudioSampleRate96KHz = 96000U,
  kWM8960_AudioSampleRate192KHz = 192000U,
  kWM8960_AudioSampleRate384KHz = 384000U }

audio sample rate definition

• enum {
  kWM8960_AudioBitWidth16bit = 16U,
  kWM8960_AudioBitWidth20bit = 20U,
  kWM8960_AudioBitWidth24bit = 24U,

```

```

kWM8960_AudioBitWidth32bit = 32U }

    audio bit width
• enum _wm8960_sysclk_source {
    kWM8960_SysClkSourceMclk = 0U,
    kWM8960_SysClkSourceInternalPLL = 1U }

    wm8960 sysclk source

```

Functions

- status_t WM8960_Init (wm8960_handle_t *handle, const wm8960_config_t *config)
 WM8960 initialize function.
- status_t WM8960_Deinit (wm8960_handle_t *handle)
 Deinit the WM8960 codec.
- status_t WM8960_SetDataRoute (wm8960_handle_t *handle, wm8960_route_t route)
 Set audio data route in WM8960.
- status_t WM8960_SetLeftInput (wm8960_handle_t *handle, wm8960_input_t input)
 Set left audio input source in WM8960.
- status_t WM8960_SetRightInput (wm8960_handle_t *handle, wm8960_input_t input)
 Set right audio input source in WM8960.
- status_t WM8960_SetProtocol (wm8960_handle_t *handle, wm8960_protocol_t protocol)
 Set the audio transfer protocol.
- void WM8960_SetMasterSlave (wm8960_handle_t *handle, bool master)
 Set WM8960 as master or slave.
- status_t WM8960_SetVolume (wm8960_handle_t *handle, wm8960_module_t module, uint32_t volume)
 Set the volume of different modules in WM8960.
- uint32_t WM8960_GetVolume (wm8960_handle_t *handle, wm8960_module_t module)
 Get the volume of different modules in WM8960.
- status_t WM8960_SetMute (wm8960_handle_t *handle, wm8960_module_t module, bool isEnabled)
 Mute modules in WM8960.
- status_t WM8960_SetModule (wm8960_handle_t *handle, wm8960_module_t module, bool isEnabled)
 Enable/disable expected devices.
- status_t WM8960_SetPlay (wm8960_handle_t *handle, uint32_t playSource)
 SET the WM8960 play source.
- status_t WM8960_ConfigDataFormat (wm8960_handle_t *handle, uint32_t sysclk, uint32_t sample_rate, uint32_t bits)
 Configure the data format of audio data.
- status_t WM8960_SetJackDetect (wm8960_handle_t *handle, bool isEnabled)
 Enable/disable jack detect feature.
- status_t WM8960_WriteReg (wm8960_handle_t *handle, uint8_t reg, uint16_t val)
 Write register to WM8960 using I2C.
- status_t WM8960_ReadReg (uint8_t reg, uint16_t *val)
 Read register from WM8960 using I2C.
- status_t WM8960_ModifyReg (wm8960_handle_t *handle, uint8_t reg, uint16_t mask, uint16_t val)
 Modify some bits in the register using I2C.

Driver version

- #define FSL_WM8960_DRIVER_VERSION (MAKE_VERSION(2, 2, 4))
CLOCK driver version 2.2.4.

29.4.2 Data Structure Documentation

29.4.2.1 struct _wm8960_audio_format

Data Fields

- uint32_t **mcclk_HZ**
master clock frequency
- uint32_t **sampleRate**
sample rate
- uint32_t **bitWidth**
bit width

29.4.2.2 struct _wm8960_master_sysclk_config

Data Fields

- **wm8960_sysclk_source_t sysclkSource**
sysclk source
- uint32_t **sysclkFreq**
PLL output frequency value.

29.4.2.3 struct **wm8960_config**

Data Fields

- **wm8960_route_t route**
Audio data route.
- **wm8960_protocol_t bus**
Audio transfer protocol.
- **wm8960_audio_format_t format**
Audio format.
- bool **master_slave**
Master or slave.
- **wm8960_master_sysclk_config_t masterClock**
master clock configurations
- bool **enableSpeaker**
True means enable class D speaker as output, false means no.
- **wm8960_input_t leftInputSource**
Left input source for WM8960.
- **wm8960_input_t rightInputSource**
Right input source for wm8960.

- `wm8960_play_source_t playSource`
play source
- `uint8_t slaveAddress`
wm8960 device address
- `codec_i2c_config_t i2cConfig`
i2c configuration

Field Documentation

- (1) `wm8960_route_t wm8960_config::route`
- (2) `bool wm8960_config::master_slave`

29.4.2.4 struct _wm8960_handle

Data Fields

- `const wm8960_config_t * config`
wm8904 config pointer
- `uint8_t i2cHandle [WM8960_I2C_HANDLER_SIZE]`
i2c handle

29.4.3 Macro Definition Documentation

29.4.3.1 #define WM8960_LINVOL 0x0U

29.4.3.2 #define WM8960_I2C_ADDR 0x1A

29.4.4 Typedef Documentation

29.4.4.1 typedef enum _wm8960_module wm8960_module_t

29.4.4.2 typedef enum _wm8960_route wm8960_route_t

Only provide some typical data route, not all route listed. Note: Users cannot combine any routes, once a new route is set, the previous one would be replaced.

29.4.4.3 typedef enum _wm8960_protocol wm8960_protocol_t

WM8960 only supports I2S format and PCM format.

29.4.5 Enumeration Type Documentation

29.4.5.1 enum _wm8960_module

Enumerator

kWM8960_ModuleADC ADC module in WM8960.
kWM8960_ModuleDAC DAC module in WM8960.
kWM8960_ModuleVREF VREF module.
kWM8960_ModuleHP Headphone.
kWM8960_ModuleMICB Mic bias.
kWM8960_ModuleMIC Input Mic.
kWM8960_ModuleLineIn Analog in PGA.
kWM8960_ModuleLineOut Line out module.
kWM8960_ModuleSpeaker Speaker module.
kWM8960_ModuleOMIX Output mixer.

29.4.5.2 anonymous enum

Enumerator

kWM8960_HeadphoneLeft wm8960 headphone left channel
kWM8960_HeadphoneRight wm8960 headphone right channel
kWM8960_SpeakerLeft wm8960 speaker left channel
kWM8960_SpeakerRight wm8960 speaker right channel

29.4.5.3 enum _wm8960_play_source

Enumerator

kWM8960_PlaySourcePGA wm8960 play source PGA
kWM8960_PlaySourceInput wm8960 play source Input
kWM8960_PlaySourceDAC wm8960 play source DAC

29.4.5.4 enum _wm8960_route

Only provide some typical data route, not all route listed. Note: Users cannot combine any routes, once a new route is set, the previous one would be replaced.

Enumerator

kWM8960_RouteBypass LINEIN->Headphone.
kWM8960_RoutePlayback I2SIN->DAC->Headphone.
kWM8960_RoutePlaybackandRecord I2SIN->DAC->Headphone, LINEIN->ADC->I2SOUT.
kWM8960_RouteRecord LINEIN->ADC->I2SOUT.

29.4.5.5 enum _wm8960_protocol

WM8960 only supports I2S format and PCM format.

Enumerator

- kWM8960_BusI2S* I2S type.
- kWM8960_BusLeftJustified* Left justified mode.
- kWM8960_BusRightJustified* Right justified mode.
- kWM8960_BusPCMA* PCM A mode.
- kWM8960_BusPCMB* PCM B mode.

29.4.5.6 enum _wm8960_input

Enumerator

- kWM8960_InputClosed* Input device is closed.
- kWM8960_InputSingleEndedMic* Input as single ended mic, only use L/RINPUT1.
- kWM8960_InputDifferentialMicInput2* Input as differential mic, use L/RINPUT1 and L/RINPUT2.
- kWM8960_InputDifferentialMicInput3* Input as differential mic, use L/RINPUT1 and L/RINPUT3.
- kWM8960_InputLineINPUT2* Input as line input, only use L/RINPUT2.
- kWM8960_InputLineINPUT3* Input as line input, only use L/RINPUT3.

29.4.5.7 anonymous enum

Enumerator

- kWM8960_AudioSampleRate8KHz* Sample rate 8000 Hz.
- kWM8960_AudioSampleRate11025Hz* Sample rate 11025 Hz.
- kWM8960_AudioSampleRate12KHz* Sample rate 12000 Hz.
- kWM8960_AudioSampleRate16KHz* Sample rate 16000 Hz.
- kWM8960_AudioSampleRate22050Hz* Sample rate 22050 Hz.
- kWM8960_AudioSampleRate24KHz* Sample rate 24000 Hz.
- kWM8960_AudioSampleRate32KHz* Sample rate 32000 Hz.
- kWM8960_AudioSampleRate44100Hz* Sample rate 44100 Hz.
- kWM8960_AudioSampleRate48KHz* Sample rate 48000 Hz.
- kWM8960_AudioSampleRate96KHz* Sample rate 96000 Hz.
- kWM8960_AudioSampleRate192KHz* Sample rate 192000 Hz.
- kWM8960_AudioSampleRate384KHz* Sample rate 384000 Hz.

29.4.5.8 anonymous enum

Enumerator

<i>kWM8960_AudioBitWidth16bit</i>	audio bit width 16
<i>kWM8960_AudioBitWidth20bit</i>	audio bit width 20
<i>kWM8960_AudioBitWidth24bit</i>	audio bit width 24
<i>kWM8960_AudioBitWidth32bit</i>	audio bit width 32

29.4.5.9 enum _wm8960_sysclk_source

Enumerator

<i>kWM8960_SysClkSourceMclk</i>	sysclk source from external MCLK
<i>kWM8960_SysClkSourceInternalPLL</i>	sysclk source from internal PLL

29.4.6 Function Documentation

29.4.6.1 status_t WM8960_Init (*wm8960_handle_t * handle*, *const wm8960_config_t * config*)

The second parameter is NULL to WM8960 in this version. If users want to change the settings, they have to use *wm8960_write_reg()* or *wm8960_modify_reg()* to set the register value of WM8960. Note: If the *codec_config* is NULL, it would initialize WM8960 using default settings. The default setting: *codec_config->route* = *kWM8960_RoutePlaybackandRecord* *codec_config->bus* = *kWM8960_BusI2S* *codec_config->master* = *slave*

Parameters

<i>handle</i>	WM8960 handle structure.
<i>config</i>	WM8960 configuration structure.

29.4.6.2 status_t WM8960_Deinit (*wm8960_handle_t * handle*)

This function close all modules in WM8960 to save power.

Parameters

<i>handle</i>	WM8960 handle structure pointer.
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29.4.6.3 status_t WM8960_SetDataRoute (*wm8960_handle_t * handle*, *wm8960_route_t route*)

This function would set the data route according to route. The route cannot be combined, as all route would enable different modules. Note: If a new route is set, the previous route would not work.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>route</i>	Audio data route in WM8960.

29.4.6.4 status_t WM8960_SetLeftInput (*wm8960_handle_t * handle*, *wm8960_input_t input*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>input</i>	Audio input source.

29.4.6.5 status_t WM8960_SetRightInput (*wm8960_handle_t * handle*, *wm8960_input_t input*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>input</i>	Audio input source.

29.4.6.6 status_t WM8960_SetProtocol (*wm8960_handle_t * handle*, *wm8960_protocol_t protocol*)

WM8960 only supports I2S, left justified, right justified, PCM A, PCM B format.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>protocol</i>	Audio data transfer protocol.

29.4.6.7 void WM8960_SetMasterSlave (*wm8960_handle_t * handle, bool master*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>master</i>	1 represent master, 0 represent slave.

29.4.6.8 status_t WM8960_SetVolume (*wm8960_handle_t * handle, wm8960_module_t module, uint32_t volume*)

This function would set the volume of WM8960 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Module:kWM8960_ModuleADC, volume range value: 0 is mute, 1-255 is -97db to 30db
 Module:kWM8960_ModuleDAC, volume range value: 0 is mute, 1-255 is -127db to 0db
 Module:kWM8960_ModuleHP, volume range value: 0 - 2F is mute, 0x30 - 0x7F is -73db to 6db
 Module:kWM8960_ModuleLineIn, volume range value: 0 - 0x3F is -17.25db to 30db
 Module:kWM8960_ModuleSpeaker, volume range value: 0 - 2F is mute, 0x30 - 0x7F is -73db to 6db

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module to set volume, it can be ADC, DAC, Headphone and so on.
<i>volume</i>	Volume value need to be set.

29.4.6.9 uint32_t WM8960_GetVolume (*wm8960_handle_t * handle, wm8960_module_t module*)

This function gets the volume of WM8960 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module to set volume, it can be ADC, DAC, Headphone and so on.

Returns

Volume value of the module.

29.4.6.10 status_t WM8960_SetMute (*wm8960_handle_t * handle, wm8960_module_t module, bool isEnabled*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Modules need to be mute.
<i>isEnabled</i>	Mute or unmute, 1 represent mute.

29.4.6.11 status_t WM8960_SetModule (*wm8960_handle_t * handle, wm8960_module_t module, bool isEnabled*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module expected to enable.
<i>isEnabled</i>	Enable or disable moudles.

29.4.6.12 status_t WM8960_SetPlay (*wm8960_handle_t * handle, uint32_t playSource*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>playSource</i>	play source , can be a value combine of kWM8960_ModuleHeadphoneSourcePG-A, kWM8960_ModuleHeadphoneSourceDAC, kWM8960_ModulePlaySourceInput, kWM8960_ModulePlayMonoRight, kWM8960_ModulePlayMonoLeft.

Returns

kStatus_WM8904_Success if successful, different code otherwise..

29.4.6.13 status_t WM8960_ConfigDataFormat (*wm8960_handle_t * handle, uint32_t sysclk, uint32_t sample_rate, uint32_t bits*)

This function would configure the registers about the sample rate, bit depths.

Parameters

<i>handle</i>	WM8960 handle structure pointer.
<i>sysclk</i>	system clock of the codec which can be generated by MCLK or PLL output.
<i>sample_rate</i>	Sample rate of audio file running in WM8960. WM8960 now supports 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k and 96k sample rate.
<i>bits</i>	Bit depth of audio file (WM8960 only supports 16bit, 20bit, 24bit and 32 bit in HW).

29.4.6.14 status_t WM8960_SetJackDetect (*wm8960_handle_t * handle, bool isEnabled*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>isEnabled</i>	Enable or disable moudles.

29.4.6.15 status_t WM8960_WriteReg (*wm8960_handle_t * handle, uint8_t reg, uint16_t val*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>reg</i>	The register address in WM8960.
<i>val</i>	Value needs to write into the register.

29.4.6.16 status_t WM8960_ReadReg (*uint8_t reg, uint16_t * val*)

Parameters

<i>reg</i>	The register address in WM8960.
<i>val</i>	Value written to.

29.4.6.17 status_t WM8960_ModifyReg (*wm8960_handle_t * handle, uint8_t reg, uint16_t mask, uint16_t val*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>reg</i>	The register address in WM8960.
<i>mask</i>	The mask code for the bits want to write. The bit you want to write should be 0.
<i>val</i>	Value needs to write into the register.

29.4.7 WM8960 Adapter

29.4.7.1 Overview

The wm8960 adapter provides a codec unify control interface.

Macros

- #define `HAL_CODEC_WM8960_HANDLER_SIZE` (`WM8960_I2C_HANDLER_SIZE + 4`)
codec handler size

Functions

- `status_t HAL_CODEC_WM8960_Init` (void *handle, void *config)
Codec initialization.
- `status_t HAL_CODEC_WM8960_Deinit` (void *handle)
Codec de-initilization.
- `status_t HAL_CODEC_WM8960_SetFormat` (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)
set audio data format.
- `status_t HAL_CODEC_WM8960_SetVolume` (void *handle, uint32_t playChannel, uint32_t volume)
set audio codec module volume.
- `status_t HAL_CODEC_WM8960_SetMute` (void *handle, uint32_t playChannel, bool isMute)
set audio codec module mute.
- `status_t HAL_CODEC_WM8960_SetPower` (void *handle, uint32_t module, bool powerOn)
set audio codec module power.
- `status_t HAL_CODEC_WM8960_SetRecord` (void *handle, uint32_t recordSource)
codec set record source.
- `status_t HAL_CODEC_WM8960_SetRecordChannel` (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)
codec set record channel.
- `status_t HAL_CODEC_WM8960_SetPlay` (void *handle, uint32_t playSource)
codec set play source.
- `status_t HAL_CODEC_WM8960_ModuleControl` (void *handle, uint32_t cmd, uint32_t data)
codec module control.
- static `status_t HAL_CODEC_Init` (void *handle, void *config)
Codec initilization.
- static `status_t HAL_CODEC_Deinit` (void *handle)
Codec de-initilization.
- static `status_t HAL_CODEC_SetFormat` (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)
set audio data format.
- static `status_t HAL_CODEC_SetVolume` (void *handle, uint32_t playChannel, uint32_t volume)
set audio codec module volume.
- static `status_t HAL_CODEC_SetMute` (void *handle, uint32_t playChannel, bool isMute)
set audio codec module mute.
- static `status_t HAL_CODEC_SetPower` (void *handle, uint32_t module, bool powerOn)

- static `status_t HAL_CODEC_SetRecord` (void *handle, uint32_t recordSource)
codec set record source.
- static `status_t HAL_CODEC_SetRecordChannel` (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)
codec set record channel.
- static `status_t HAL_CODEC_SetPlay` (void *handle, uint32_t playSource)
codec set play source.
- static `status_t HAL_CODEC_ModuleControl` (void *handle, uint32_t cmd, uint32_t data)
codec module control.

29.4.7.2 Function Documentation

29.4.7.2.1 `status_t HAL_CODEC_WM8960_Init(void * handle, void * config)`

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus_Success is success, else initial failed.

29.4.7.2.2 `status_t HAL_CODEC_WM8960_Deinit(void * handle)`

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus_Success is success, else de-initial failed.

29.4.7.2.3 `status_t HAL_CODEC_WM8960_SetFormat(void * handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.4 status_t HAL_CODEC_WM8960_SetVolume (void * *handle*, uint32_t *playChannel*, uint32_t *volume*)

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.5 status_t HAL_CODEC_WM8960_SetMute (void * *handle*, uint32_t *playChannel*, bool *isMute*)

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.6 status_t HAL_CODEC_WM8960_SetPower (void * *handle*, uint32_t *module*, bool *powerOn*)

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.7 status_t HAL_CODEC_WM8960_SetRecord (void * *handle*, uint32_t *recordSource*)

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.8 status_t HAL_CODEC_WM8960_SetRecordChannel (void * *handle*, uint32_t *leftRecordChannel*, uint32_t *rightRecordChannel*)

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.9 status_t HAL_CODEC_WM8960_SetPlay (void * *handle*, uint32_t *playSource*)

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.10 status_t HAL_CODEC_WM8960_ModuleControl (void * *handle*, uint32_t *cmd*, uint32_t *data*)

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.11 static status_t HAL_CODEC_Init (void * *handle*, void * *config*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus_Success is success, else initial failed.

29.4.7.2.12 static status_t HAL_CODEC_Deinit (void * *handle*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus_Success is success, else de-initial failed.

29.4.7.2.13 static status_t HAL_CODEC_SetFormat(void * *handle*, uint32_t *mclk*, uint32_t *sampleRate*, uint32_t *bitWidth*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.14 static status_t HAL_CODEC_SetVolume(void * *handle*, uint32_t *playChannel*, uint32_t *volume*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.15 static status_t HAL_CODEC_SetMute(void * *handle*, uint32_t *playChannel*, bool *isMute*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.16 static status_t HAL_CODEC_SetPower (void * *handle*, uint32_t *module*, bool *powerOn*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.17 static status_t HAL_CODEC_SetRecord (void * *handle*, uint32_t *recordSource*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.18 static status_t HAL_CODEC_SetRecordChannel (void * *handle*, uint32_t *leftRecordChannel*, uint32_t *rightRecordChannel*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.19 static status_t HAL_CODEC_SetPlay (void * *handle*, uint32_t *playSource*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus_Success is success, else configure failed.

29.4.7.2.20 static status_t HAL_CODEC_ModuleControl (void * *handle*, uint32_t *cmd*, uint32_t *data*) [inline], [static]

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

Chapter 30

Serial Manager

30.1 Overview

This chapter describes the programming interface of the serial manager component.

The serial manager component provides a series of APIs to operate different serial port types. The port types it supports are UART, USB CDC and SWO.

Modules

- [Serial Port SWO](#)
- [Serial Port Uart](#)

Data Structures

- [struct _serial_manager_config](#)
serial manager config structure [More...](#)
- [struct _serial_manager_callback_message](#)
Callback message structure. [More...](#)

Macros

- [#define SERIAL_MANAGER_NON_BLOCKING_MODE \(1U\)](#)
Enable or disable serial manager non-blocking mode (1 - enable, 0 - disable)
- [#define SERIAL_MANAGER_RING_BUFFER_FLOWCONTROL \(0U\)](#)
Enable or ring buffer flow control (1 - enable, 0 - disable)
- [#define SERIAL_PORT_TYPE_UART \(0U\)](#)
Enable or disable uart port (1 - enable, 0 - disable)
- [#define SERIAL_PORT_TYPE_UART_DMA \(0U\)](#)
Enable or disable uart dma port (1 - enable, 0 - disable)
- [#define SERIAL_PORT_TYPE_USBCDC \(0U\)](#)
Enable or disable USB CDC port (1 - enable, 0 - disable)
- [#define SERIAL_PORT_TYPE_SWO \(0U\)](#)
Enable or disable SWO port (1 - enable, 0 - disable)
- [#define SERIAL_PORT_TYPE_VIRTUAL \(0U\)](#)
Enable or disable USB CDC virtual port (1 - enable, 0 - disable)
- [#define SERIAL_PORT_TYPE_RPMSG \(0U\)](#)
Enable or disable rpmsg port (1 - enable, 0 - disable)
- [#define SERIAL_PORT_TYPE_SPI_MASTER \(0U\)](#)
Enable or disable SPI Master port (1 - enable, 0 - disable)
- [#define SERIAL_PORT_TYPE_SPI_SLAVE \(0U\)](#)
Enable or disable SPI Slave port (1 - enable, 0 - disable)
- [#define SERIAL_PORT_TYPE_BLE_WU \(0U\)](#)
Enable or disable BLE WU port (1 - enable, 0 - disable)
- [#define SERIAL_MANAGER_WRITE_TIME_DELAY_DEFAULT_VALUE \(1U\)](#)

- `#define SERIAL_MANAGER_READ_TIME_DELAY_DEFAULT_VALUE (1U)`
Set the default delay time in ms used by SerialManager_WriteTimeDelay().
- `#define SERIAL_MANAGER_TASK_HANDLE_RX_AVAILABLE_NOTIFY (0U)`
Set the default delay time in ms used by SerialManager_ReadTimeDelay().
- `#define SERIAL_MANAGER_WRITE_HANDLE_SIZE (44U)`
Enable or disable SerialManager_Task() handle RX data available notify.
- `#define SERIAL_MANAGER_USE_COMMON_TASK (0U)`
Set serial manager write handle size.
- `SERIAL_PORT_UART_HANDLE_SIZE/SERIAL_PORT_USB_CDC_HANDLE_SIZE + serial manager dedicated size.`
- `#define SERIAL_MANAGER_HANDLE_SIZE (SERIAL_MANAGER_HANDLE_SIZE_TEMP + 124U)`
Definition of serial manager handle size.
- `#define SERIAL_MANAGER_HANDLE_DEFINE(name) uint32_t name[((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`
Defines the serial manager handle.
- `#define SERIAL_MANAGER_WRITE_HANDLE_DEFINE(name) uint32_t name[((SERIAL_MANAGER_WRITE_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`
Defines the serial manager write handle.
- `#define SERIAL_MANAGER_READ_HANDLE_DEFINE(name) uint32_t name[((SERIAL_MANAGER_READ_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`
Defines the serial manager read handle.
- `#define SERIAL_MANAGER_TASK_PRIORITY (2U)`
Macro to set serial manager task priority.
- `#define SERIAL_MANAGER_TASK_STACK_SIZE (1000U)`
Macro to set serial manager task stack size.

Typedefs

- `typedef void * serial_handle_t`
The handle of the serial manager module.
- `typedef void * serial_write_handle_t`
The write handle of the serial manager module.
- `typedef void * serial_read_handle_t`
The read handle of the serial manager module.
- `typedef enum _serial_port_type serial_port_type_t`
serial port type
- `typedef enum _serial_manager_type serial_manager_type_t`
serial manager type
- `typedef struct _serial_manager_config serial_manager_config_t`
serial manager config structure
- `typedef enum _serial_manager_status serial_manager_status_t`
serial manager error code
- `typedef struct _serial_manager_callback_message serial_manager_callback_message_t`
Callback message structure.
- `typedef void(* serial_manager_callback_t)(void *callbackParam, serial_manager_callback_message_t *message, serial_manager_status_t status)`
serial manager callback function

- `typedef int32_t(* serial_manager_lowpower_critical_callback_t)(int32_t power_mode)`
serial manager Lowpower Critical callback function

Enumerations

- `enum _serial_port_type {`
 `kSerialPort_None = 0U,`
 `kSerialPort_Uart = 1U,`
 `kSerialPort_UsbCdc,`
 `kSerialPort_Swo,`
 `kSerialPort_Virtual,`
 `kSerialPort_Rpmsg,`
 `kSerialPort_UartDma,`
 `kSerialPort_SpiMaster,`
 `kSerialPort_SpiSlave,`
 `kSerialPort_BleWu }`
serial port type
- `enum _serial_manager_type {`
 `kSerialManager_NonBlocking = 0x0U,`
 `kSerialManager_Blocking = 0x8F41U }`
serial manager type
- `enum _serial_manager_status {`
 `kStatus_SerialManager_Success = kStatus_Success,`
 `kStatus_SerialManager_Error = MAKE_STATUS(kStatusGroup_SERIALMANAGER, 1),`
 `kStatus_SerialManager_Busy = MAKE_STATUS(kStatusGroup_SERIALMANAGER, 2),`
 `kStatus_SerialManager_Notify = MAKE_STATUS(kStatusGroup_SERIALMANAGER, 3),`
 `kStatus_SerialManager_Canceled,`
 `kStatus_SerialManager_HandleConflict = MAKE_STATUS(kStatusGroup_SERIALMANAGER,`
 `5),`
 `kStatus_SerialManager_RingBufferOverflow,`
 `kStatus_SerialManager_NotConnected = MAKE_STATUS(kStatusGroup_SERIALMANAGER,`
 `7) }`
serial manager error code

Functions

- `serial_manager_status_t SerialManager_Init (serial_handle_t serialHandle, const serial_manager_config_t *serialConfig)`
Initializes a serial manager module with the serial manager handle and the user configuration structure.
- `serial_manager_status_t SerialManager_Deinit (serial_handle_t serialHandle)`
De-initializes the serial manager module instance.
- `serial_manager_status_t SerialManager_OpenWriteHandle (serial_handle_t serialHandle, serial_write_handle_t writeHandle)`
Opens a writing handle for the serial manager module.
- `serial_manager_status_t SerialManager_CloseWriteHandle (serial_write_handle_t writeHandle)`
Closes a writing handle for the serial manager module.
- `serial_manager_status_t SerialManager_OpenReadHandle (serial_handle_t serialHandle, serial_read_handle_t readHandle)`

- *Opens a reading handle for the serial manager module.*
serial_manager_status_t SerialManager_CloseReadHandle (*serial_read_handle_t* *readHandle*)
Closes a reading for the serial manager module.
- **serial_manager_status_t SerialManager_WriteBlocking** (*serial_write_handle_t* *writeHandle*, *uint8_t *buffer*, *uint32_t length*)
Transmits data with the blocking mode.
- **serial_manager_status_t SerialManager_ReadBlocking** (*serial_read_handle_t* *readHandle*, *uint8_t *buffer*, *uint32_t length*)
Reads data with the blocking mode.
- **serial_manager_status_t SerialManager_WriteNonBlocking** (*serial_write_handle_t* *writeHandle*, *uint8_t *buffer*, *uint32_t length*)
Transmits data with the non-blocking mode.
- **serial_manager_status_t SerialManager_ReadNonBlocking** (*serial_read_handle_t* *readHandle*, *uint8_t *buffer*, *uint32_t length*)
Reads data with the non-blocking mode.
- **serial_manager_status_t SerialManager_TryRead** (*serial_read_handle_t* *readHandle*, *uint8_t *buffer*, *uint32_t length*, *uint32_t *receivedLength*)
Tries to read data.
- **serial_manager_status_t SerialManager_CancelWriting** (*serial_write_handle_t* *writeHandle*)
Cancels unfinished send transmission.
- **serial_manager_status_t SerialManager_CancelReading** (*serial_read_handle_t* *readHandle*)
Cancels unfinished receive transmission.
- **serial_manager_status_t SerialManager_InstallTxCallback** (*serial_write_handle_t* *writeHandle*, *serial_manager_callback_t callback*, *void *callbackParam*)
Installs a TX callback and callback parameter.
- **serial_manager_status_t SerialManager_InstallRxCallback** (*serial_read_handle_t* *readHandle*, *serial_manager_callback_t callback*, *void *callbackParam*)
Installs a RX callback and callback parameter.
- **static bool SerialManager_needPollingIsr** (*void*)
Check if need polling ISR.
- **serial_manager_status_t SerialManager_EnterLowpower** (*serial_handle_t* *serialHandle*)
Prepares to enter low power consumption.
- **serial_manager_status_t SerialManager_ExitLowpower** (*serial_handle_t* *serialHandle*)
Restores from low power consumption.
- **void SerialManager_SetLowpowerCriticalCb** (*const serial_manager_lowpower_critical_CBs_t *pf-Callback*)
This function performs initialization of the callbacks structure used to disable lowpower when serial manager is active.

30.2 Data Structure Documentation

30.2.1 struct _serial_manager_config

Data Fields

- **uint8_t * ringBuffer**
Ring buffer address, it is used to buffer data received by the hardware.
- **uint32_t ringBufferSize**
The size of the ring buffer.

- `serial_port_type_t type`
Serial port type.
- `serial_manager_type_t blockType`
Serial manager port type.
- `void * portConfig`
Serial port configuration.

Field Documentation**(1) `uint8_t* _serial_manager_config::ringBuffer`**

Besides, the memory space cannot be free during the lifetime of the serial manager module.

30.2.2 `struct _serial_manager_callback_message`**Data Fields**

- `uint8_t * buffer`
Transferred buffer.
- `uint32_t length`
Transferred data length.

30.3 Macro Definition Documentation**30.3.1 `#define SERIAL_MANAGER_WRITE_TIME_DELAY_DEFAULT_VALUE (1U)`****30.3.2 `#define SERIAL_MANAGER_READ_TIME_DELAY_DEFAULT_VALUE (1U)`****30.3.3 `#define SERIAL_MANAGER_USE_COMMON_TASK (0U)`**

Macro to determine whether use common task.

30.3.4 `#define SERIAL_MANAGER_HANDLE_SIZE (SERIAL_MANAGER_HANDLE_SIZE_TEMP + 124U)`**30.3.5 `#define SERIAL_MANAGER_HANDLE_DEFINE(name) uint32_t name[((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`**

This macro is used to define a 4 byte aligned serial manager handle. Then use "(serial_handle_t)name" to get the serial manager handle.

The macro should be global and could be optional. You could also define serial manager handle by yourself.

This is an example,

```
* SERIAL_MANAGER_HANDLE_DEFINE(serialManagerHandle);
*
```

Parameters

<i>name</i>	The name string of the serial manager handle.
-------------	---

30.3.6 #define SERIAL_MANAGER_WRITE_HANDLE_DEFINE(*name*) uint32_t name[((SERIAL_MANAGER_WRITE_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]

This macro is used to define a 4 byte aligned serial manager write handle. Then use "(serial_write_handle-_t)*name*" to get the serial manager write handle.

The macro should be global and could be optional. You could also define serial manager write handle by yourself.

This is an example,

```
* SERIAL_MANAGER_WRITE_HANDLE_DEFINE(serialManagerwriteHandle);
*
```

Parameters

<i>name</i>	The name string of the serial manager write handle.
-------------	---

30.3.7 #define SERIAL_MANAGER_READ_HANDLE_DEFINE(*name*) uint32_t name[((SERIAL_MANAGER_READ_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]

This macro is used to define a 4 byte aligned serial manager read handle. Then use "(serial_read_handle-_t)*name*" to get the serial manager read handle.

The macro should be global and could be optional. You could also define serial manager read handle by yourself.

This is an example,

```
* SERIAL_MANAGER_READ_HANDLE_DEFINE(serialManagerReadHandle);
*
```

Parameters

<i>name</i>	The name string of the serial manager read handle.
-------------	--

30.3.8 #define SERIAL_MANAGER_TASK_PRIORITY (2U)

30.3.9 #define SERIAL_MANAGER_TASK_STACK_SIZE (1000U)

30.4 Enumeration Type Documentation

30.4.1 enum _serial_port_type

Enumerator

- kSerialPort_None* Serial port is none.
- kSerialPort_Uart* Serial port UART.
- kSerialPort_UsbCdc* Serial port USB CDC.
- kSerialPort_Swo* Serial port SWO.
- kSerialPort_Virtual* Serial port Virtual.
- kSerialPort_Rpmsg* Serial port RPMSG.
- kSerialPort_UartDma* Serial port UART DMA.
- kSerialPort_SpiMaster* Serial port SPIMASTER.
- kSerialPort_SpiSlave* Serial port SPISLAVE.
- kSerialPort_BleWu* Serial port BLE WU.

30.4.2 enum _serial_manager_type

Enumerator

- kSerialManager_NonBlocking* None blocking handle.
- kSerialManager_Blocking* Blocking handle.

30.4.3 enum _serial_manager_status

Enumerator

- kStatus_SerialManager_Success* Success.
- kStatus_SerialManager_Error* Failed.
- kStatus_SerialManager_Busy* Busy.
- kStatus_SerialManager_Notify* Ring buffer is not empty.
- kStatus_SerialManager_Canceled* the non-blocking request is canceled

kStatus_SerialManager_HandleConflict The handle is opened.

kStatus_SerialManager_RingBufferOverflow The ring buffer is overflowed.

kStatus_SerialManager_NotConnected The host is not connected.

30.5 Function Documentation

30.5.1 `serial_manager_status_t SerialManager_Init (serial_handle_t serialHandle, const serial_manager_config_t * serialConfig)`

This function configures the Serial Manager module with user-defined settings. The user can configure the configuration structure. The parameter `serialHandle` is a pointer to point to a memory space of size `SERIAL_MANAGER_HANDLE_SIZE` allocated by the caller. The Serial Manager module supports three types of serial port, UART (includes UART, USART, LPSCI, LPUART, etc), USB CDC and swo. Please refer to `serial_port_type_t` for serial port setting. These three types can be set by using `serial_manager_config_t`.

Example below shows how to use this API to configure the Serial Manager. For UART,

```
* #define SERIAL_MANAGER_RING_BUFFER_SIZE (256U)
* static SERIAL_MANAGER_HANDLE_DEFINE(s_serialHandle);
* static uint8_t s_ringBuffer[SERIAL_MANAGER_RING_BUFFER_SIZE];
*
* serial_manager_config_t config;
* serial_port_uart_config_t uartConfig;
* config.type = kSerialPort_Uart;
* config.ringBuffer = &s_ringBuffer[0];
* config.ringBufferSize = SERIAL_MANAGER_RING_BUFFER_SIZE;
* uartConfig.instance = 0;
* uartConfig.clockRate = 24000000;
* uartConfig.baudRate = 115200;
* uartConfig.parityMode = kSerialManager_UartParityDisabled;
* uartConfig.stopBitCount = kSerialManager_UartOneStopBit;
* uartConfig.enableRx = 1;
* uartConfig.enableTx = 1;
* uartConfig.enableRxRTS = 0;
* uartConfig.enableTxCTS = 0;
* config.portConfig = &uartConfig;
* SerialManager_Init((serial_handle_t)s_serialHandle, &config);
*
```

For USB CDC,

```
* #define SERIAL_MANAGER_RING_BUFFER_SIZE (256U)
* static SERIAL_MANAGER_HANDLE_DEFINE(s_serialHandle);
* static uint8_t s_ringBuffer[SERIAL_MANAGER_RING_BUFFER_SIZE];
*
* serial_manager_config_t config;
* serial_port_usb_cdc_config_t usbCdcConfig;
* config.type = kSerialPort_UsbCdc;
* config.ringBuffer = &s_ringBuffer[0];
* config.ringBufferSize = SERIAL_MANAGER_RING_BUFFER_SIZE;
* usbCdcConfig.controllerIndex = kSerialManager_UsbControllerKhci0;
* config.portConfig = &usbCdcConfig;
* SerialManager_Init((serial_handle_t)s_serialHandle, &config);
*
```

Parameters

<i>serialHandle</i>	Pointer to point to a memory space of size S SERIAL_MANAGER_HANDLE_SIZE allocated by the caller. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: S SERIAL_MANAGER_HANDLE_DEFINE(serialHandle) ; or <code>uint32_t serialHandle[((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code>
<i>serialConfig</i>	Pointer to user-defined configuration structure.

Return values

<i>kStatus_SerialManager_Error</i>	An error occurred.
<i>kStatus_SerialManager_Success</i>	The Serial Manager module initialization succeed.

30.5.2 **serial_manager_status_t SerialManager_Deinit (serial_handle_t serialHandle)**

This function de-initializes the serial manager module instance. If the opened writing or reading handle is not closed, the function will return `kStatus_SerialManager_Busy`.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer.
---------------------	---

Return values

<i>kStatus_SerialManager_Success</i>	The serial manager de-initialization succeed.
<i>kStatus_SerialManager_Busy</i>	Opened reading or writing handle is not closed.

30.5.3 **serial_manager_status_t SerialManager_OpenWriteHandle (serial_handle_t serialHandle, serial_write_handle_t writeHandle)**

This function Opens a writing handle for the serial manager module. If the serial manager needs to be used in different tasks, the task should open a dedicated write handle for itself by calling [SerialManager_OpenWriteHandle](#). Since there can only one buffer for transmission for the writing handle at the same time, multiple writing handles need to be opened when the multiple transmission is needed for a task.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices.
<i>writeHandle</i>	The serial manager module writing handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: SERIAL_MANAGER_WRITE_HANDLE_DEFINE(writeHandle) ; or <code>uint32_t writeHandle[((SERIAL_MANAGER_WRITE_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code>

Return values

<i>kStatus_SerialManager_Error</i>	An error occurred.
<i>kStatus_SerialManager_HandleConflict</i>	The writing handle was opened.
<i>kStatus_SerialManager_Success</i>	The writing handle is opened.

Example below shows how to use this API to write data. For task 1,

```
* static SERIAL_MANAGER_WRITE_HANDLE_DEFINE(s_serialWriteHandle1);
* static uint8_t s_nonBlockingWelcome1[] = "This is non-blocking writing log for task1!\r\n";
* SerialManager_OpenWriteHandle((serial_handle_t)serialHandle
*     , (serial_write_handle_t)s_serialWriteHandle1);
* SerialManager_InstallTxCallback()
*     serial_write_handle_t)s_serialWriteHandle1,
*             Task1_SerialManagerTxCallback,
*             s_serialWriteHandle1);
* SerialManager_WriteNonBlocking(
*     serial_write_handle_t)s_serialWriteHandle1,
*             s_nonBlockingWelcome1,
*             sizeof(s_nonBlockingWelcome1) - 1U);
*
*
```

For task 2,

```
* static SERIAL_MANAGER_WRITE_HANDLE_DEFINE(s_serialWriteHandle2);
* static uint8_t s_nonBlockingWelcome2[] = "This is non-blocking writing log for task2!\r\n";
* SerialManager_OpenWriteHandle((serial_handle_t)serialHandle
*     , (serial_write_handle_t)s_serialWriteHandle2);
* SerialManager_InstallTxCallback()
*     serial_write_handle_t)s_serialWriteHandle2,
*             Task2_SerialManagerTxCallback,
*             s_serialWriteHandle2);
* SerialManager_WriteNonBlocking(
*     serial_write_handle_t)s_serialWriteHandle2,
*             s_nonBlockingWelcome2,
*             sizeof(s_nonBlockingWelcome2) - 1U);
*
*
```

30.5.4 **serial_manager_status_t SerialManager_CloseWriteHandle (** **serial_write_handle_t writeHandle)**

This function Closes a writing handle for the serial manager module.

Parameters

<i>writeHandle</i>	The serial manager module writing handle pointer.
--------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	The writing handle is closed.
---------------------------------------	-------------------------------

30.5.5 **serial_manager_status_t SerialManager_OpenReadHandle (serial_handle_t serialHandle, serial_read_handle_t readHandle)**

This function Opens a reading handle for the serial manager module. The reading handle can not be opened multiple at the same time. The error code **kStatus_SerialManager_Busy** would be returned when the previous reading handle is not closed. And there can only be one buffer for receiving for the reading handle at the same time.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices.
<i>readHandle</i>	The serial manager module reading handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: SERIAL_MANAGER_READ_HANDLE_DEFINE(readHandle) ; or uint32_t readHandle[((SERIAL_MANAGER_READ_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];

Return values

<i>kStatus_SerialManager_-Error</i>	An error occurred.
<i>kStatus_SerialManager_-Success</i>	The reading handle is opened.
<i>kStatus_SerialManager_-Busy</i>	Previous reading handle is not closed.

Example below shows how to use this API to read data.

```
* static SERIAL_MANAGER_READ_HANDLE_DEFINE(s_serialReadHandle);
* SerialManager_OpenReadHandle((serial_handle_t)serialHandle,
*                               (serial_read_handle_t)s_serialReadHandle);
* static uint8_t s_nonBlockingBuffer[64];
* SerialManager_InstallRxCallback(
*   serial_read_handle_t)s_serialReadHandle,
*   APP_SerialManagerRxCallback,
*   s_serialReadHandle);
```

```
*   SerialManager_ReadNonBlocking(
    serial_read_handle_t)s_serialReadHandle,
*
*           s_nonBlockingBuffer,
*           sizeof(s_nonBlockingBuffer));
*
```

30.5.6 **serial_manager_status_t SerialManager_CloseReadHandle (serial_read_handle_t *readHandle*)**

This function Closes a reading for the serial manager module.

Parameters

<i>readHandle</i>	The serial manager module reading handle pointer.
-------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	The reading handle is closed.
---------------------------------------	-------------------------------

30.5.7 **serial_manager_status_t SerialManager_WriteBlocking (serial_write_handle_t *writeHandle*, uint8_t * *buffer*, uint32_t *length*)**

This is a blocking function, which polls the sending queue, waits for the sending queue to be empty. This function sends data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for transmission for the writing handle at the same time.

Note

The function [SerialManager_WriteBlocking](#) and the function [SerialManager_WriteNonBlocking](#) cannot be used at the same time. And, the function [SerialManager_CancelWriting](#) cannot be used to abort the transmission of this function.

Parameters

<i>writeHandle</i>	The serial manager module handle pointer.
--------------------	---

<i>buffer</i>	Start address of the data to write.
<i>length</i>	Length of the data to write.

Return values

<i>kStatus_SerialManager_-Success</i>	Successfully sent all data.
<i>kStatus_SerialManager_-Busy</i>	Previous transmission still not finished; data not all sent yet.
<i>kStatus_SerialManager_-Error</i>	An error occurred.

30.5.8 `serial_manager_status_t SerialManager_ReadBlocking (serial_read_handle_t readHandle, uint8_t * buffer, uint32_t length)`

This is a blocking function, which polls the receiving buffer, waits for the receiving buffer to be full. This function receives data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for receiving for the reading handle at the same time.

Note

The function `SerialManager_ReadBlocking` and the function `SerialManager_ReadNonBlocking` cannot be used at the same time. And, the function `SerialManager_CancelReading` cannot be used to abort the transmission of this function.

Parameters

<i>readHandle</i>	The serial manager module handle pointer.
<i>buffer</i>	Start address of the data to store the received data.
<i>length</i>	The length of the data to be received.

Return values

<i>kStatus_SerialManager_-Success</i>	Successfully received all data.
---------------------------------------	---------------------------------

<code>kStatus_SerialManager_- Busy</code>	Previous transmission still not finished; data not all received yet.
<code>kStatus_SerialManager_- Error</code>	An error occurred.

30.5.9 `serial_manager_status_t SerialManager_WriteNonBlocking (` `serial_write_handle_t writeHandle, uint8_t * buffer, uint32_t length)`

This is a non-blocking function, which returns directly without waiting for all data to be sent. When all data is sent, the module notifies the upper layer through a TX callback function and passes the status parameter `kStatus_SerialManager_Success`. This function sends data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for transmission for the writing handle at the same time.

Note

The function `SerialManager_WriteBlocking` and the function `SerialManager_WriteNonBlocking` cannot be used at the same time. And, the TX callback is mandatory before the function could be used.

Parameters

<code>writeHandle</code>	The serial manager module handle pointer.
<code>buffer</code>	Start address of the data to write.
<code>length</code>	Length of the data to write.

Return values

<code>kStatus_SerialManager_- Success</code>	Successfully sent all data.
<code>kStatus_SerialManager_- Busy</code>	Previous transmission still not finished; data not all sent yet.
<code>kStatus_SerialManager_- Error</code>	An error occurred.

30.5.10 `serial_manager_status_t SerialManager_ReadNonBlocking (` `serial_read_handle_t readHandle, uint8_t * buffer, uint32_t length)`

This is a non-blocking function, which returns directly without waiting for all data to be received. When all data is received, the module driver notifies the upper layer through a RX callback function and passes the

status parameter `kStatus_SerialManager_Success`. This function receives data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for receiving for the reading handle at the same time.

Note

The function `SerialManager_ReadBlocking` and the function `SerialManager_ReadNonBlocking` cannot be used at the same time. And, the RX callback is mandatory before the function could be used.

Parameters

<code>readHandle</code>	The serial manager module handle pointer.
<code>buffer</code>	Start address of the data to store the received data.
<code>length</code>	The length of the data to be received.

Return values

<code>kStatus_SerialManager_-Success</code>	Successfully received all data.
<code>kStatus_SerialManager_-Busy</code>	Previous transmission still not finished; data not all received yet.
<code>kStatus_SerialManager_-Error</code>	An error occurred.

30.5.11 `serial_manager_status_t SerialManager_TryRead(serial_read_handle_t readHandle, uint8_t * buffer, uint32_t length, uint32_t * receivedLength)`

The function tries to read data from internal ring buffer. If the ring buffer is not empty, the data will be copied from ring buffer to up layer buffer. The copied length is the minimum of the ring buffer and up layer length. After the data is copied, the actual data length is passed by the parameter length. And There can only one buffer for receiving for the reading handle at the same time.

Parameters

<code>readHandle</code>	The serial manager module handle pointer.
<code>buffer</code>	Start address of the data to store the received data.
<code>length</code>	The length of the data to be received.
<code>receivedLength</code>	Length received from the ring buffer directly.

Return values

<i>kStatus_SerialManager_-Success</i>	Successfully received all data.
<i>kStatus_SerialManager_-Busy</i>	Previous transmission still not finished; data not all received yet.
<i>kStatus_SerialManager_-Error</i>	An error occurred.

30.5.12 **serial_manager_status_t SerialManager_CancelWriting (serial_write_handle_t writeHandle)**

The function cancels unfinished send transmission. When the transfer is canceled, the module notifies the upper layer through a TX callback function and passes the status parameter [kStatus_SerialManager_-Canceled](#).

Note

The function [SerialManager_CancelWriting](#) cannot be used to abort the transmission of the function [SerialManager_WriteBlocking](#).

Parameters

<i>writeHandle</i>	The serial manager module handle pointer.
--------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	Get successfully abort the sending.
<i>kStatus_SerialManager_-Error</i>	An error occurred.

30.5.13 **serial_manager_status_t SerialManager_CancelReading (serial_read_handle_t readHandle)**

The function cancels unfinished receive transmission. When the transfer is canceled, the module notifies the upper layer through a RX callback function and passes the status parameter [kStatus_SerialManager_-Canceled](#).

Note

The function [SerialManager_CancelReading](#) cannot be used to abort the transmission of the function [SerialManager_ReadBlocking](#).

Parameters

<i>readHandle</i>	The serial manager module handle pointer.
-------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	Get successfully abort the receiving.
<i>kStatus_SerialManager_-Error</i>	An error occurred.

30.5.14 **serial_manager_status_t SerialManager_InstallTxCallback (** **serial_write_handle_t writeHandle, serial_manager_callback_t callback,** **void * callbackParam)**

This function is used to install the TX callback and callback parameter for the serial manager module. When any status of TX transmission changed, the driver will notify the upper layer by the installed callback function. And the status is also passed as status parameter when the callback is called.

Parameters

<i>writeHandle</i>	The serial manager module handle pointer.
<i>callback</i>	The callback function.
<i>callbackParam</i>	The parameter of the callback function.

Return values

<i>kStatus_SerialManager_-Success</i>	Successfully install the callback.
---------------------------------------	------------------------------------

30.5.15 **serial_manager_status_t SerialManager_InstallRxCallback (** **serial_read_handle_t readHandle, serial_manager_callback_t callback,** **void * callbackParam)**

This function is used to install the RX callback and callback parameter for the serial manager module. When any status of RX transmission changed, the driver will notify the upper layer by the installed callback

function. And the status is also passed as status parameter when the callback is called.

Parameters

<i>readHandle</i>	The serial manager module handle pointer.
<i>callback</i>	The callback function.
<i>callbackParam</i>	The parameter of the callback function.

Return values

<i>kStatus_SerialManager_-Success</i>	Successfully install the callback.
---------------------------------------	------------------------------------

30.5.16 static bool SerialManager_needPollingIsr(void) [inline], [static]

This function is used to check if need polling ISR.

Return values

<i>TRUE</i>	if need polling.
-------------	------------------

30.5.17 serial_manager_status_t SerialManager_EnterLowpower(serial_handle_t serialHandle)

This function is used to prepare to enter low power consumption.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer.
---------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	Successful operation.
---------------------------------------	-----------------------

30.5.18 serial_manager_status_t SerialManager_ExitLowpower(serial_handle_t serialHandle)

This function is used to restore from low power consumption.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer.
---------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	Successful operation.
---------------------------------------	-----------------------

30.5.19 void SerialManager_SetLowpowerCriticalCb (const serial_manager_lowpower_critical_CBs_t * *pfCallback*)

Parameters

<i>pfCallback</i>	Pointer to the function structure used to allow/disable lowpower.
-------------------	---

30.6 Serial Port Uart

30.6.1 Overview

Macros

- #define **SERIAL_PORT_UART_DMA_RECEIVE_DATA_LENGTH** (64U)
serial port uart handle size
- #define **SERIAL_USE_CONFIGURE_STRUCTURE** (0U)
Enable or disable the configure structure pointer.

Typedefs

- typedef enum
_serial_port_uart_parity_mode **serial_port_uart_parity_mode_t**
serial port uart parity mode
- typedef enum
_serial_port_uart_stop_bit_count **serial_port_uart_stop_bit_count_t**
serial port uart stop bit count

Enumerations

- enum **_serial_port_uart_parity_mode** {
 kSerialManager_UartParityDisabled = 0x0U,
 kSerialManager_UartParityEven = 0x2U,
 kSerialManager_UartParityOdd = 0x3U }
serial port uart parity mode
- enum **_serial_port_uart_stop_bit_count** {
 kSerialManager_UartOneStopBit = 0U,
 kSerialManager_UartTwoStopBit = 1U }
serial port uart stop bit count

30.6.2 Enumeration Type Documentation

30.6.2.1 enum _serial_port_uart_parity_mode

Enumerator

kSerialManager_UartParityDisabled Parity disabled.
kSerialManager_UartParityEven Parity even enabled.
kSerialManager_UartParityOdd Parity odd enabled.

30.6.2.2 enum _serial_port_uart_stop_bit_count

Enumerator

kSerialManager_UartOneStopBit One stop bit.

kSerialManager_UartTwoStopBit Two stop bits.

30.7 Serial Port SWO

30.7.1 Overview

Data Structures

- struct `_serial_port_swo_config`
serial port swo config struct [More...](#)

Macros

- #define `SERIAL_PORT_SWO_HANDLE_SIZE` (12U)
serial port swo handle size

Typedefs

- typedef enum
`_serial_port_swo_protocol` `serial_port_swo_protocol_t`
serial port swo protocol
- typedef struct
`_serial_port_swo_config` `serial_port_swo_config_t`
serial port swo config struct

Enumerations

- enum `_serial_port_swo_protocol` {
`kSerialManager_SwoProtocolManchester` = 1U,
`kSerialManager_SwoProtocolNrz` = 2U }
serial port swo protocol

30.7.2 Data Structure Documentation

30.7.2.1 struct `_serial_port_swo_config`

Data Fields

- `uint32_t clockRate`
clock rate
- `uint32_t baudRate`
baud rate
- `uint32_t port`
Port used to transfer data.
- `serial_port_swo_protocol_t protocol`
SWO protocol.

30.7.3 Enumeration Type Documentation

30.7.3.1 enum _serial_port_swo_protocol

Enumerator

kSerialManager_SwoProtocolManchester SWO Manchester protocol.

kSerialManager_SwoProtocolNrz SWO UART/NRZ protocol.

Chapter 31

Enet_cmsis_driver

This section describes the programming interface of the ENET Cortex Microcontroller Software Interface Standard (CMSIS) driver. This driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method see <http://www.keil.com/pack/doc/cmsis/Driver/html/index.html>.

The ENET CMSIS driver includes transactional APIs.

Transactional APIs are transaction target high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code accessing the hardware registers.

31.1 Typical use case

```
void ENET_SignalEvent_t(uint32_t event)
{
    if (event == ARM_ETH_MAC_EVENT_RX_FRAME)
    {
        uint32_t size;
        uint32_t len;

        /* Get the Frame size */
        size = EXAMPLE_ENET.GetRxFrameSize();
        /* Call ENET_ReadFrame when there is a received frame. */
        if (size != 0)
        {
            /* Received valid frame. Deliver the rx buffer with the size equal to length. */
            uint8_t *data = (uint8_t *)malloc(size);
            if (data)
            {
                len = EXAMPLE_ENET.ReadFrame(data, size);
                if (size == len)
                {
                    /* Increase the received frame numbers. */
                    if (g_rxIndex < ENET_EXAMPLE_LOOP_COUNT)
                    {
                        g_rxIndex++;
                    }
                }
                free(data);
            }
        }
    }
    if (event == ARM_ETH_MAC_EVENT_TX_FRAME)
    {
        g_testTxNum++;
    }
}

/* Initialize the ENET module. */
EXAMPLE_ENET.Initialize(ENET_SignalEvent_t);
```

```

EXAMPLE_ENET.PowerControl(ARM_POWER_FULL);
EXAMPLE_ENET.SetMacAddress((ARM_ETH_MAC_ADDR *)g_macAddr);
EXAMPLE_ENET.Control(ARM_ETH_MAC_CONFIGURE, linkInfo.speed << ARM_ETH_MAC_SPEED_Pos | linkInfo.duplex << ARM_ETH_MAC_DUPLEX_Pos | ARM_ETH_MAC_ADDRESS_BROADCAST);
EXAMPLE_ENET_PHY.PowerControl(ARM_POWER_FULL);
EXAMPLE_ENET_PHY.SetMode(ARM_ETH_PHY_AUTO_NEGOTIATE);
EXAMPLE_ENET.Control(ARM_ETH_MAC_CONTROL_RX, 1);
EXAMPLE_ENET.Control(ARM_ETH_MAC_CONTROL_TX, 1);
if (EXAMPLE_ENET_PHY.GetLinkState() == ARM_ETH_LINK_UP)
{
    linkInfo = EXAMPLE_ENET_PHY.GetLinkInfo();
}
else
{
    PRINTF("\r\nPHY Link down, please check the cable connection and link partner setting.\r\n");
}

/* Build broadcast for sending. */
ENET_BuildBroadCastFrame();

while (1)
{
    /* Check the total number of received number. */
    if (g_rxCheckIdx != g_rxIndex)
    {
        PRINTF("The %d frame has been successfully received!\r\n", g_rxIndex);
        g_rxCheckIdx = g_rxIndex;
    }
    if (g_testTxNum && (g_txCheckIdx != g_testTxNum))
    {
        g_txCheckIdx = g_testTxNum;
        PRINTF("The %d frame transmitted success!\r\n", g_txCheckIdx);
    }
    /* Get the Frame size */
    if (txnumber < ENET_EXAMPLE_LOOP_COUNT)
    {
        txnumber++;
        /* Send a multicast frame when the PHY is link up. */
        if (EXAMPLE_ENET.SendFrame(&g_frame[0], ENET_DATA_LENGTH, ARM_ETH_MAC_TX_FRAME_EVENT) == ARM_DRIVER_OK)
        {
            for (uint32_t count = 0; count < 0x3FF; count++)
            {
                __ASM("nop");
            }
        }
        else
        {
            PRINTF("\r\nTransmit frame failed!\r\n");
        }
    }
}

```

31.1.1 CODEC Adapter

31.1.1.1 Overview

Enumerations

- enum {

kCODEC_WM8904,
 kCODEC_WM8960,
 kCODEC_WM8524,
 kCODEC_SGTL5000,
 kCODEC_DA7212,
 kCODEC_CS42888,
 kCODEC_CS42448,
 kCODEC_AK4497,
 kCODEC_AK4458,
 kCODEC_TFA9XXX,
 kCODEC_TFA9896,
 kCODEC_WM8962,
 kCODEC_PCM512X,
 kCODEC_PCM186X }
- codec type*

31.1.1.2 Enumeration Type Documentation

31.1.1.2.1 anonymous enum

Enumerator

kCODEC_WM8904	wm8904
kCODEC_WM8960	wm8960
kCODEC_WM8524	wm8524
kCODEC_SGTL5000	sgtl5000
kCODEC_DA7212	da7212
kCODEC_CS42888	CS42888.
kCODEC_CS42448	CS42448.
kCODEC_AK4497	AK4497.
kCODEC_AK4458	ak4458
kCODEC_TFA9XXX	tfa9xxx
kCODEC_TFA9896	tfa9896
kCODEC_WM8962	wm8962
kCODEC_PCM512X	pcm512x
kCODEC_PCM186X	pcm186x

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