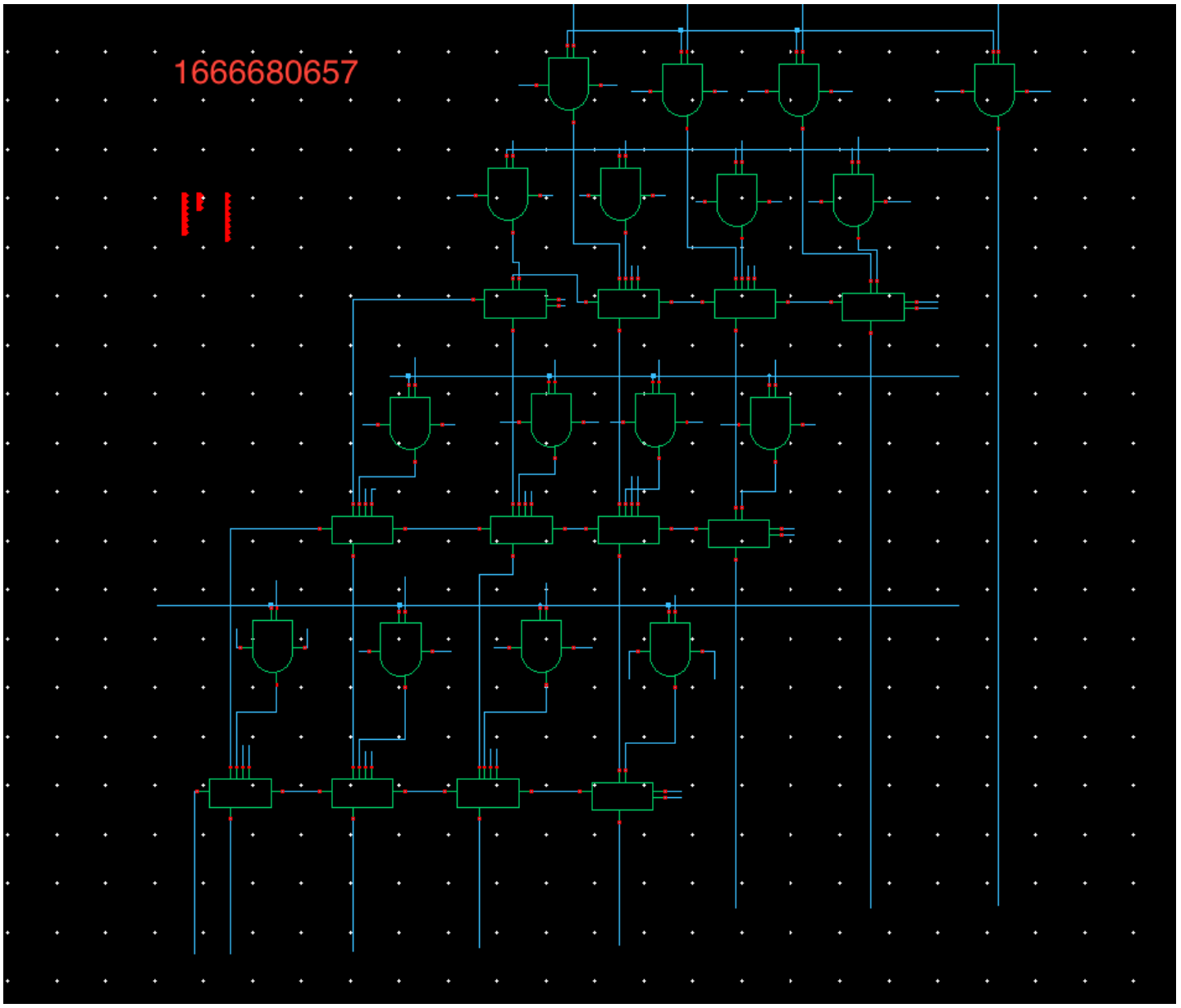
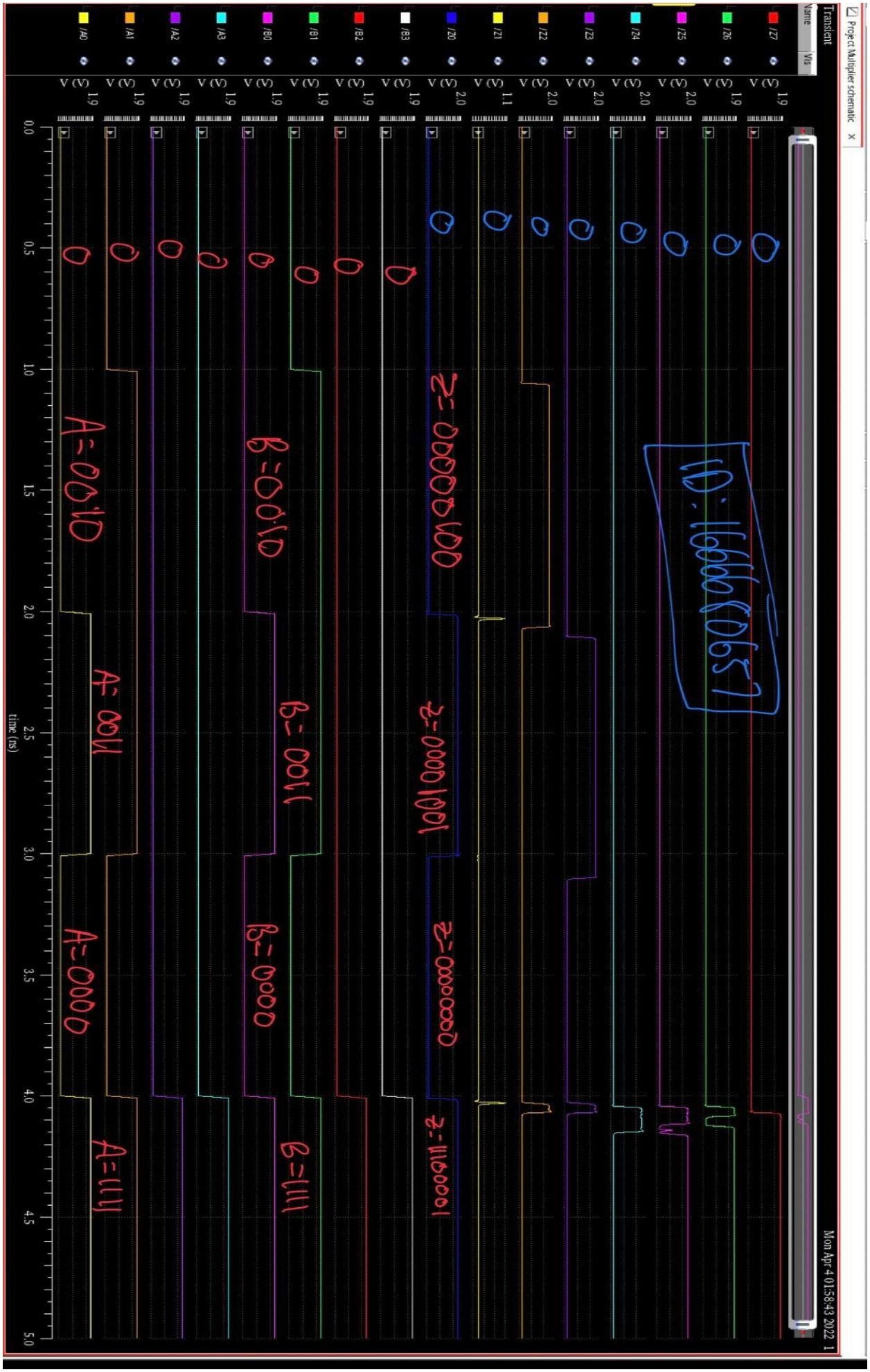
EE 477 - Project
Phase 1 Report

Part 1(Multiplier):

- **Schematic:**



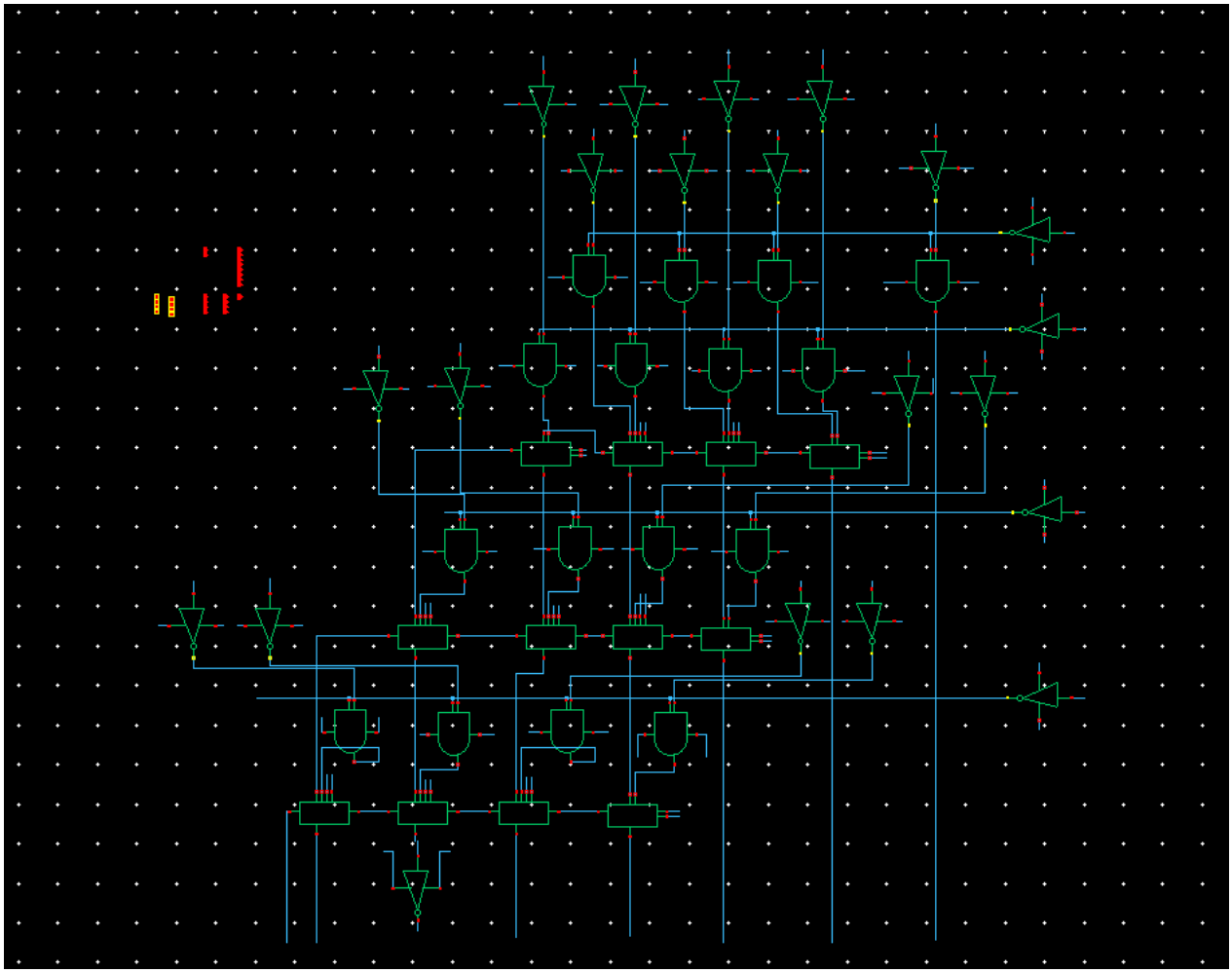
- **Functionality Verification:**



- **Inputs and expected outputs:**

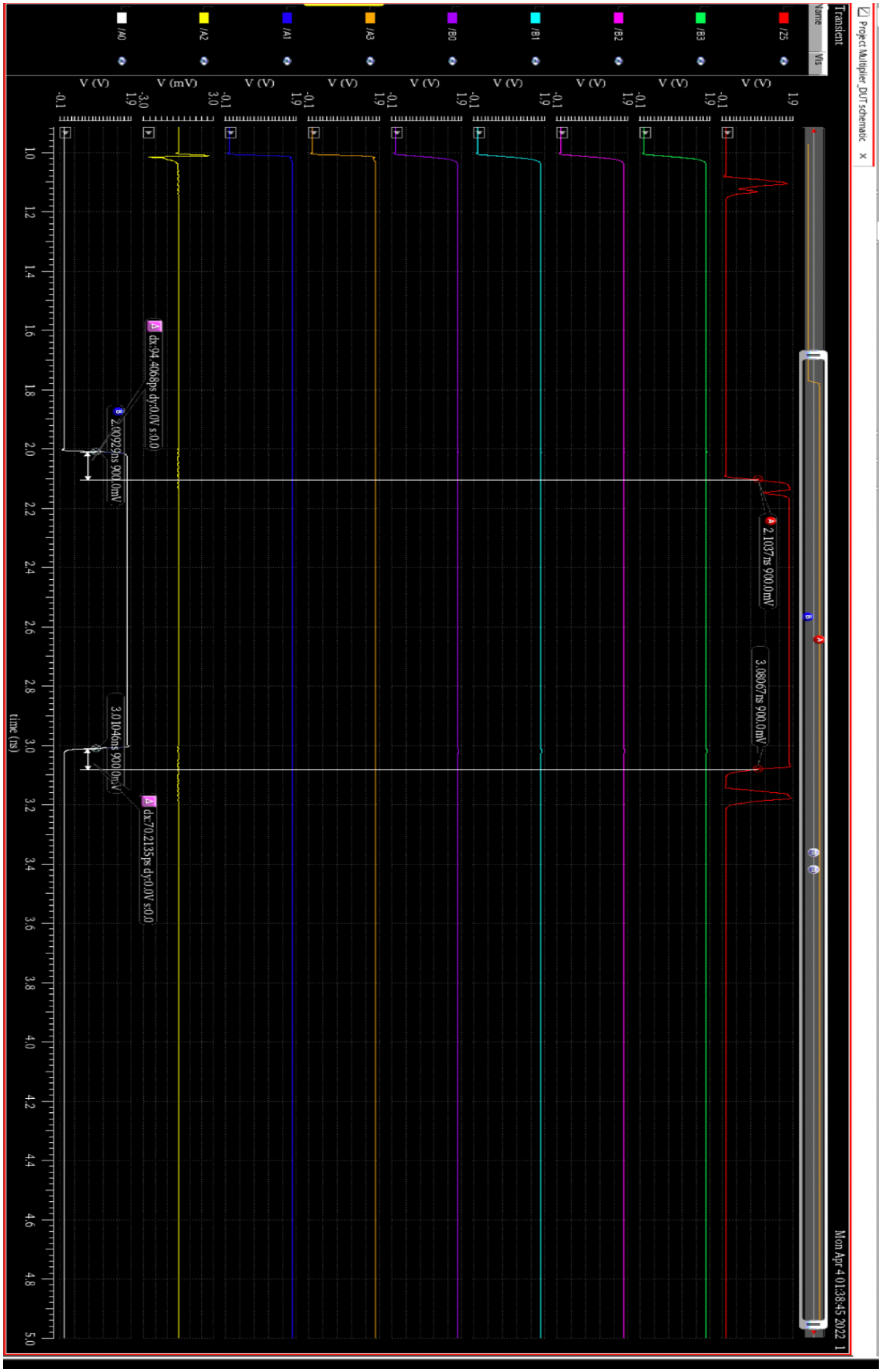
Input A	Input B	Expected Output
0000	0000	00000000
0010	0010	00000100
0011	0011	00001001
1111	1111	11100001

- Multiplier DUT schematic:



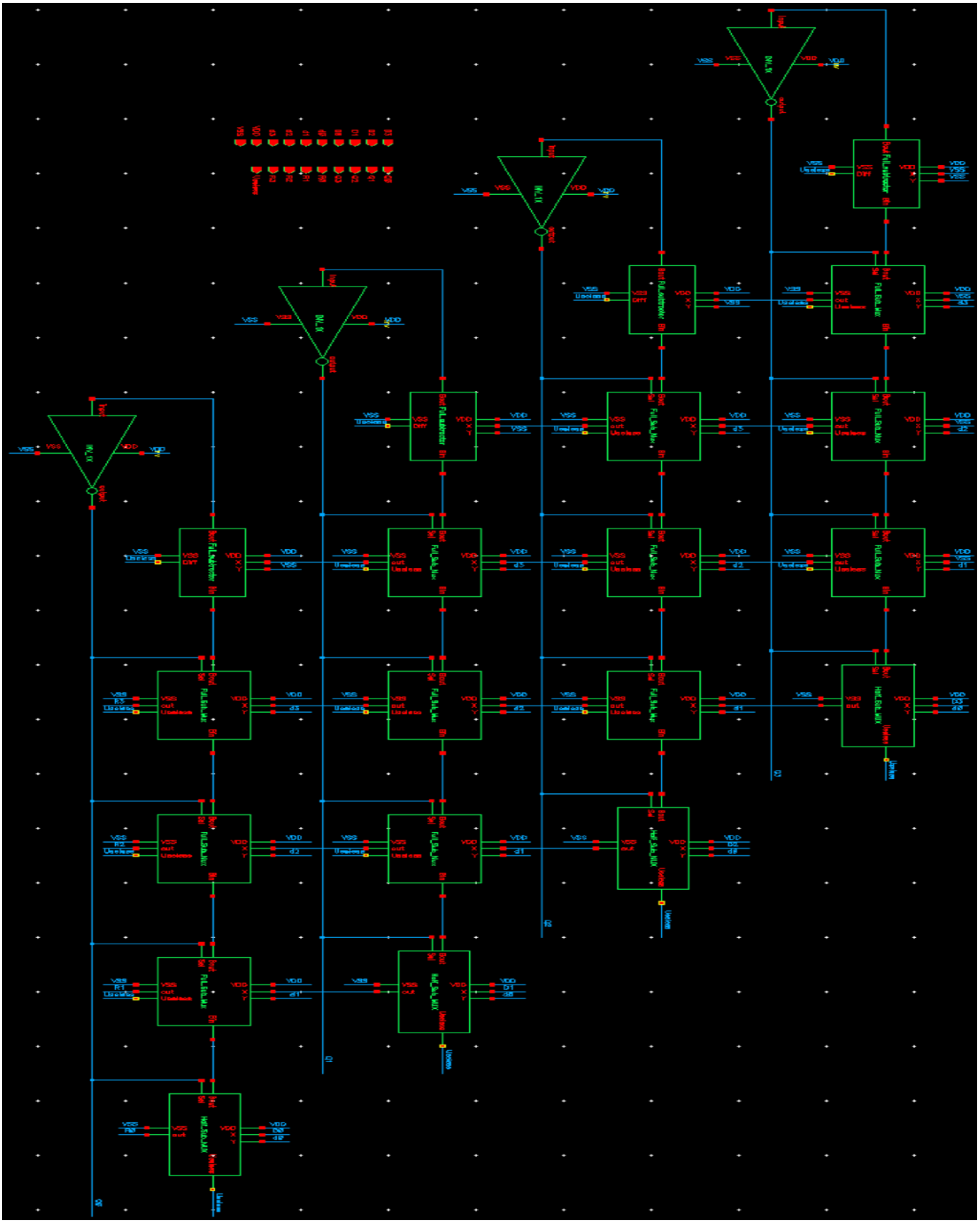
- **Multiplier DUT Propagation Delay:**
  - Rising delay = **94.4068 ps**
  - Falling delay = **70.2135 ps**
  - (Proof shown in figure on following page)

- Multiplier DUT Delay Functionality Waveform:



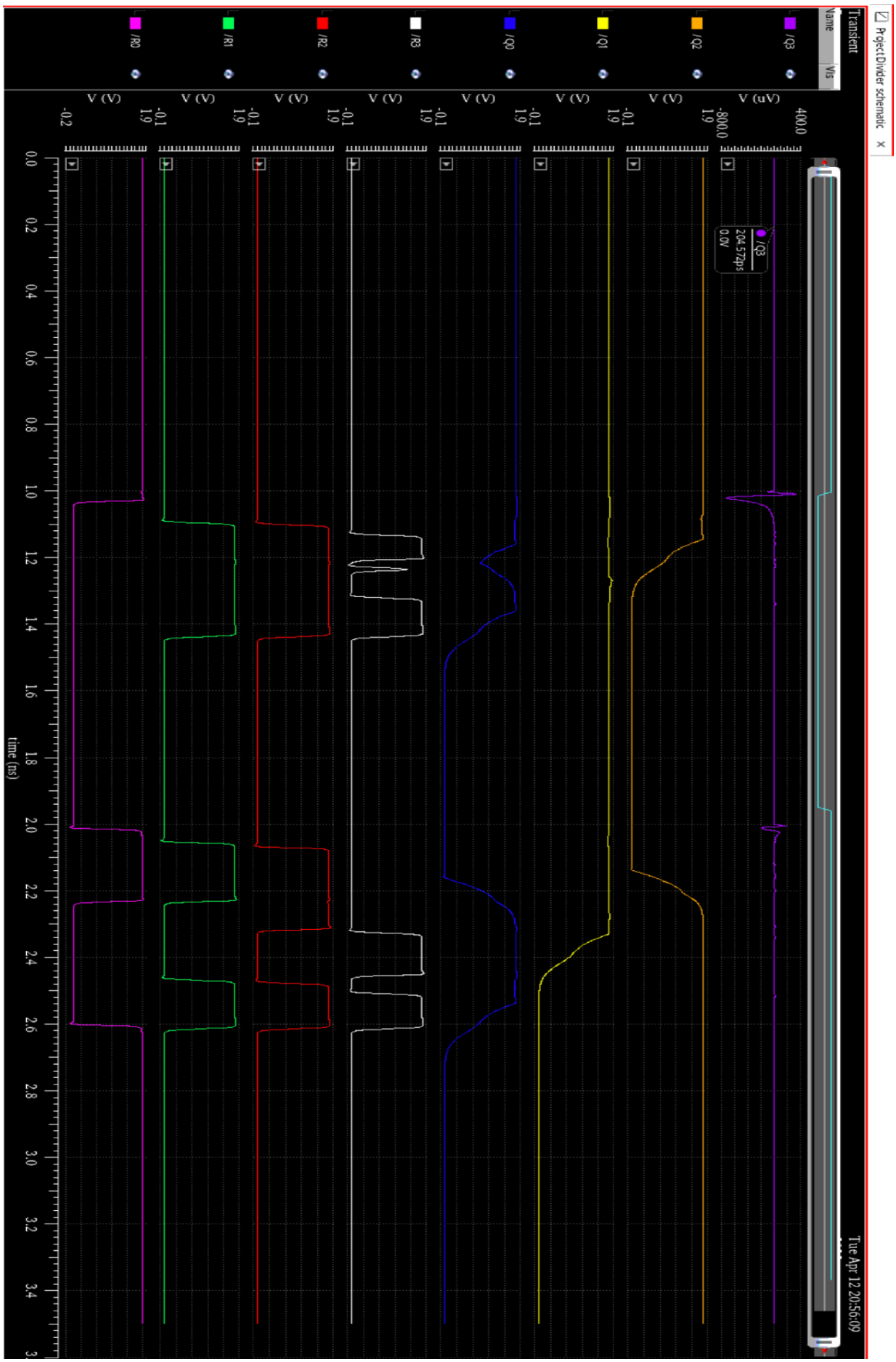
Part 2(Divider):

- **Schematic:**



(Flip page horizontally to see)

- **Functionality Verification:**



- **Inputs applied and expected outputs:**
    - From 0 ns to 1 ns:
        - D = **1111**, d = **0010**
        - Expected Q = **0111**, Expected R = **0001**
    - From 1 ns to 2 ns:
        - D = **0100**, d = **0010**
        - Expected Q = **0010**, Expected R = **0000**
    - From 2 ns to 3.5 ns:
        - D = **1101**, d = **0011**
        - Expected Q = **0100**, Expected R = **0001**