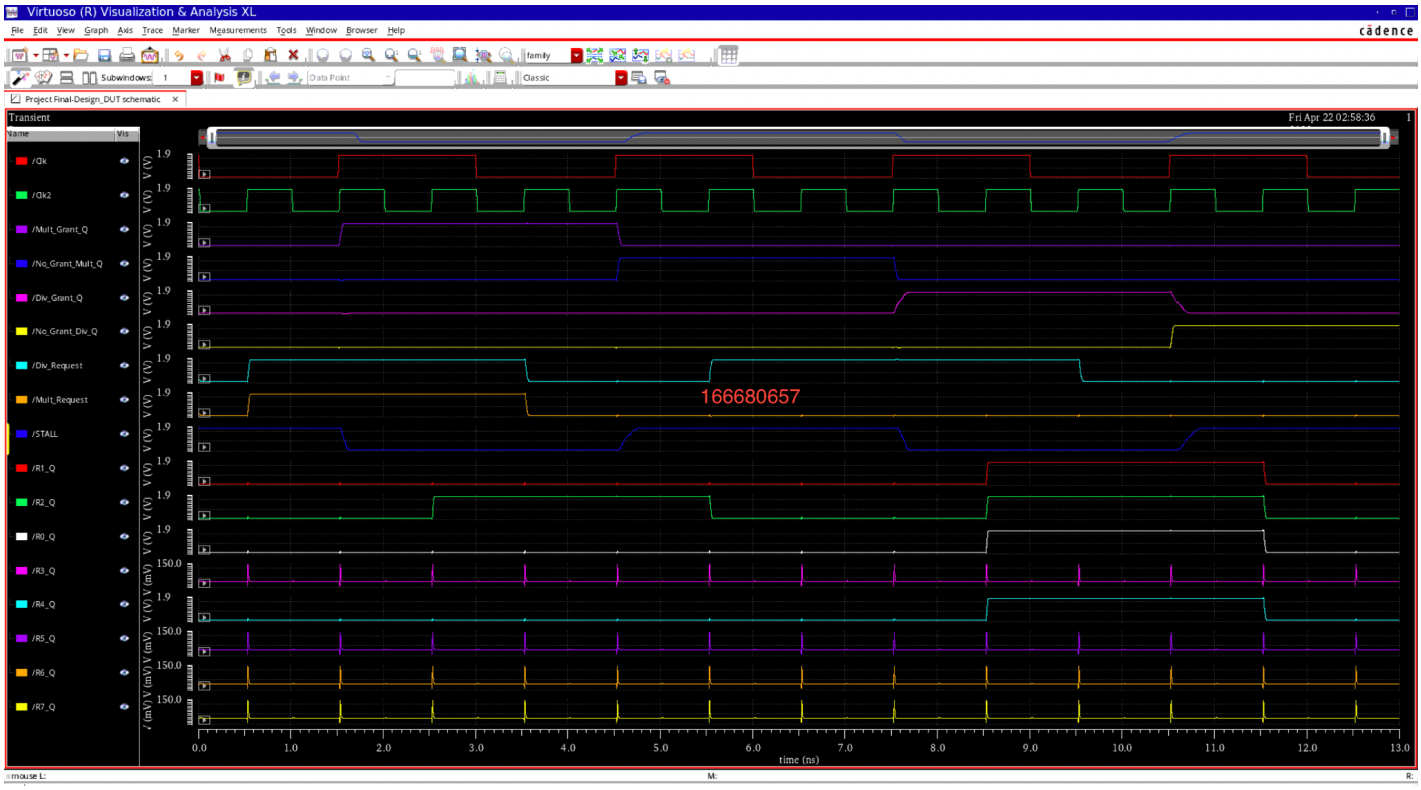
EE477 Phase 2 Report

Functional Analysis



States:

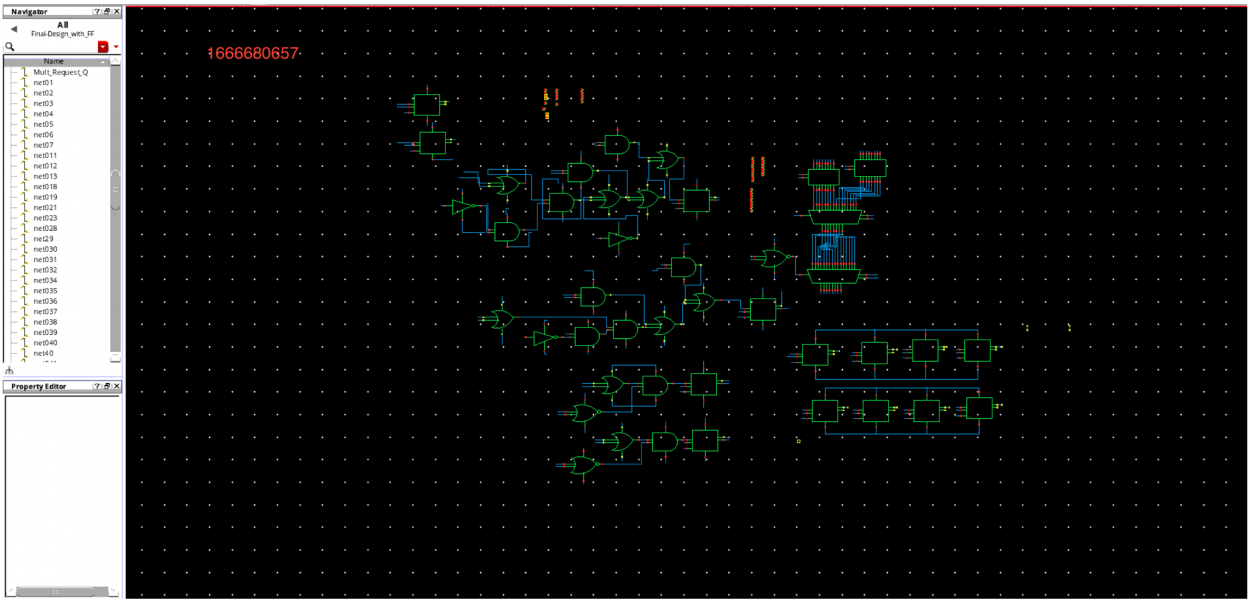
1. Mult_Grant_Q: Multiplier has been granted access to output bus
2. Div_Grant_Q: Divider has been granted access to output bus
3. No_Grant_Mult_Q: No one requests access. Previous state was Mult_Grant_Q
4. No_Grant_Div_Q: No one requests access. Previous state was Div_Grant_Q

1 Hot encoding was used and therefore 4 Flip-Flops were needed to store the state. It can be seen in the figure above that no one state is HIGH at the same time. This design is also a Moore machine as we didn't feel the need to use the current state in our Output Function Logic.

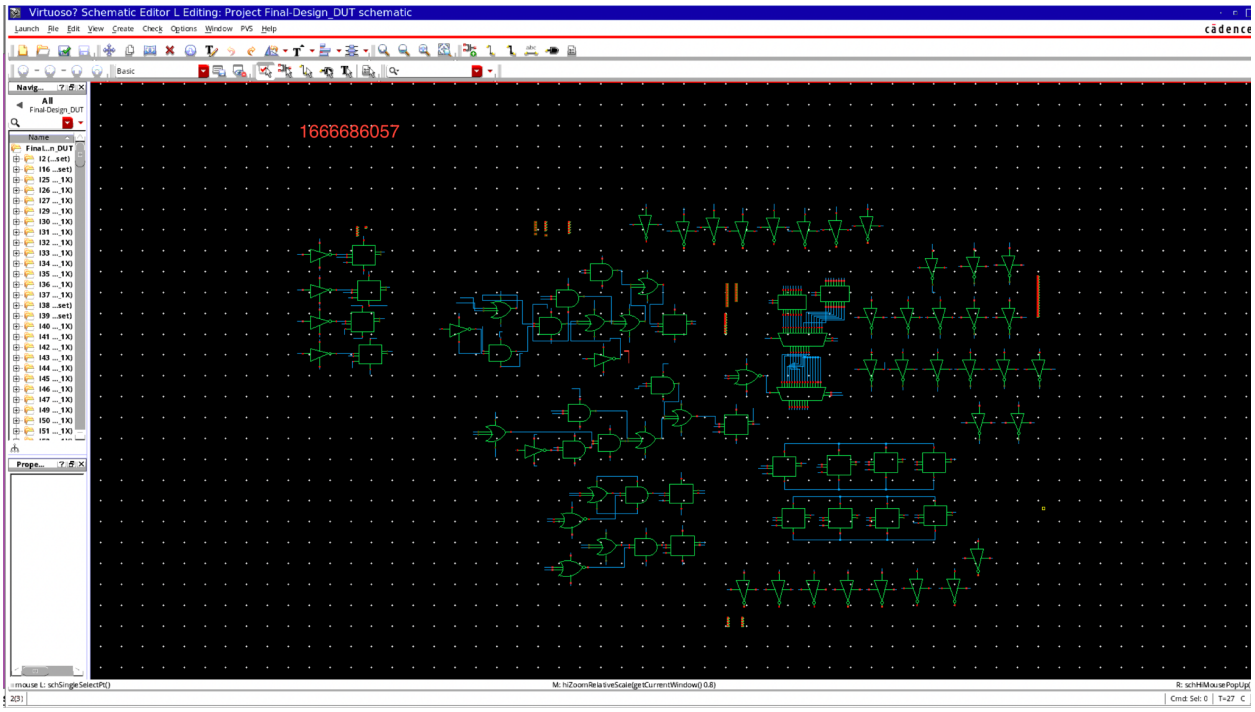
For simplicity, Multiplier inputs were 0010 (A3-A0) & 0010 (B3-B0) the entire simulation period
Expected result was 00000100 (4decimal)
Likewise, Divider inputs were 1111 (Di3-Di0) and 0010 (d3-d0). Expected result was 0111 (Q3-Q0) and 0001 (R3-R0) or 7 remainder 1 in decimal.

2 clocks were used (333MHz for the state machine and 1GHz for input/output flip flops). The minimum time period for the state machine flip flops was 3ns. The minimum time period for the flip flops recording inputs and outputs was 1ns.

Schematic



(Non-DUT above)



(DUT above)

Citations: Flip flop design was adopted from

https://en.wikipedia.org/wiki/Flip-flop_(electronics)#/media/File:True_single-phase_edge-triggered_flip-flop_with_reset.svg