ECE552: Lab 1 Report

October 8th, 2021 | Student Names: Andreea Varlan & Ben Pak

Performance Slowdown

The calculated CPI for both questions resulted in **1.33.** This signifies a performance slowdown of 33%.

$$(CPI_{new} - CPI_{old}) / CPI_{old} = (1.33 - 1.00) / 1.00 = 0.33 \Rightarrow 33\% \text{ slowdown}$$

Microbenchmark Statistic Collection and Correctness Review

In the sim-safe file, we added the following statistics:

- sim_num_RAW_hazard_q1/q2_stall1cycle: total number of RAW hazards for the 5/6-stage pipeline that require 1-cycle stall
- sim_num_RAW_hazard_q1/q2_stall2cycle: total number of RAW hazards for the 5/6-stage pipeline that require 2-cycle stalls
- formula for CPI_from_RAW_hazard_q1/q2: " 1 (ideal CPI) + ∑stall_frequency * stall_cycles"
  - as stall_frequency = num_hazards/total_num_insn, the CPI calculation for our cases becomes: "1 + sim_num_RAW_hazard_q1/q2_stall2cycle/sim_num_insn * 2 + sim_num_RAW_hazard_q1/q2_stall1cycle/sim_num_insn * 1"

```
                          1  2  3  4  5  6  7
I1  addu    $17,$16,2 | F  D  X  M  W
I2  addu    $16,$16,6 |    F  D  X  M  W
I3  addu    $18,$17,5 |    F  d* D  X  M  W
```

Reg $17 is written at I1 and read at I3; this creates a RAW hazard since there is no bypassing or forwarding for the 5 stage pipeline; we have a hazard **once** which requires **1 data cycle stall** during I3 to have reg $17 written in the first half of cycle 5 in WriteBack stage, and ready in the 2nd half of the cycle in the Decode stage of I3.

```
                          1  2  3  4  5  6  7  8  9  10 11
I4  addu    $3,$3,1     | F  D  X  M  W
I5  slt     $2,$3,$4    |    F  d* d* D  X  M  W
I6  bne     $2,$0,$L17  |       p* p* F  d* d* D  X  M  W
```

We observe **two 2-cycl**e stall data hazards caused by RAW hazard of reg $3 between I4 and I5, and reg $2 between I5 and I6. In both cases we need to wait until WB of the first insn to write the value of the reg in the first half of the cycle for the Decode of the next insn to use the correct value in the second half of the cycle.

From the sim-safe statistic output we get:

```
sim_num_RAW_hazard_q1_stall1cycle    100001217
sim_num_RAW_hazard_q1_stall2cycle    200003553
```

As our microbenchmark loop iterates 100000000 times, we can deduce that indeed 1 hazard requiring 1 -cycle stall (100001217 / 100000000 ~= 1), and two hazards requiring 2-cycle stalls (200003553 / 100000000 ~= 2)

We used the Optimization 1 (O1) compilation flag.