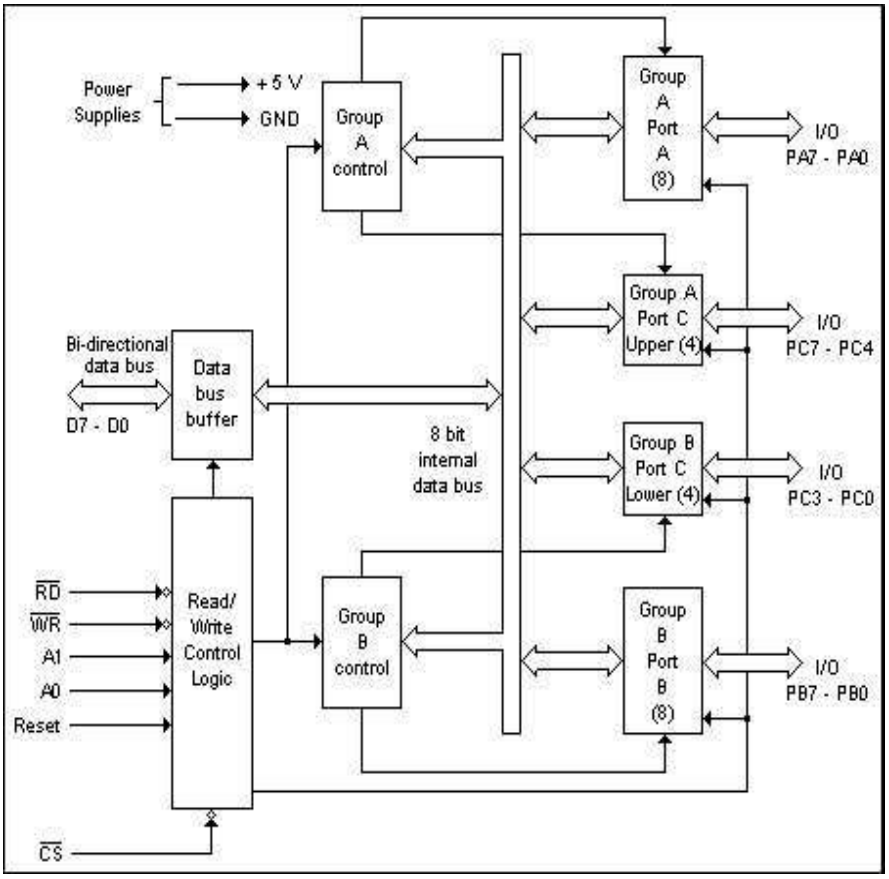
UNIT-IV

PPI 8255A

A programmable interface device is designed to perform various input/output functions. Such a device can be set up to perform specific functions by writing an instruction in its internal register, called the control register, and the instruction written to this control register is known as control word.

Functions can be changed anytime during execution of the program by writing a new instruction in the control register.

Block Diagram:



Data Bus Buffer

This Tri-state Bi-Directional 8-bit buffer is used to interface the 8255 to the system data bus.

Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU.

Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words.

It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

1.Chip Select: A "low" on this input pin enables the communication between the 8255 and the CPU.

2.Read: A "low" on this input pin enables 8255 to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255.

3.Write: A "low" on this input pin enables the CPU to write data or control words into the 8255.

4. (A0 and A1) Port Select 0 and Port Select 1: These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

5. (RESET)Reset: A "high" on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode.

A1	A0	SELECTION
0	0	PORT A
0	1	PORT B
1	0	PORT C
1	1	CONTROL

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Ports A, B, and C

The 8255 contains three 8-bit ports (A, B, and C).

All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull- up" and "pull-down" bus-hold devices are present on Port A.

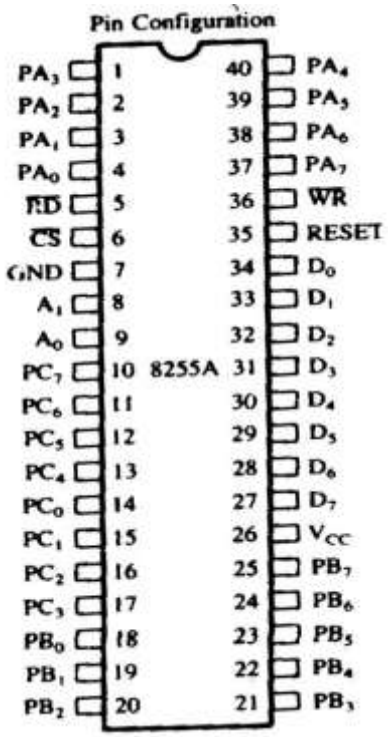
Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B.

PIN DIAGRAM:

8255 is a 40 pin chip. It has three ports Port A, B and C. Each port has 8 lines. Port A PA0 to PA7, Port B PB0 to PB7 and Port C PC0 to PC7.

Each pin can be used as input pin or output pin. It can be configured from control word of 8255.



Port C has three functions.

It can be used as Simple I/O ports.

It can also be used to provide handshake signals

It can also be used in Bit Set/Reset (BSR) mode to switch ON or OFF devices.

Port C can be used as two 4-bit ports also.

Same way it has D0 to D7, these lines are connected to D0 to D7 of 8085. These lines bring data to and from 8255.

There are SIX control signals associated with 8255.

1. Chip select signal, it is active low signal, when it is low it enables the 8255.
2. RESET It is used to reset all ports, control word and status word to initial values.
3. It is connected with 8085, whenever it goes low, 8255 will perform Read operation.
4. It is connected with 8085, whenever it goes low, 8255 will perform Write operation.
5. A0, A1 These are the address lines, based on status of A0 and A1, ports will be selected.

A1	A0	Port Selection
0	0	Port A
0	1	Port B
1	0	Port C

There are two power signals.

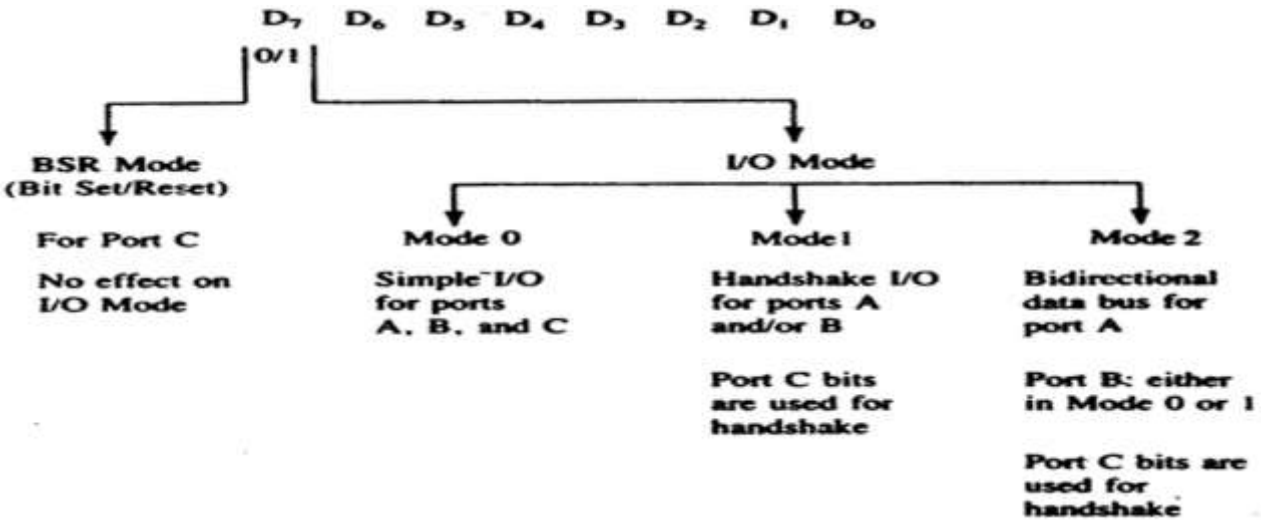
Vcc connected to 5 V

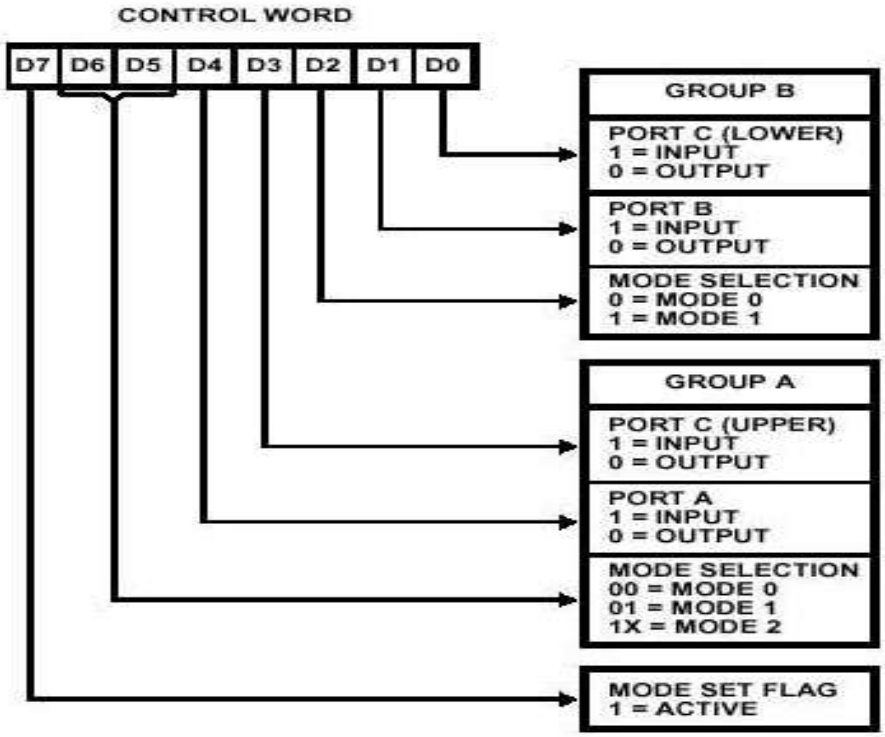
GND connected to ground.

To communicate with peripherals through 8255A, three steps are necessary:

1. Determine the address of Port A, B and C and of the control register according to the Chip Select logic and address lines A0 and A1.
2. Write a control word in the control register.
3. Write I/O instructions to communicate with peripherals through ports A, B and C

Control Word





Mode selection:

There are three basic modes of operation that can be selected by the system software.

1) Mode 0: Basic Input/Output

2) Mode 1: Strobes Input/Output

3) Mode 2: Bi-directional bus

Example: (Mode-0 I/O Mode):

Identify Port address

Identify mode-0 control word to configure port A and CUpper as output ports and port B and CLower as input ports.

Write a program to read DIP switches and display reading from port B to port A and port CLower to port CUpper

Solution:

Port Address: It should be clear from interfacing circuit, that it has memory related operations. So, it is memory mapping. A15 is connected with Chip select and A1 and A0 with A1 and A0 of 8255

A15	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**Port**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Port A**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**Port B**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**Port C**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**Contro l**

Control word:

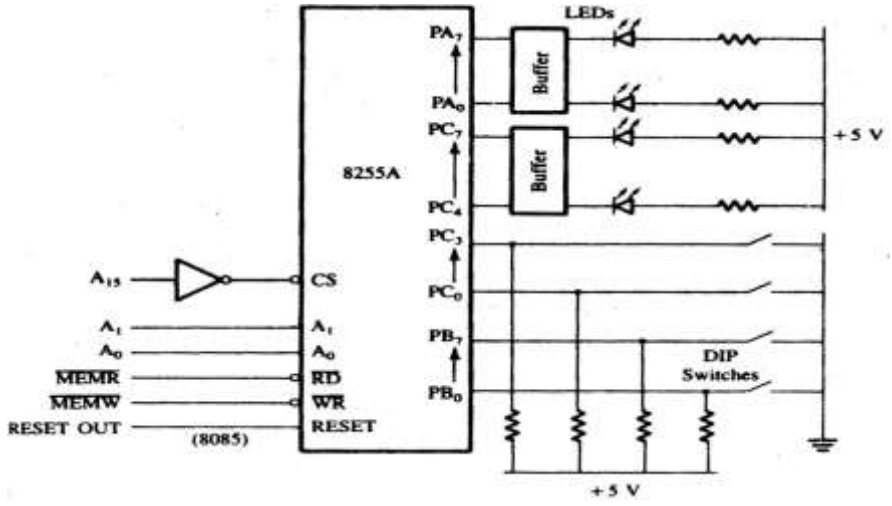
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Control Word**
1	0	0	0	0	0	1	1	83H

Program:

-

Instructions	Comments
MVI A, 83h	Load Control Word
STA 8003h	Write into Control Register
LDA 8001h	Read switches at port B

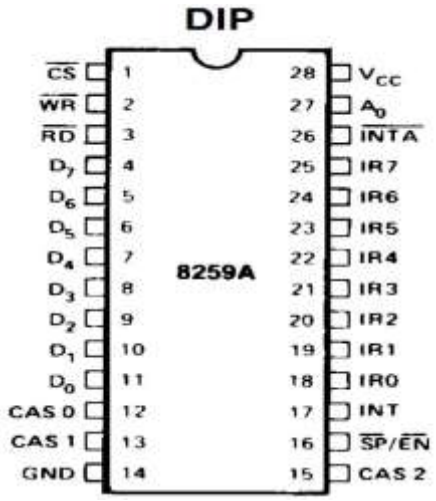
STA 8000h	Display at port A
LDA 8002h	Read switches at port CL
ANI 0Fh	Mask higher bits
RLC	
RLC	
RLC	
RLC	
STA 8002h	Display switches at port CU
HLT	



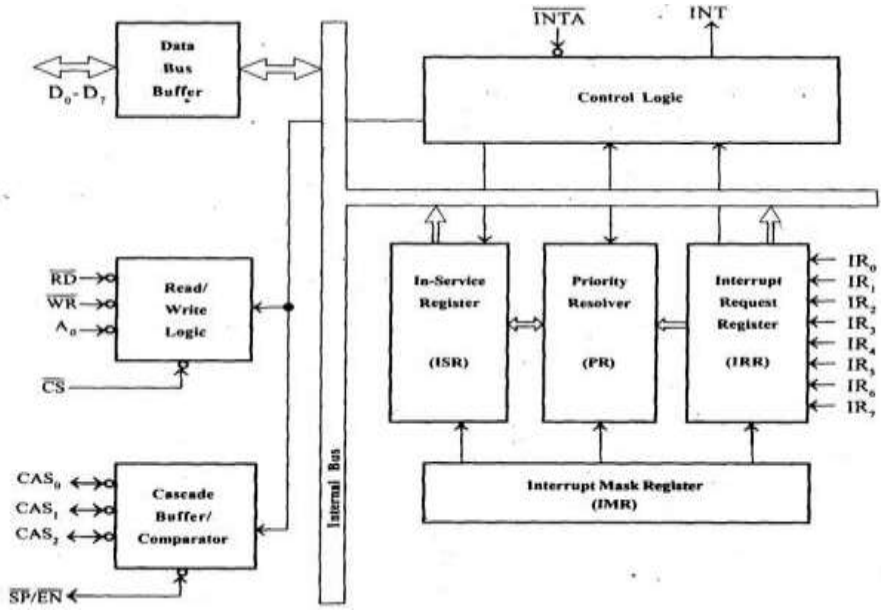
PIC 8259A

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts.

PIN DIAGRAM



Block Diagram



Symbol	Pin No.	Type	Name and Function
V_{CC}	28	I	**SUPPLY:** +5V Supply.
GND	14	I	**GROUND**
$\overline{CS}$	1	I	**CHIP SELECT:** A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 8259A. INTA functions are independent of CS.
$\overline{WR}$	2	I	**WRITE:** A low on this pin when CS is low enables the 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	**READ:** A low on this pin when CS is low enables the 8259A to release status onto the data bus for the CPU.
D_7-D_0	4–11	I/O	**BIDIRECTIONAL DATA BUS:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0-CAS_2	12, 13, 15	I/O	**CASCADE LINES:** The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	**SLAVE PROGRAM/ENABLE BUFFER:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**INTERRUPT:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0-IR_7	18–25	I	**INTERRUPT REQUESTS:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	**INTERRUPT ACKNOWLEDGE:** This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	**AO ADDRESS LINE:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 8086, 8088).

Read/Write Logic

It is typical R/W logic.

When address line A0 is at logic 0, the controller is selected to write a command word or read status

Control Logic

It has two pins: INT as output and INTA as input. The INT is connected to INTR pin of MPU

Interrupt Request Register (IRR) and Interrupt In-Service Register (ISR) Interrupt input lines are handled by two registers in cascade IRR and ISR IRR is used to store all interrupt which are requesting service.

ISR is used to store all interrupts which are being serviced

Priority Resolver

This logic block determines the priorities of the bit set in IRR.

Highest priority is selected and strobed into corresponding bit of ISR during INTA pulse.

Interrupt Mask Register

It stores bits which mask the interrupt lines to be masked

IMR operates on the IRR. Masking of high priority input will not affect the interrupt request lines

- Functional block diagram stores and compares the IDs of 8259's used in

Cascade Buffer / Comparator

system

Associated three input lines CAS0-2 are used as output lines when 8259 is used as Master and input lines when 8259 is used as slave

As a master 8259 send the address of slave 8259 onto the CAS0-2 lines.

Interrupt operation

To implements interrupts, the interrupt enable flip flop in the microprocessor should be enable by writing the EI instruction, and 8259A should be initialized by writing control words into control register.

The 8259A require two types command word: Initialization command words (ICW) and Operation command words (OCW).

ICWs are used to set up the proper condition and specify RST vector addresses. 8259A must be initialized by writing two to four command words into the respective command word registers.

The OCWs are used to perform function such as masking interrupts, setting up status read operations, etc. After 8258A initialized, the following sequence of events occurs when one or more interrupt request lines go high.

1) The IRR store the request
2) The priority resolver checks three registers: the IRR for interrupt requests, the IMR for the masking bits, and the ISR for the interrupt request being served. It resolve the priority and set the INT high when appropriate.
3) The MPU acknowledges the Interruptby sending $\overline{\text{INTA}}$ pulse.

4) After $\overline{\text{INTA}}$ is received, the appropriate priority bit in the ISR is set to indicate which interrupt level being served, and corresponding bit in the IRR is reset to indicate that the request is accepted. Then, the opcode for the CALL instruction is placed on the data bus.

5) When MPU decode CALL instruction; it placed two more $\overline{\text{INTA}}$ signal on the data bus.

6) When 8259A receive second $\overline{\text{INTA}}$, it placed lower order byte of the CALL address on the data bus. At the third $\overline{\text{INTA}}$, it places the high-order byte on the data bus. The CALL address is the vector memory location for the interrupt; this address is placed in the control register during the initialization.

7) During the third $\overline{\text{INTA}}$ pulse, the ISR bit is reset either automatically(Automatic End Of Interrupt-AEOI) or by command word that must be issued at the end of the service routine(End Of Interrupt).This option is determined by the initialization command word(ICW).

8) The program sequence is transferred to the memory location specified by the CALL instruction.

OPERATING MODES OF 8259

The different modes of operation of 8259A can be programmed by setting or resting the appropriate bits of the ICWs or OCWs.

The different modes of operation of 8259A are explained in the following text.

Fully Nested Mode

This is the default mode of operation of 8259A. IR0 has the highest priority and IR7 has the lowest one.

In addition, any IR can be assigned the highest priority in this mode; the priority sequence will then begin at that IR. In this example below, IR4has the highest priority, and IR3has lowest priority.

IR0	IR1	IR2	IR3	IR4	IR5	IR6	IR7
4	5	6	7	0	1	2	3

Automatic Rotation Mode

In this mode, a device, after being serviced, received lowest priority. Assuming that the IR2has just been

serviced, it will receive the seventh priority, as shown below:

IR0	IR1	IR2	IR3	IR4	IR5	IR6	IR7
1	6	7	0	1	2	3	4

9) Specific Rotation mode

This is similar to automatic rotationmode, except that user can select any IR for the lowest priority, thus fixing all priorities.

End of Interrupt (EOI)

After the completion of an interrupt service, the corresponding IR bit needs to be reset to update the information in the ISR. This is called End of interrupt(EOI) command.it can issued in three formats:

1) Specific EOI commands

When this command send to 8259A, it reset the highest priority ISR bit.

2) Non-specific EOI commands.

This command specifies which ISR bit to reset.

3) Automatic EOI Mode

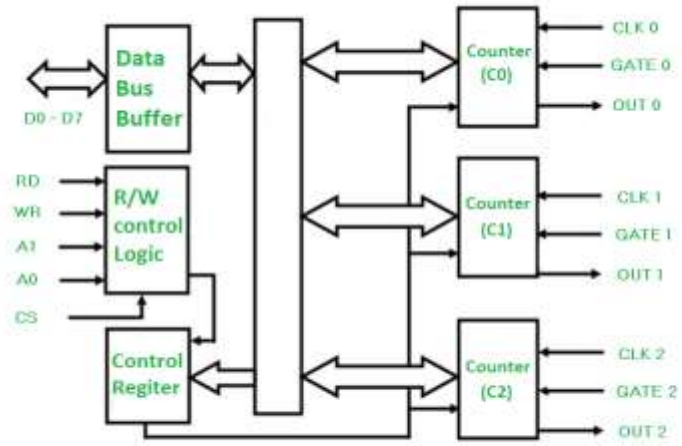
In this mode no command is necessary. During the third $\overline{\text{INTA}}$, the ISR bit is reset. The major drawback with this mode is that the ISR does not have information on which IR is being serviced. Thus, any IR can interrupt the service routine, irrespective of priority, if the interrupt enable flip-flop is set.

PPI 8254A

8254 is a device designed to solve the timing control problems in a microprocessor.

It has 3 independent counters, each capable of handling clock inputs up to 10 MHz and size of each counter is 16 bit. It operates in +5V regulated power supply and has 24 pin signals. All modes are software programmable. The 8254 is an advanced version of 8253 which did not offered the feature of read back command.

The basic block diagram of 8254 is:



It has 3 counters each with two inputs (Clock and Gate) and one output. Gate is used to enable or disable counting. When any value of count is loaded and value of gate is set(1), after every step value of count is decremented by 1 until it becomes zero.
Depending upon the value of CS, A1 and A0 we can determine addresses of selected counter.

CS	A1	A0	SELECETION
0	0	0	C0
0	0	1	C1
0	1	0	C2
0	1	1	Control Register

Control Word of 8254 –
The format of Control Word of 8254 is:

Here by using the value of SC1 and SC0 we select a specific counter:

SC1	SC0	SELECTION
0	0	C0
0	1	C1
1	0	C2
1	1	Read back status

The values of RW1 and RW0 are used to decide the Read – Write operation:

RW1	RW0	SELECTION
0	0	Counter Latch Command
0	1	Read/Write lower byte
1	0	Read/Write higher byte

RW1	RW0	SELECTION
1	1	Read/Write lower byte followed by higher byte

The values of M2, M1, M0 are used to decide the operating modes of 8254:

M2	M1	M0	OPERATING MODE
0	0	0	MODE 0
0	0	1	MODE 1
X (0/1)	1	0	MODE 2
X (0/1)	1	1	MODE 3
1	0	0	MODE 4
1	0	1	MODE 5

The LSB of Control Word is used to select whether the counter is Binary or BCD. If the bit is 0 it works as binary counter and if its value is 1 it works as BCD coounter.

Operating Modes of 8254:

1. **Mode 0 (Interrupt on Terminal Count) –** Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the counter reaches zero it is decremented by 1 after every clock cycle. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the counter. GATE = 1 enables counting, GATE = 0 disables counting.
2. **Mode 1 (Hardware Retriggreable One Shot) –** OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the counter reaches zero.
3. **Mode 2 (Rate Generator) –** Initially value of OUT is low. When counting is enabled, it becomes high and this process repeats periodically. Value of count = Input Frequency / Output Frequency. This mode works as a frequency divider.
4. **Mode 3 (Square Wave Generator) –** Counting is enabled when GATE = 1 and disabled when GATE = 0. This mode is used to generate square waveform and time period (equal to count) is generated.

If N is count and is even then ontime of wave = N/2 and offtime = N/2
If N is odd the ontime = (N + 1) / 2 and offtime = (N – 1) / 2

5. **Mode 4 (Software Triggered Strobe) –** In this mode counting is enabled by using GATE = 1 and disabled by GATE = 0. Initially value of OUT is high and becomes low when value of count is at last stage. Count is reloaded again for subsequent clock pulse.

6. **Mode 5 (Hardware Triggered Strobe) –** OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one clock pulse and then go high again. After writing the Control Word and initial count, the counter will not be loaded until the clock pulse after a trigger

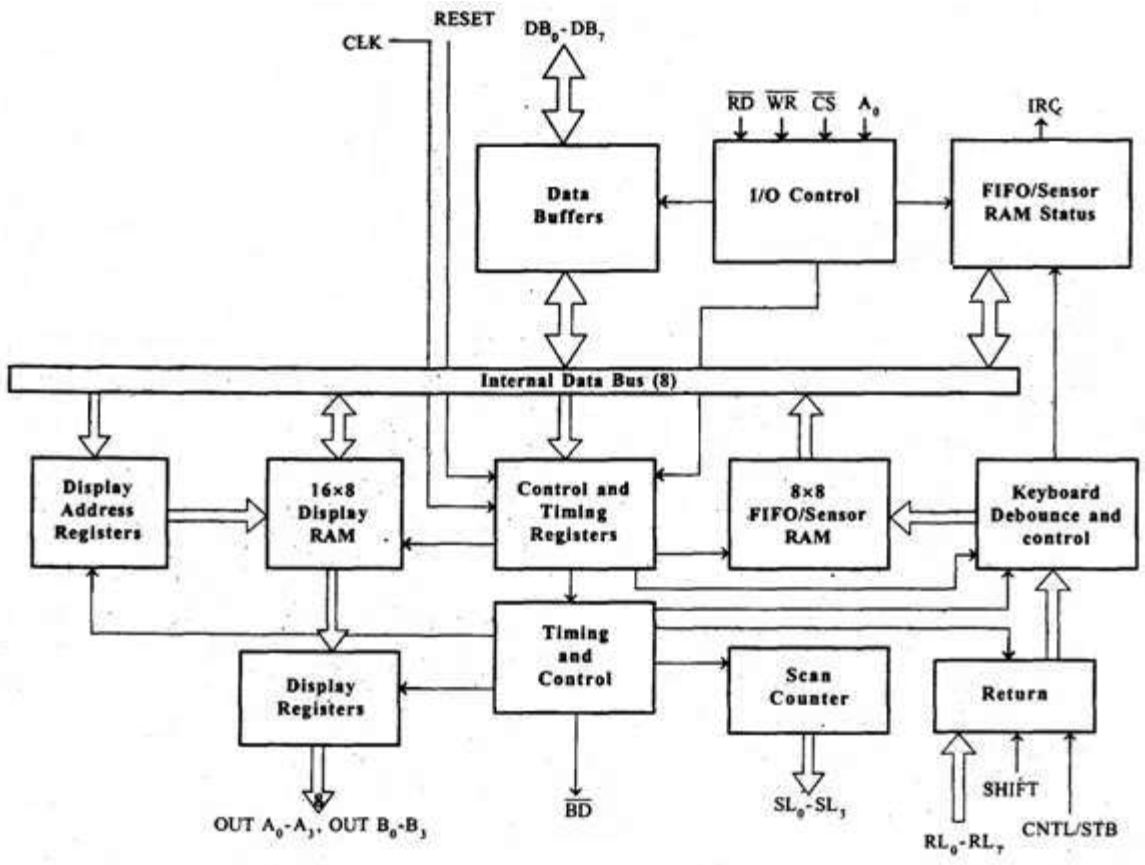
PIC8279A

8279 programmable keyboard/display controller is designed by Intel that interfaces a keyboard with the CPU. The keyboard first scans the keyboard and identifies if any key has been pressed. It then sends their relative response of the pressed key to the CPU and vice-a-versa.

The keyboard consists of maximum 64 keys, which are interfaced with the CPU by using the key-codes. These key-codes are de-bounced and stored in an 8-byte FIFORAM, which can be accessed by the CPU. If more than 8 characters are entered in the FIFO, then it means more than eight keys are pressed at a time. This is when the overrun status is set.

If a FIFO contains a valid key entry, then the CPU is interrupted in an interrupt mode else the CPU checks the status in polling to read the entry. Once the CPU reads a key entry, then FIFO is updated, and the key entry is pushed out of the FIFO to generate space for new entries.

Architecture and Description



I/O Control and Data Buffer

This unit controls the flow of data through the microprocessor. It is enabled only when D is low. Its data buffer interfaces the external bus of the system with the internal bus of the microprocessor. The pins A0, RD, and WR are used for command, status or data read/write operations.

Control and Timing Register and Timing Control

This unit contains registers to store the keyboard, display modes, and other operations as programmed by the CPU. The timing and control unit handles the timings for the operation of the circuit.

Scan Counter

It has two modes i.e. **Encoded mode** and Decoded mode. In the encoded mode, the counter provides the binary count that is to be externally decoded to provide the scan lines for the keyboard and display.

In the **decoded scan mode**, the counter internally decodes the least significant 2 bits and provides a decoded 1 out of 4 scan on SL_0-SL_3.

Return Buffers, Keyboard Debounce, and Control

This unit first scans the key closure row-wise, if found then the keyboard debounce unit debounces the key entry. In case, the same key is detected, then the code of that key is directly transferred to the sensor RAM along with SHIFT & CONTROL key status.

FIFO/Sensor RAM and Status Logic

This unit acts as 8-byte first-in-first-out (FIFO) RAM where the key code of every pressed key is entered into the RAM as per their sequence. The status logic generates an interrupt request after each FIFO read operation till the FIFO gets empty.

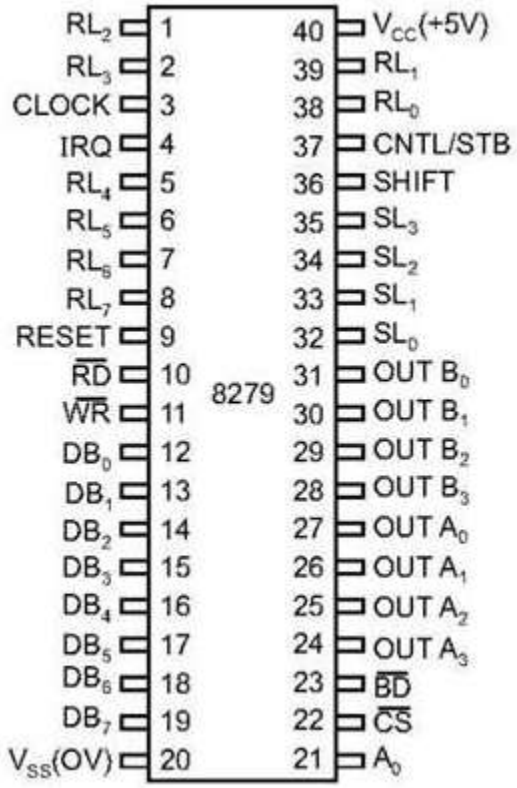
In the scanned sensor matrix mode, this unit acts as sensor RAM where its each row is loaded with the status of their corresponding row of sensors into the matrix. When the sensor changes its state, the IRQ line changes to high and interrupts the CPU.

Display Address Registers and Display RAM

This unit consists of display address registers which holds the addresses of the word currently read/written by the CPU to/from the display RAM.

8279 – Pin Description

The following figure shows the pin diagram of 8279 –



Data Bus Lines, DB_0 - DB_7

These are 8 bidirectional data bus lines used to transfer the data to/from the CPU.

CLK

The clock input is used to generate internal timings required by the microprocessor.

RESET

As the name suggests this pin is used to reset the microprocessor.

CS Chip Select

When this pin is set to low, it allows read/write operations, else this pin should be set to high.

A_0

This pin indicates the transfer of command/status information. When it is low, it indicates the transfer of data.

RD, WR

This Read/Write pin enables the data buffer to send/receive data over the data bus.

IRQ

This interrupt output line goes high when there is data in the FIFO sensor RAM. The interrupt line goes low with each FIFO RAM read operation. However, if the FIFO RAM further contains any key-code entry to be read by the CPU, this pin again goes high to generate an interrupt to the CPU.

V_{ss}, V_{cc}

These are the ground and power supply lines of the microprocessor.

$SL_0 - SL_3$

These are the scan lines used to scan the keyboard matrix and display the digits. These lines can be programmed as encoded or decoded, using the mode control register.

$RL_0 - RL_7$

These are the Return Lines which are connected to one terminal of keys, while the other terminal of the keys is connected to the decoded scan lines. These lines are set to 0 when any key is pressed.

SHIFT

The Shift input line status is stored along with every key code in FIFO in the scanned keyboard mode. Till it is pulled low with a key closure, it is pulled up internally to keep it high

CNTL/STB - CONTROL/STROBED I/P Mode

In the keyboard mode, this line is used as a control input and stored in FIFO on a key closure. The line is a strobe line that enters the data into FIFO RAM, in the strobed input mode. It has an internal pull up. The line is pulled down with a key closure.

BD

It stands for blank display. It is used to blank the display during digit switching.

$OUTA_0 - OUTA_3$ and $OUTB_0 - OUTB_3$

These are the output ports for two 16x4 or one 16x8 internal display refresh registers. The data from these lines is synchronized with the scan lines to scan the display and the keyboard.

Operational Modes of 8279

There are two modes of operation on 8279 – **Input Mode** and **Output Mode**.

Input Mode

This mode deals with the input given by the keyboard and this mode is further classified into 3 modes.

- **Scanned Keyboard Mode** – In this mode, the key matrix can be interfaced using either encoded or decoded scans. In the encoded scan, an 8×8 keyboard or in the decoded scan, a 4×8 keyboard can be interfaced. The code of key pressed with SHIFT and CONTROL status is stored into the FIFO RAM.
- **Scanned Sensor Matrix** – In this mode, a sensor array can be interfaced with the processor using either encoder or decoder scans. In the encoder scan, 8×8 sensor matrix or with decoder scan 4×8 sensor matrix can be interfaced.
- **Strobed Input** – In this mode, when the control line is set to 0, the data on the return lines is stored in the FIFO byte by byte.

Output Mode

This mode deals with display-related operations. This mode is further classified into two output modes.

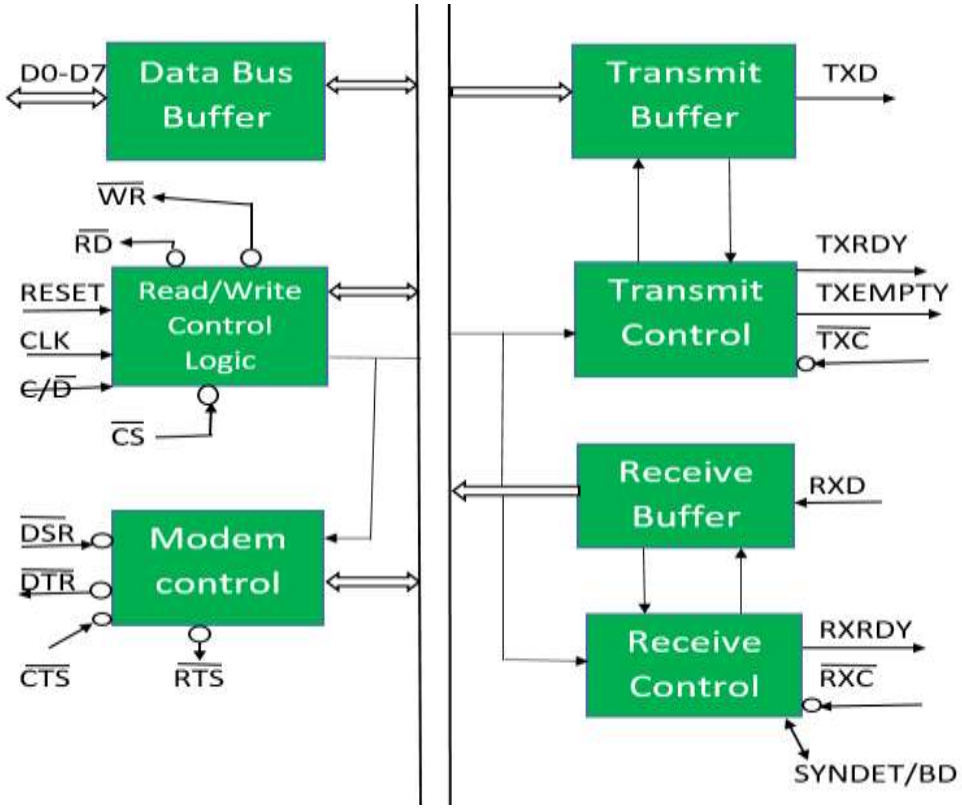
- **Display Scan** – This mode allows 8/16 character multiplexed displays to be organized as dual 4-bit/single 8-bit display units.
- **Display Entry** – This mode allows the data to be entered for display either from the right side/left side.

PIC 8255A

8251 universal synchronous asynchronous receiver transmitter (USART) acts as a mediator between microprocessor and peripheral to transmit serial data into parallel form and vice versa.

1. It takes data serially from peripheral (outside devices) and converts into parallel data.
2. After converting the data into parallel form, it transmits it to the CPU.
3. Similarly, it receives parallel data from microprocessor and converts it into serial form.
4. After converting data into serial form, it transmits it to outside device (peripheral).

Block Diagram of 8251 USART –



It contains the following blocks:

1. **Data bus buffer –**
   This block helps in interfacing the internal data bus of 8251 to the system data bus.

The data transmission is possible between 8251 and CPU by the data bus buffer block.

2. **Read/Write control logic –**
   It is a control block for overall device. It controls the overall working by selecting the operation to be done. The operation selection depends upon input signals as:

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Operation
1	X	X	X	Invalid
0	0	0	1	data CPU< ----- 8251
0	0	1	0	data CPU ----- > 8251
0	1	0	1	Status word CPU < ----------8251
0	1	1	0	Control word CPU---------- > 8251

In this way, this unit selects one of the three registers- data buffer register, control register, status register.

3. **Modem control (modulator/demodulator) –**
   A device converts analog signals to digital signals and vice-versa and helps the computers to communicate over telephone lines or cable wires. The following are active-low pins of Modem.

   - **DSR:** Data Set Ready signal is an input signal.
   - **DTR:** Data terminal Ready is an output signal.
   - **CTS:** It is an input signal which controls the data transmit circuit.
     RTS: It is an output signal which is used to set the status RTS.

4. **Transmit buffer –**
   This block is used for parallel to serial converter that receives a parallel byte for conversion into serial signal and further transmission onto the common channel.

   - **TXD:** It is an output signal, if its value is one, means transmitter will transmit the data.

5. **Transmit control –**
   This block is used to control the data transmission with the help of following pins:

   - **TXRDY:** It means transmitter is ready to transmit data character.
   - **TXEMPTY:** An output signal which indicates that TXEMPTY pin has transmitted all the data characters and transmitter is empty now.
   - **TXC:** An active-low input pin which controls the data transmission rate of transmitted data.

6. **Receive buffer –**
   This block acts as a buffer for the received data.

   - **RXD:** An input signal which receives the data.

7. **Receive control –**
   This block controls the receiving data.

   - **RXRDY:** An input signal indicates that it is ready to receive the data.
   - **RXC:** An active-low input signal which controls the data transmission rate of received data.
   - **SYNDET/BD:** An input or output terminal. External synchronous mode-input terminal and asynchronous mode-output terminal.