UNIT-III

Memory Interfacing

Microprocessor while executing an instruction, there is a necessity for the microprocessor to access memory frequently for reading various instruction codes and data which are stored in the memory.

Since microprocessor doesn't have on-chip memory, we need to connect it externally. The interfacing circuit is used for accessing the memory.

Memory requires some signals to read from and write to registers. Similarly the microprocessor transmits some signals for reading or writing a data.

- Memory in a microprocessor system can be classified into two main types:

    1) Main memory (RAM and ROM)

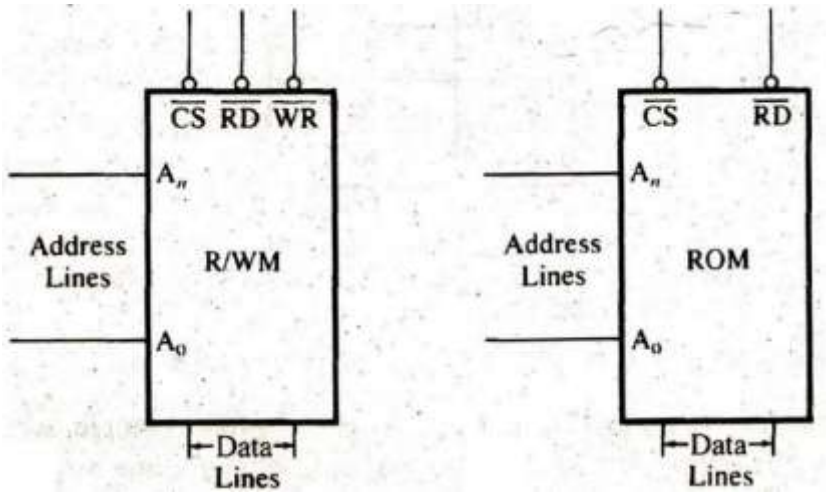
    2) Storage memory (Disks, CD ROMs, etc.)

Microprocessor access (Read or Write) information in memory (RAM or ROM), it needs to do the following:

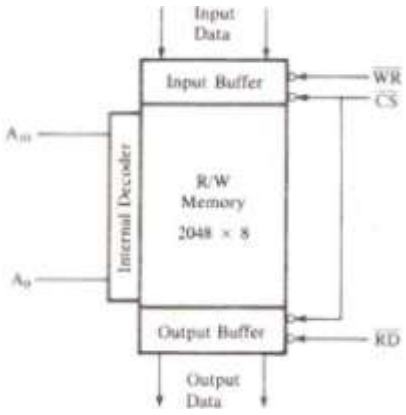
1) Select the right memory chip (using part of the address bus).

2) Identify the memory location (using the rest of the address bus).

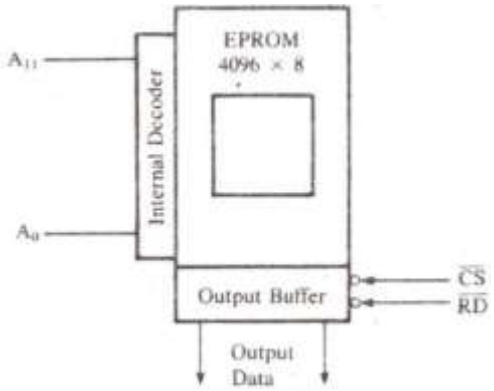
3) Access the data (using the data bus).



R/W Memory Cell



- ✓ It is typical RAM(2048X8), it has total Registers are 2048 and each register can store 8 bits of information.
- ✓ This chip has 2048 registers; it means it requires 11 address lines A0 to A10. Remaining address lines can be used for chip selection purpose.



- ✓ Another two control lines are $\overline{RD}$ and $\overline{WR}$ signals.

It is typical 4096 X 8 bits of ROM. It says it has 4096 registers with each register of 8 bit. So, we need total 12 address line, A0 to A11 address lines for register selection. Remaining address lines can be used for chip selection purpose.

- ✓ It requires only one control signal $\overline{RD}$.

Ex: Interfacing of 2K byte RAM using 3:8 Decoder.

Solution:

1. No. of address lines required for 2K Byte ROM.

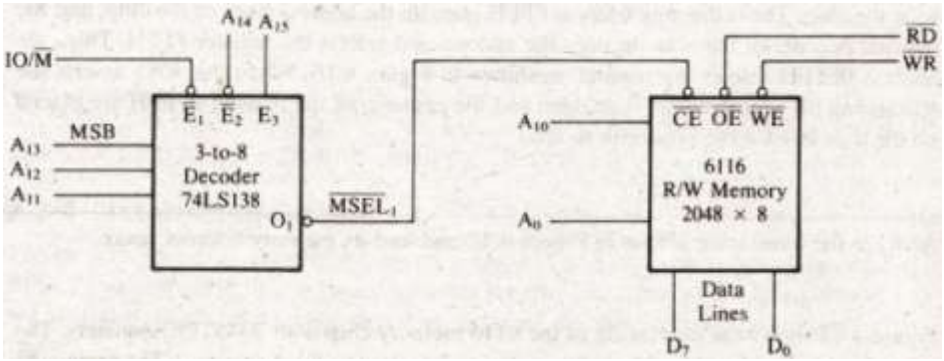
2 = 2048

n = 11 i.e $2^{10}X2^1$

So, A0 to A10 will be used for internal address decoding purpose

2. Remaining address lines are 16-11 = 5 for chip selection purpose.
3. Memory size is 2K x 8, it means that it requires 8 data lines.
4. As it is RAM, it requires $\bar{\bar{R}}\bar{D}$ and $\bar{\bar{W}}\bar{R}$ control signals with $\bar{\bar{M}}\bar{\bar{E}}\bar{\bar{M}}\bar{R}$ and $\bar{\bar{M}}\bar{\bar{E}}\bar{\bar{M}}\bar{W}$ control signal.
5. $\bar{\bar{C}}\bar{S}$ is connected with O1. O1 is output of decoder, it goes only low when A13=0, A12=0 and A11=1. But decoder is enabled by A14=0 and A15=1. Also IO/$\bar{M}$ is zero.
6. So, decoding logic is

A15	A14	A13	A12	A11
1	0	0	0	1



7. Similarly A0 to A10 will change from all zero to all one for internal decoding purpose. So, final addressing will be

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	**Address**
1	0	0	0	1	0 ↓	0 ↓	0 ↓	0 ↓	0 ↓	0 ↓	0 ↓	0 ↓	0 ↓	0 ↓	0 ↓	**8800H to**

					1	1	1	1	1	1	1	1	1	1	1	**8FFFH**

8. It means that as per given circuit and logic, address range of Memory will be 8800H to 8FFFH.
9. It requires connecting both control signals $\overline{RD}$ and $\overline{WR}$ of 8085 with $\overline{RD}$ and $\overline{WR}$ of

Memory. IO/$\overline{M}$ I is connected with E1. So, whenever memory operation is there it will be zero and in turn it will enable the decoder.

- Interfacing of 4K Byte ROM

Ex:Interfacing of 4K Byte ROM

Solution:

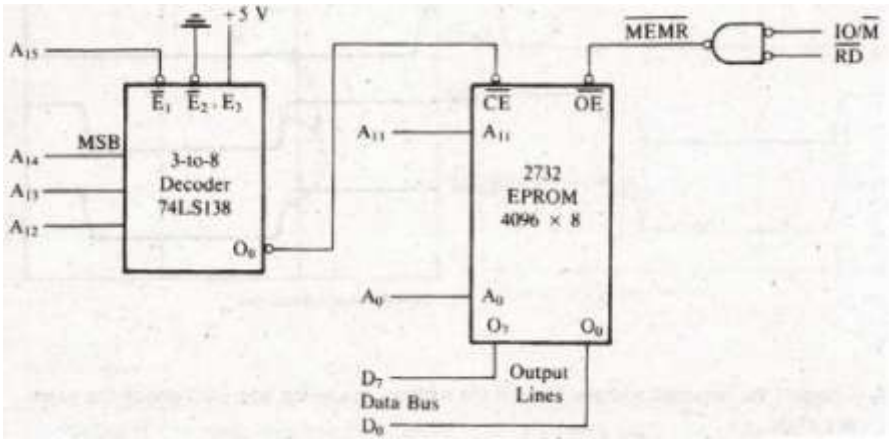
1. No. of address lines required for 4K ROM.

$2^{n} = 4096$

$n = 12$ i.e $2^{10}X2^{2}$

So, A0 to A11 will be used for internal decoding purpose

2. Remaining address lines are 16-12 = 4 for chip selection purpose.
3. Memory size is 4K x 8, it means that it requires 8 data lines.
4. As it is ROM, it only requires $\overline{RD}$ with $\overline{MEMR}$ signal.



5. As in figure 6.7, $\overline{CS}$ is connected with O0. O0 is output of decoder, it goes only low when A14=0, A13=0 and A12=0. But decoder is enabled A15=0. $\overline{\overline{E2}}$ must be grounded and E3 must be connected to Vcc.

6. So, decoding logic is

A15	A14	A13	A12
0	0	0	0

7. Similarly A0 to A11 will change from all zero to all one for internal decoding purpose. So, final addressing will be

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	**Address**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0000H**
				↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	**to**
				1	1	1	1	1	1	1	1	1	1	1	1	**0FFFH**

8. It means that as per given circuit and logic, address range of Memory will be 0000H to 0FFFH.

9. It requires $\overline{\overline{OE}}$ enable signal, that could be $\overline{\overline{MEMR}}$ control signal which can be generated

using $\overline{\overline{RD}}$ and IO/$\overline{M}$. IO/$\overline{M}$ is connected with $\overline{\overline{RD}}$ signal to a NAND gate via NOT gate. So,

when $\overline{\overline{RD}}$=0 and IO/$\overline{M}$ is zero, only then $\overline{\overline{RD}}$ goes low and memory sends data from

register to data lines of 8085.

2. INPUT/OUTPUT(I/O) INTERFACING METHODS

- There are two method of interfacing memory or I/O devices with the microprocessor are as follows:
  1) I/O mapped I/O Interfacing
  2) Memory mapped I/O Interfacing

PERIPHERAL MAPPED I/O INTERFACING

In this method, the I/O devices are treated differently from memory chips. The control signals I/O read ($\overline{IOR}$) and I/O write ($\overline{IOW}$), which are derived from the IO/$\overline{M}$, RD and WR signals of the 8085, are used to activate input and output devices, respectively.

IN instruction is used to access input device and OUT instruction is used to access output device. Each I/O device is identified by a unique 8-bit address assigned to it. Since the control signals used to access input and output devices are different, and all I/O device use 8-bit address, a maximum of 256 (2^8) input devices and 256 output devices can be interfaced with 8085.

MEMORY MAPPED I/O INTERFACING

In memory-mapped I/O, each input or output device is treated as if it is a memory location.

The MEMR and MEMW control signals are used to activate the devices. Each input or output device is identified by unique 16-bit address, similar to 16-bit address assigned to memory location. All memory related instruction like LDA 2000H, LDAX B, MOV A, M can be used. Since the I/O devices use some of the memory address space of 8085, the maximum memory capacity is lesser than 64 KB in this method.

1) I/O Mapped I/O Interfacing

- In this Interfacing technique, I/O device is treated as an I/O device and memory as memory. Each I/O device uses eight address lines.
- If eight address lines are used to interface to generate the address of the I/O port, then 256(2^8) Input/output devices can be interfaced with the microprocessor.
- The 8085 microprocessor has 16 bit address bus, so we can either use lower order address lines (A_0 – A_7) or higher order address lines (A_8 – A_{15}) to address I/O devices. We used lower order address bus & address available on A_0 – A_7 will be copied on the address lines A_8 – A_{15}.
- In I/O mapped I/O, the complete 64 Kbytes of memory can be used to address memory locations separately as the address space is not shared with I/O devices.
- In this interface type, the data transfer is possible between accumulator (A) and I/O devices only. Arithmetic and logical operation are not possible directly with accumulator.
- As 8 bit device address used, Address decoding is simple so less hardware is required.
- The separate control signals are used to access I/O devices and memory such as $\overline{IOR}$, $\overline{IOW}$ for I/O port and $\overline{MEMR}$, $\overline{MEMW}$ for memory hence memory location are protected from the I/O access.

2) Memory Mapped I/O Interfacing

- In this Interfacing technique, I/O devices are treated as memory and memory as memory, hence the address of the I/O devices are as same as that of memory i.e. 16 bit for 8085 microprocessor.
- So, the address space of the memory i.e. 64 Kbytes will be shared by the I/O devices as well as by memory. All 16 address lines i.e. A_0-A_{15} is used to address memory locations as well as I/O devices.
- The control signals $\overline{MEMR}$ and $\overline{MEMW}$ are used to access memory devices as well as I/O devices.
- The data transfer is possible between any register of the microprocessor and I/O device/memory device. Hence, all memory related instructions can be used to access devices as they are treated as memory locations.

- Address decoding of the I/O devices and memory devices are complicated and expensive as more hardware is required.
- The 8085 microprocessor can access either 64K I/O ports or memory locations, hence the total numbers of the I/O ports and memory locations should not be greater than 64K.
- In this interface type, I/O devices and memory locations are distinguished by the addresses only.

❖ **Comparison of Memory-Mapped I/O and Peripheral Mapped I/O**

No	Characteristics	Memory mapped I/O	I/O mapped I/O
1	Device Address	16 bit	8 Bit
2	Control signals	$\overline{MEMR}$ & $\overline{MEMW}$	$\overline{IOR}$ & $\overline{IOW}$
3	Instruction Available	All memory related instruction : LDA; STA; LDAX; STAX; MOV M,R; ADD M; SUB M	IN and OUT instructions only
4	Data Transfer	Between any register and I/O devices.	Between I/O device and Accumulator only.
5	Maximum Numbers of I/Os Possible	Memory Map (64K) is shared between I/Os and System memory.	I/O Mapped is independent of memory map; 256 Input and 256 output devices can be connected.
6	Execution Speed	13 T-State (LDA, STA,...) 7 T-State (MOV M,R)	10 T-State
7	Hardware Requirement	More hardware is needed to decode 16 bit address	Less hardware is needed to decode 8 bit address
8	Other Feature	Arithmetic and logical operations are directly performed with I/O devices.	Not available