CSE3666

Homework 6 Solutions

1

```
0x00400200: 0xFE542023

1111 1110 0101 0100 0010 0000 0010 0011

opcode:   0100011 (S-type)

rs1:      01000
rs2:      00101
rd:       00000
immediate:      0b111111100000  sign extended to 0xFFFFFFE0
ALUOperation:   0b0010   to calculate memory address
BranchTarget:   0x00400200 + 0xFFFFFFE0 = 0x004001E0
PCSrc:          0
NextPC:         0x00400204
```

This is a store instruction. The output of the main control for SW instruction is listed in lecture slides (and in the textbook).

2

```
0x00400000: 0x01020233          # add  x4, x4, x16
```

PC is 0x00400004

Register x4 is changed to `0x090A1AFC` (sum of x4 and x16).

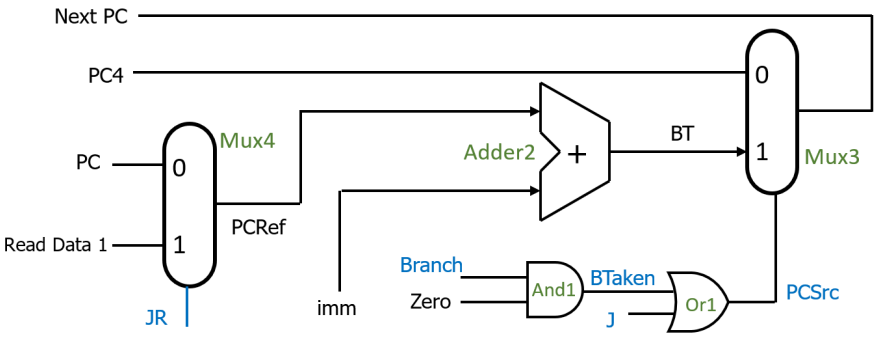
In data memory, the word at address `0x090A1AFC` is changed to `0x090A0B0C` (the value in x16). The address is the output of the ALU.

3

a.

Revise the diagram as shown in b) and c).

b. Generating target address



Computing target address

The target address of JAL is PC + imm.
The target address of JALR is Read Data 1 + imm.
Mux4 selects the data going into input 1 of Adder2. Read data 1 (from the register file) is selected if the instruction is JR. Otherwise, PC is selected, for J and branches.

Selecting target address

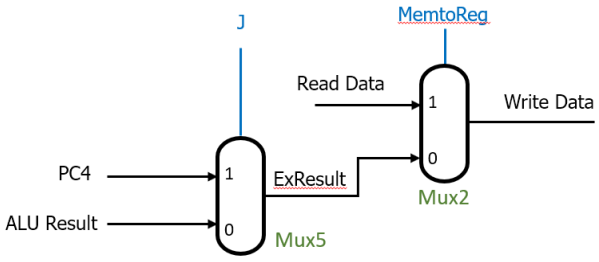
The select signal of Mux4 is JR.

Mux3 is controlled by PCSrc. PCSrc is now generated by the following logic. The output of And1, BTaken, indicates if the branch is taken.

```
PCSrc = J | (Branch & Zero)
```

If the instruction being executed is JAL or JALR, NextPC is always BranchTarget.

c. Writing PC4 to register file.



Both JAL and JALR write PC4 to rd. We add Mux5 to select the data going into input 0 of Mux2. Input 0 of Mux5 is the output of ALU, and input 1 is PC4.

The select signal of Mux5 is J so PC4 is selected if the instruction being executed is JAL or JALR.

d. Control signals

With the above changes, the control signals for JAL and JALR are as follows.

Inst.	ALU Src	Memto Reg	Reg Write	Mem Read	Mem Write	Branch	J	JR
JAL	X	0	1	0	0	0	1	0
JALR	X	0	1	0	0	0	1	1

Execution of JAL

When the processor executes the JAL instruction,

- Mux4 selects PC to Adder2.
- Adder2 calculates BranchTarget = PC + immediate.
- PCSrcJ is 1. Mux3 selects BranchTarget as NextPC, which is PC + immediate.
- Mux5 selects PC4, the address of the instruction that follows JAL.
- Mux2 selects PC4 as Write Data, which will be written to register rd.

Execution of JALR

When the processor executes the JALR instruction,

- Mux4 sends Read data 1 to Adder2.
- Adder 2 calculates BranchTarget = Reg[rs1] + immediate.
- PCSrcJ is 1. Mux3 selects BranchTarget as NextPC, which is Reg[rs1] + immediate.
- Mux5 selects PC4, the address of the instruction that follows JAL.
- Mux2 selects PC4 as Write Data, which will be written to register rd.