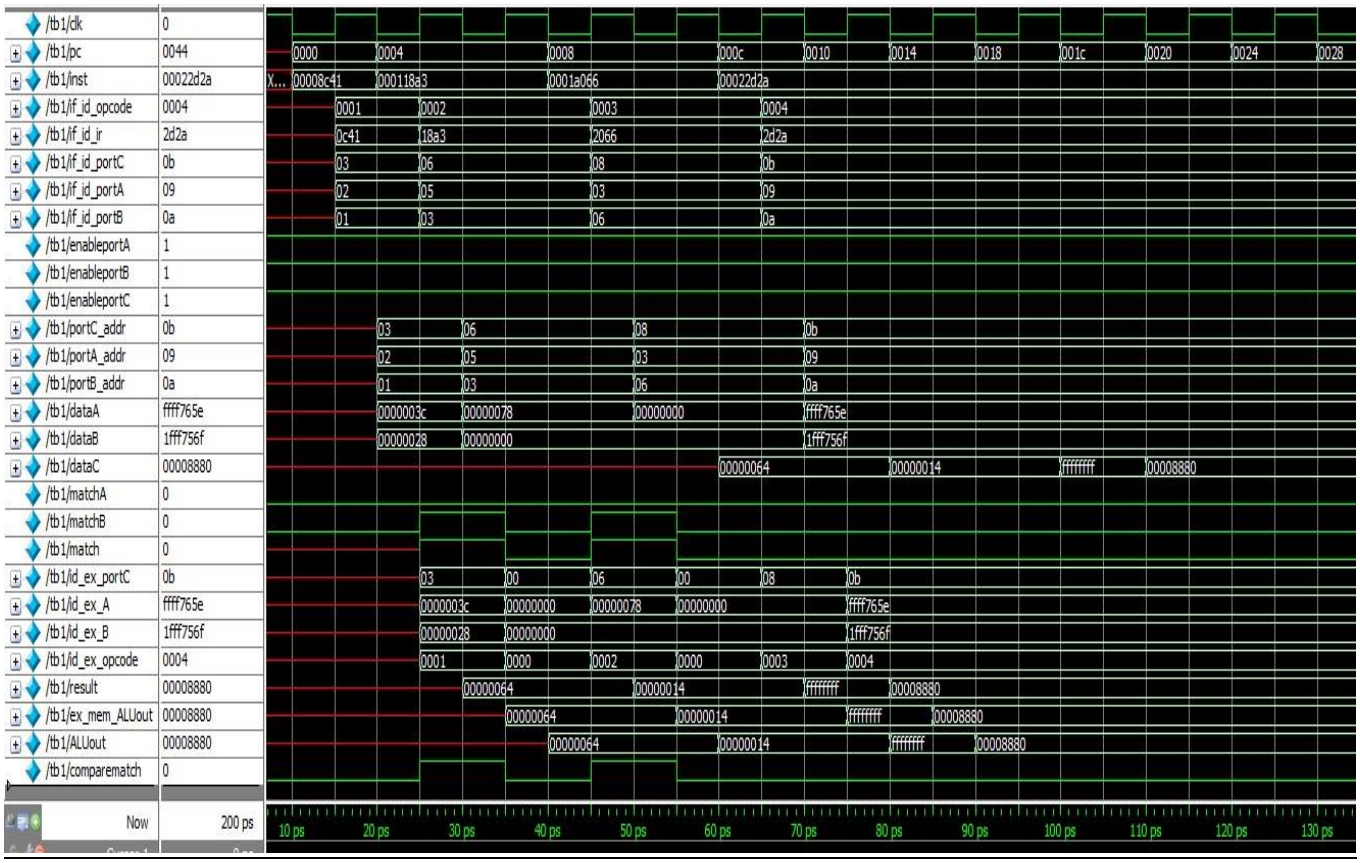
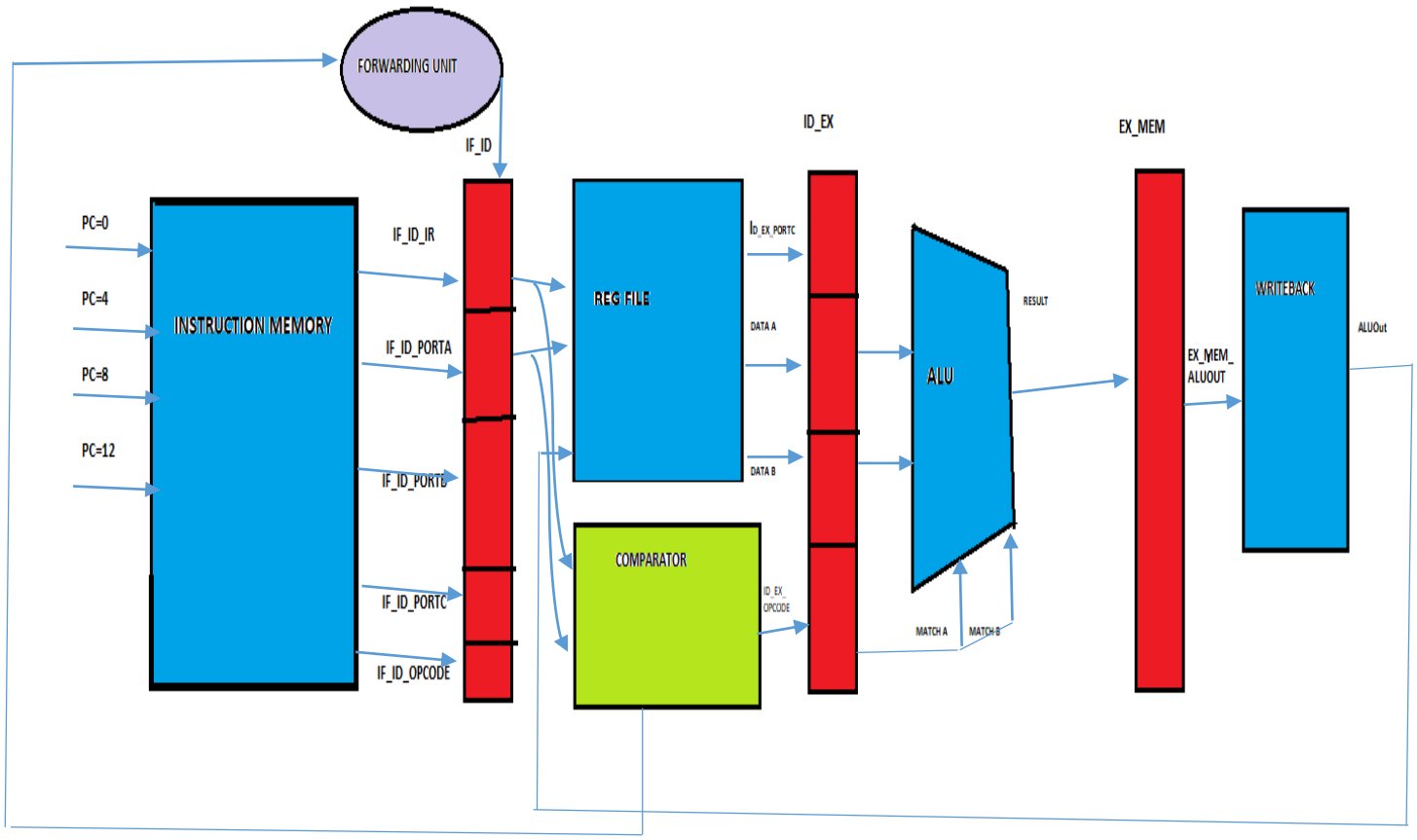
MINI PROJECT 2

IMPLEMENTATION OF 5 STAGED PIPELINED OF MIPS ISA OVERCOMING DATA HAZARDS

PARTA: IMPLEMENTED USING CONCEPT OF STALLING

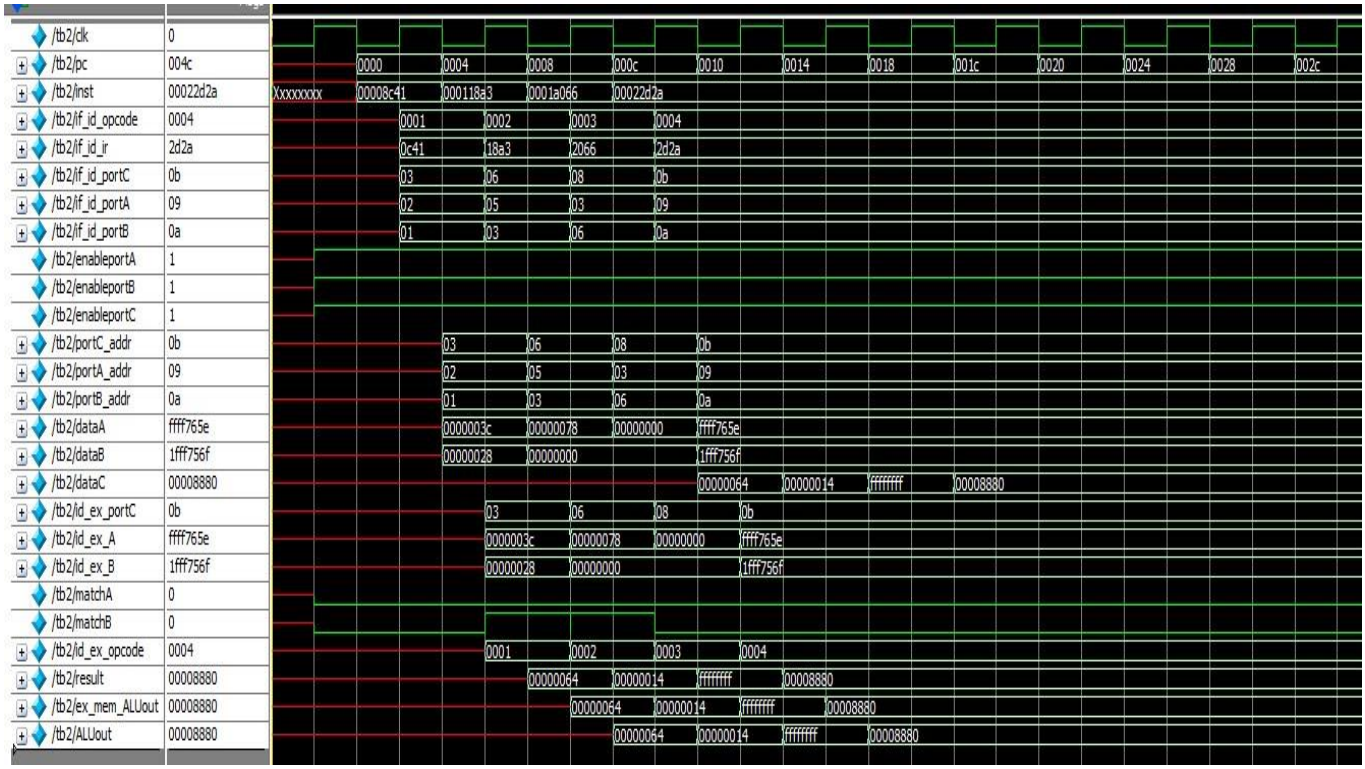


SIMULATION

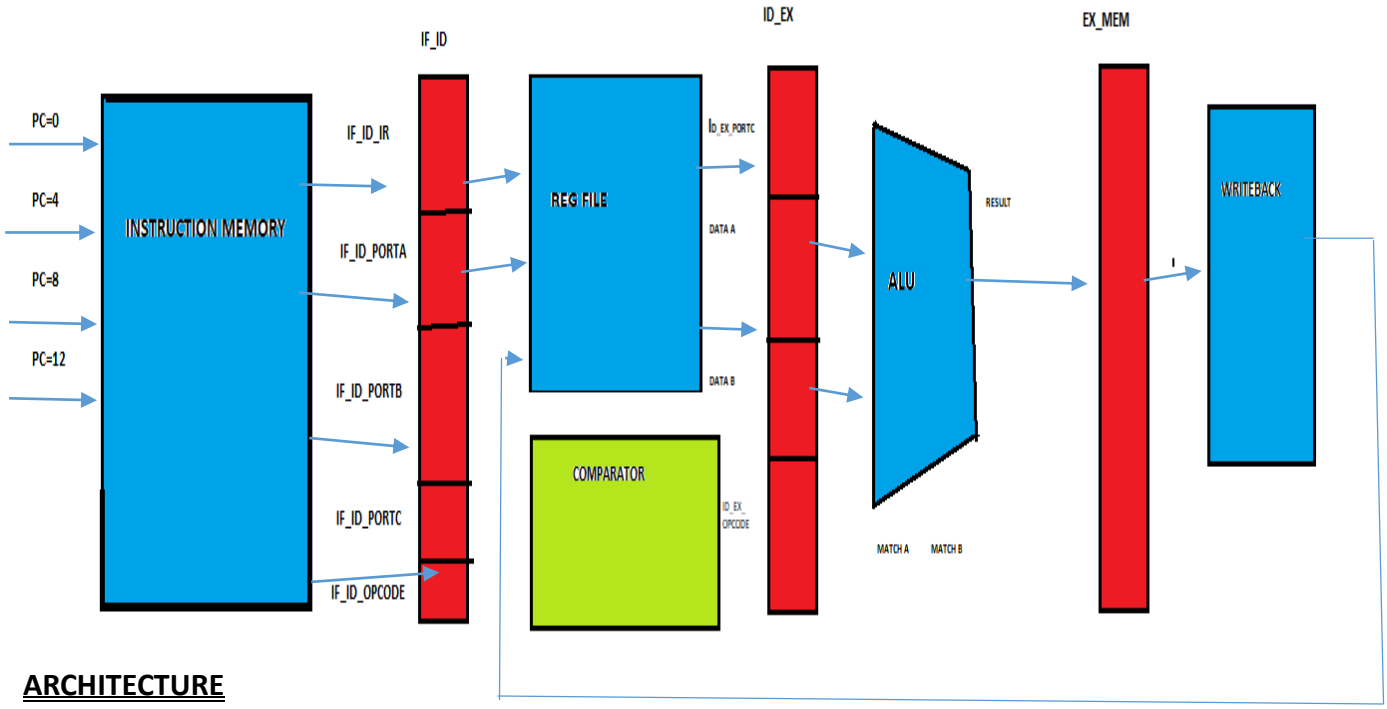


ARCHITECTURE

PARTB: IMPLEMENTED USING CONCEPT OF DATA FORWARDING



SIMULATION



ARCHITECTURE

Sheet for uploading

Fill the following table:

To detect data hazard using data forwarding and data stalling.

Memory Address	Instructions	Register status (Show the registers which are only affected). Remarks on hazards and what is the solution? ( ) → represents Decimal
0000	ADD R3 , R2, R1	R2 = 3C (60) , R1= 28 (40) R3 = 64 (100) First instruction doesn't have any data hazard.
0004	SUB R6 , R5 ,R3	R5 = 78 (120) , R3 = 0(0) [Initially stored as 0 in the register file and later overwritten by the previous inst. Destination register) , R6 = 14 (20) RAW hazard found at R3 register with respect to first instruction.
0008	NAND R8 ,R3 , R6	R3 =0 , R6 =0 (Initially) Overwritten as R3 = 64(100) , R6 = 14(20) RAW hazard found at R6 register and R3 register with respect to second instruction. R8 = 0xFFFFFFFF.
000C	NOR R11 , R9 , R10	R9 = 0xFFFF765E , R10 = 0x1FFF756F , No data hazard found destination register R11 = 0x0008880.

Honor Code Declaration by student:

- My answers to the above questions are my own work.
- I have not shared the codes/answers written by me with any other students. (I might have helped clear doubts of other students).
- I have not copied other's code/answers to improve my results. (I might have got some doubts cleared from other students).

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