GATE

COA

Short Notes and PYQ's

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[Date]

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Floating Point Representation

Notes

> The number is represented in the format:

Sign	Exponent	Mantissa

> Exponent are stored in Biased form

 # Biased Exponent

> $Stored\ Exponent(E) = Original\ Exponent(e) + Bias$

> If no. of bits used for representing E is k, then $\boldsymbol{Bias = 2^{k+1}}$

 # Mantissa: - (101.11)

> Explicit Normalization = $\mathbf{0.10111 * 2^3}$
- Biased Exponent = 3 + Bias
- Mantissa = 10111

> Implicit Normalization = $\mathbf{1.0111 * 2^2}$
- e = 2
- E = 2 + Bias
- M = 0111

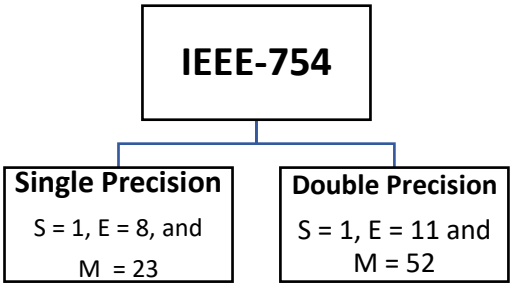
 # Value Formula: -

> Explicit = $\boldsymbol{(-1)^S * 0.M * 2^{E-Bias}}$

> Implicit = $\boldsymbol{(-1)^S * 1.M * 2^{E-Bias}}$

> These are conventional method and can't store 0 or small value around 0.

IEEE-754 Floating Point Representation



> E and M all 0's then,
1. S = 0 then + 0
2. S = 1 then – 0

> E all 1's and M all 0's then,
1. S = 0 then **+∞**
2. S = 1 then **-∞**

> S anything and M not all 0's then
1. E all 1's then N.A.N
2. E all 0's then Denormalized number

> S and M anything and E neither all 0's nor all 1's then Implicit Normalized.

 # Value Formula: -

> Explicit = $\boldsymbol{(-1)^S * 0.M * 2^{-126}}$

> Implicit = $\boldsymbol{(-1)^S * 1.M * 2^{E-Bias}}$

PYQ's

2025

S1

Q.25 The number −6 can be represented as 1010 in 4-bit 2's complement representation. Which of the following is/are CORRECT 2's complement representation(s) of −6?

(A) 1000 1010 in 8-bits

(B) 1111 1010 in 8-bits

(C) 1000 0000 0000 1010 in 16-bits

(D) 1111 1111 1111 1010 in 16-bits ANS: - B, D

Q.36 Consider a memory system with 1M bytes of main memory and 16K bytes of cache memory. Assume that the processor generates 20-bit memory address, and the cache block size is 16 bytes. If the cache uses direct mapping, how many bits will be required to store all the tag values? [Assume memory is byte addressable, $\mathbf{1K = 2^{10}}$, $\mathbf{1M = 2^{20}}$**.]**

(A) $6 * 2^{10}$

(B) $8 * 2^{10}$

(C) 2^{12}

(D) 2^{14} ANS: - A

S2

Q.32 The following two signed 2's complement numbers (multiplicand M and multiplier Q) are being multiplied using Booth's algorithm: M: 1100 1101 1110 1101 and Q: 1010 0100 1010 1010 The total number of addition and subtraction operations to be performed is _____. (Answer in integer) ANS: - 13

Q.49 Three floating point numbers X, Y, and Z are stored in three registers R_X, R_Y, and R_Z, respectively in IEEE 754 single precision format as given below in hexadecimal:

R_X = 0xC1100000, R_Y = 0x40C00000, and R_Z = 0x41400000

Which of the following option(s) is/are CORRECT?

(A) $4(X + Y) + Z = 0$ (B) $2Y - Z = 0$

(C) $4X + 3Z = 0$ (D) $X + Y + Z = 0$ ANS: - A, B, C

I/O Organization

Notes

IO Mapped IO	Memory Mapped IO
1. Address bus and Data bus are same for memory and IO but control signals are different	1. All the buses are same for both
2. No memory wastage	2. Some memory wastage
3. IO devices have their own address	3. No separate address space for IO
4. IO access and Memory access instruction are different	4. All memory access instruction can be used for IO access
5. Less instruction for IO access	5. More instruction for IO access
6. Less addressing for IO access	6. More addressing mode for IO access
7. Less devices can be connected to system	7. More devices can be connected to system
8. ALU operation can't be performed on ALU Data directly	8. ALU operation can be performed on IO data directly.

Mode of Transfer: -

1. Programmed IO or Program Controlled IO
2. Interrupt IO or Interrupt Driven IO
3. Direct Memory Access (DMA)

Programmed IO	Interrupt IO
1. There is no any provision through which IO can inform CPU about data transfer	1.IO devices has a provision (Interrupt Signal) to inform to CPU about communication
2. IO sets its own status and wait	2. When CPU receives interrupt: - **(2 GATE Question)** ➢ It completes execution of current instruction ➢ Saves the status (PC, PSW etc) of current instruction onto the stack ➢ Branches to service the interrupt ➢ Resumes the previous process by taking out the value from the stack
3. CPU runs program periodically and checks the status of each device one-by-one.	
4. If any device has its status set the CPU perform data transfer	
5. Wastage of CPU time in unnecessary Polling	

PYQ's

2025

Q.11 Suppose a program is running on a non-pipelined single processor computer system. The computer is connected to an external device that can interrupt the processor asynchronously. The processor needs to execute the interrupt service routine (ISR) to serve this interrupt. The following steps (not necessarily in order) are taken by the processor when the interrupt arrives:

(i) The processor saves the content of the program counter.

(ii) The program counter is loaded with the start address of the ISR

(iii) The processor finishes the present instruction.

Which ONE of the following is the CORRECT sequence of steps?

A. (iii), (i), (ii)
B. (i), (iii), (ii)
C. (i), (ii), (iii)
D. (iii), (ii), (i)

ANS: - A https://gateoverflow.in/460080/gate-cse-2025-set-1-question-1

2024

Set – 1

Q.15 Which one of the following statements is FALSE?

(A) In the cycle stealing mode of DMA, one word of data is transferred between an I/O device and main memory in a stolen cycle

(B) For bulk data transfer, the burst mode of DMA has a higher throughput than the cycle stealing mode

(C) Programmed I/O mechanism has a better CPU utilization than the interrupt driven I/O mechanism

(D) The CPU can start executing an interrupt service routine faster with vectored interrupts than with non-vectored interrupts

ANS: - C

Set – 2

Q 11 Consider a computer with a 4 MHz processor. Its DMA controller can transfer 8 bytes in 1 cycle from a device to main memory through cycle stealing at regular intervals. Which one of the following is the data transfer rate (in bits per second) of the DMA controller if 1% of the processor cycles are used for DMA?

(A) 2,56,000 (C) 25,60,000

(B) 3,200 (D) 32,000

2018

Q.9 The following are some events that occur after a device controller issues an interrupt while process L is under execution.

(P) The processor pushes the process status of L onto the control stack.
(Q) The processor finishes the execution of the current instruction.
(R) The processor executes the interrupt service routine.
(S) The processor pops the process status of L from the control stack.
(T) The processor loads the new PC value based on the interrupt.

Which one of the following is the correct order in which the events above occur?

(A) QPTRS (B) PTRSQ (C) TRPQS (D) QTPRS

ANS: - A

Memory Management

PYQ's

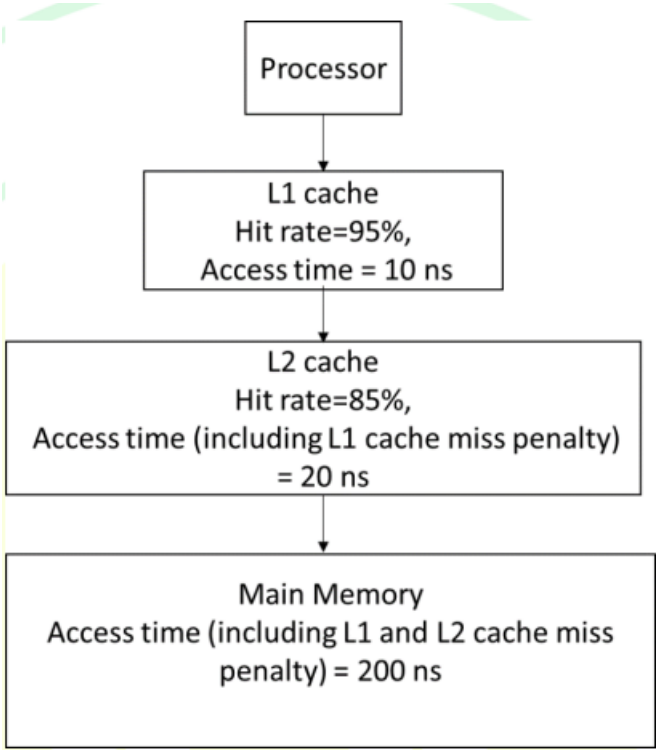
Cache Organization

PYQ's

2025

S1

Q.53 A computer has a memory hierarchy consisting of two-level cache (L1 and L2) and a main memory. If the processor needs to access data from memory, it first looks into L1 cache. If the data is not found in L1 cache, it goes to L2 cache. If it fails to get the data from L2 cache, it goes to main memory, where the data is definitely available. Hit rates and access times of various memory units are shown in the figure. The average memory access time in nanoseconds (ns) is _____. (rounded off to two decimal places)



ANS: - 11.83 to 11.87

S2

Q.39 For a direct-mapped cache, 4 bits are used for the tag field and 12 bits are used to index into a cache block. The size of each cache block is one byte. Assume that there is no other information stored for each cache block. Which ONE of the following is the CORRECT option for the sizes of the main memory and the cache memory in this system (byte addressable), respectively?

(A)	64 KB and 4 KB	(B)	128 KB and 16 KB	
(C)	64 KB and 8 KB	(D)	128 KB and 6 KB	ANS: - A

Q.55 **Given a computing system with two levels of cache (L1 and L2) and a main memory. The first level (L1) cache access time is 1 nanosecond (ns) and the "hit rate" for L1 cache is 90% while the processor is accessing the data from L1 cache. Whereas, for the second level (L2) cache, the "hit rate" is 80% and the "miss penalty" for transferring data from L2 cache to L1 cache is 10 ns. The "miss penalty" for the data to be transferred from main memory to L2 cache is 100 ns. Then the average memory access time in this system in nanoseconds is _____ .**

(rounded off to one decimal place) ANS: - 4

Q.56 **A 5-stage instruction pipeline has stage delays of 180, 250, 150, 170, and 250, respectively, in nanoseconds. The delay of an inter-stage latch is 10 nanoseconds. Assume that there are no pipeline stalls due to branches and other hazards. The time taken to process 1000 instructions in microseconds is _____ .** (rounded off to two decimal places) ANS: - 560.20 to 261.20

DISK

PYQ's

Pipeline Processing

PYQ's

2025

S2

Q.61 An application executes 6.4 × 108 number of instructions in 6.3 seconds. There are four types of instructions, the details of which are given in the table. The duration of a clock cycle in nanoseconds is _____. (rounded off to one decimal place)

Instruction type	Clock cycles required per instruction (CPI)	Number of instructions executed
Branch	2	$2.25 * 10^8$
Load	5	$1.20 * 10^8$
Store	4	$1.65 * 10^8$
Arithmetic	3	$1.30 * 10^8$

ANS: - 3.0

Instruction & Addressing Mode

PYQ's

2025

S1

Q.37 A processor has 64 general-purpose registers and 50 distinct instruction types. An instruction is encoded in 32-bits. What is the maximum number of bits that can be used to store the immediate operand for the given instruction?

ADD R1, #25 // R1 = R1 + 25

(A) 16

(B) 20

(C) 22

(D) 24 ANS: - B

S2

Q.28 Which of the following is/are part of an Instruction Set Architecture of a processor?

(A) The size of the cache memory

(B) The clock frequency of the processor

(C) The number of cache memory levels

(D) The total number of registers ANS: - D

CPU & Control Unit

PYQ's