Cornell Notes: S-R Latch

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Cues / Questions

- What is an S-R Latch?
- What are its inputs and outputs?
- How does it behave with different input combinations?
- What is the invalid state?
- What is the difference between NOR and NAND based latches?
- What are its applications?

Notes

Definition:
The **S-R (Set-Reset) Latch** is a fundamental sequential circuit used to store 1-bit of data. It has two inputs: **Set (S)** and **Reset (R)**, and two outputs: **Q** and its complement **Q'**.

NOR-based S-R Latch (Active-High)

Truth Table (NOR-based S-R Latch):

S	R	Q (Next State)	Q'
0	0	No Change	Previous
0	1	0	1
1	0	1	0
1	1	Invalid	Invalid

NAND-based S-R Latch (Active-Low)

Truth Table (NAND-based S-R Latch):

$\overline{S}$	$\overline{R}$	Q	Q'
1	1	No Change	Previous
1	0	0	1
0	1	1	0
0	0	Invalid	Invalid

Applications:

- Single-bit memory storage
- Switch debouncing circuits
- Basic control circuits
- Building block for flip-flops (D, JK)

Summary

The S-R Latch is a foundational digital storage device. It operates with either NOR (active-high) or NAND (active-low) logic gates and can hold a binary state. Care must be taken to avoid the invalid condition where both inputs are active simultaneously. It forms the basis for more complex sequential logic elements like flip-flops.