

CS & IT ENGINEERING



COMPUTER ORGANIZATION AND ARCHITECTURE

Cache Organization

Lecture No.- 2

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Recap of Previous Lecture



Topic

Locality of Reference

Topic

Cache Memory

Topics to be Covered



Topic

Cache Memory

Topic

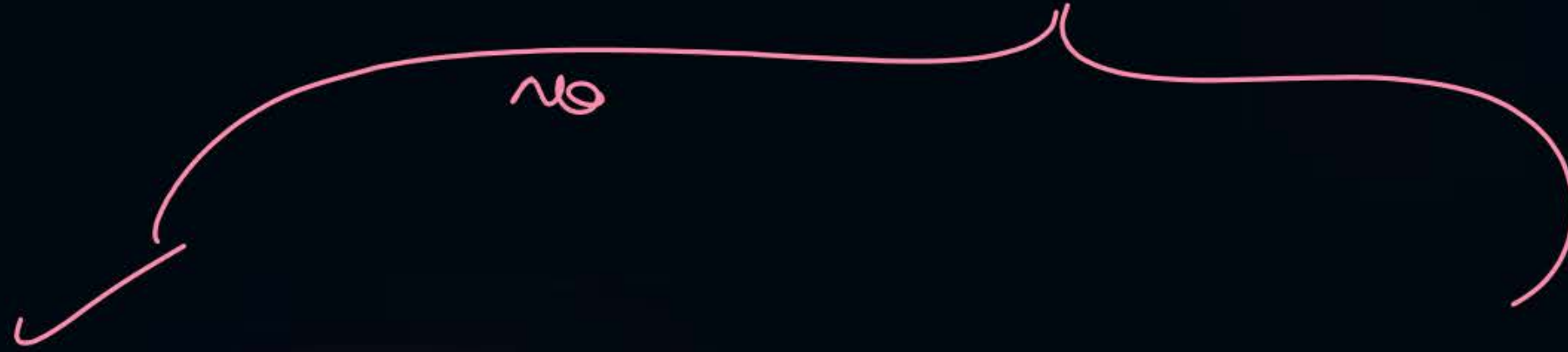
Average Memory Access Time

Topic

Cache Write



Topic : When to Use Which Formula



#Q. Assume that for a certain processor, a read request takes 100 nanoseconds on a cache miss and 15 nanoseconds on a cache hit. Suppose while running a program, it was observed that 70% of the processor's read requests result in a cache hit. The average read access time in nanoseconds is_____?

general formula:-

$$\begin{aligned} T_{avg} &= 0.7 * 15 + 0.3 * 100 \\ &= 10.5 + 30 \\ &= 40.5 \text{ ns} \end{aligned}$$

#Q. In a two-level hierarchy, if the top level has an access time of 10 ns and the bottom level has an access time of 60 ns, what is the hit rate on the top level required to give an average access time of 15ns?



$$t_{cm} = 10 \text{ ns}$$
$$t_{mm} = 60 \text{ ns}$$
$$t_{avg} = 15$$

hierarchical :-

$$15 = 10 + (1-H)60$$

$$5 = (1-H)60$$

$$H = \underline{\underline{0.9167}} \text{ Ans.}$$

#Q. In previous question if hit rate of the top-level memory is 100%, then the access time of bottom level memory will be 60 ns?

$$\begin{aligned} \text{if } H &= 100\% \\ &= 1.0 \end{aligned}$$

$$t_{avg} = t_{cm} + (1-H) t_{mm}$$

$$t_{avg} = t_{cm}$$

Ques) In prev. questⁿ speed up of CPU's mem. access time using cache as compared to without cache?

Solⁿ

$$\text{speed up} = \frac{t_{\text{mem}}}{t_{\text{avg}}} = \frac{60 \text{ ns}}{15 \text{ ns}} = 4$$

Ques)

hierarchical access

$$t_{cm} = 10 \text{ ns}$$

$$t_{mm} = 90 \text{ ns}$$

$$H = 2$$

$$t_{avg} = 9 \text{ ns}$$

Invalid

$$\text{as } t_{avg} < t_{cm}$$

not possible

#Q. Assume that for a certain processor, a read request takes 200 nanoseconds on a cache miss and 20 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The performance gain in memory access time of using cache as compared to not using cache in memory is 3.57?

$$= \frac{200}{(0.8 * 20) + (0.2 * 200)} = 3.57$$

0.31 Ans

#Q. A computer system contains a cache. Uncached memory access takes 9 times longer than access to cache. If cache has a hit ratio 0.8. The ratio of cached memory access time to uncached memory access time is? (2 decimal)

uncached \Rightarrow mem. system w/o cache \Rightarrow only mm \Rightarrow ^{access time} t_{mm}
 cached \Rightarrow —||— with cache \Rightarrow cm, mm both \Rightarrow t_{avg}

$$\begin{aligned}
 t_{cm} &= x \\
 t_{mm} &= 9x \\
 &= \frac{t_{avg}}{t_{mm}} = \frac{x + 0.2 * 9x}{9x} = \frac{2.8}{9} \\
 &= 0.31
 \end{aligned}$$



Topic : T_{avg} When Locality of Reference is Used

↓
when there is a miss, the missed block copied from mm to cm.

t_{bt} = time to transfer a block from mm to cache.

Sim. :- $T_{avg} = H * t_{cm} + (1-H) t_{bt}$

Der. :- $T_{avg} = H * t_{cm} + (1-H) (t_{cm} + t_{bt})$
or
 $= t_{cm} + (1-H) t_{bt}$

#Q. In a two-level hierarchy, the top level has an access time of 10 ns and hit rate of 90%. If the block transfer from main memory to cache takes 500ns in case of miss then average memory access time is ____?

$$t_{bt} = 500ns$$

$$\begin{aligned} t_{avg} &= 10 + 0.1 * 500ns \\ &= \underline{\underline{60ns}} \quad \text{Ans.} \end{aligned}$$

#Q. Byte transfer time from mm to cache = 50ns

block size = 16 bytes

Block transfer time from mm to cache = 800 ns?

$$\begin{aligned} t_{bt} &= 16 * 50ns \\ &= 800ns \end{aligned}$$

#Q. Byte transfer time from mm to cache = 50ns

block size = 16 words = $16 * 4B = 64B$

1 Word = 4 bytes

Block transfer time from mm to cache = 3200 ns?

$$\begin{aligned} t_{bt} &= 64 * 50ns \\ &= 3200ns \end{aligned}$$

#Q. Word transfer time from mm to cache = 50ns

block size = 16 words

Block transfer time from mm to cache = 800 ns?

$$16 * 50 = 800ns$$

#Q. Word transfer time from mm to cache = 50ns

$$\text{block size} = 64 \text{ bytes} = \frac{64 \text{ B}}{4 \text{ B}} = 16 \text{ words}$$

1 Word = 4 bytes

Block transfer time from mm to cache = 800 ns?

$$16 * 50 \text{ ns} = 800 \text{ ns}$$

#Q. First byte transfer time from mm to cache = 10ns
Remaining each byte transfer time from mm to cache = 2ns
block size = 32 bytes
Block transfer time from mm to cache = 72 ns?

$$= 10ns + (31 * 2ns)$$

$$= 72ns$$

- #Q. First word transfer time from mm to cache = 10ns
Remaining each word transfer time from mm to cache = 2ns
block size = 128 bytes = $\frac{128 \text{ B}}{2 \text{ B}} = 64 \text{ words}$
Word size = 2 bytes
Block transfer time from mm to cache = 136 ns?

$$\begin{aligned} t_{bt} &= 10 + (64 * 2) \\ &= 136 \text{ ns} \end{aligned}$$

#Q. A ~~direct mapped~~ cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20 ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. The average memory access time in ns (round off to 1 decimal place) is _____?

$$\text{block} = 256 \text{ B} = \frac{256 \text{ B}}{8 \text{ B}} = 32 \text{ words}$$

$$\text{cm size} = 1 \text{ MB}$$

$$t_{\text{cm}} = 3 \text{ ns}$$

$$H = 94\%$$

$$\begin{aligned} \text{word} &= 64 \text{ bits} \\ &= 8 \text{ B} \end{aligned}$$

$$\begin{aligned} t_{\text{bt}} &= 20 + (31 * 5) \text{ ns} \\ &= 175 \text{ ns} \end{aligned}$$

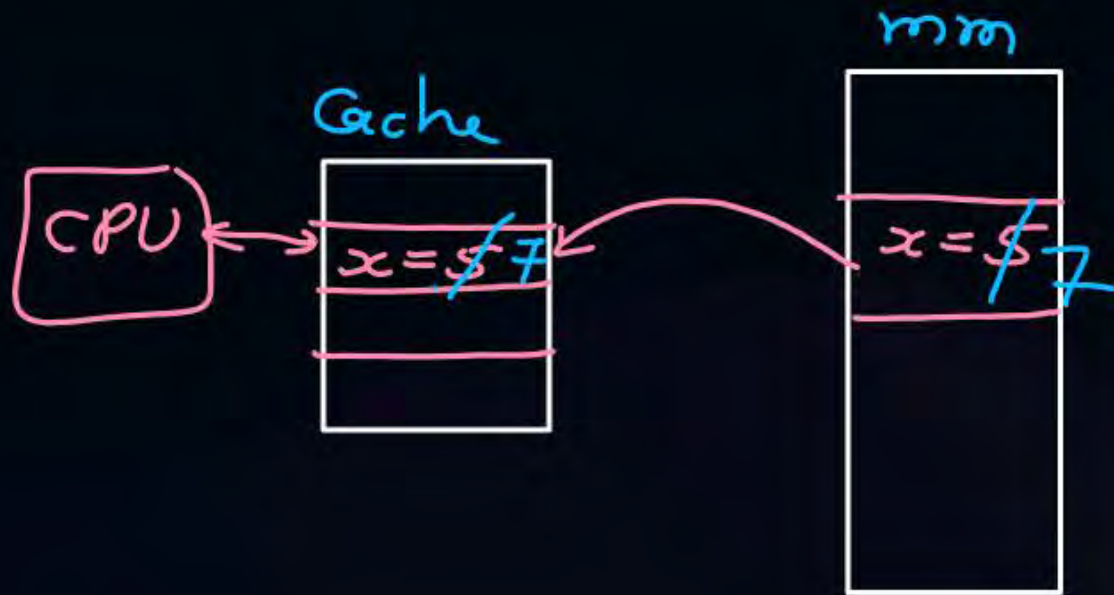
$$\text{Sim. } t_{\text{avg}} = 0.94 * 3 + 0.06 * 175 = 13.3 \text{ ns}$$

$$\text{Nil. } t_{\text{avg}} = 3 + 0.06 * 175 = 13.5 \text{ ns}$$



Topic : Cache Write or Write Propagation

If CPU performs write in cache then original content in mm should also be updated.





Topic : Cache Write or Write Propagation

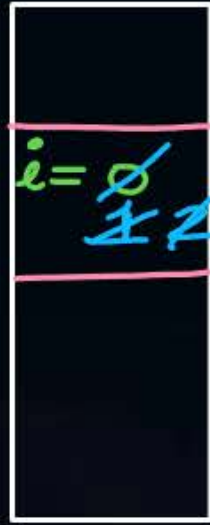
1. Write Through
2. Write Back



Topic : Write Through

CPU

cm



mm



```
for(i=0; i<1000; i++)  
{  
    ...  
}
```



Consistency in content of
cm and mm.



Time Consuming

↓
for write operation even if there is a hit in
cache, then too mm is accessed.

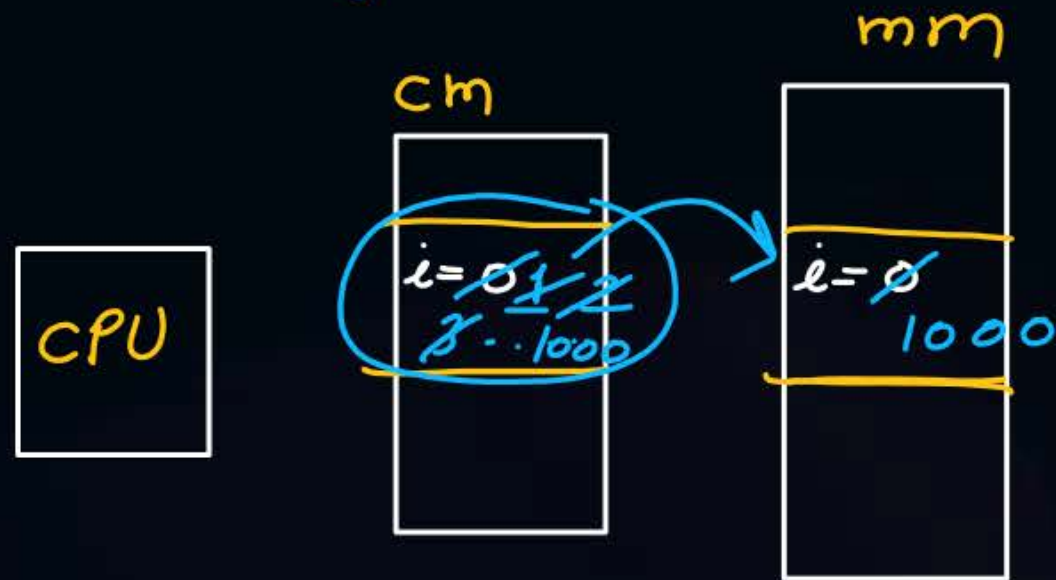
CPU performs write in
mm and cm simultaneously.

⇒ when a block is replaced from cache,
then it is removed from cache.
There is no need to write it into mm.



Topic : Write Back

cpu performs write only in cache and mm content is updated when the updated block is replaced from cache.



😊 Time Saving

☹ Inconsistency in content of cm and mm.



2 mins Summary



Topic

Locality of Reference

Topic

Cache Memory



Happy Learning

THANK - YOU