Open source tools for logic synthesis and SOC Design: An overview

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About me

- CS graduate
- Currently pursuing Mtech in embedded system @ NIELIT Calicut.
- Passionate About RTL|Digital Design and FPGA based systems and accelerators.
- Other fields of interest
    - Bare Metal C Programming | HW/SW CO Design | Computer Architecture

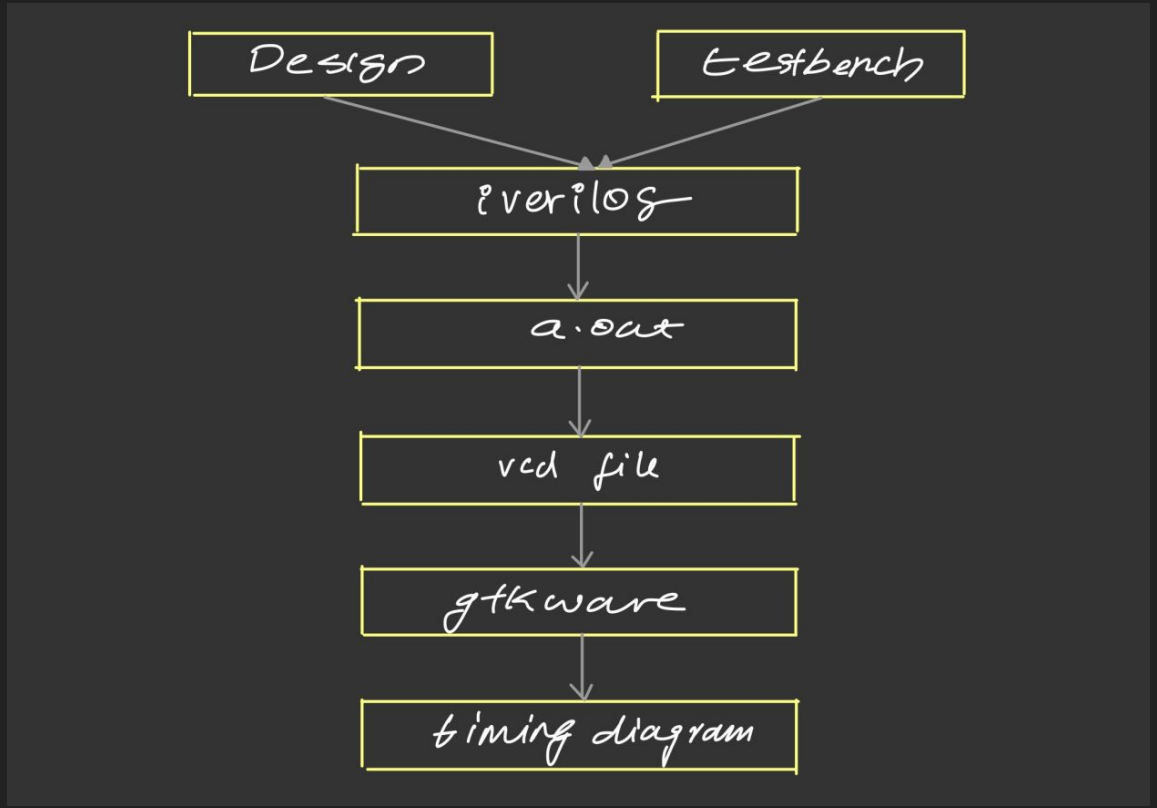
Agenda

- Open source tools for logic synthesis
  - Functional verification of digital design
  - Synthesis and Mapping
  - Gate Level Simulation
  - Demo : Generating bitstream for an FPGA using a open source flow
- Litex
  - How to install litex
  - How to run your first simulation with microwatt with litex.

Functional Verification

- Simulation
  - Simulation is the process of checking whether the design is adhering to the given specs. The tool used for simulating the design is called a simulator.
- Inputs to the simulator
  - The Design.
  - The Testbench.
- Tool Used
  - iverilog

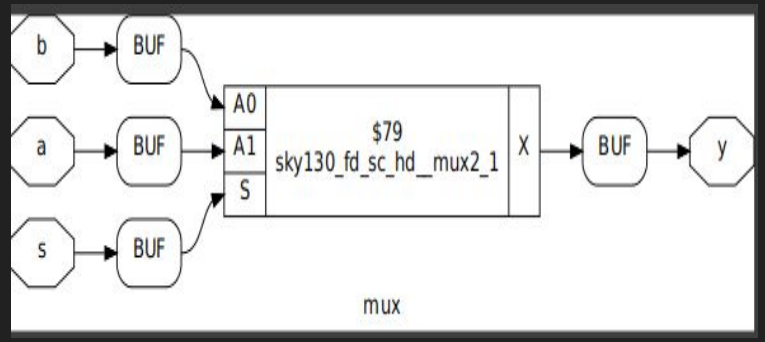
Functional Verification - iverilog flow



Logic Synthesis - What is it.?

mux.v > {} mux

```
1   module mux(a,b,s,y);
2       input a,b,s;
3       output y;
4
5       assign y=s?a:b;
6   endmodule
```



Logic Synthesis - Translation

mux.v > {} mux

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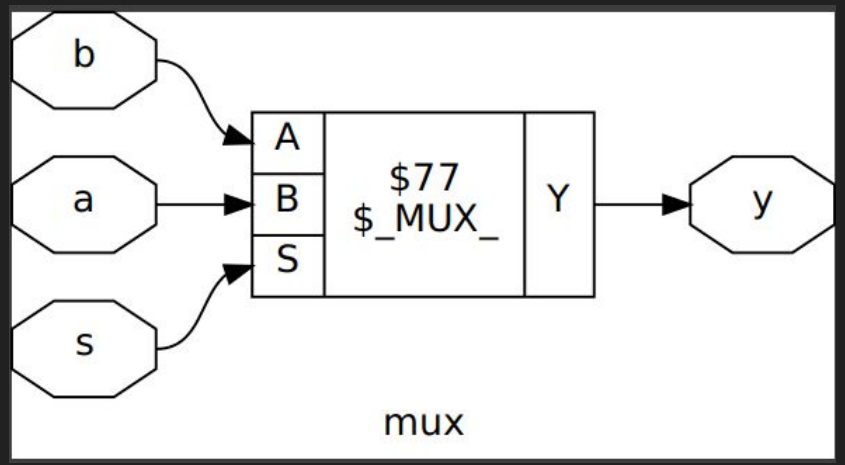
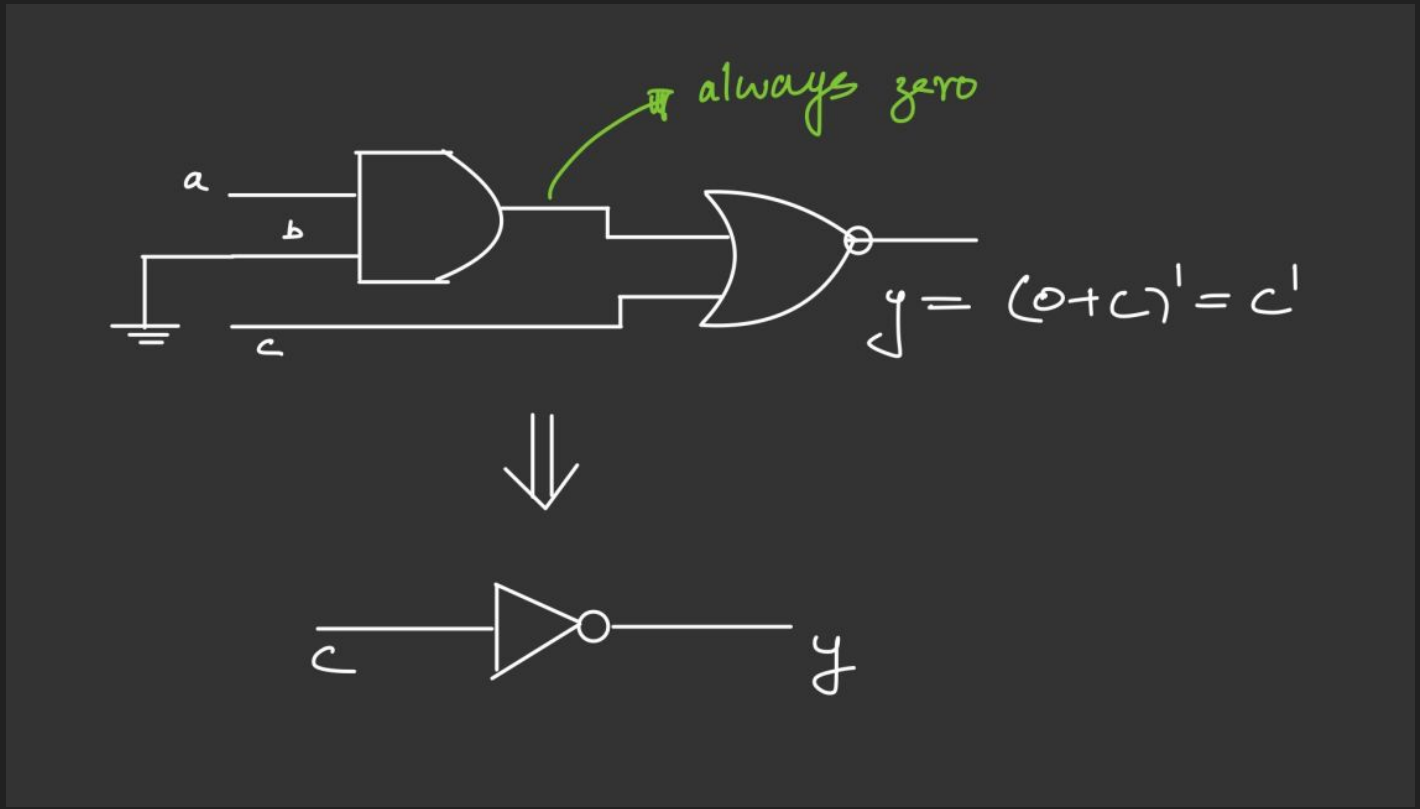
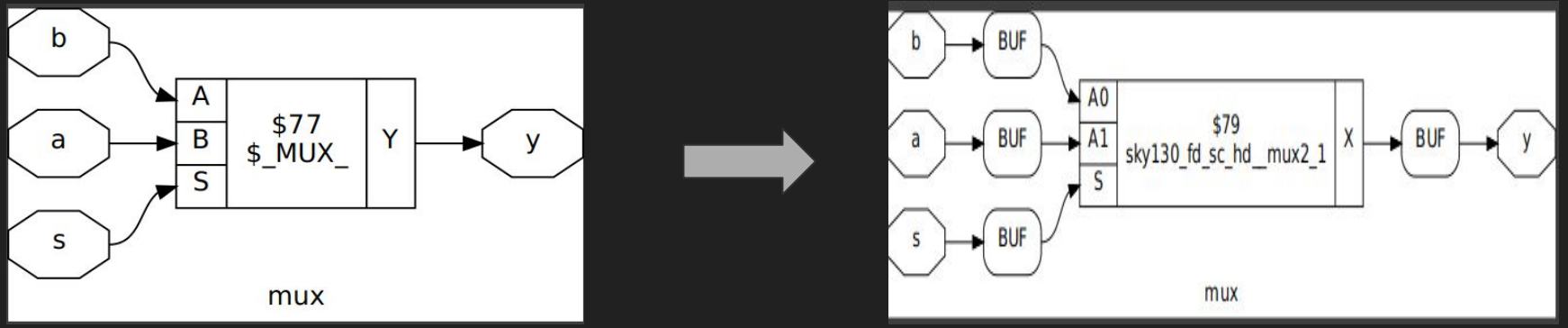


Logic Synthesis - Optimisations



Logic Synthesis - Mapping

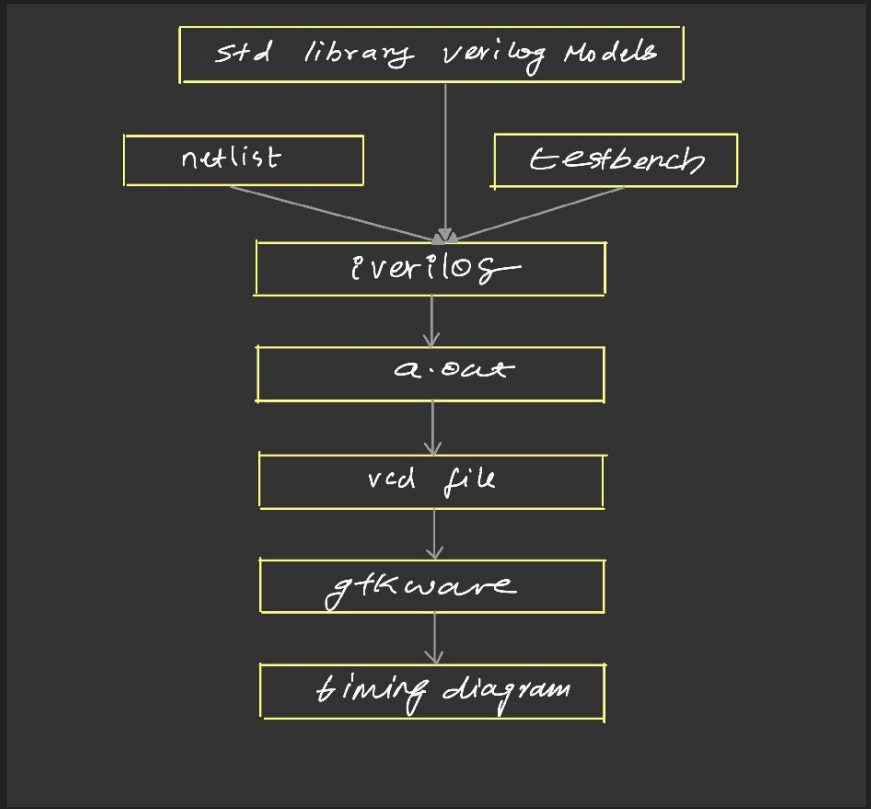


- The standard cell library
  - A standard cell library is a collection of characterized logic gates that can be used to implement digital circuits. This is usually part of set of file created by the foundry called the PDK(Process Development Kit).
  - Has many type of files including the timing/power liberty file.
  - The SkyWater Open Source PDK
    - The SkyWater Open Source PDK is a collaboration between Google and SkyWater Technology Foundry to provide a fully open source Process Design Kit and related resources, which can be used to create manufacturable designs at SkyWater’s facility.

Gate Level Simulation

- Why GLS
  - check the correctness of the design after synthesis
- Synthesis Simulations Mismatches
  - Missing signals in sensitivity list
  - Blocking and Nonblocking statements
  - Missing statements in if|case blocks

GLS with iverilog

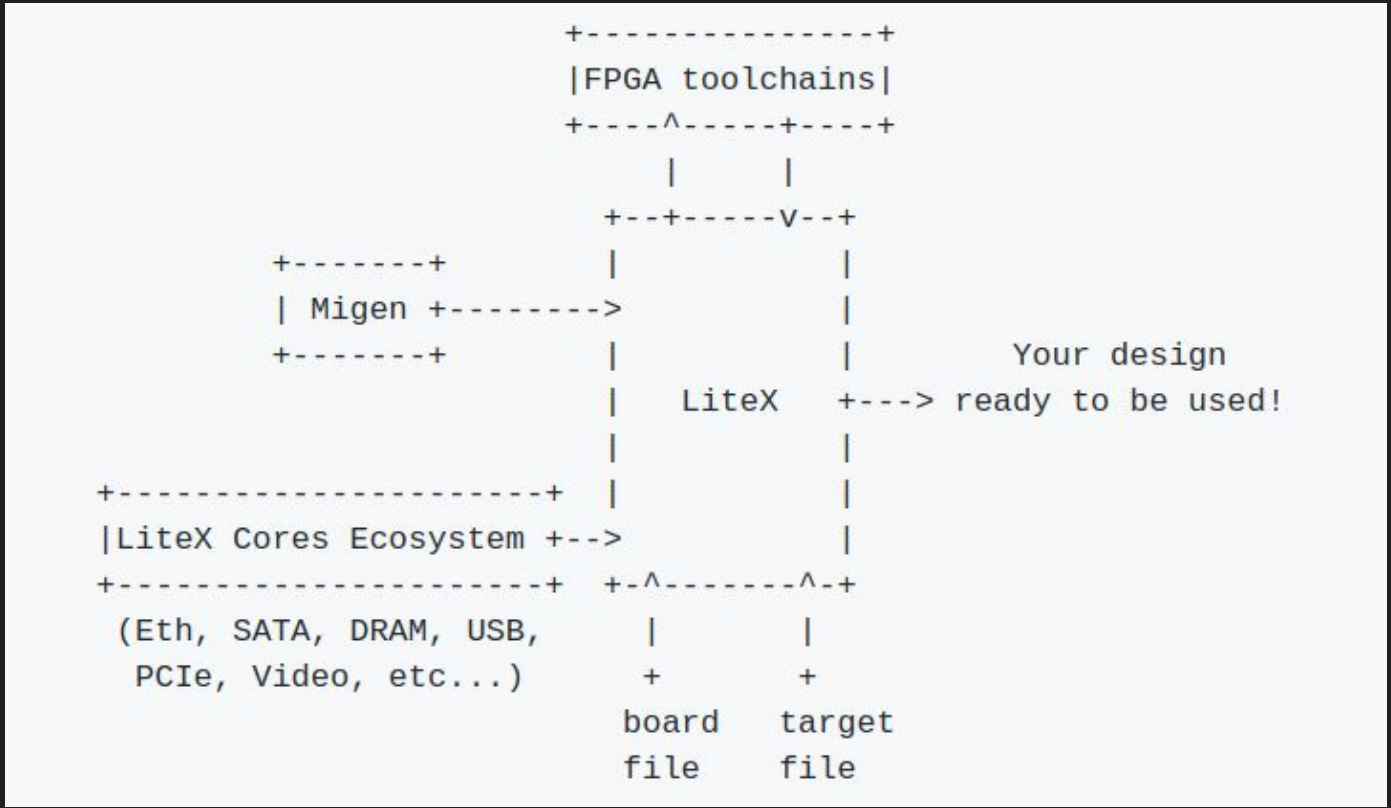


Demo

Litex

- A Framework that provides a convenient and efficient infrastructure to create FPGA Cores/SoCs
- Migen
- Buses including Wishbone and AXI
- Easy to integrate VHDL/Verilog/SystemVerilog code in LiteX!
- LiteX already supports various softcores CPUs including microwatt!!

Typical LiteX design flow



Demo - Simulating a microwatt based SOC with Litex