AMWC Final Project- Low Noise Amplifier (using Avago VMMK-1218) Design at WIFI band

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***Abstract*— We designed the Low Noise Amplifier (LNA) operating at 2.4GHz for WIFI-band using ADS software with Rogers 4350B substrate. The main goal of the paper is to design a LNA with maximum gain and with low noise figure. We used Avago VMMK-1218 ADS model which is the Enhancement mode HEMT. We simulated the S-parameters of the LNA. These simulated results are matched closely with the given Avago VMMK-1218 data sheet and if any discrepancies are there explained with proper reasoning.**

I. INTRODUCTION

The Low-noise amplifier is the first block in the receiver after the antenna and band-pass filter. This block is critical since the over-all noise figure of the system is mainly dominated by the LNA noise figure and its gain. So it is really important to design the LNA which has the maximum gain along with low-noise figure (NF) value. Generally there is a trade-off between the gain of the LNA and NF of the LNA where we can't achieve the both in the same time. In this paper we try to design the LNA with maximum gain with decent low noise figure. The following figure shows the RF receiver block diagram which has the LNA as the first block after antenna.

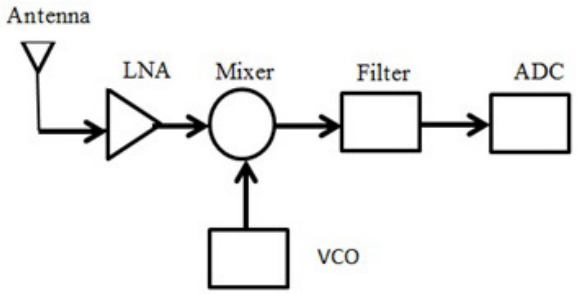

Fig. 1. RF receiver block diagram

The following equations shows the cascaded noise figure.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + ... \quad (1)$$

$$NF = 10log(F) \quad (2)$$

from the above equations the LNA nose figure and gain are critical in overall noise figure value. In this paper we designed the ***HEMT*** based LNA which is operated in enhancement mode *i.e.*the gate voltage is positive compared to depletion mode FET's. So this FET uses the uni-polarity power-supplies at gate and drain.

The Paper mainly discuss mainly about the design of Low Noise Amplifier (LNA) from fundamental level starting from design and selection of the noise figure and design the matched network for source and load. We simulated S-parameters of the designed low noise amplifier. In our class, professor gave us brief introduction about the design of the LNA which is much useful in this complete design and we followed all the steps to design the LNA. We used the Avago VMMK-1218 ADS model in the design.

The design of low noise-amplifier (LNA) involves multiple steps mainly, I-V characteristics (DC bias), Bias-Tee, Stability, Noise figure circles, source impedance selection and match network at source and load. Each one of the step is explained clearly in the later sections. We used Rogers 4350B substrate with ϵ_r is 3.745 and loss tangent of 0.0031, the height of the substrate is 60 mils and thickness of the substrate is 1.4 mil.

From this data sheet of the Avago VMMK-1218, the low noise amplifier designed is operating at 2.4 GHz needs dc power supplies of the 3v for drain and gate voltage varies from 0v to 1v. The drain current at bias point is limited by 20 mA. The gate maximum current is limited by 0.4 uA for safe operation. The maximum current is limited by 100 mAmp from the data sheet.

We simulated the small-signal gain vs frequency which is the S-parameters of the low noise amplifier. In the simulations of s-parameters the $S21(dB)$ shows the forward gain vs frequency of the transistor. We have to check the $S12(dB)$ to know how-much reverse path gain is attained at the designed band of interest.

Once we fabricate this design, we can measure the linear and the non-linear measurements are like Pin vs Pout, IM3, 1-dB compression point can be measured to check the linearity of the low noise amplifier. These measurements are performed using 2-tone test which we did similar to our previous labs.

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II. Design of the Low Noise Amplifier

A. Theory of the operation

The LNA design is nothing but the trade-off of noise figure and gain selection based on the requirements. The design contains DC bias, bias stability, finding the noise figure circles, that touches the gain circles. Based on this we select particular source impedance which matches with our requirements. Now for this source impedance design the source matching network and use conjugate match for load side to get maximum gain.
Noise figure circles are given by the following formulas.

$$F = F_{min} + \frac{R_N}{G_S}(Y_s - Y_{opt})^2 \tag{3}$$

Here F is the desired NF value, F_{min} is the minimum NF value by the transistor, R_N is the noise resistance of the transistor, Y_s is equal to $G_s + j * B_s$ source admittance of the transistor, Y_{opt} is source admittance of the transistor for minimum noise figure. The values of the F_{min}, R_N and Y_{opt} are given by the manufacturer. The $S2P$ file contains these details. From the admittance of the source, we can calculate the reflection (Γ) of the source. Typical R_N is 5-20 Ohms. For Avago VMMK-1218 these values are

Parameter (Units)	Value
R_N (Ohms)	5
F_{min} (dB)	0.19
Γ_{opt}	0.56+j*0.4045
I_{ds} (A)	20e-3
V_{ds} (V)	3

TABLE I
MANUFACTURER PARAMETERS OF THE AVAGO VMMK-1218

The second term specifies the sensitivity of the transistor. The admittance can be written in reflection coefficient. The NF value can be described using reflection coefficients as given below.

$$y_s = \frac{1}{Z_0}\frac{1-\Gamma_s}{1+\Gamma_s} \tag{4}$$

$$y_{opt} = \frac{1}{Z_0}\frac{1-\Gamma_{opt}}{1+\Gamma_{opt}} \tag{5}$$

$$F = F_{min} + \frac{4R_N}{Z_0}\frac{(\Gamma_s - \Gamma_{opt})^2}{(1+\Gamma_{opt})^2(1+\Gamma_s)^2} \tag{6}$$

The noise figure circles has center and radius and plotted for different NF values.

$$C_{NF} = \frac{\Gamma_{opt}}{N+1} \tag{7}$$

$$R_{NF} = \frac{\sqrt{(N(N+1+(\Gamma_{opt})^2)}}{N+1} \tag{8}$$

Once the gain circles are plotted, choose the Z_{in} where it touches both of the circles. (not to select intersecting circles). As mentioned in the Introduction, design of the low noise-amplifier (LNA) involves multiple steps mainly, I-V characteristics (DC bias), Bias-Tee, Stability, Noise figure circles, source impedance selection and match network at source and load. At each stage we need to check the stability of the LNA at operating frequency (2.4GHz) and with in desired band of interest. In this section each step is explained in-detail in a separate sub-section.

B. I-V characteristics (DC bias)

In this section, We picked the bias-point to operate the transistor in enhancement mode, the gate voltage is positive. We vary the V_{DS} and V_{GS} to see the operating point to pick. *e.g.*We are looking for less drain current at 3V supply voltage. The given ADS template has this step which plots the I-V characteristics. We choose an operating point such that it matches with the 3V and 20mA data-sheet S-parameters.

Design: We imported the Avago VMMK-1218 transistor model which is a 3-port model which is same as real-transistor.

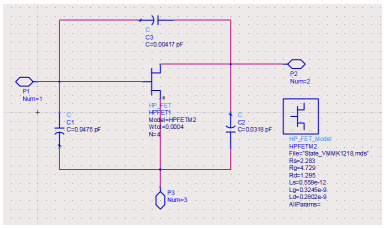

Fig. 2. Avago VMMK-1218 Transistor in ADS

The I-V characteristics are performed as shown below. The DC power consumption is 0.059 watts. The results are

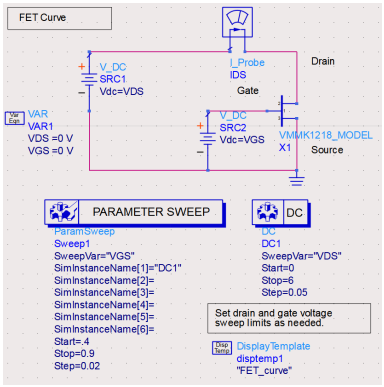

Fig. 3. I-V characteristics Schematic

shown below from ADS data set. From this graph, it is clear that 3V and 20mA operating point is at V_{gs} 0.54 Volts. After completing this section we understood the operating point selection, gate voltage and DC power consumption for the selecting bias-point.

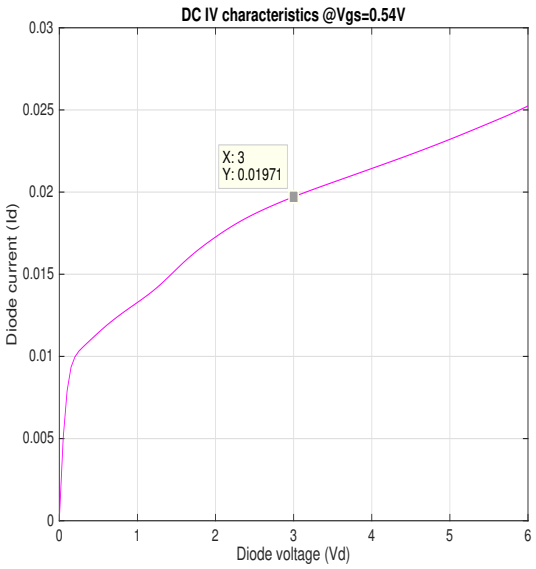

Fig. 4. I-V characteristics data set

C. Bias-Tee design

In this section, we added bias-tee sections to both gate and drain side. Ideally we need an RF choke and DC-blocker capacitor. It uses to protect the transistor to avoid any DC input from signal and DC output to load. The RF choke protects the RF is not coming from DC power supplies. The bias tee is designed as per the class notes using the radial stub. It is simple here that, we used high impedance transmission (Tx) line as inductor, added capacitor to block DC at inductor, the capacitor is connected with GND. But to avoid the vias, we used the $\lambda/4$ tx line, so that convert from short circuit (SC) to open circuit (OC). This $\lambda/4$ tx line is designed using the radial stub, so that we can operate over broad-band rather than the lumped elements and occupies less space compared to normal tx lines.

From the Class-notes the bias-tee can be designed in different ways to replace this ideal components with micro-strip stubs or transmission lines. Her we picked the radial stub method. We used the Line-cal tool in ADS to design the stub lengths and width from electrical lengths to physical lengths. We used the settings of the Rogers 4350B substrate to compute the physical lengths. The following figure shows the Line-cal settings for MStub. From the lecture notes the bias-tee of the gate side is more crucial for LNA design. We used the radial-stub one to design the bias-tee in the drain side too. The radial stub is used since it is simpler than lumped bias-tee (few components), more compact than linear stub and wide-band bandwidth than linear stub. Lumped bias-tee with high-Z quarter-wave transformer is wide band but complex to fabricate.

In this design the inductor is replaced with a high-Z transmission line, added more capacitors at gate side is conventional design, but caps need the short circuit which need the via. Instead of capacitors with SC if we design (90 deg) open line which acts as short circuit at inductor. This is connected using the magic-tee. Now open stub is replaced by radial stub. Here we tune the couple of parameters using **Tuning** option in ADS schematic to get the maximum stability. We added an extra transmission line from drain to this setup. The following figure shows the bias-tee at gate side. In the same way the drain bias-tee is designed. At drain

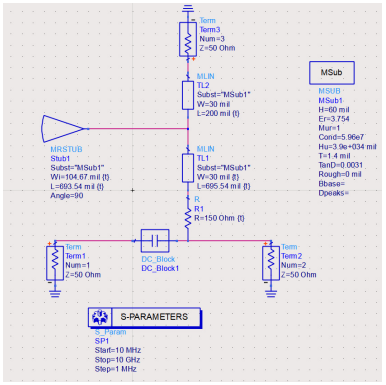

Fig. 5. Bias-tee at gate side

bias-tee, we don't need this complex design, but we designed the same way as gate side. The following figure shows the bias-tee at drain side. The following figures shows the S-

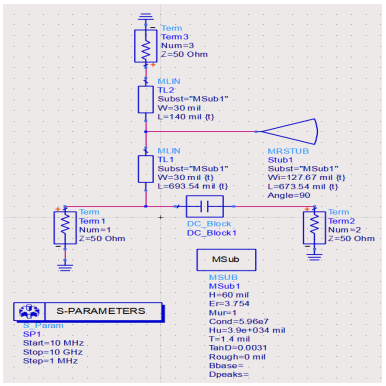

Fig. 6. Bias-tee at drain side

parameters of the bias-tee at output and input.

D. Stability

The important parameter need to verify at each stage of LNA design is Stability. We need to verify the transistor is un-conditionally stable always or not, if not un-conditional stable need to find the regions where the transistor is stable. The measurement of stability is provided in ADS by different parameters like Stabfact, Mu parameters in ADS. In the gate bias, we added an extra resistor in to reduce the gate current where we used 150 ohms here. We added a resistor and a capacitor in parallel to make gate bias more stable. We used resistor of 33 ohms and capacitor of 0.5 pF. We used the **Tuning** option in Schematic to vary

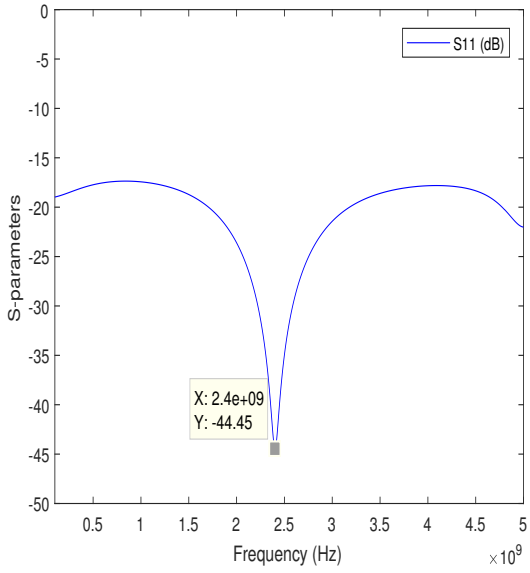

Fig. 7. $S11$ of the Input Bias

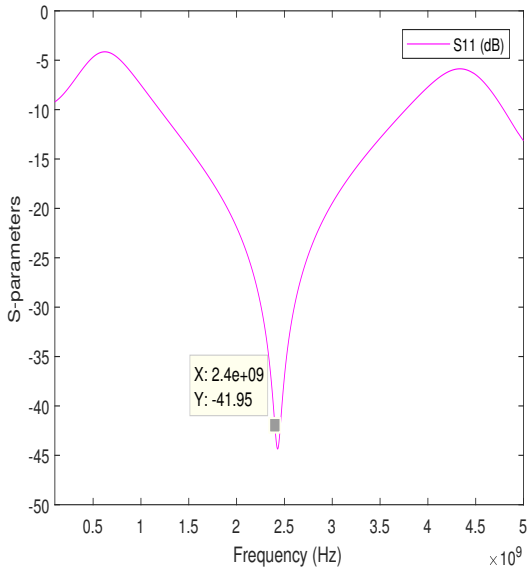

Fig. 8. $S11$ of the output Bias

the parameters of the resistor and capacitor. The following figure shows the schematic with bias-tee and stability. The following figure shows the Maximum gain, stability factor and Mu factor for the schematic shown above.

From the above figures, we can assure the transistor is almost stable over the desired band. The S-parameters are shown below for the transistor gives the forward gain over the frequency range.

So Clearly the low-noise amplifier is stable till this point. Now we weed to design the optimum source impedance and matched network for the transistor. This matched network is required for both source and load side and found by performing the following sections.

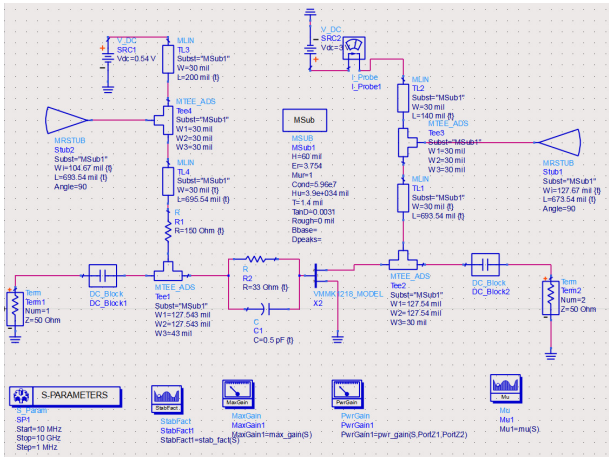

Fig. 9. Schematic with Bias-tee circuit

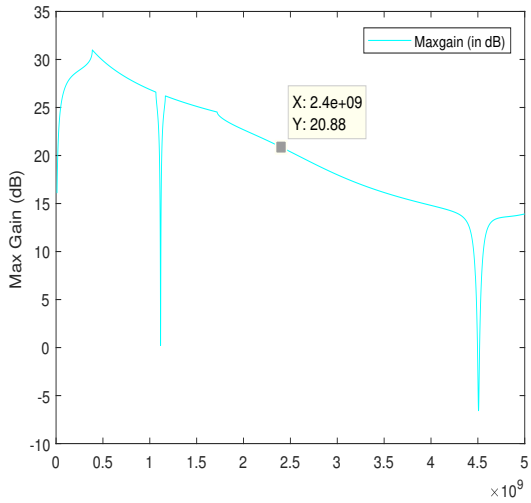

Fig. 10. Maximum gain for the Bias-tee circuit

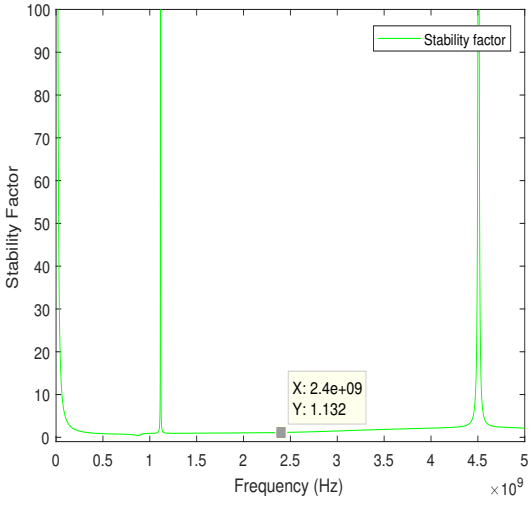

Fig. 11. Stability factor for the Bias-tee circuit

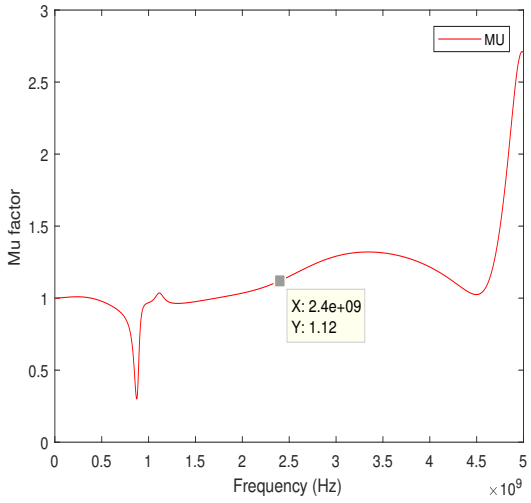

Fig. 12. Mu factor for the Bias-tee circuit

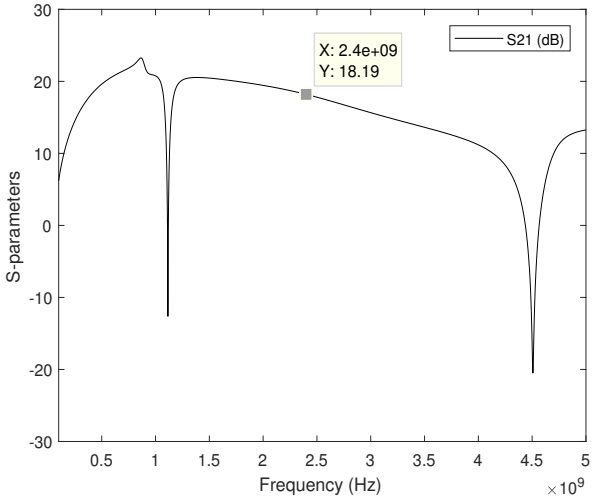

Fig. 13. S-parameters for the Bias-tee circuit

E. Noise figure & gain circles

Understanding this step is critical in the design since we need to choose either our LNA designed should be for maximum gain or low noise figure. In this step, ADS draws the noise figure circles and gain circles to find the source impedance of the source that gives best gain or best noise figure value. In the ADS data set, we can see the contours of the gain circles and noise figure circles. At the end of this step, we have to pick an impedance which gave either maximum gain or best noise figure. Clearly from theory of operation, both NF and G are important to reduce the overall noise figure values where there is a trade-off. Here we pick the point for decent gain with low-noise figure. We used NF value of 0.3 dB and available gain of 17.87 dB.

The following figures shows the Noise figure parameters from manufacturer and interpolated at all frequencies. The table provides the interpolated parameters at 2.4 GHz.

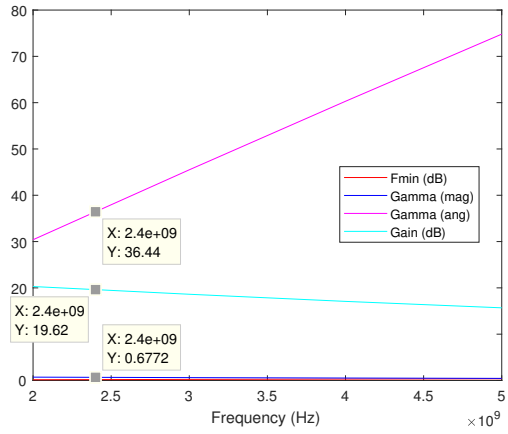

Fig. 14. NF parameters extraction

Parameter (Units)	Value
R_N (Ohms)	5
F_{min} (dB)	0.19
Γ_{opt}	0.56+j*0.4045
$Gain$ (dB)	19.62

TABLE II
NF PARAMETERS OF THE AVAGO VMMK-1218

Setup: We gave the operating point DC power supply values which we got in the I-V characteristics section. We connected the transistor with bias-tee which we designed in the last-step. We draw the noise figure circles and gain circles. We used this source-impedance in the matched load design at source. The following figures shows the Noise figure circles schematic and its example results data-set for gain of 18.32 dB and NF of 0.37 dB.

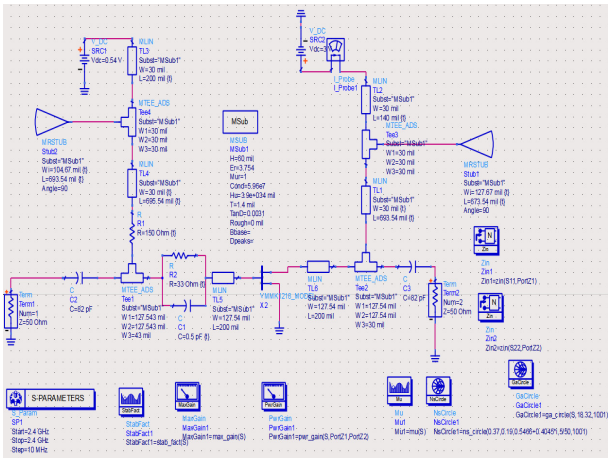

Fig. 15. Noise figure & gain circles schematic

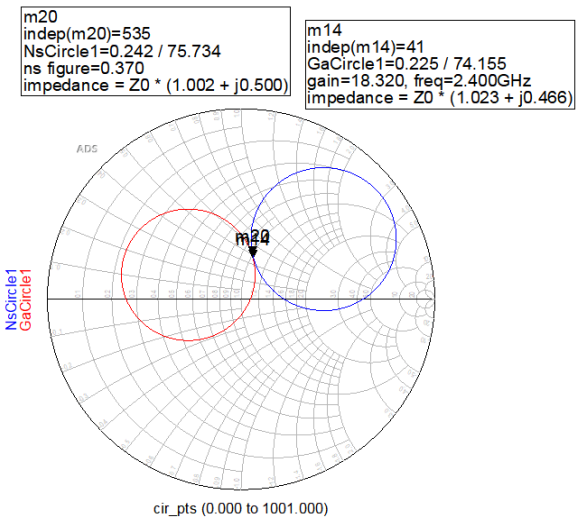

Fig. 16. Data set for Noise figure & gain circles schematic

We got the source-impedance which maximizes the power-gain and has minimum NF value. We plotted multiple gain circles and NF circles and finds the best impedance. The following figures shows the Noise figure circles and gain circles overlap each other (Gain circles, NF circles). The

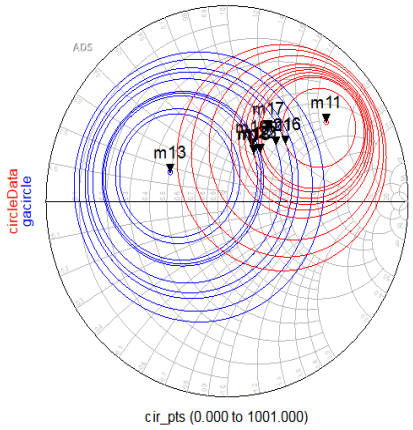

Fig. 17. Noise figure & gain circles schematic

following equations used to plot the circles. For gain circles the parameters are index value, $(maximumgain-x)$ which is the gain circle we want to draw and #points in the circle. For NF circle, the parameters are new NF value, NF circle center value, Γ_{opt}, R_N and #points in the circle.

$$ga_{circle} = ga_{circle}(S[indx], MaxGain1[indx] - 0, 1, 2, 51) \quad (9)$$

$$cir_{Data} = ns_{cir}(0.19+0.1, 0.5, 0.19, 0.54+0.4*i, 5/50, 51) \quad (10)$$

Here we choose decent gain of 17.87dB, NF value of 0.3dB results the normalized Z_{in}=(1.241+j*0.689). So the source-impedance is **62.05+j*34.45 ohms**.

F. Source-matched network

As described in the previous section, using ADS smith chart utility we designed the source matched network. Source impedance is 62.05+j*34.45 ohms. This impedance should be matched to 50ohms line of source. We need to design the matched network for this source impedance. The ADS software with smith chart utility has the the flexibility to design the matched network. The following figure shows the source matched network.

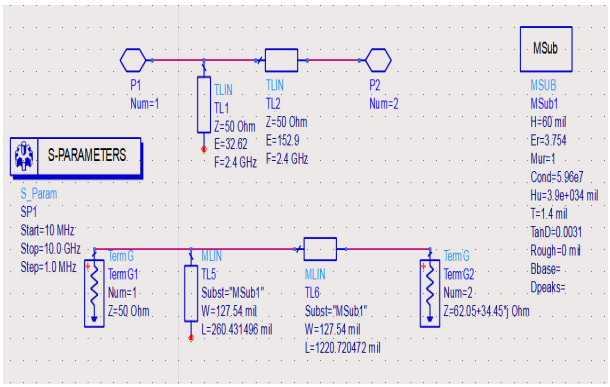

Fig. 18. Source matching network

We simulated the S-parameters for the matched network and the following figure shows the perfect matching at the desired band.

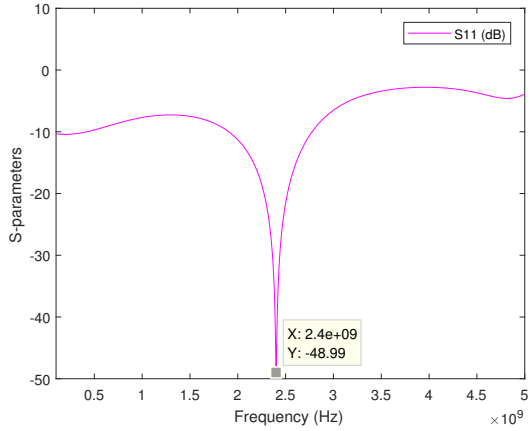

Fig. 19. S-parameters of the source matching network

G. Load-matched network

From the previous steps, we got the source impedance which gives better gain and NF values and load-impedance which gives the maximum power delivered to the load. So we used the conjugate match at the load to deliver maximum power to load. The computed NF value is independent of the load-impedance. We computed the Z_{out} of the transistor which is 32.25-j*39.146 ohms and set the load impedance to match is conjugate of this value. The load-impedance is

32.25+j*39.146 ohms. Using the Smith Chart Utility, we got the schematics with equivalent electrical lengths. By using the Line-cal tool in ADS, we got the equivalent physical length of the transmission lines. We used open stubs which are easy to design, since these don't need to connect to via. The following figure shows the load-matched network.

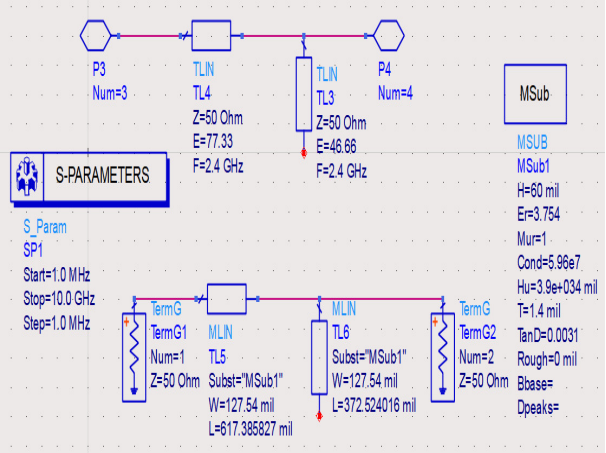

Fig. 20. Load-matching network

We simulated the S-parameters for the matched network and the following figure shows the perfect matching at the desired band.

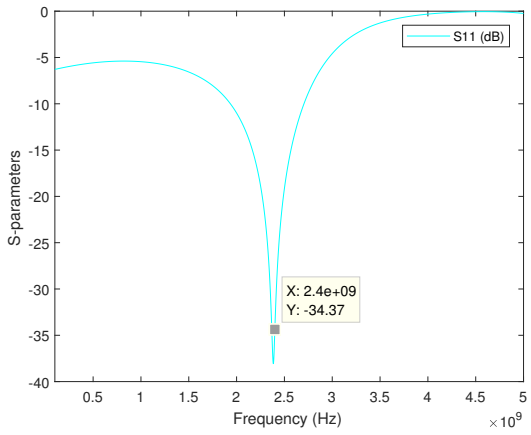

Fig. 21. S-parameters of the load matching network

H. Complete design

In this section, we integrate all the schematic of all the sections designed till now. The following figure shows the complete design of the LNA. We added a few transmission lines to connect the ports and for soldering components. We added coupling capacitor of 27 pF at source and load. The transistor and caps used are 0402 size. The gain and NF circles are given below for gain of 17.52 dB and 0.3 dB. The following figure shows the gain and noise figure circles for the complete design. The complete schematic is shown

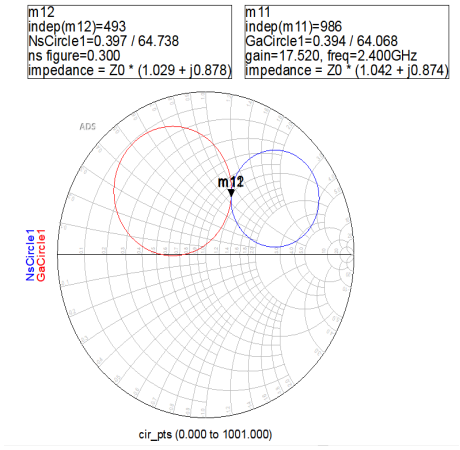

Fig. 22. Gain and NF circles of the complete LNA

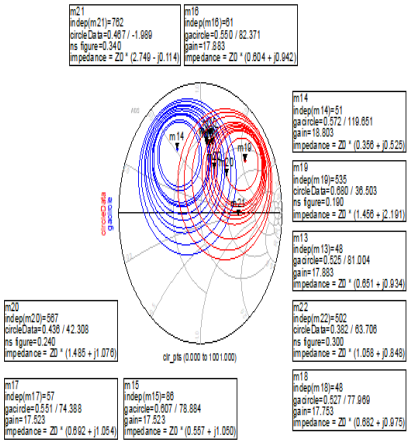

Fig. 23. Gain and NF circles of the LNA

below figure 24.

I. Layout design

We integrated the matched network with the bias-tee schematic. In this step, we replace all the lumped elements with its equivalent circuits. The capacitor equivalent circuits are designed using the real components S-parameters loaded to schematic. The resistors used in the design are 150 ohms and 33 ohms. The capacitor used in the design is 27 pF and 0.5 pF. In the schematic, additional transmission line of 200 mils is added to make sure we have enough transmission line to place the ports of the transistors. The capacitors are "$JT1R07S0R5$" series can bear maximum voltage till 50V. The following figure shows the schematic used for layout generation. We created the layout for the specified design. The following figure shows the layout of the LNA.

III. S-PARAMETERS OF THE LNA

It is necessary to measure the S-parameters of the LNA, which provides significant in-sight about the forward gain, reverse gain and reflections at input and output ports. We provided the DC power supply of 3 volts to drain and

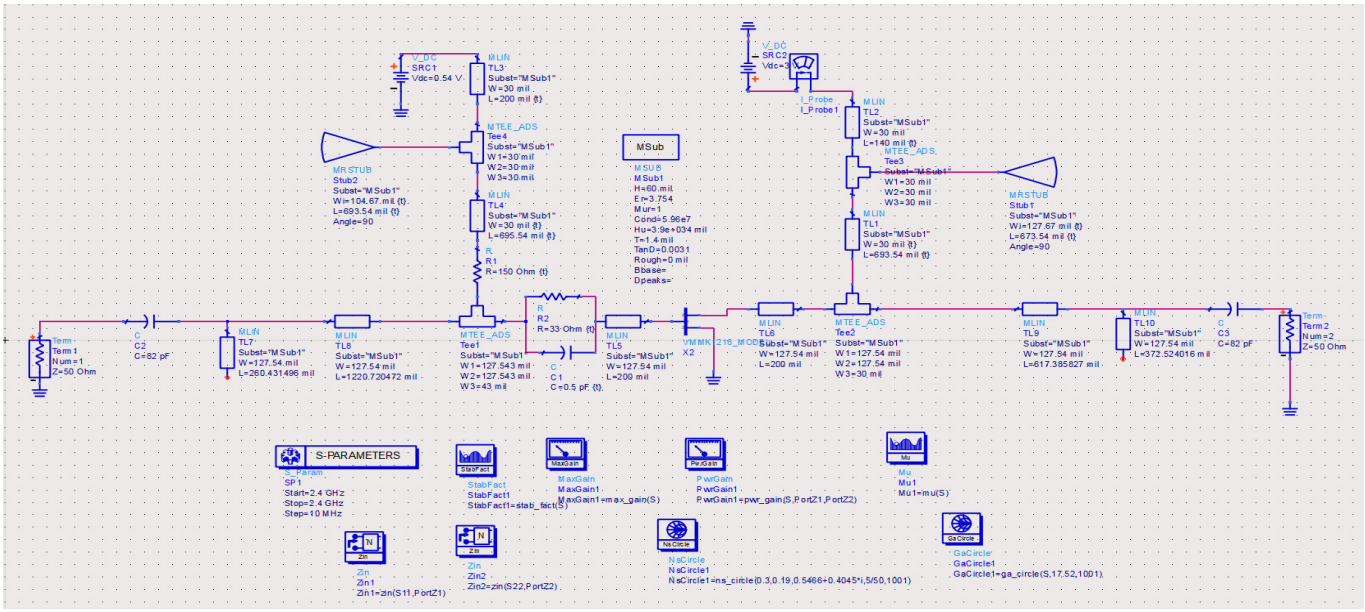

Fig. 24. Schematic of the Low Noise Amplifier (LNA)

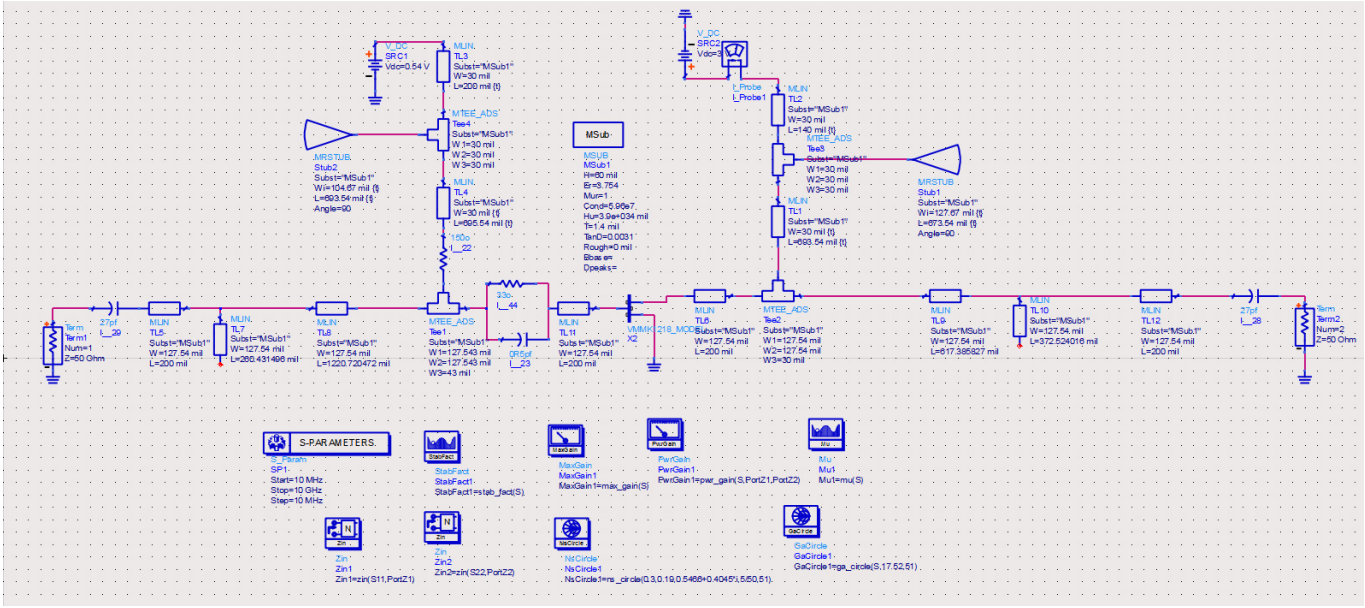

Fig. 25. Schematic of the Low Noise Amplifier (LNA)

0.54 volts to gate so that the drain current reaches the 20 mAmp. The LNA designed to operates at 2.4 GHz, select the frequency range of 10 MHz to 5 GHz. The S-parameters of the complete low noise amplifier are simulated and given below. Clearly at 2.4 GHz WIFI band we can see a forward gain of S_{21} **17.28 dB** and return loss S_{11} is better than **-5.88 dB**. These are the results with 82pF capacitor as DC blocking capacitor. The following figure shows the S-parameters of the final LNA with 82 pF cap.

Observations: The S_{11} is less than 10dB, this is due to we matched the source impedance for max gain and low NF results more reflections, implies the S_{11} decreases in performance. This is the expected trade-off for LNA design. The S_{21} is resulted as 17.3 dB which is pretty much high value for the LNA. The noise figure (NF) of the over-all system is 0.3 dB which is a decent value for WIFI band wireless communications.

From the layout, it is clear that we extended the transmission lines for the power-supply lines. The S_{12} is around **-28.18 dB** and S_{22} is **-30.18 dB** from simulation respectively. The following figures shows the reverse gain and output return loss values. From the reverse gain is really good one across the desired band which is less than -28 dB. By looking the S-parameters it is clear the transistor is designed for optimum at 2.4 GHz. But by using the 27pF and 0.5pF caps,

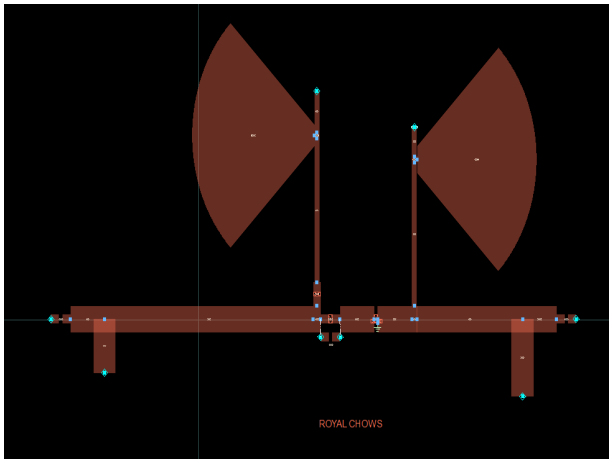

Fig. 26. Layout of the Low Noise Amplifier (LNA)

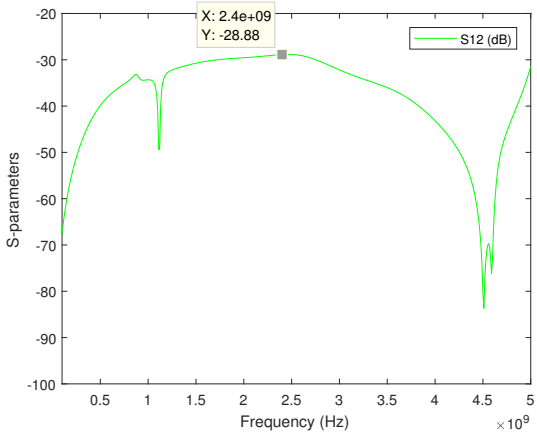

Fig. 29. S12 (dB) of the LNA

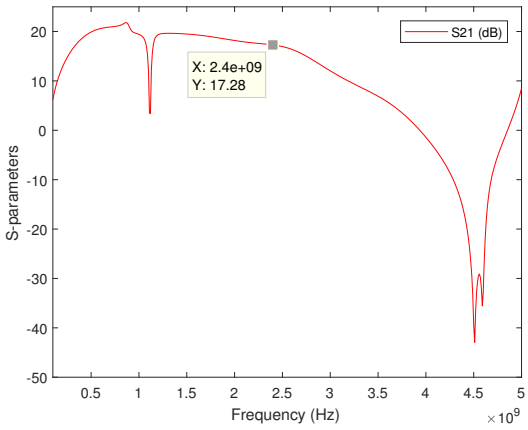

Fig. 27. S21 (dB) of the LNA

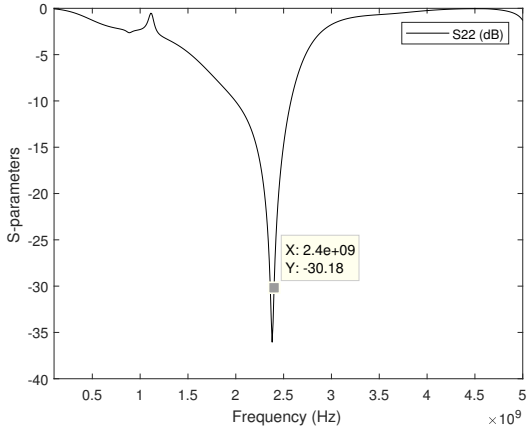

Fig. 30. S22 (dB) of the LNA

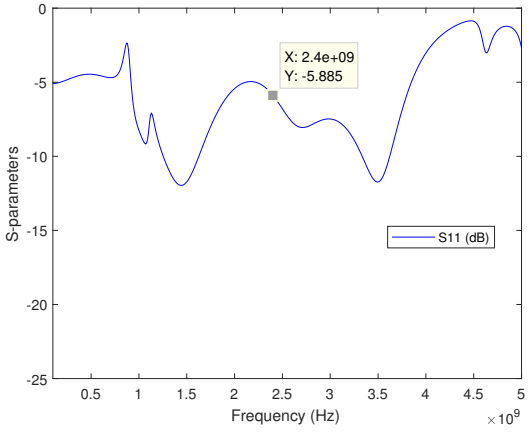

Fig. 28. S11 (dB) of the LNA

the S_{11} is improved by 2-3 dB, where as S_{21} is decreased by 2 dB and S_{22} is decreased by 14 dB.

Once we fabricate this model, we can observe the linear measurement to verify the S-parameters and non-linear measurements like $P1$ dB and $OIP3$ values using 2-tone tests.

IV. CONCLUSIONS

We designed the low noise amplifier with Rogers 4350B substrate with Effective permittivity is 3.745 from scratch and understood each component in the design effects the LNA performance . We simulated the S-parameters of the LNA and found 17.3 dB gain by the LAN with NF value is 0.3 dB. We understood how to setup the DC values for LNA. We verified the simulated values are closely matching with the data sheet values. This gave us confidence to design any RF component in the day to day life. This LNA gave the best performance at WIFI band which is 2.4 GHz.

REFERENCES

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