Lab 3 - Part II: Design the Power Amplifier (CREE CGH40010F) and Measurements on Power Amplifier

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***Abstract*— We designed the Power Amplifier (PA) operating at 2.45GHz for WIFI-band using ADS software and fabricated using Rogers 4350B substrate. We performed the linear and non-linear measurements on the Cree CGH40010F transistor which is operating at 2.45 GHz. The linear measurements are the small signal gain vs frequency, which is observed using S-parameters of the transistor. The non-linear measurements are the large-signal gain analysis, which includes the Pin vs Pout graph and IM3 vs frequency. These measurement results are matched closely with the given Cree CGH40010F data sheet.**

I. INTRODUCTION

The Paper mainly discuss in 2-parts, where as in part-I discuss mainly about the design of Power Amplifier (PA) which includes the fabrication and part-II discuss mainly about the measurements on the designed PA. We measured few parameters of the designed power amplifier. Those are linear and non-linear measurements. In our lab, professor gave us a CREE CGH40010F transistor and attached this to the designed board which is operating at 2.45 GHz. This board has RF ports for input and output.

The design of power-amplifier (PA) involves multiple steps mainly, I-V characteristics, Bias-Tee, Stability, Load-pull, Source-pull and match network. Each of the step is explained in the later sections. The Fabrication is done with LPKF machine using Rogers 4350B substrate and Heat sink is attached to the design board. The fabrication process is explained separately in the later section in-detail.

From this data sheet of the Cree CGH40010F, the power amplifier designed is operating at 2.45 GHz needs dc power supplies of the 28v for drain and gate voltage varies from -4v to -1v. The breakdown voltage is 110v. Since by using the bias point we are not sure of operating at which class, since class A has peak voltage of $2Vds$, where as class E has $3.56Vds$, so it is safe to operate the drain at 28v. The drain maximum current is limited by 200 mA. The gate maximum current is limited by 10 mA for safe operation. The maximum current is limited by 1.5 Amp from the data sheet.

The linear measurements are the small-signal gain vs frequency. These are measured using the S-parameters of the power amplifier. In that measurement of s-pram's the $S21(dB)$ shows the forward gain vs frequency of the transistor. We have to check the $S12(dB)$ to know how-much reverse path gain is attained at the designed band of interest. The non-linear measurements are like Pin vs Pout, IM3, 1-dB compression point. These measurements are performed using 2-tone test which we did similar to our previous labs.

The power rating of the PA is 13 watts. We used a couple of attenuators in our circuit to protect the PA and test equipment. From the above figure we can see an attenuators of 10dB with high power rating. The spectrum analyzer handles maximum power of 1watt. We added one more 10dB attenuators with lower power rating. Accounting the cable losses in all measurements are important.We designed the CREE CGH40010F Power amplifier and measured the RF performance. The performance metrics are compared with the data-sheet values and explained if any discrepancy exists.

II. DESIGN OF THE POWER AMPLIFIER

As mentioned in the Introduction, design of PA includes the following steps mainly I-V characteristics, Bias-Tee, Stability, Load-pull, Source-pull and match network. At each stage we need to check the stability of the PA at operating frequency and desired band of interest. In this section each step is explained in-detail.

A. I-V characteristics

In this section, we show that what is the operating point of the PA which mainly says the operating class and what are the bias-point we are looking to achieve certain parameters. Example are we looking for more-gain, more-efficiency, more output power..etc. The given ADS template have this step which plots the I-V characteristics. We can choose an operating point such that it maximizes either power output or efficiency. This steps results the $Ropt$ optimum output resistance for the load.

Design: We imported the CREE 40010F transistor model which is a 6-port model includes the parasitic effects same as real-transistor.

The transistor has t=25 and rth is 8 ohms.

The I-V characteristics are performed as shown below.

The results are shown below from ADS data set.

From the data set, it is observed that to operate at Class-A, the Ropt is 37.5 ohms. It has efficiency of 50 percentage,

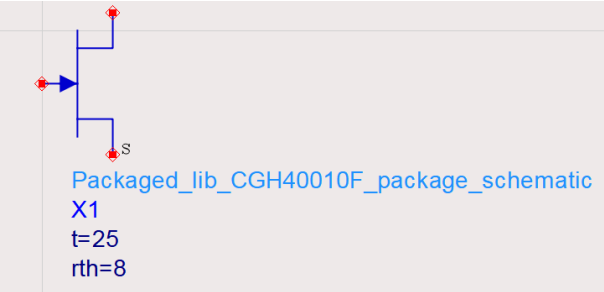

Fig. 1. CG40010F Transistor in ADS

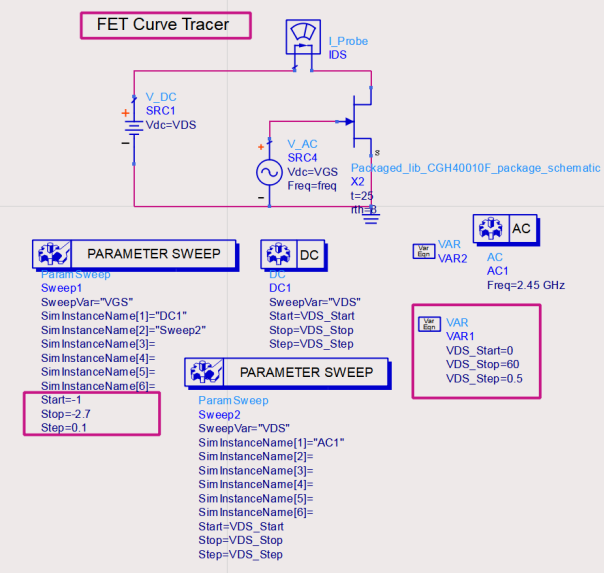

Fig. 2. I-V characteristics Schematic

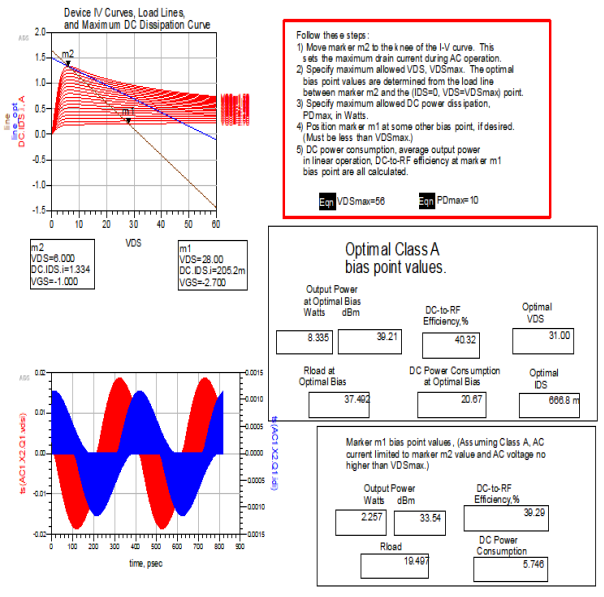

Fig. 3. I-V characteristics data set

but we are operating at much lower than class-A bias point. we picked a point at VDS=28v and Ids=200mA. At this operating point, we can see DC power-consumption is reduced. The current and voltage curves over time are also provided for class-A. This the current internal to transistor so we can see Q1 in the names.

After completing this section we understood the operating point selection, DC power consumption, maximum output power and *Ropt* for the selecting bias-point. For the choose operating point (m1), the *Ropt* results as 19.5 ohms.

B. Bias-Tee design

In this section, we added bias-tee sections to both gate and drain side. Ideal we need an RF choke and dc-blocker capacitor. It uses to protect the transistor to avoid any dc input from signal and DC output to load.The following figures shows the bias-tee at gate and drain side.

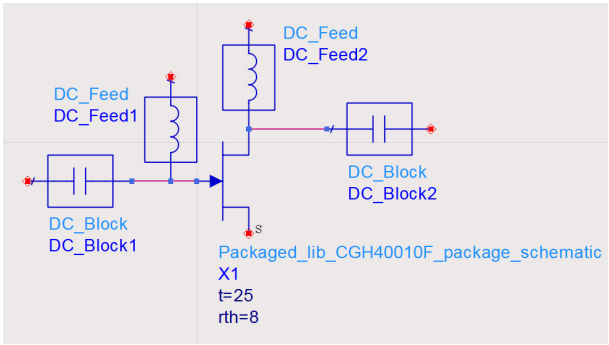

Fig. 4. Load and Source Ideal bias-tee

From the Class-notes the bias-tee can be designed in different ways to replace this ideal components with micro-strip stubs or transmission lines. We used the Line-cal tool in ADS to design the stub lengths and width. The following figure shows the Line-cal settings for MStub.

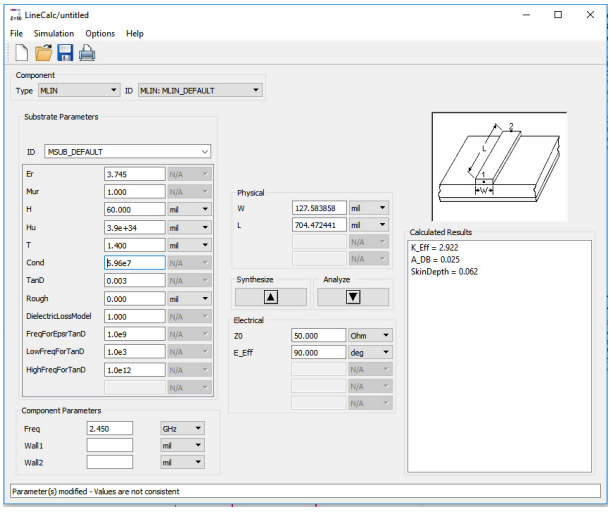

Fig. 5. Line-Cal settings in ADS

The Line-Cal tool gives us the length and width of the transmission lines for the specified impedance and Transmission lines length. From the lecture notes the bias-tee of the drain side is more crucial and many ways are there to design this. We used the radial-stub one to design the bias-tee in the drain side. The radial stub is used since it is simpler than lumped bias-tee (few components), more compact than linear stub and wide-band bandwidth than linear stub. Lumped bias-tee with high-Z quarter-wave transformer is wide band but complex to fabricate.

In this design the inductor is replaced with a high-Z transmission line, added more capacitors at drain side is conventional design, but caps need the short circuit which need the via.Instead of capacitors with SC if we design (90 deg) open line which acts as short circuit at inductor. This is connected using the magic-tee. Now open stub is replaced by radial stub. Here we tune the couple of parameters using **Tuning** option in ADS schematic to get the maximum stability. We added an extra transmission line from drain to this setup. The following figure shows the bias-tee at drain side.

In the same way the input bias-tee is designed. At gate

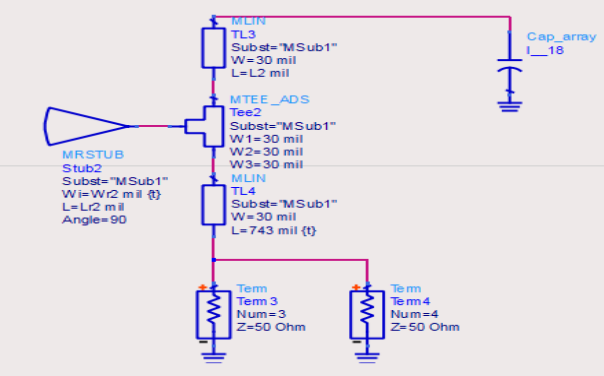

Fig. 6. Bias-tee at drain

bias-tee, we don't need this complex design, but we designed the same way at drain side. The following figure shows the bias-tee at gate side.

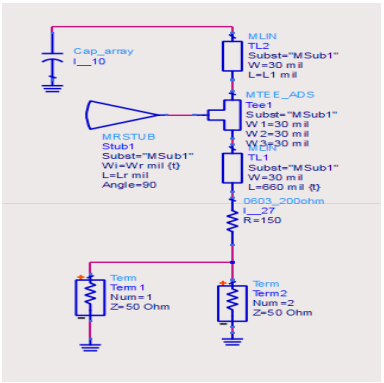

Fig. 7. Bias-tee at gate

The following figures shows the S-parameters of the bias-tee at output and input.

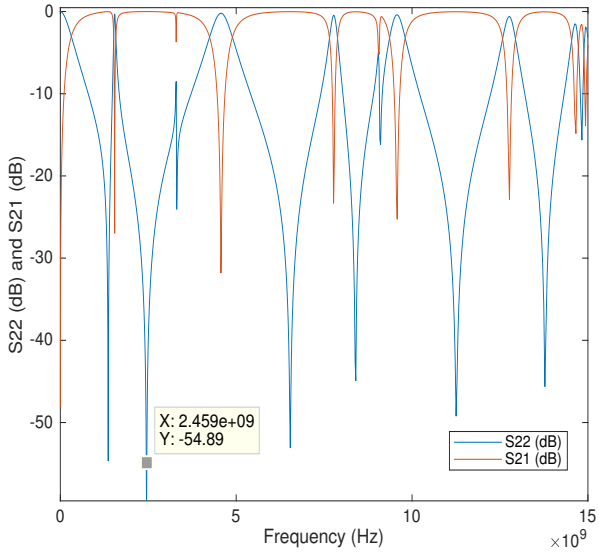

Fig. 8. S-parameters of the output Bias

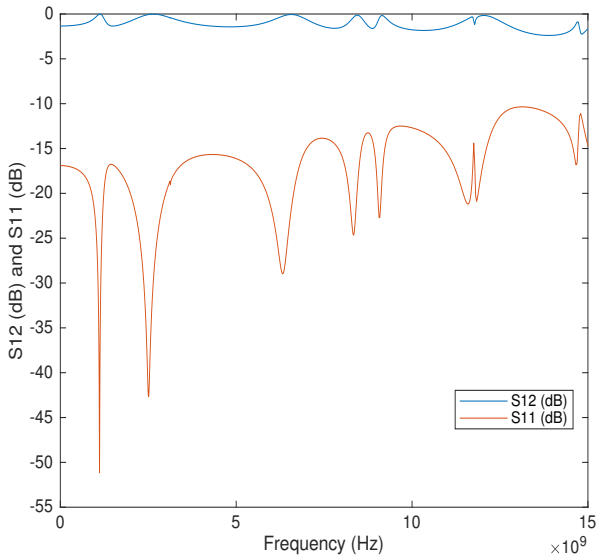

Fig. 9. S-parameters of the Input Bias

The length of radial stub at drain and gate are 460 mil and 365 mil respectively. The width of the radial stubs are 30 mil each. The length of the additional stubs at the drain and gate are 100 mil and 300 mil respectively.

C. Stability

The important parameter need to verify at each stage of PA design is Stability. We need to verify the transistor is un-conditionally stable always or not, if not un-conditional

stable need to find the regions where the transistor is stable. The measurement of stability is provided in ADS by different parameters like Stabfact, Mu parameters in ADS.

In the gate bias, we added an extra resistor in to reduce the gate current where we used 150 ohms here. We added resistor and capacitor in parallel in gate to make gate bias more stable. We used resistor of 15 ohms and capacitor of 9pf. We used the **Tuning** option in Schematic to vary the parameters of the resistor and capacitor. The following figure shows the schematic with bias-tee and stability. The

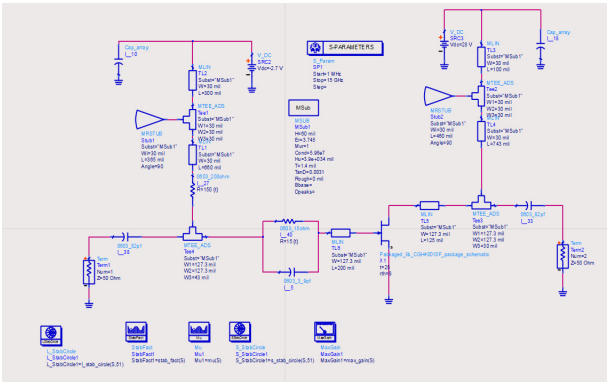

Fig. 10. Schematic with Bias-tee circuit

following figure shows the Maximum gain, stability factor and Mu factor for the schematic shown above.

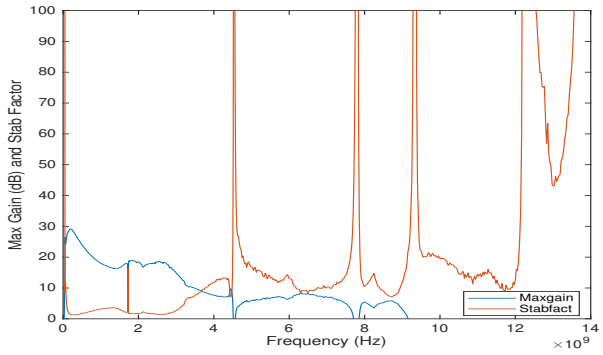

Fig. 11. Maximum gain and stability factor for the Bias-tee circuit

From the above figures, we can assure the transistor is stable over the desired band. The S-parameters are shown below for the transistor gives the forward gain over the frequency range.
So Clearly the Power amplifier is stable till this point. Now we weed to design the matched network for the transistor. This matched network is required for both source and load side and found by performing the following sections namely Load-pull and Source-pull parts.

D. Load-pull initial step

Understanding this step is critical in the design since we need to choose either our PA should be for maximum

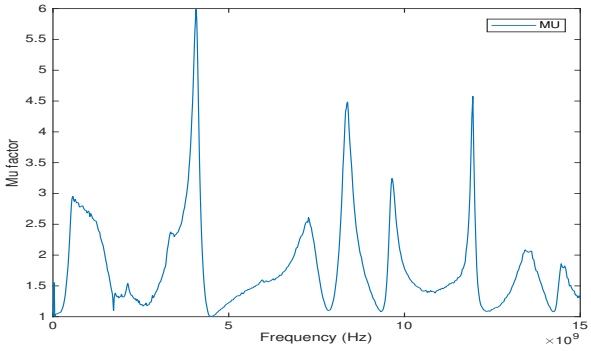

Fig. 12. Mu factor for the Bias-tee circuit

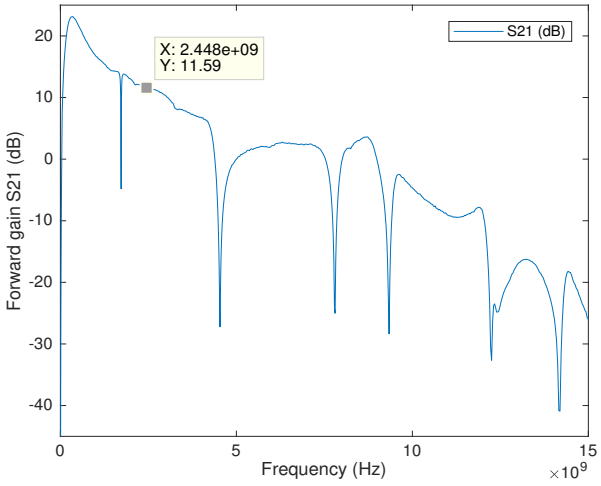

Fig. 13. S-parameters for the Bias-tee circuit

power or maximum efficiency. In this step, ADS varies the load impedances and finds the power delivered to the load and efficiency of the PA. In the ADS data set, we can see the contours of the power and efficiency by varying the load-impedance. At the end of this step, we can pick an impedance which gave either maxim power or maximum efficiency. Here we pick the point for maxim power delivered to the load. We used Pavg is 25dBm.

Setup: We gave the operating point DC power supply values which we got in the I-V characteristics section. We Connected the transistor with bias-tee which we designed in the last-step. We get the load-impedance for maximum power which is 18.68-j28.2. We used this load-impedance in the source-pull. The following figures shows the load-pull schematic and its results data-set.

E. Source-pull

From the previous step, we got the load-impedance which maximizes the output power. Now we used that load-impedance to compute the source impedance to get

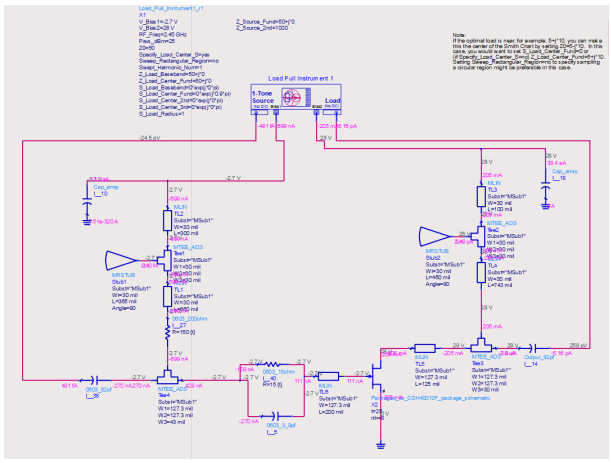

Fig. 14. Load-pull Schematic

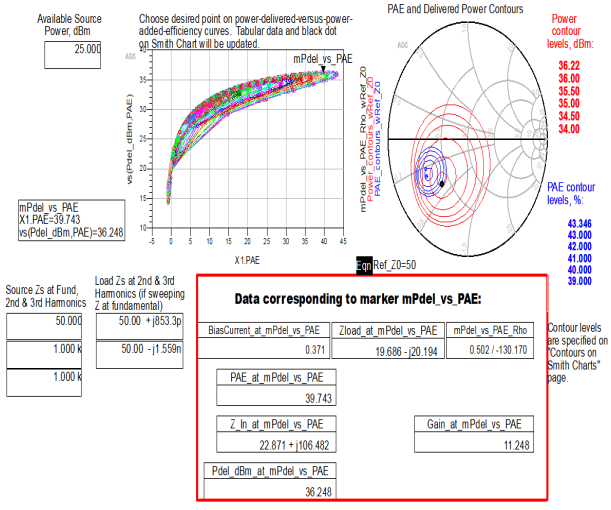

Fig. 15. Data set for Load-pull Schematic

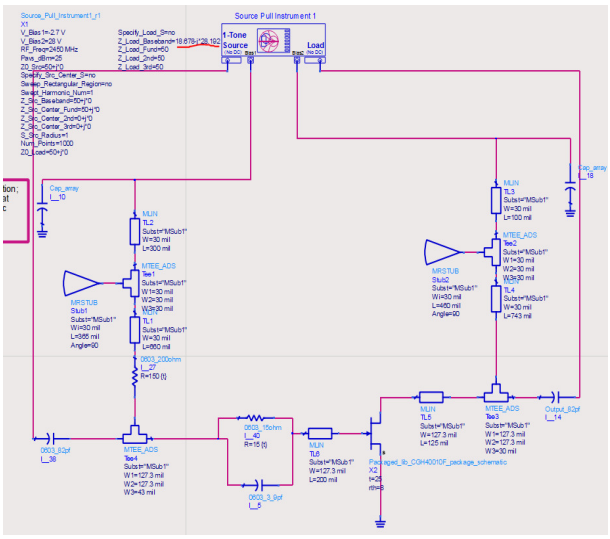

Fig. 16. Data set for Source-pull Schematic

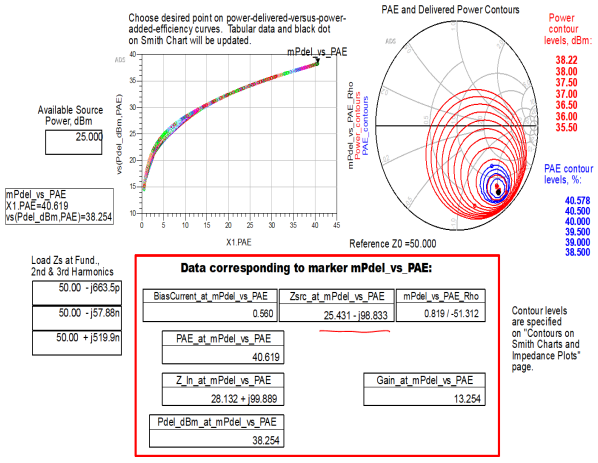

Fig. 17. Data set for Source-pull Schematic

maximum gain. We used ADS schematic for source-pull to find the source impedance for maxim gain. The source impedance we get in this step is 25.43-j*98.83. The following figures shows the load-pull schematic and its results data-set.

F. Load-pull Final step

In this step, we used the source-impedance from source-pull to find the load-impedance with source matched network. We did the same load-pull with only source impedance is set to 25.43-j*98.83 ohms. In this case we got the load impedance as 20.8-j*30.6 ohms.

G. Load-matched network

From the previous steps, we got the source impedance which gives maximum gain and load-impedance which gives the maximum power delivered to the load. Now we need to design design the matched network for the source and and load-impedance. The ADS software with smith chart utility has the the flexibility to design the matched network. The following figure shows the smith chart utility in ADS.

In this step, we will design load-impedance for maximum power delivered to load, so we don't use conjugate match here. load-impedance is 20.8-j*30.6 ohms. The following figure shows the load-matched network.

Using the Smith Chart Utility, we got the schematics with equivalent electrical lengths. By using the Line-cal tool in ADS Refer Figure 5: for settings in Line cal, we got the equivalent physical length of the transmission lines. We used open stubs which is easy to design, since these don't need to connect to via.

H. Source-matched network

As described in the previous section, using ADS smith chart utility we designed the source matched network. Source impedance is 25.43-j98.83 ohms. This impedance to

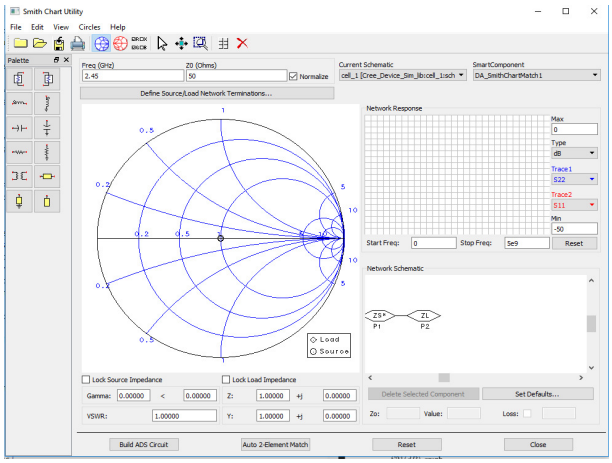

Fig. 18. ADS Smith Chart Utility

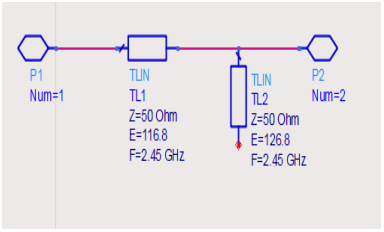

Fig. 19. Load-matching network with stub electrical length

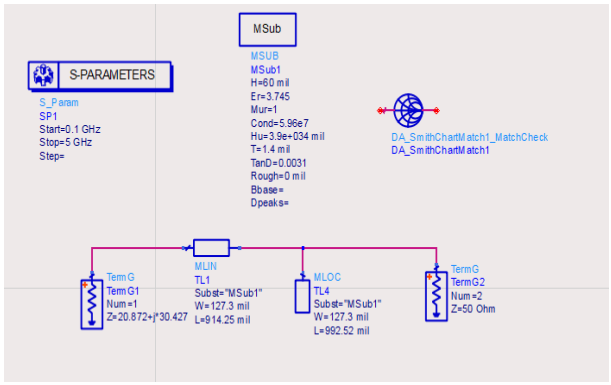

Fig. 20. Load-matching network with stub physical length

be matched to 50ohms line of source. Since we are using the conjugate match, we need to design the matched network for maximum gain, source impedance to be 25.43+j*98.83 ohms. The following figure shows the source matched network.

We use do the same step using smith chart and manual calculation of source and load-matching network. We did the S-parameters for the only matched networks and the following figure shows the matched network is perfectly matched at desired band.

I. Layout design

We integrated the matched network with the bias-tee schematic. In this step, we replace all the lumped elements

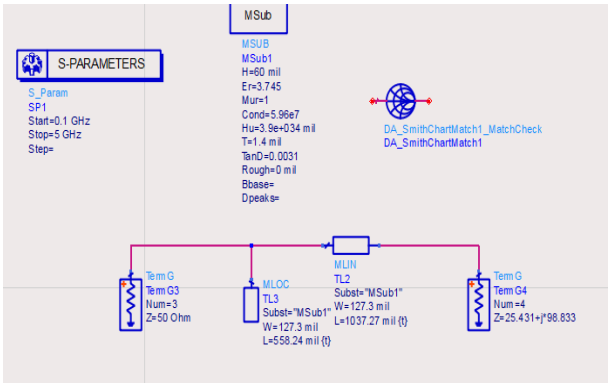

Fig. 21. Source matching network

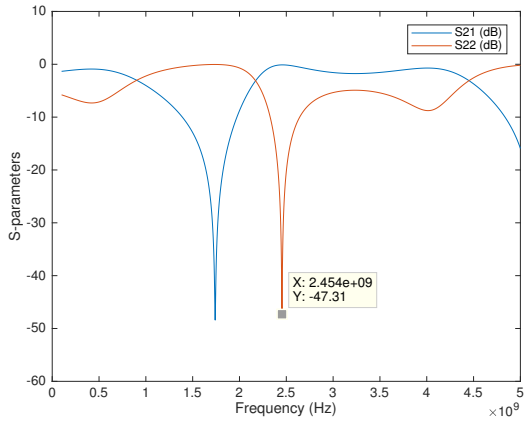

Fig. 22. S-parameters of the load matching network

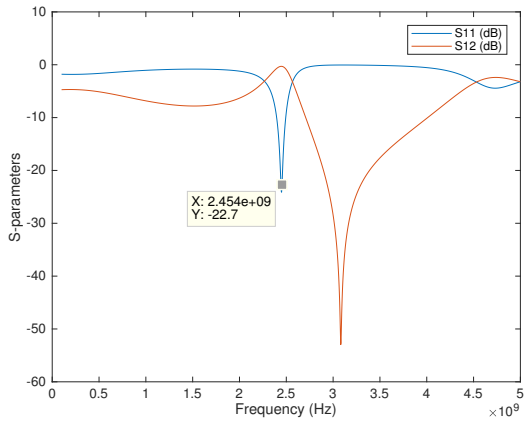

Fig. 23. S-parameters of the source matching network

with its equivalent circuits. For example, we replace the resistor with the following schematic. The same is done for all the lumped elements like resistors and capacitors. The resistor or capacitor equivalent circuits are designed using the real components S-parameters loaded to schematic. The resistors used in the design are 150 ohms and 15 ohms. The capacitors used in the design are 68 pF, 3.9 pF and 82 pF. The capacitors selected in the drain side are cable of

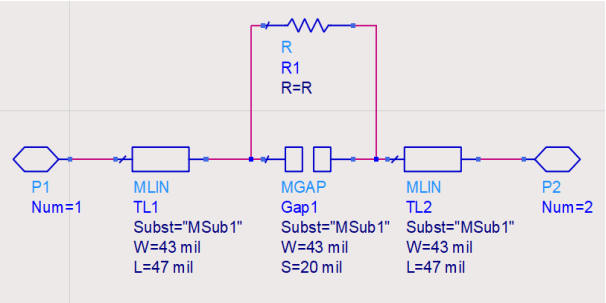

Fig. 24. Resistor equivalent circuit

handling high current than in the gate side. In the schematic, additional transmission line of 200 mils is added to make sure we have enough transmission line to place the ports of the transistors. The layout is generated using this schematic

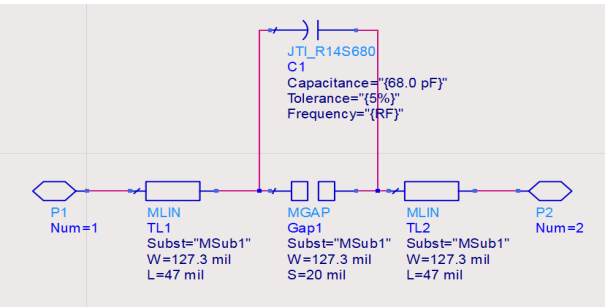

Fig. 25. Capacitor equivalent circuit

which is shown in the below figure. The S-parameters of

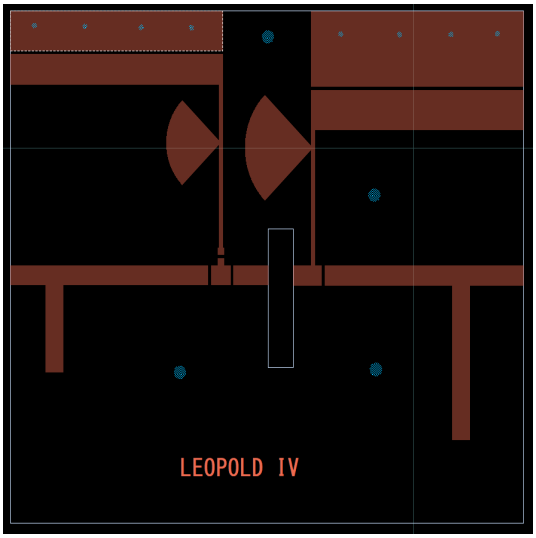

Fig. 26. Power Amplifier layout

the complete power-amplifier are simulated and given below. Clearly at 2.45GHz WIFI band we can see a gain of xx dB and return loss is better than yy dB. The following figure shows the S-parameters of the final power amplifier. (???)

The complete schematic is shown below figure 29.

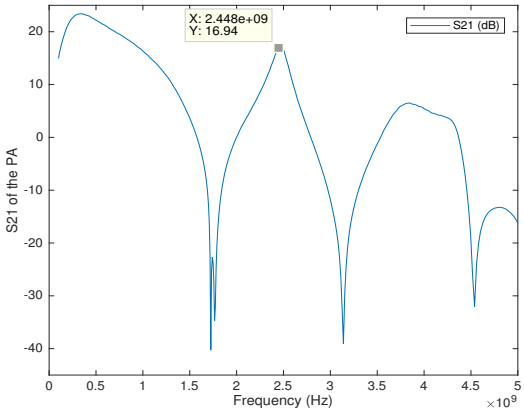

Fig. 27. S21 (dB) of the Power Amplifier

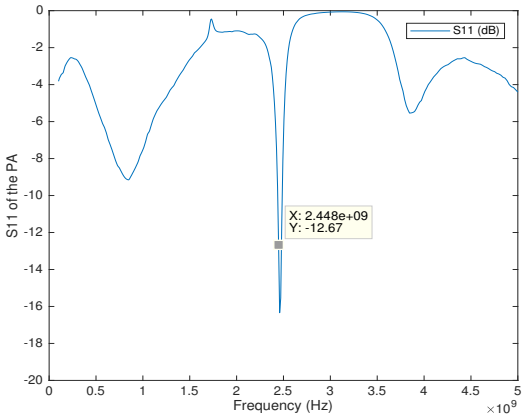

Fig. 28. S11 (dB) of the Power Amplifier

From the layout, it is clear that we extended the transmission lines for the power-supply lines. We added holes for screws of the heat-sink (the diameter of the hole is 2.2mm). We dig the holes for capacitors in the power-supply. The S21 is around 16.94 dB and S11 is -12.57 dB from simulation respectively.

III. Fabrication

The layout using Gerber file is fabricated using the LPKF machine. We used the Rogers 4350B substrate with effective resistance of 3.754, thickness is 60mil, 1oz copper (1.4 mil), loss tangent of 0.0031 and conductivity of 5.96e7. We selected the appropriate settings for the milling. The following figure shows after fabrication from LPKF machine.

A. Capacitors, Power-supply lines and Heat-sink

We soldered the capacitors on the fabricated design. We soldered the power-supply lines and attached the heat-sink. To attach the Heat-sink, we first, drilled the holes in

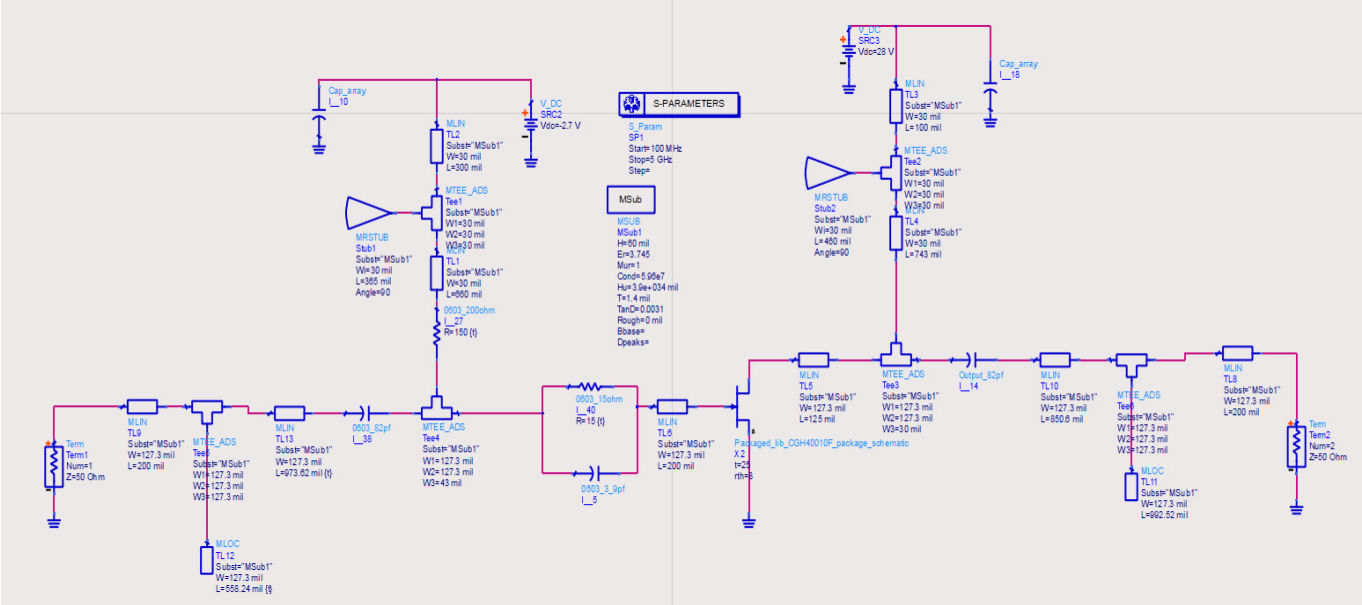

Fig. 29. Schematic of the Power-Amplifier

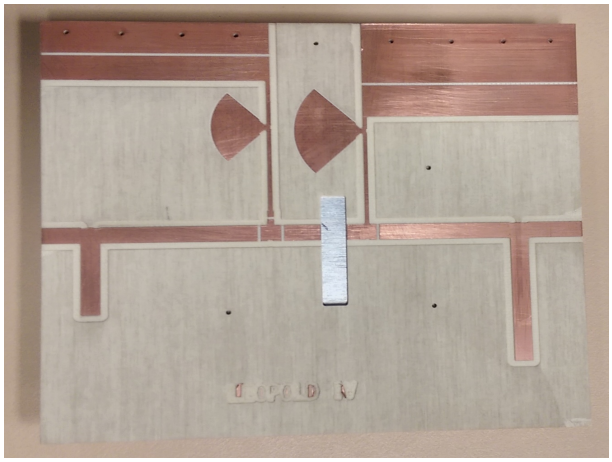

Fig. 30. Fabricated PA with LPKF machine

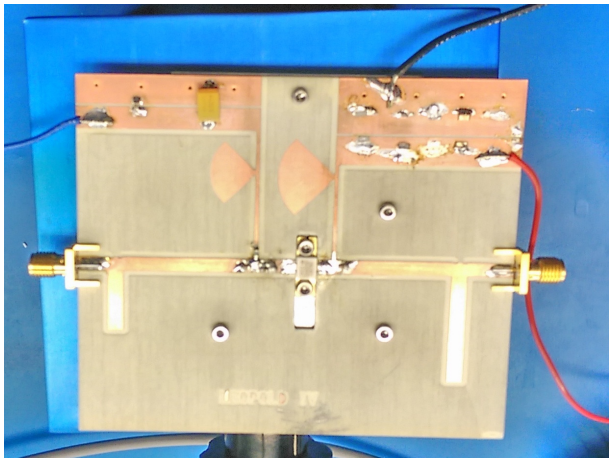

Fig. 31. PA after soldering the components

Aluminum heat sink and in fabricated substrate. We added some gel to stick the substrate and heat-sink. We added the 2-ports for input and output with 3.5mm SMA female connectors. The following figure shows after heat-sink and adding capacitors and power-supply cables.

IV. Small Signal Gain

It is crucial to measure the S-parameters of the PA, which provides significant in-sight about the forward gain, reverse gain and reflections at input and output ports.

A. Calibration

Before measuring the S-parameters, it is better to calibrate the cables and know the cables loss and prepare the table for each frequency what are the cable loss.

Before inserting the PA in the design, perform the port1 and port2 calibration step using 85052C calibration kit. This is done by connecting 3-different loads like Open, Short and matched load (50 Ohms). The Keysight vector network analyzer (PXA) has the option to verify the calibration of each port with these options.

For port1 do the following steps

1) Connect the Open circuit load to port-1, do the calibration in PXA box.
2) Connect the Short circuit load to port-1, do the calibration in PXA box.
3) Connect the matched load (50 Ohms) load to port-1, do the calibration in PXA box.

Repeat the same for port-2 as well.

B. Measurement setup

Now insert the PA in between port-1 and port-2 of the PXA. We provided the dc power supply of 28volts to drain and -2.5volts to gate so that the drain current reaches the 200 mAmp. The PA designed to operates at 2.45GHz, select the frequency range of 10MHz to 10GHz. With proper dc power supplies at this stage the $S21(dB)$ is **12.5 dB @ 2.45 GHz**.

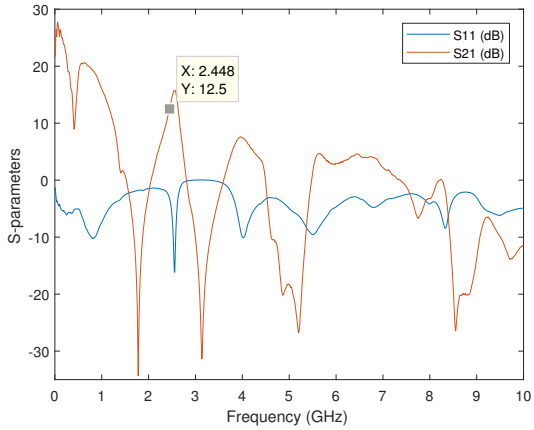

Fig. 32. S-parameters of the Power Amplifier (S11 and S21)

We can save this calibration table to a file in PXA. These are the S-parameters for backward gain and output return loss. From the reverse gain is really good one across

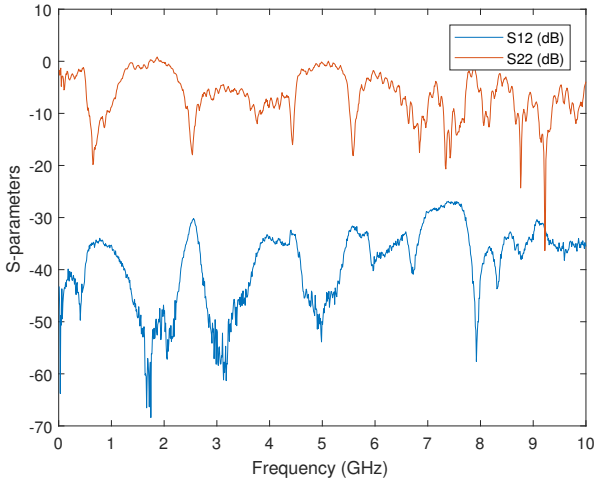

Fig. 33. S-parameters of the power amplifier (S12 and S22)

the desired band which is less than -30 dB. By looking the S-parameters it is clear the transistor is designed for optimum at 2.547 GHz which is 10MHz offset from our desired band.

V. Non-linear measurements

In this section we perform the non-linear measurements of the designed CGH40010F power amplifier using one-tone and two-tone tests. In this section, we discussed mainly about the Pin-Pout curve and third order inter-modulation values. The measurement setup is same as our-previous lab setup.

A. Requirements

In-order to use the PA in the full range, we need an auxiliary amplifier to boost the input signal before fed to PA input. We used a microwave buffer amplifier (part number: 87415A) which operates at frequencies range of 2-8 GHz.

B. Losses measured in each stage

We measured the total loss with and without power amplifier (PA) and auxiliary amplifier. We got the loss due to each component. The Coupler and Splitter gave the loss of 3.54 dB, the each cable has loss of 1.09 dB. With PA and aux amp loss is measured. Without PA, but with aux amp gain is 30.1 dB. The gain before the power amplifier is 30.1 dB and loss in output section after power amplifier is -31.7 dB.

C. Pin-Pout curve

We used a single tone (1-tone) input at various power levels and measured the Pout using the VSA. Initially we increased power in steps of 10 dBm, but later power is increased in steps of 1 dBm and 0.1 dBm. The following figure shows the Pin vs Pout graph.

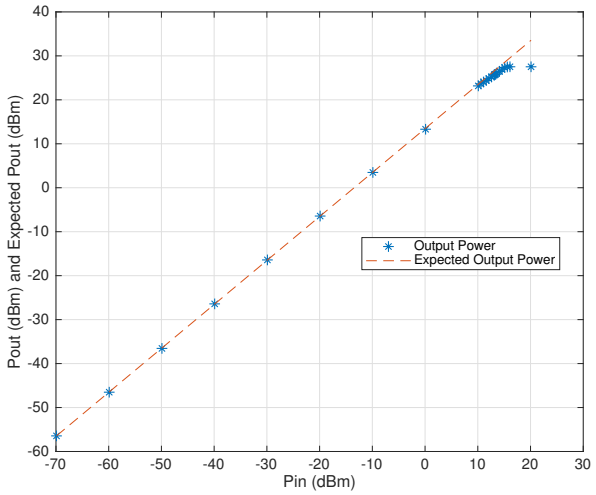

Fig. 34. Pin-Pout characteristics

Clearly from the curve at 13.4 dBm input power, there is 1-dB compression point which results Pout is 25.85 dBm. So the **gain of the Power amplifier is 12.45 dB**.

D. IM3 vs Frequency

We used a two tone (2-tone) inputs at same power levels and measured the Pout at inter-mods using the PXA. Initially we increased the input power in steps of 10 dBm, but later input power is increased in steps of 1 dBm. To find the IM3 point, the Pout at f1 and IM3 at 2f2-f1 power levels should meet. So we interpolated this data for more number of power levels.
The Third-order inter-modulations curve is derived based on few observations and interpolated throughout the Pin (dBm).

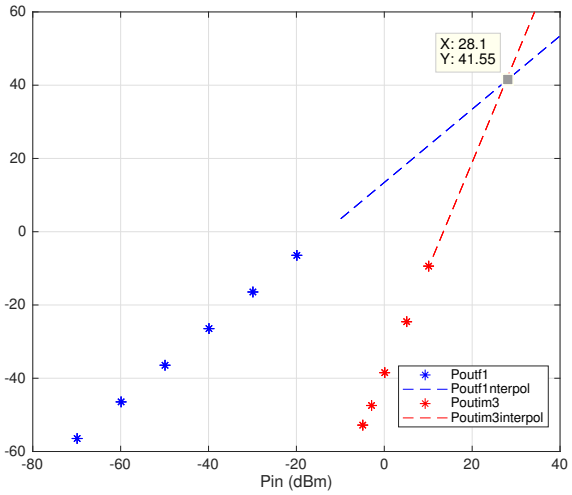

Fig. 35. Third-order inter-modulations vs Pin

Pin (dBm)	IM3 Power (dBm)
-4.9	-52.8
-2.9	-47.44
0.1	-38.47
5.1	-24.56
10.1	-9.4

TABLE I
IM3 POWER VS PIN

We observed the OP1dB and IM3 power are intersecting at input power of 28 dBm as IIP3 value and 40.55 dBm as OIP3 values.The following table shows the all the measurement values of the PA

IP1dB (dBm)	OP1dB (dBm)	IIP3 (dBm)	OIP3 (dBm)
13.4	25.85	28	40.55

TABLE II
MEASURED VALUES

From the IIP3 and OIP3 the gain is around 12.5dB is observed. The same value is observed from the IP1 and OP1 values too.

VI. CONCLUSIONS

We designed the power-amplifier from scratch and understood each component in the design effects the PA performance. We fabricated the PA using LPKF machine with Rogers 4350B substrate with Effective permittivity is 3.745. We attached the heat-sink to the fabricated design. We performed the power amplifier linear and non-linear measurements. We understood how to setup the dc-values for PA and how to measure the S-parameters using PXA. We verified the measured values are closely matching with the data sheet values. This gave us confidence to design and measure any active component in the coming labs. Coming to small signal analysis, we took the S21 (dB) values and mapped to the linear gain. For non-linear measurements, we used one-tone and two-tone tests, same as with our previous labs. The compression point and IM3 points are measured and verified using data sheets.

REFERENCES

[1] http://literature.cdn.keysight.com/litweb/pdf/5091-1358E.pdf.
[2] CGH40010F datasheet.pdf.