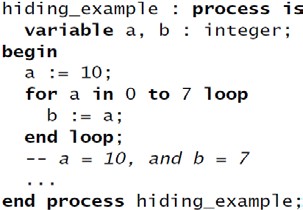
Rapid prototyping and ASIC design M.S.V.VARUN

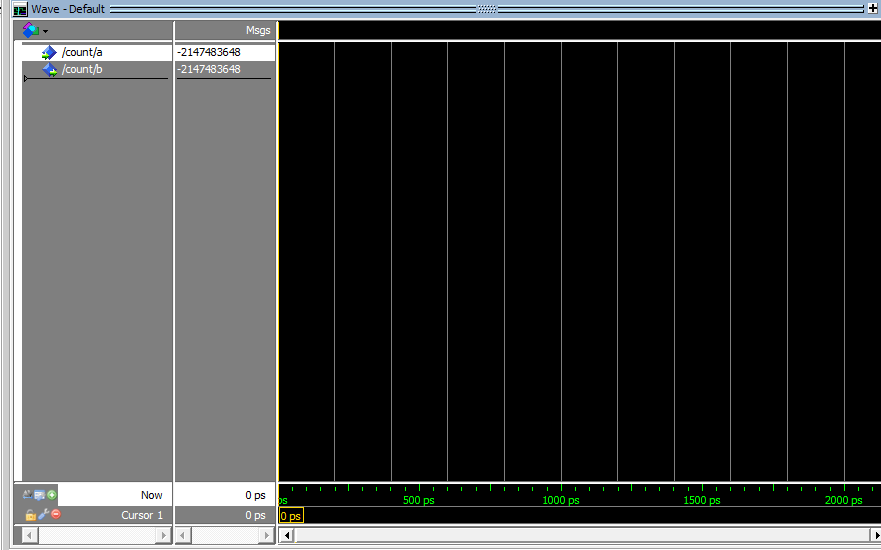
Assignment -3 K00379544

1. Please design a module and verify the usage of for loop in the Modelsim.

What is the values of a and b after the end loop? Please provide the vhdl code and screenshot of the simulation result.



Ans 1)



entity ct is

port ( a : in integer;

b : out integer );

end entity ct;

architecture fixed\_length\_series of ct is

begin

summation : process is

variable a : integer:=10;

variable b : integer;

begin

a:=10;

for a in 0 to 7 loop

b:=a;

wait;

end process summation;

end architecture fixed\_length\_series;

2. Please design a module and verify the usage of conditional variable assignment in the Modelsim.

Whether this conditional variable assignment can be used in the process? Please provide the vhdl code and screenshot of the simulation result.



Ans 2 )

--declaration

entity addsub is

port (a,b : in real;

mode : in string;

result : out real);

end entity addsub;

--architecture

architecture behav of addsub is

begin process is

begin

result:= a - b when mode = subtract else a + b;

end process ;

end architecture behav;

--test bench

entity test\_addsub is

end entity test\_addsub;

architecture behavioral of test\_addsub is

signal a,b,result: real;

signal mode: string;

begin

ass: entity work.addsub(behav)

port map (a,b,result,mode);

abc : process is

begin

a<='5';

b<='2';

mode<='subtract';

wait for 20 ns;

end process abc;

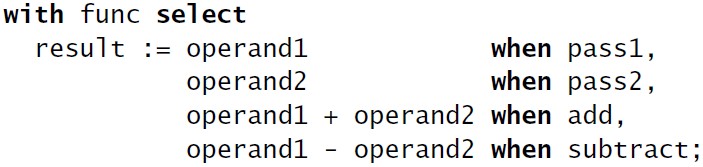
end architecture behavioral;

--

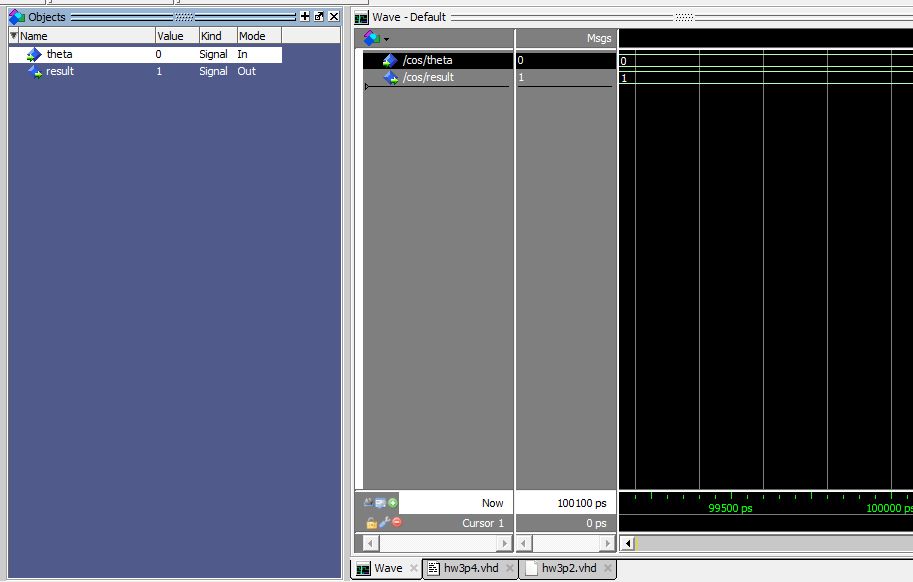
\*\* Error: E:/Study/TAMUK/TAMUK/2 SEM/ASIC/Modelsim/hw3p2.vhd(13): (vcom-1441) CONDITIONAL VARIABLE ASSIGNMENT is not defined for this version of the language.

3. Please design a module and verify the usage of selected variable assignment in the Modelsim.

Whether this selected variable assignment can be used in the process? Please provide the vhdl code and screenshot of the simulation result.



Ans 3)

library ieee;

use ieee.std\_ulogic\_1164.all;

entity hw3\_1 is

port(

pass1, pass2, add, subtract: in string;

result: out real);

end entity hw3\_1;

architecture behavioral of hw3\_1 is

begin

Proc\_hw3\_1: process is

variable operand1: real;

variable operand2: real;

begin

with func select

result:= operand1 when pass1,

operand2 when pass2,

operand1+operand2 when add,

operand1-operand2 when subtract;

end process Proc\_hw3\_1;

end architecture behavioral;

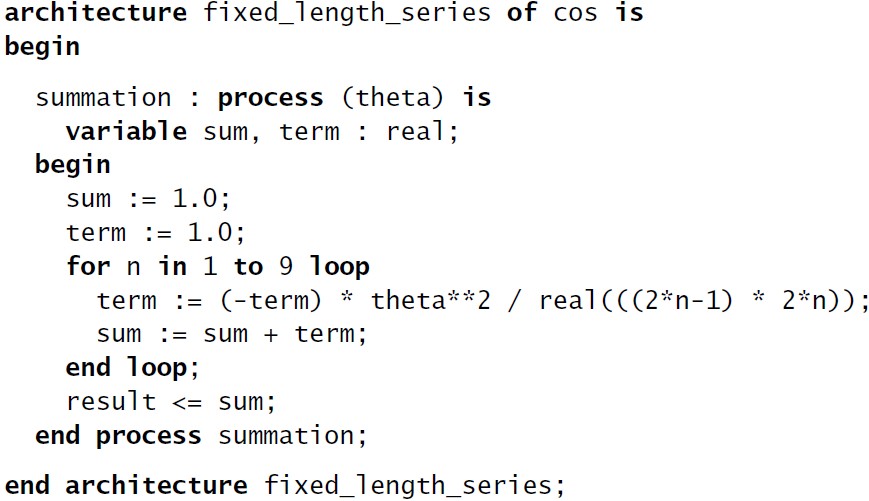
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\* Error: C:/altera/13.0sp1/HW3\_1VarAs.vhd(17): Signal "result" cannot be target of variable assignment statement.

`

4. Please design a module and verify the usage of for loop in the Modelsim.

Whether n should be defined as a variable or constant? Please provide the vhdl code and screenshot of the simulation result.



Ans 4)

entity cos is

port ( theta : in real; result : out real );

end entity cos;

architecture fixed\_length\_series of cos is

begin

summation : process (theta) is

variable sum, term, n : real;

begin

sum := 1.0;

term := 1.0;

for n in 1 to 9 loop

term := (-term) \* theta\*\*2 / real(((2\*n-1) \* 2\*n));

sum := sum + term;

end loop;

result <= sum;

end process summation;

end architecture fixed\_length\_series;