ECE2330 – Digital Logic Design

Arithmetic and Logic Unit (ALU)

Learning Objective

After this activity, you will be able to

- Design an Arithmetic and Logic Unit (ALU) using analytical digital design techniques, and
- Verify that the implementation you specify satisfies the requirements

Problem Statement

For this learning activity, you are **required** to design an ALU shown in Figure 1.

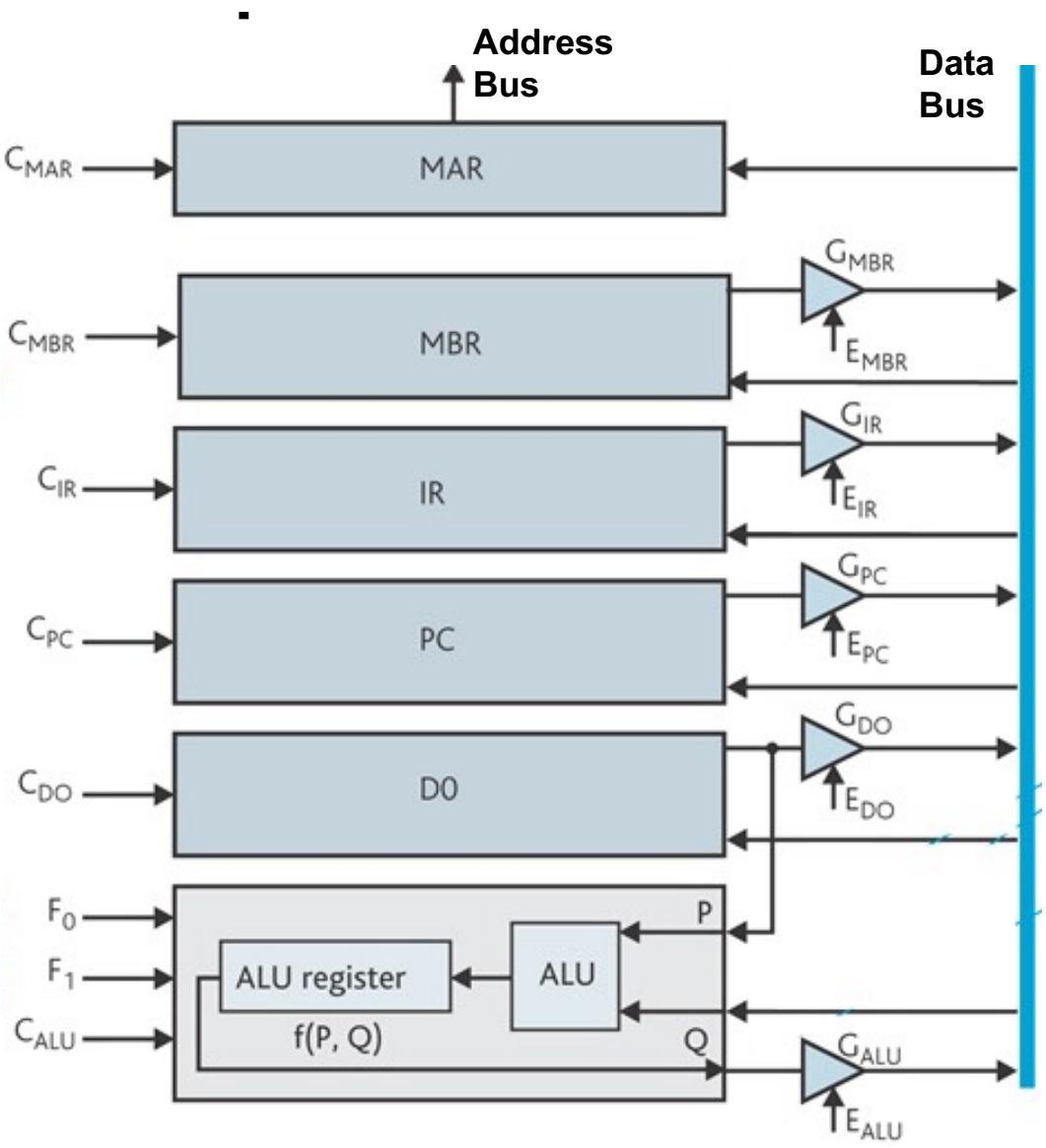

Figure 1: Simple CPU Datapath

The function of the ALU is to perform the 4 arithmetic operations defined by F1 and F0 as shown in Table 1. Shown in Figure 2 is a symbol for the ALU (that thus defines the VHDL entity for the design). As a design strategy, one approach is to design a gate-level 1-bit full adder circuit (shown in Figure 3), and then use that as a component to design an 8-bit adder/subtractor circuit (shown in Figure 4), which can then be used as the basis for designing the ALU.

Shown in Figure 5 are simulation results. Obviously, the simulation results are not exhaustive but simply demonstrate each of the functions defined in Table 1.

As the design engineer, you must decide what tests are sufficient to demonstrate that your design implementation satisfies the requirements.

Table 1: Arithmetic Functions Define by F0 and F1

F_1	F_0	Operation
0	0	Add P to Q, P + Q
0	1	Subtract Q from P, P – Q
1	0	Increment Q, Q + 1
1	1	Decrement Q, Q – 1

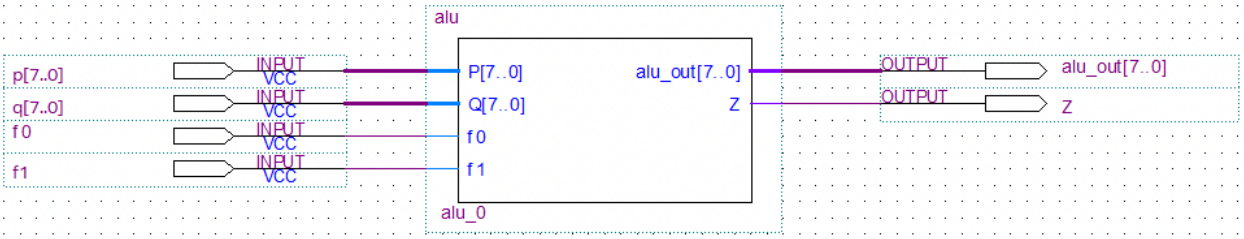

Figure 2: 8-bit ALU

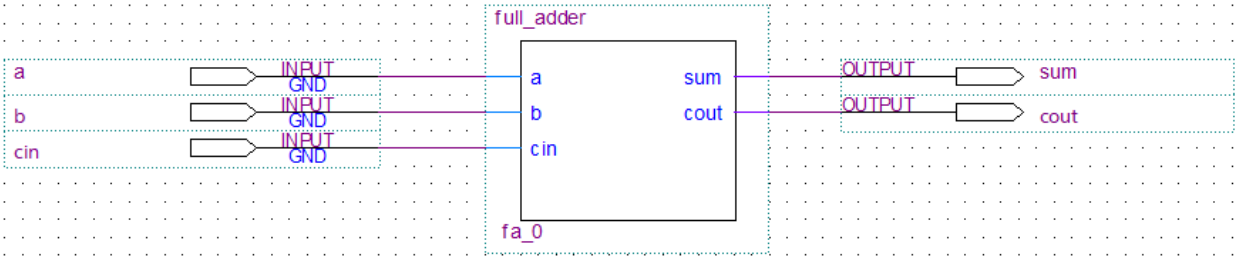

Figure 3: Gate-level, 1-bit full-adder

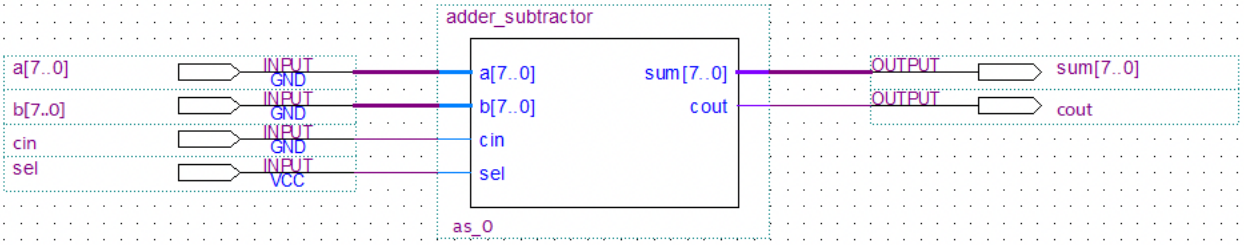

Figure 4: 8-bit Adder-Subtractor

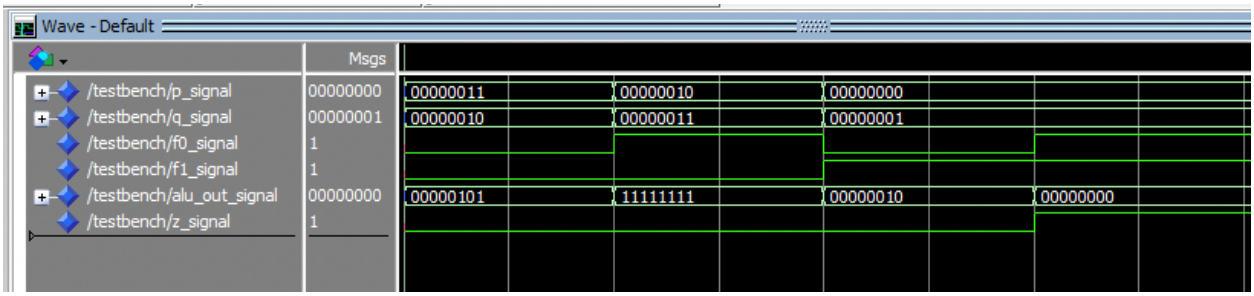

Figure 5: Simulation results

What To Submit

You will submit the VHDL file you create as part of this assignment, along with simulation results for verification (as a PDF file, annotated appropriately where necessary).

Grading Rubric

This assignment is worth a total of 10 points:

- VHDL file of ALU design
- VHDL file of testbench
- Numerical Verification