ECE2330 – Digital Logic Design

Datapath

Learning Objective

After this activity, you will be able to

- Design a datapath using analytical digital design techniques, and
- Verify that the implementation you specify satisfies the requirements

Problem Statement

For this learning activity, you are **required** to design a datapath shown in Figure 1, which will effectively complete your simple Central Processing Unit (CPU) design. A schematic for it is shown in Figure 2

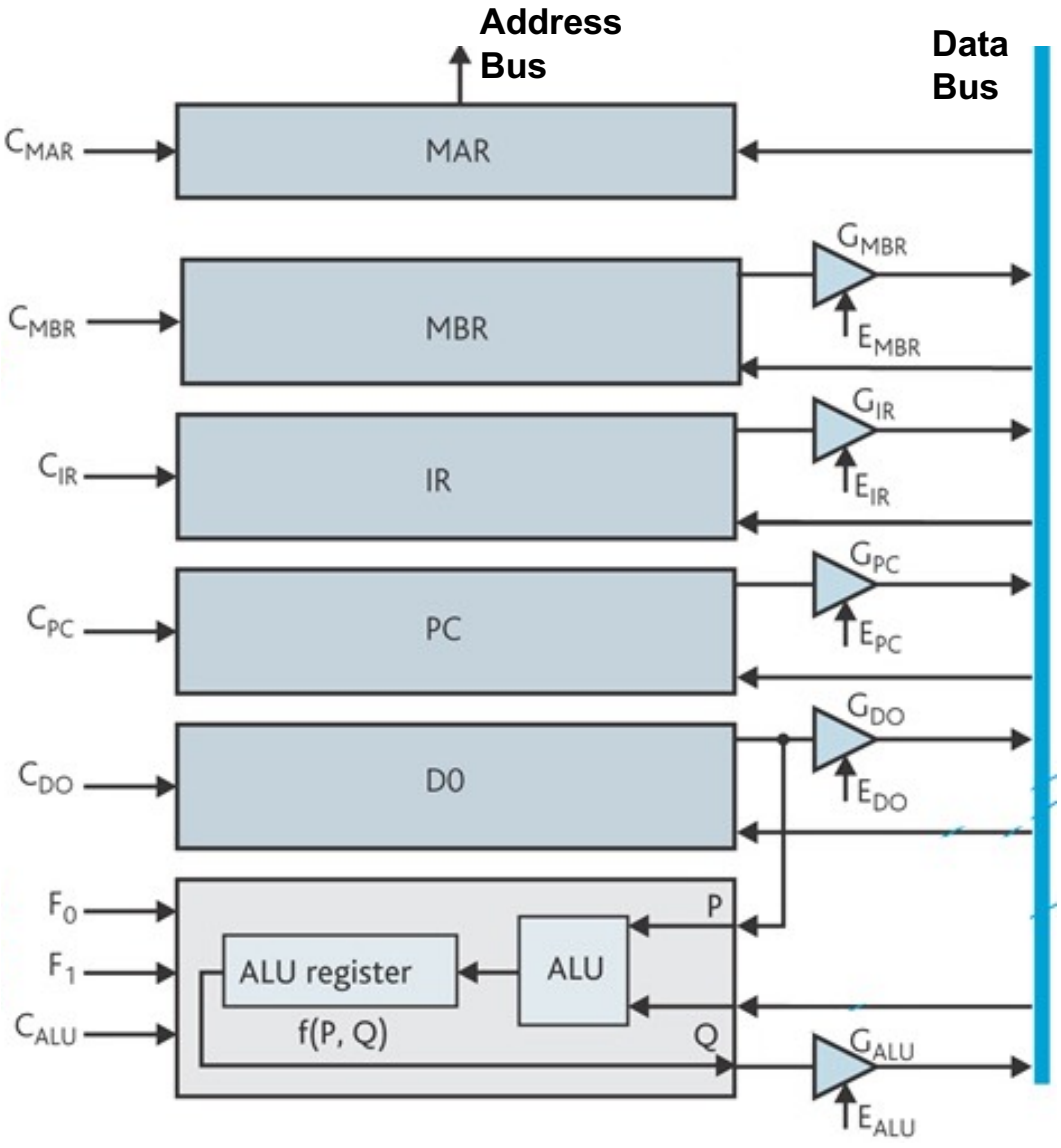

Figure 1: Simple CPU Datapath

The function of the datapath is store all of the information that is used to define the state of the CPU at any given time. This information is stored in the Memory Address Register (MAR), the Memory Buffer Register (MBR), the Instruction Register (IR), the Program Counter (PC), and Data register 0 (D0). In addition, the datapath contains an Arithmetic and Logic Unit (ALU) that is used perform the 4 arithmetic operations shown in Table 1. Finally, note that there is an additional ALU register used to store the result of the arithmetic operation defined by F1 and F0.

Table 1: Arithmetic Functions Define by F0 and F1

F_1	F_0	Operation
0	0	Add P to Q, P + Q
0	1	Subtract Q from P, P – Q
1	0	Increment Q, Q + 1
1	1	Decrement Q, Q – 1

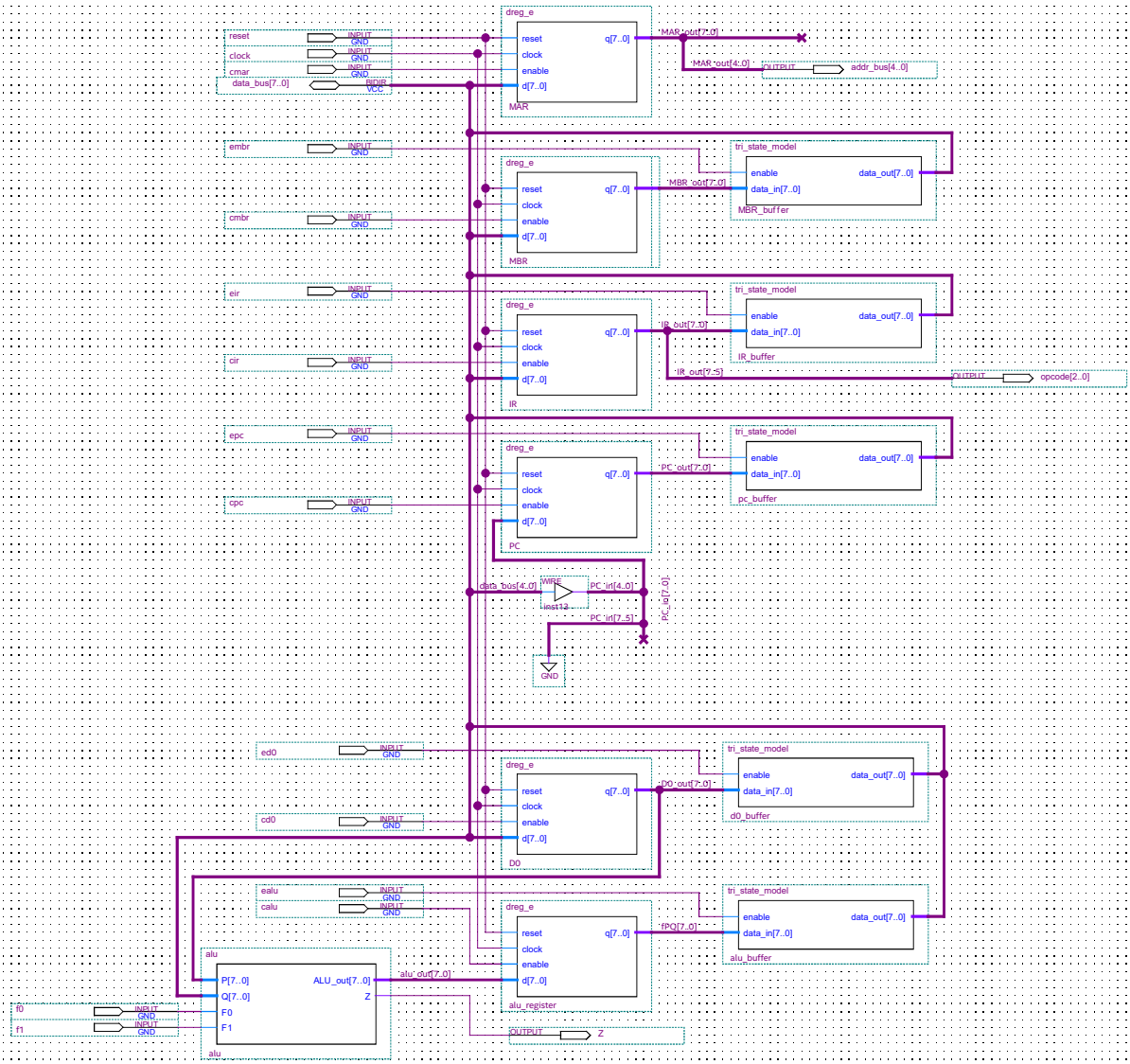

Figure 2: Datapath implementation

Simulation results for testing the datapath are shown in Figure 3. Here, the basis test strategy is to load the various registers with values, and the successively drive the data bus with the values stored in the registers. Again, while this is not exhaustive testing, so you as the design engineer will need to decide if this is sufficient to demonstrate that your implementation satisfies the requirements.

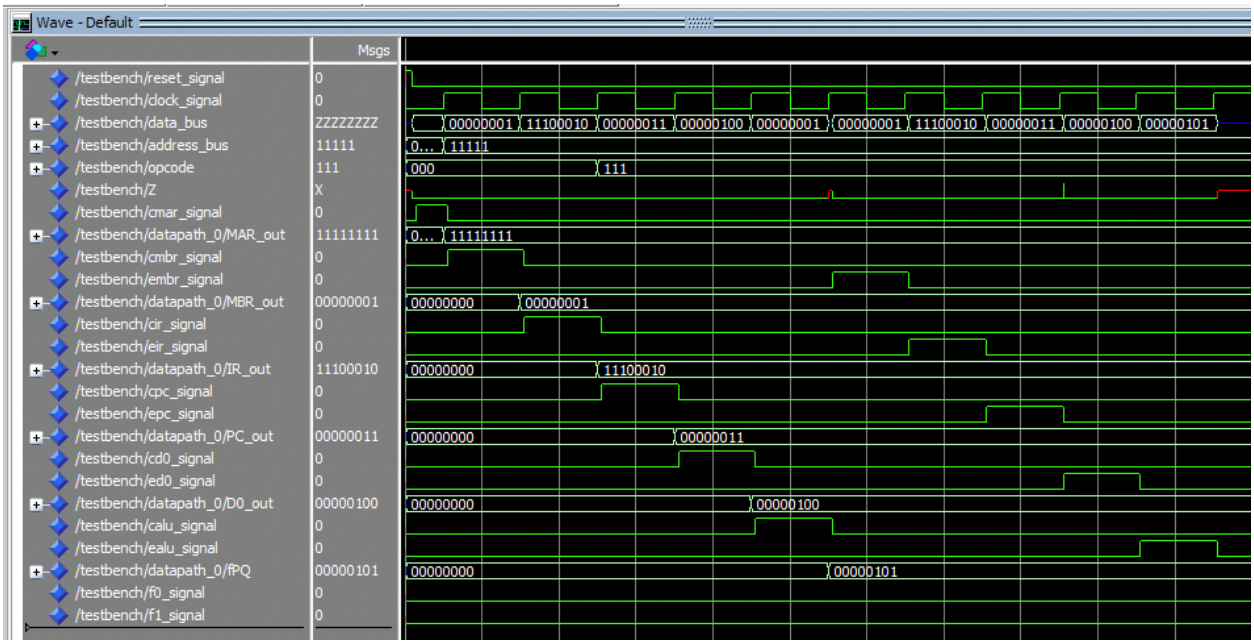

Figure 3: Simulation results

What To Submit

You will submit the VHDL file you create as part of this assignment, along with simulation results for verification (as a PDF file, annotated appropriately where necessary).

Grading Rubric

This assignment is worth a total of 10 points:

- VHDL file of datapath design
- VHDL file of testbench
- Numerical Verification