2023/24 NTU-TUM MSC Integrated Circuit Design

NM6007

Analog IC Laboratory Course

Individual Assignment
Class-AB Audio Amplifier with Translinear Loop

8 Jan – 12 Jan
15 Jan - 19 Jan

9:30 am – 4:30 pm

IC Design III

NM6007 Assignment: Class-AB Audio Amplifier

1. Individual Assignment

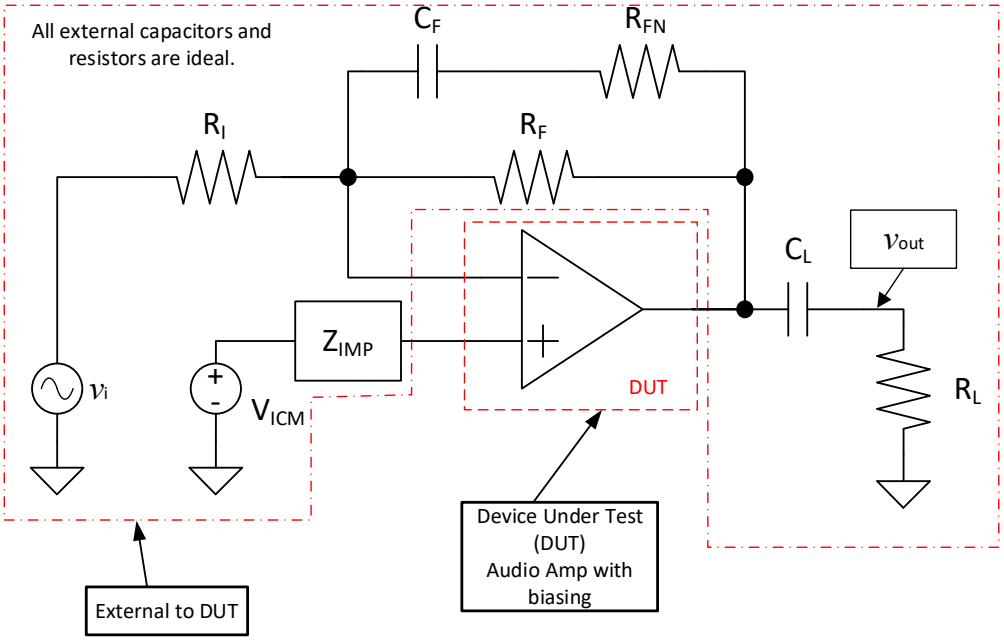


Figure 1: System Architecture of the Class-AB Audio Amplifier

The body terminal of all the NMOS and PMOS transistors in the following 2 figures(Figure 2 & 3) are to be connected to ground and V_{DD} respectively.

Also in Figure 2 & 3. all resistors are high-valued polysilicon with temperature coefficients, and capacitors are mim caps.

All other components outside the DUT(device under test) are ideal components.

The DUT is the circuits of Figure 2 &3.

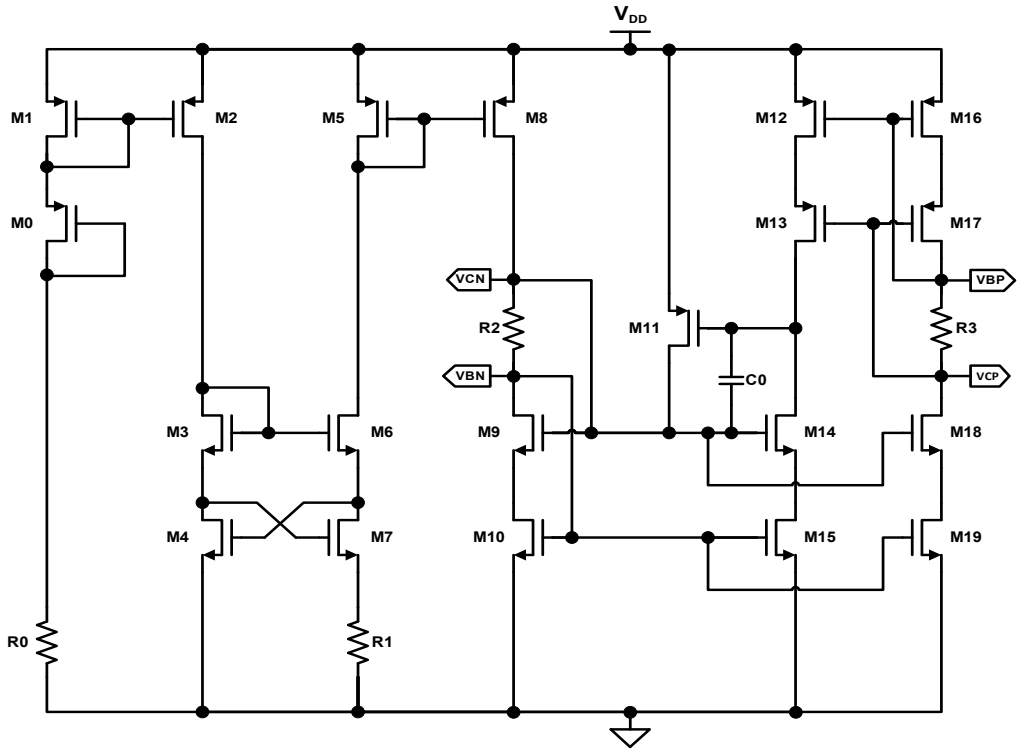


Figure 2: Constant-gm Biasing Circuit with start-up circuitry

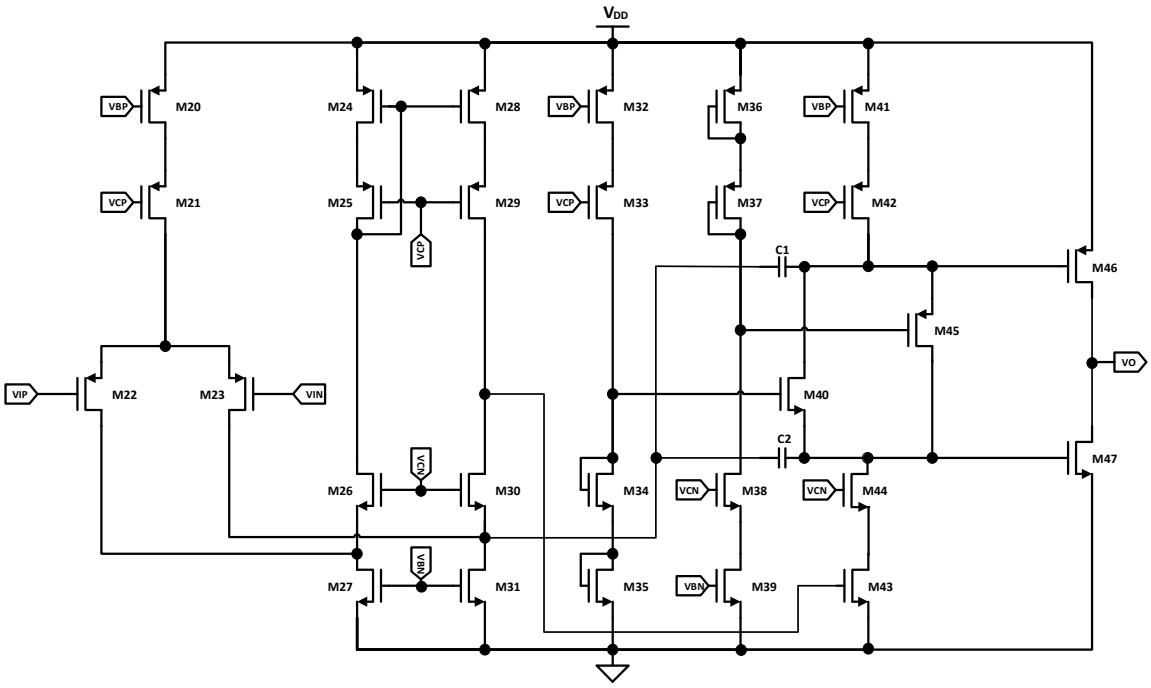


Figure 3: Class-AB Audio Amplifier with Translinear Loop Control

2. Design Requirements

Design the Class-AB Audio Amplifier and its biasing circuitry (shown in Figure *1* to Figure 3) using CSM 0.18µm CMOS process. You must go through the design cycle (simulation, layout, parasitic extraction, and post-layout simulation).

The **conditions** listed below **MUST** be used when characterizing the performance of the Class-AB Audio Amplifier:

- Operating Temperature: Typical temperature = **60°C**, Range of **-40°C to 100°C**
- Supply voltages: Typical V_{DD} = **1.6V**, V_{SS} = 0V, Range of V_{DD} = **1.5V to 1.8V**
- Determine V_{ICM} such that the output of the amplifier is ½V_{DD}
- All components in Figure 2 & 3 are implemented on the chip except the rest of the components R_I, R_F, C_F, R_{FN}, Z_{IMP}, C_L and R_L = 16Ω, which are external. Determine and justify a suitable C_L for audio application.

The Closed-Loop Gain, Common-mode Gain and Total Harmonic Distortion requirements of the final circuit must be satisfied for all the fast-slow/slow-fast/fast-fast/slow-slow transistor models in process corner simulation, temperature variation and voltage supply variation.

Satisfy all the specifications for TYPICAL mode FIRST before attempting the four corners, temperature variation and voltage supply variation.

Hint 1: You may want to begin your initial design iteration with a suitable overdrive voltage ΔV by examining the output voltage swing requirement

Hint 2: Always keep the allocated area at the back of your mind, while the design is usually part of a more extensive system, and the area might need to be more negotiable.

3. Specification Table (@ VDD = 1.6V and @ 60°C)

Specification	Units		Pre-Simulation	Post-Simulation
Closed Loop Gain (×4)	**dB**	**-**	**12 (± 5%)**	**12 (± 5%)**
Closed Loop **Unity** Gain Bandwidth	kHz	≥	300	300
Common-mode Gain	**dB**	**≤**	**-75**	**-73**
Feedback Loop Gain	dB	≥	80	75
Feedback Loop Phase Margin	degree	≥	60	60
Power Supply Rejection Ratio	dB	≤	-70	-65
Quiescent Current Consumption	mA	≤	2	2
Output Swing **(@V_{DD} = 1.5V)**	V	-	$0.1 \le V_o \le 1.4$	$0.1 \le V_o \le 1.4$
Total Harmonic Distortion	**dB**	**≤**	**-80**	**-77**
Settling Time	μs	≤	0.45	0.50
Slew Rate	V/μS	≥	4	4
Chip Area	μm^2	≤	-	250 x 200

4. Simulation Procedure

I apologized for not being able to provide any figures to guide you along the way, as this assignment will be strictly graded. **BUT** do not be worried. I will instead explain in greater detail to guide you through this assignment. You are highly encouraged to raise questions and actively discuss them with me. Wonderful. Let's begin our journey **NOW**.

Spend at least 8 hours to FULLY understand the basic working principle of the amplifier and the biasing circuit (Fig. 1 to 3)

You must characterize the device before proceeding with any calculation. If you have any doubts regarding the circuits, please kindly approach the teaching assistants or me. They are very nice and patient. I am very sure that they will be delighted to assist you. Trust me, and you need to have a solid understanding of the working principle of both circuits before embarking on the journey ahead. You are advised to proceed only if you fully understand the circuit operation in Figures 1 to 3.

1. In Cadence, under Library Manager, set up a new library called **NM6007_Assignment**. In this new library, set up a new cell view and named it **NM6007_Circuit**.

2. In the **schematic window**, set up and wired the circuit connections in Fig. 2 to 3, respectively. **The body terminal of all the NMOS and PMOS transistors in Figure 2 & 3 are to be connected to ground and V_{DD} respectively.** It is easier said than done. This alone will take at least **four hours** for you to complete. I advise you to wire the circuit carefully, as faulty wiring would lead to inaccurate simulation results later.

3. Now, go to Tools and Analog Environment. Click on Setup, Temperature and change to **60°C**. Press OK. Click on Analyses and press Choose. Setup as dc and click on Save DC Operating point. Remember to include the model library files for all devices. Press Netlist & Run button.

4. This will run a DC simulation. WHY are we doing this? If you cannot understand, please do not feel sad about it. We are always learning, and I'm sure you will learn a lot throughout the entire course of this assignment.

5. Go to **Results**, **Annotate,** and click **DC Operating Points**. In your schematic window, zoom in and a set of values will appear beside each transistor. Make sure that ***vds is greater than vdsat*** as this will ensure that the transistor will be operating in the saturation region.

6. For some of the transistors in **Fig. 3**, the (W/L) ratio is relatively large. Please feel **FREE** to increase the (W/L) ratio of **ANY** transistor in Fig. 3; try to put them in terms of the multiplier, **m**.

7. Note: All transistors should have their bodies tied to the ground for NMOS and V_{DD} for PMOS, except those explicitly marked. Also, **the minimum length of the transistor is L = 0.18um** for this 0.18um process. **However, use L of 4 to 5 times larger than 0.18um else the output impedance of the transistor would not be high enough. Of course, with the exceptions of the input transistors(M22 and M23) and output transistors(M46 and M47) and perhaps also for M35 and M36.**

This section will take about **three to four days** to complete. The biasing condition is critical so expect numerous design iterations. If you are complacent, you will find the subsequent design extremely challenging.

For the next section, whenever you are done with your design, you may contact the TA for verification. You will be awarded **1 Personal Signature for every specification satisfied in the specification table (page 18)**.

The **Personal Signature** is to be collated in the **Score Sheet** (last page of this document). The **Personal Signature** is given based on the performance of the Class-AB Audio Amplifier from the post-simulation result**.** As the specification are interdependent, the TA will verify the performance of your design in a single sitting. You **cannot** have your Closed-loop Gain verified and then move on to satisfy the other specification, etc.

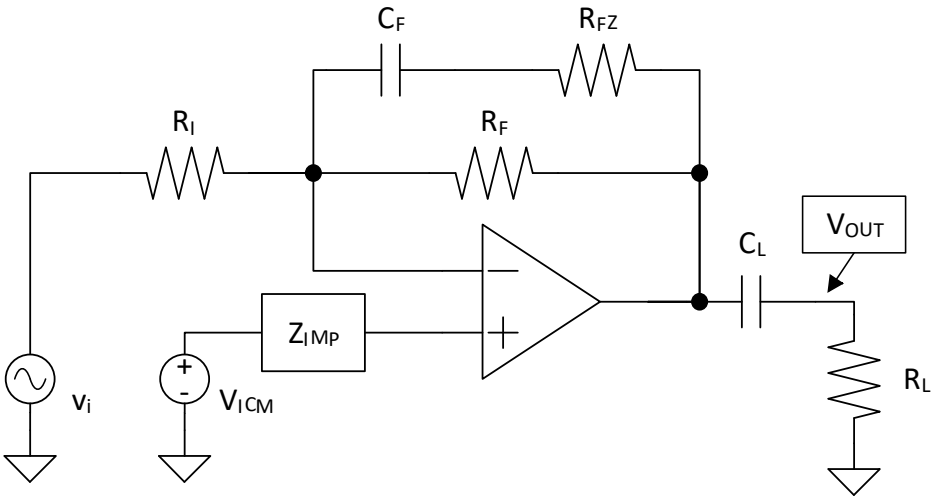
NM6007 Assignment: Class-AB Audio Amplifier

You will have to attach this Score Sheet, as an appendix to your design/lab report, upon completion of the entire assignment. Please refer to NM6007 – Course Overview for more details regarding the design/lab report submission.

4.1 Closed Loop Gain & Unity Gain Bandwidth

Assume that the common-mode DC level of the input signal is 0V or grounded. Obtain the closed-loop gain $\mathbf{A_{VCL} = v_{OUT}/v_i = 4}$ (shown below). The value of $\mathbf{v_i}$ should be set to 1V AC. **Determine $\mathbf{V_{ICM}}$ and $\mathbf{Z_{IMP}}$** such that the output of the amplifier is at $\frac{1}{2}V_{DD}$.

Is there a difference if the input is applied at the positive input terminal (without Z_{IMP})?



Hint 1: In the **Analog Environment**, go to **Analyses** and **Choose**. Set up an AC simulation by pressing **ac**, **frequency** under sweep variable. **Start: 1** and **Stop**: **1M**. Press **OK**.

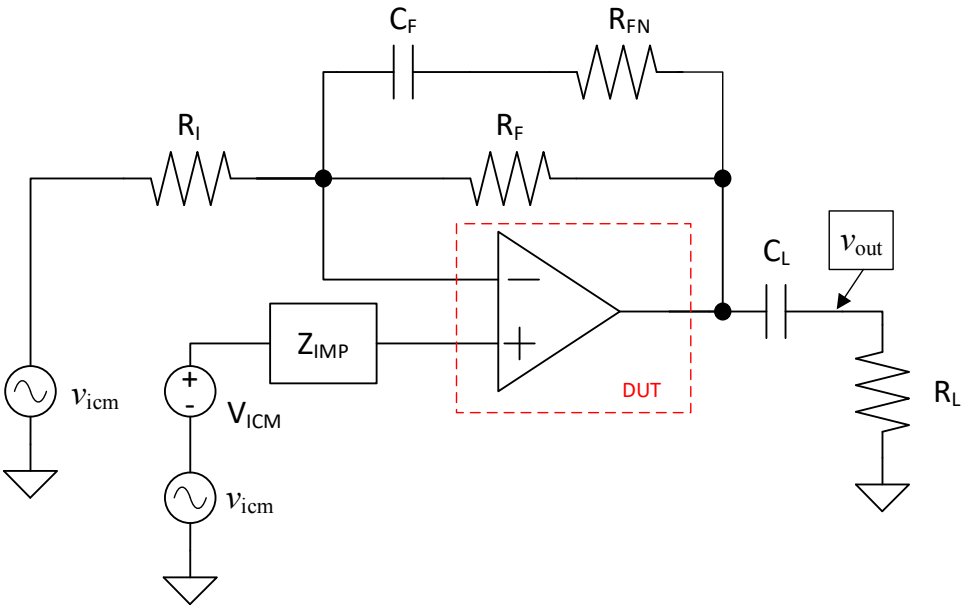
Hint 2: Brainstorm how to measure the AC gain for your circuit in Cadence simulation. Please ask your teaching assistant for advice if you need any help here. However, I would prefer you spend some time thinking about measuring the AC gain.

Hint 3: You would need to adjust the (W/L) of some transistors and, more importantly, the values of the resistor: R_F and R_I. There is a trade-off to be made with the other specification.

4.2 Common Mode Gain

Apply the common-mode signal v_{icm} by setting it to 1V AC and minimize the common-mode gain $\mathbf{A_{CM} = v_{OUT}/v_{icm}}$ (shown below). **Determine $\mathbf{V_{ICM}}$ and $\mathbf{Z_{IMP}}$** such that the output of the amplifier is at $\frac{1}{2}V_{DD}$.

What are the differences with and without Z_{IMP} for the common-mode ac signal?



Hint 1: In the **Analog Environment**, go to **Analyses** and **Choose**. Setup an AC simulation by pressing **ac**, **frequency** under the sweep variable. **Start: 1** and **Stop**: **1M**. Press **OK**.

Hint 2: The steps to measure DC gain for your circuit is like AC gain in Cadence simulation.

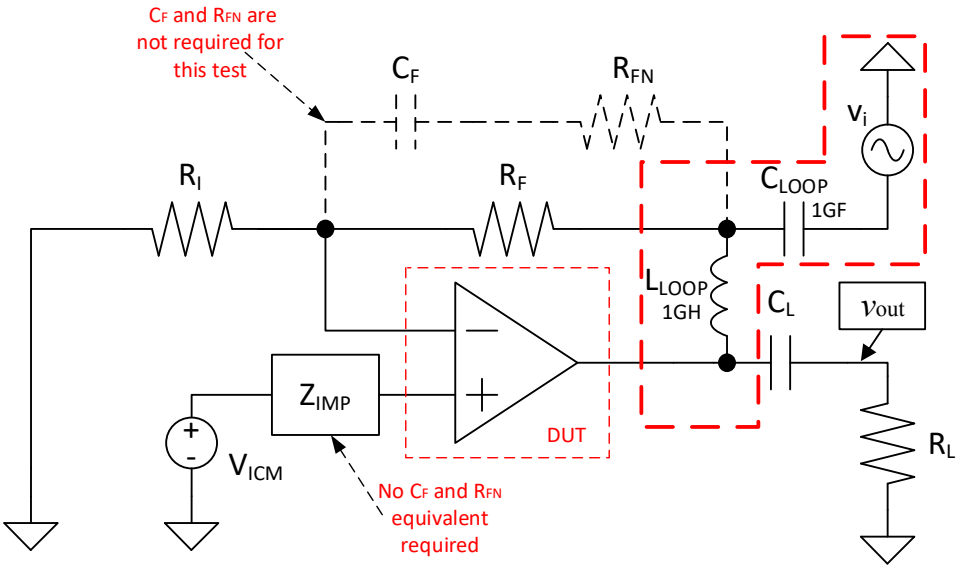
Trust me yet again. This is the most straightforward specification to meet. The difficult ones come later. Do **ALWAYS** make sure that all the transistors are biased in the **SATURATION** region after adjusting its (W/L) ratio.

4.3 CMFB Loop Gain, Loop Unity Gain Bandwidth & Loop Phase Margin

Setup the test by inserting the ideal components (enclosed in the dotted box) shown below into your design.

Can you explain why the test is conducted this way and its limitation?

Certain assumptions are made for this setup. Can you identify what additional steps should be taken to improve the accuracy of the simulation results?



Hint 1: The ideal components **ind** and **cap** can be found in the **analogLib**

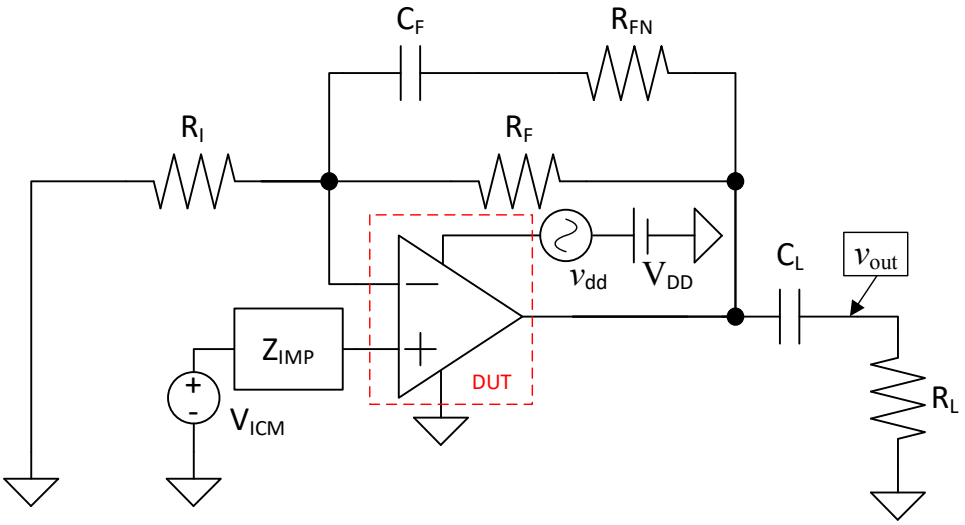
Hint 2: A more straightforward way is by using **stb** analysis. You should figure out how this is done, as it will save you much effort!

Hint 3: The capacitor C_F and R_{FN} are used limit the audio signal bandwidth!

4.4 Power Supply Rejection Ratio

Apply a small signal on the supply by introducing v_{dd} of 1V AC superimposed on the V_{DD}. Minimize the supply rejection **PSRR = v_{OUT}/v_{dd}** (shown below).

Is there a difference between applying a superimposed signal at V_{DD} and at ground?



If you can satisfy all the specifications till now, you are **SAFE**. The rest of the specifications should be easily satisfied as you are very "experienced" now.

Do **ALWAYS** ensure that all transistors are biased in the **SATURATION** region.

4.5 Current Consumption

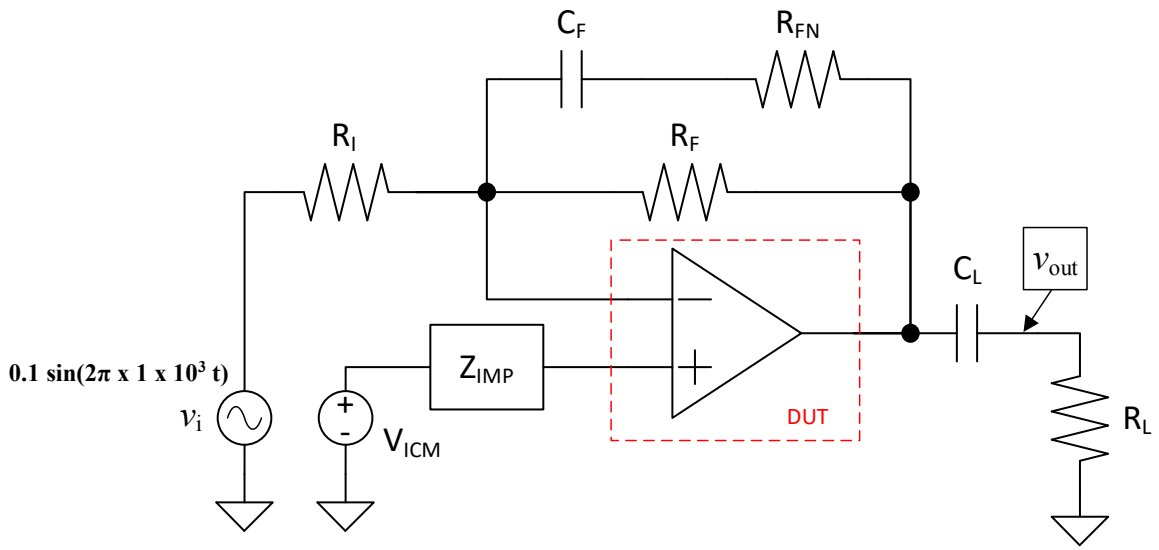
You must ensure that the total quiescent current consumption always falls below 2mA.

> **Hint 1:** The (W/L) ratio of the transistor biased with $V_{BN,}$ and the biasing block directly correlates with the total current consumed in the entire circuit.

4.6 Total Harmonic Distortion

Apply 1kHz sine waveform with an amplitude of 100mV_{peak} to the input and find the total harmonic distortion (THD).

Will there be a difference if we apply a 10kHz signal? Why?

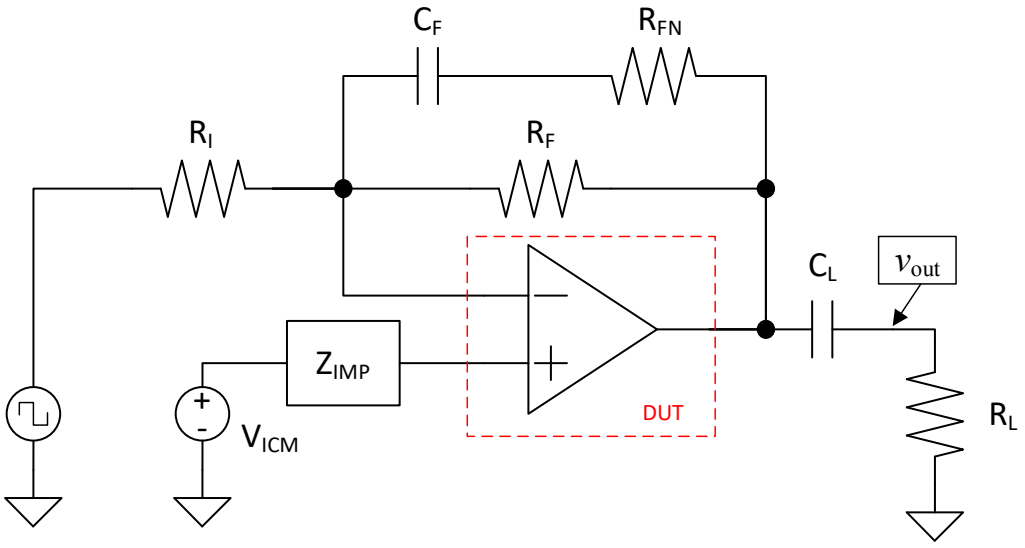


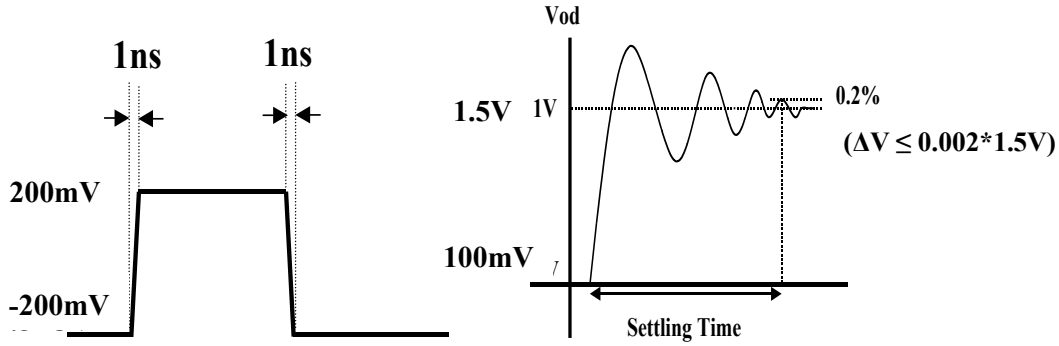
Hint 1: In the **Analog Environment**, go to **Analyses** and **Choose**. Choose a transient simulation by pressing **tran**. **Stop Time**: **1.05u**. Click **Conservative**. Press **Options**, type in **step: 0.0001e-03**, **maxstep: 0.0005e-3,** and click **method: Gear2only**.

Hint 2: In the **Analog Environment,** go to **Simulation**, **Options**, click **Analog**. Type **reltol: 1e-5**, **vabstol: 3e-8** and **iabstol: 1e-13**.

4.7 Settling Time

Apply a pulse to the input. The low voltage of the pulse is -200mV, and the high voltage is 200mV. The transition time of the rising and falling edge is 1ns. Find the settling time.





For the **pulse input source**, key in the following parameters:

V1 = 200mV
V2 = -200mV
Delay = 100ns
Rise Time = 1ns
Fall Time = 1ns
Pulse Width = 50μs
Period = 100μs

Hint 1: In the **Analog Environment**, go to **Analyses** and **Choose**. Choose the transient simulation by pressing **tran**. **Stop Time**: **300**μ. Click **Conservative**.

Hint 2: You must figure out how to measure the settling time. Please ask for guidance if you need help.

4.8 Slew Rate

Apply the above-mentioned pulse to the input. Find the slew rate of both the rising and falling edge.

Hint 1: Measure the 10% to 90% of the transition and vice versa for the rising and falling edge, respectively.

Hint 2: Run the simulation. You should have satisfied all your specifications for the **TYPICAL** mode.

Hint 3: The biasing current might improve the slew rate at the expense of excessive current consumption.

4.9 Process, Supply Voltage and Temperature Variation

You need to satisfy the **Closed-Loop Gain**, **Common-mode Gain** and **Total Harmonic Distortion** for the **FOUR** different **corners, temperature variation and voltage supply variation** while **ensuring that all specifications are satisfied at typical values**:

- V_{DD}: **1.5V – 1.8V**
- Temperature: **-40˚C – 100˚C**
- Fast - Fast (ff)
- Slow- Slow (ss)
- Slow - Fast (sf)
- Fast - Slow (fs)

Go to **Analog Environment window**, **Setup** and click on **Model Libraries**. Click on the **mos model library file** and change **typ** to **ff**. Press **OK**. Run the simulation and see if your results satisfy the specification listed. Do that for the other corners, e.g., ss, sf and fs.

This is the last part of the simulation process and is **CERTAINLY** the most tedious, challenging, and time-consuming part. You will take about **10 days** to complete and satisfy all the specifications for the four corners.

Hang on there! Please persevere and keep going.

Rule of Thumb

The sky gets darkest when dawn is approaching!

5. Layout

At this junction, you would have completed the circuit design & simulation successfully. The process corners are challenging and require numerous iterations with insight into the trade-off. Do not be too worried about it. I believe that it will not affect your grade adversely. The most crucial objective of this assignment is for you to **LEARN** through **ACTIVE PARTICIPATION**. In fact, it is already an achievement to satisfy the **TYPICAL** mode for all the different specifications successfully.

In fact, the most challenging part of this assignment is **OVER**. Now, it can be considered **HONEYMOON**.

Before continuing with the layout drawing, you will realize that the (W/L) ratio of the transistors in Fig. 3 is too large. This makes it difficult to draw the layout. Therefore, you must create **MULTIPLIERS** for the transistor. For example, if the width is 240, you can reduce the width to 12 by having 20 multipliers. To recap: the (W/L) ratio of individual transistors is added for parallel connection topology.

For the layout of your circuit, do follow the lab exercises which you completed in the previous exercise. The concept is generally the same. Do make use of what you have learnt during NM6002, noting that matching is essential for analog circuits. Also, frequent ground and V_{DD} ties are necessary for NMOS and PMOS, respectively, for matching and prevention of latch-up and threshold voltage variation. Kindly take note that there are 6 metal layers available in this design kit. However, use only the first 4 metals; the other TOP metal is for global interconnections or routing at the SoC level.

Please remember to **run DRC** frequently to confirm that there are no design rule violations. After DRC is correctly validated, you must perform **Layout Vs Schematic (LVS)** followed by **Parasitic Extraction (PEX)**. Lastly, you would need to perform the **post-layout simulation**. Ensure parasitic resistance and capacitance are present in the netlist after being extracted by PEX.

6. Additional Information

The performance of the Audio Amplifier is determined/measured with the result of the post-simulation. Therefore, it is important to reserve some design margins for the required specification during the pre-simulation.

Probably, there will be **NO** time to re-simulate the circuit and modify the layout when the designer finds that the performance of the post-layout simulation fails to meet the specifications.

To help you visualize the layers associated with this process, the cross-sectional view shows how the various layers interact with one another. In the Cadence Virtuoso Layout XL, your design is observed from a top-view perspective.

Personal Score Sheet

Name: _____ Date: _____

Specification		**Signature**
Closed Loop Gain		
Closed Loop Unity Gain Bandwidth		
Common-mode Gain		
Feedback Loop Gain		
Feedback Loop Phase Margin		
Power Supply Rejection Ratio		
Current Consumption		
Total Harmonic Distortion		
Settling Time		
Slew Rate		
Chip Area		

Please scan a copy of this page which must be included in the appendix of the final report.