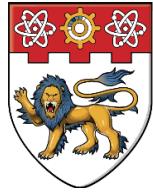




Technische Universität München



NANYANG  
TECHNOLOGICAL  
UNIVERSITY

# NM6007

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Analog IC Design Course (Lab)

**Individual Lab Assignment  
Class AB Audio Amplifier with  
Translinear Loop**

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# Chapter 1: Introduction

This report is a detailed explanation of a Class AB Audio Amplifier with translinear loop design which was undertaken as part of the Analog IC Design Lab assignment at Nanyang Technological University. The Amplifier is designed to have a closed loop gain of 12dB, closed loop bandwidth of  $\geq 300$  kHz. Class AB amplifiers are a popular choice due to their ability to achieve a balance between efficiency and linearity compared to Class A or Class B designs. This lab experiment focused on designing and analyzing a Class AB audio amplifier circuit that incorporates a translinear loop and a constant gm biasing circuit.

This amplifier was designed in the  $0.18\text{ }\mu\text{m}$  CMOS process (CSM) for a wide operating range ( $-40^\circ\text{C}$  to  $100^\circ\text{C}$ ) with a typical supply voltage of 1.6V (1.5V – 1.8 V range). The designed circuit ensures functionality across variations in process, temperature and supply voltage.

We begin by characterizing the PMOS and NMOS transistors, determining parameters such as a single transistor such as process transconductance ( $k_n', k_p'$ ), channel length modulation ( $\lambda_n, \lambda_p$ ) and threshold voltages ( $V_{tn}, V_{tp}$ ). Proceeding to schematic design and pre-simulation realizing all the specifications by transistor sizing and tuning components namely resistors and capacitors. Once the specifications are satisfied in pre-simulation, we proceed to draw the corresponding layout and run the DRC and LVS checks to see the layout matches the schematic. Next comes parasitic extraction (PEX) and then post simulation.

Table 1: Class AB Audio Amplifier design specification

Specification	Units		Pre-simulation	Post-simulation
Closed Loop Gain (x4)	dB	-	$12 (\pm 5\%)$	$12 (\pm 5\%)$
Closed Loop Unity Gain Bandwidth	kHz	$\geq$	300	300
Common-mode Gain	dB	$\leq$	-75	-73
Feedback Loop Gain	dB	$\geq$	80	75
Feedback Loop Phase Margin	degree	$\geq$	60	60
Power Supply Rejection Ratio	dB	$\leq$	-70	-65
Current Consumption	mA	$\leq$	2	2
Output Swing (@ VDD = 1.5V)	V	-	$0.1 \leq V_o \leq 1.4$	$0.1 \leq V_o \leq 1.4$
Total Harmonic Distortion	dB	$\leq$	-80	-77
Settling Time	$\mu\text{s}$	$\leq$	0.45	0.50
Slew Rate	$\text{V}/\mu\text{s}$	$\geq$	4	4
Chip Area	$\text{um}^2$	$\leq$	-	$250 \times 200$

# Chapter 2: Theoretical Analysis of the Design

## 2.1 Biasing Circuit – Analysis

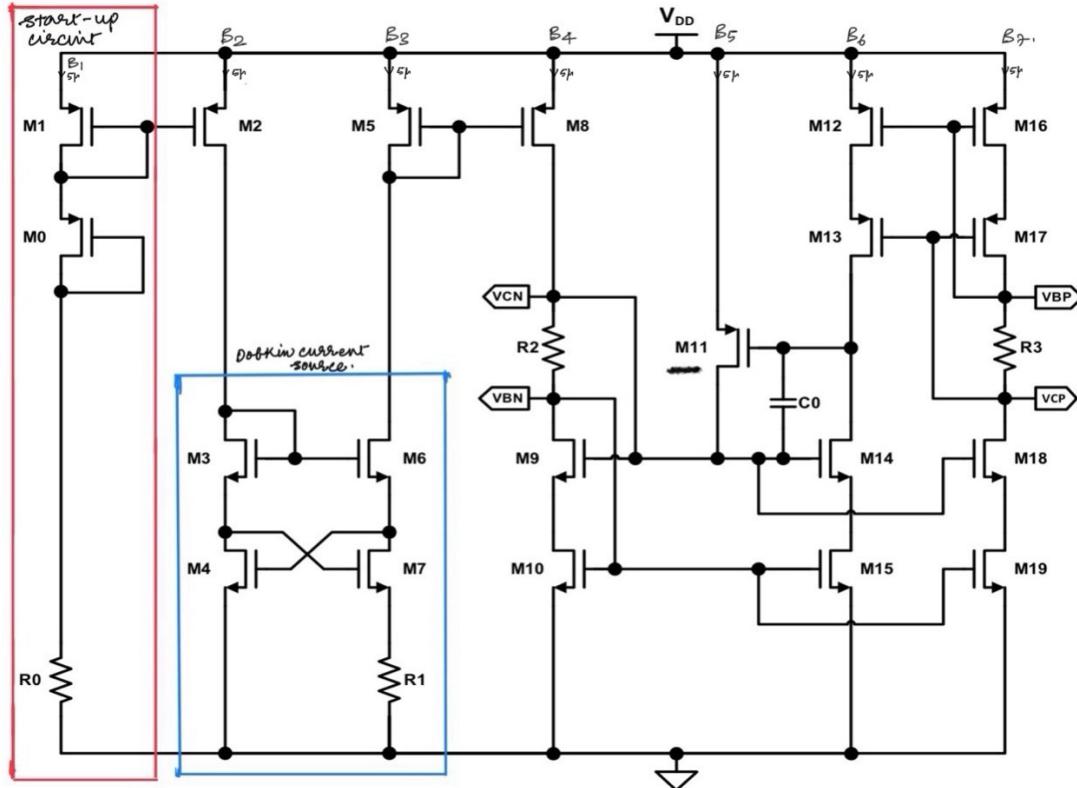


Figure 1: Biasing Circuit

As shown in the Figure 1 above, Once the circuit is powered up, the startup circuit consist of M0, M1 and R1. A 2VGS voltage drop across the transistors and the spare voltage is dropped across the resistor R0. We can modulate the current flowing through the startup based on the size of the resistor R0. Since the current through the biasing circuit goes waste, we would like to use a larger resistor for smaller current. Once the current through M1 is stable it is mirrored through M2. The transistors M3, M4, M6 and M7 form a Dobkin Current source it ensures that the mirrored current has a constant gm. So, the transistors M3 and M4 become crucial to ensure transistors M6 and M7 are properly turned on. Once these conditions are met depending on their ratios a constant gm current is established. The equation for the Dobkin Current source is:

$$V_{GS3} + V_{GS7} + V_{R1} = V_{GS4} + V_{GS6}$$

The current from branch containing M5 is mirrored to branch containing M8. From Where the voltage is dropped across R2 which is equal to the overdrive voltage. Currents from branches containing transistors like M10 get mirrored to those with transistors like M19. The voltage drop across R3 is also equal to overdrive voltage. A critical aspect of this circuit's operation lies in its feedback mechanism facilitated by the push-pull situation at

point 1 in the circuit. Transistor pairs in branch B6 PMOS-NMOS undergo a ‘tug-of-war’ if their currents aren’t balanced - transistor M11 steps in here as a regulator ensuring equilibrium between them. The presence of capacitor C0 adds an extra layer of stability preventing any oscillations or instabilities within the circuit. The drop across the resistors R2 and R3 give rise to VCN/VBN and VCP/VBP respectively.

### 2.1.1 Dobkin Current Source

As mentioned in the above explanation and marked in Figure 1 about a Dobkin Current Source providing a constant gm current.

Consider Figure 2 A Dobkin Current Source, which provides constant gm bias current.

$$\text{Assuming } \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_6 = \frac{1}{4} \left(\frac{W}{L}\right)_7$$

From the circuit we can write,

$$V_{GS4} = V_{GS7} + I_{D7}R_1$$

$$I_{D7}R_1 = V_{GS4} - V_{GS7}$$

$$I_{D7}R_1 = V_{THn} + \sqrt{\frac{2I_{D4}}{\mu_n C_{ox}(W/L)_4}} - V_{TH7} - \sqrt{\frac{2I_{D7}}{\mu_n C_{ox}(W/L)_7}}$$

$$I_{D7}R_1 = \sqrt{\frac{2I_{D4}}{\mu_n C_{ox}(W/L)_4}} - \sqrt{\frac{2I_{D7}}{\mu_n C_{ox}(W/L)_7}}$$

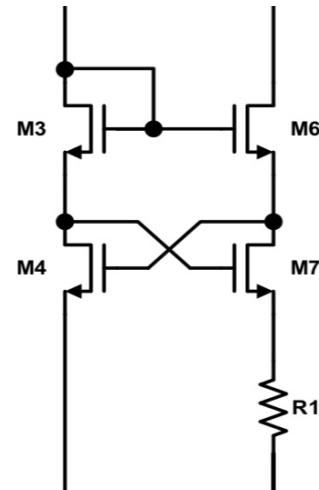


Figure 2: Dobkin Current Source

Perfect current mirror,  $I_{D3} = I_{D4} = I_{D6} = I_{D7} = I_D$

$$I_D R_1 = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)_4}} \times \left(1 - \sqrt{\frac{(W/L)_2}{(W/L)_7}}\right)$$

$$R_1 = 2 \sqrt{\frac{1}{2I_D \mu_n C_{ox}(W/L)_4}} \times \left(1 - \sqrt{\frac{(W/L)_4}{(W/L)_7}}\right)$$

$$g_m = \frac{2}{R_1} \times \left(1 - \sqrt{\frac{(W/L)_4}{(W/L)_7}}\right)$$

As considered, we know that  $\frac{(W/L)_4}{(W/L)_7} = \frac{1}{4}$ , then we have  $g_m = \frac{2}{R_1} \times \left(1 - \frac{1}{2}\right) = \frac{1}{R_1}$

As it's evident from the above equation,  $g_m$  only depends on  $R_1$ , independent of any supply or process variation. As determined above  $g_m = \frac{1}{R_1}$ , this gives us a way to determine the value of  $R_1$  while sizing the transistors.

## 2.2 Class AB Audio Amplifier with Translinear Loop – Analysis

As shown in Figure 3, is the Class AB Audio Amplifier with Translinear Loop, it comprises of 3 stages, Folded Cascode Differential Amplifier stage, Gain Stage and Translinear Loop Stage.

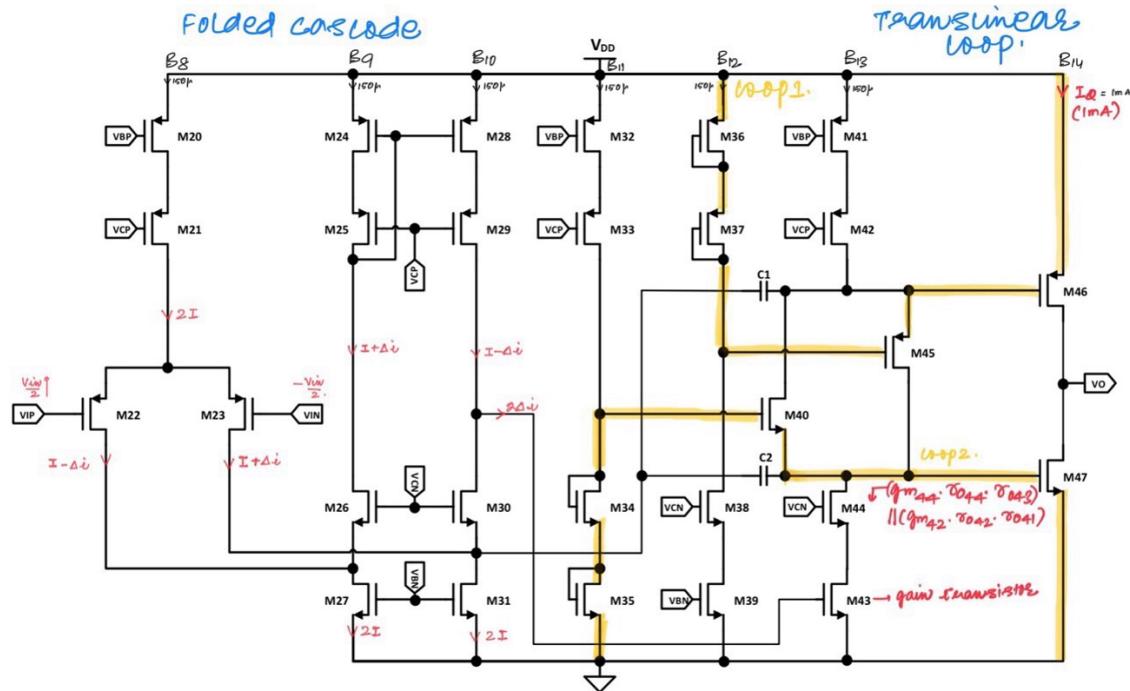


Figure 3: Class AB Audio Amplifier with Translinear loop

The Folded cascode Differential Amplifier, the input differential pair, formed by transistors M22 and M23, serves as the initial stage, converting the input voltage signal ( $V_{IN}$ ) into a differential current. This current is proportional to the transconductance ( $g_m$ ) of the input transistors and the input voltage, following the relationship:  $I = g_m * V_{IN}$ . It is good to remember that for a high gain or high  $g_m$  we should size transistors of M22 and M23 good enough for a high gain. The current from the input differential pair is then mirrored by the transistors M26, M27, M30, and M31, acting as a current mirror, directing the current to the translinear loop.

Beginning by calculating the minimum input voltage for differential input pair M22-M23

$$V_{IN_{min}} = GND + 2\Delta V - V_{SG22}$$

$$V_{IN_{min}} = GND + \Delta V - V_{TH} = \Delta V - V_{TH}$$

As  $\Delta V - V_{th} < 0$  i.e. the minimum input voltage for PMOS input folded cascode is lower than ground, it can handle and work on an AC signal riding on GND. Considering balanced condition - the current flowing through the branch B8 is  $2I$  and B9 and B10 are  $I$  each, the current splits equally between the two transistors M22 and M23. Considering the voltage at the input is raised i.e. VIP. This leads to the  $V_{GS22}$  to reduce leading to the current through M22, M23 become  $I - \Delta i, I + \Delta i$  respectively. There is a  $2\Delta i$  current going out of the branch B10 that is charging the gate capacitor of M43 causing the gate voltage to increase leading to the transistor M43 to turn on, M43 pulls all the current provided from the biasing M41 and M42, pulling more current to ground turning off M47 and turning on M46. If the voltage is low, the current is less and leading to M47 to turn on and M46 to turn off leading to pull down current from the load. M46, M45, M37, M36 form a translinear loop, consider the branch B12 the NMOS are biased from the biasing circuit, leading to a constant current in the branch as both the PMOS's in the branch are diode connected the voltages across them are also constant. The constant DC voltage across M37 and M46 balance the  $V_{GS}$  across M46 and M45. Consider M46 is conduction this means a large proportion of voltage is dropped across the gate of M46 and the  $V_{GS}$  across M37 is less, it might be so low that the MOS may go into sub-threshold. Similarly, M47, M40, M34, M35 form another translinear loop. Under quiescent condition the current flowing through PMOS and NMOS i.e. M46 and M47 are equal we have loops which share transistors having same current, which could be very useful in sizing the transistors. The capacitor C1 and C2 are used for Ahuja Compensation. The primary purpose of these capacitors is to provide a dominant pole-zero pair that shapes the frequency response of the amplifier, improving its stability and phase margin. Capacitor C1 creates a dominant pole at a relatively low frequency by shunting the high-impedance node at the output of the second stage. This dominant pole ensures that the open-loop gain rolls off at a controlled rate, preventing excessive high-frequency gain and potential instability. Capacitor C2, in conjunction with the feedback resistor RF, forms a zero in the amplifier's frequency response. This zero helps to cancel the effect of a non-dominant pole that would otherwise occur at a higher frequency, typically due to the parasitic capacitances in the circuit. By strategically positioning the dominant pole and the compensating zero, the Ahuja compensation technique effectively shapes the frequency response of the amplifier, ensuring a stable closed-loop operation and a sufficient phase margin. This, in turn, prevents oscillations, ringing, or other undesirable transient behaviour in the amplifier's output. The translinear loop plays a crucial role in enabling Class-AB operation by adapting the bias currents provided to the input differential pair and the output stage based on the input signal level. As the input signal level increases, the loop adjusts the bias currents of the output stage transistors, M46 and M47, allowing them to be fully turned on and provide high output drive capability while maintaining linearity. The translinear loop's adaptive biasing of the output stage transistors, combined with the input stage's differential pair and current mirroring, enables the amplifier to operate in Class-AB mode, offering improved linearity and power efficiency compared to traditional Class-A or Class-B amplifiers.

# Chapter 3: Schematic Design

## 3.1 Transistor Characterization

We begin with characterizing the transistor, in which parameters like  $k_n'$ ,  $k_p'$  i.e. process transconductance parameters and  $V_{THn}$ ,  $V_{THp}$  i.e. threshold voltages. We find these by the input characteristic curve (  $I_D$  vs  $V_{GS}$  ).

For a MOSFET in saturation  $i_D = \frac{k_n' W}{2 L} (V_{GS} - V_{THn})^2$ .

Here, basic NMOS ( $W/L$ ) =  $(1.06\mu/0.720\mu) = 1.4$ , we consider the overdrive voltage  $\Delta V = 200\text{mV}$ , from the circuit annotations  $|I_D| = 5.79818 \text{ u}$ .

Substituting the values in the current equation  $i_D = \frac{k_n' W}{2 L} (V_{GS} - V_{THn})^2$

$$k_n' = 690.564 \mu \text{ A/V}^2$$

$$\text{As } \Delta V_{sat} = V_{GS} - V_{THn}$$

$$\text{Substituting } \Delta V_{sat} = 306.565\text{mV} \text{ and } V_{GS} = 0.8 \text{ V we get } V_{THn} = 0.493435\text{V}.$$

Similarly, we characterize for PMOS we obtain

Here, basic PMOS ( $W/L$ ) =  $(2.12\mu/0.720\mu) = 2.8$ , we consider the overdrive voltage  $\Delta V = 200\text{mV}$ , from the circuit annotations  $|I_D| = 10.2442 \text{ u}$ .

Substituting the values in the current equation  $i_D = \frac{k_n' W}{2 L} (V_{GS} - V_{THn})^2$

$$k_p' = 182.932 \mu \text{ A/V}^2$$

$$\text{As } \Delta V_{sat} = V_{GS} - V_{THn}$$

$$\text{Substituting } \Delta V_{sat} = -333.911\text{mV} \text{ and } V_{GS} = 0.8 \text{ V we get } |V_{THp}| = 0.466089\text{V}.$$

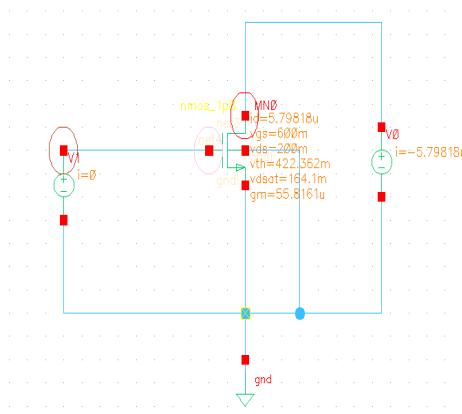


Figure 4: parameter analyses circuit

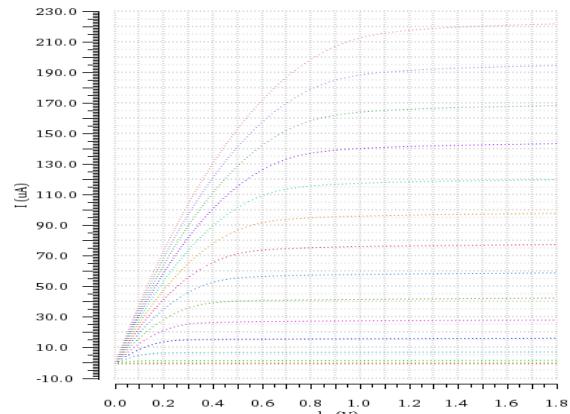


Figure 5: family curves of  $i_D$  with respect to  $V_{GS}$

Table 2: process transconductance parameter and threshold voltage MOSFET

Parameter	$k_n'$	$k_p'$	$V_{THn}$	$ V_{THp} $
Test value	$690.564\mu A/V^2$	$182.932\mu A/V^2$	0.4934V	0.4661V

### 3.2 Transistor Sizing of Biasing Circuit

We first allocate current that we decide should flow through branches of the biasing circuit. The current consumption of the entire circuit is  $< 2mA$ . It must be noted that a larger proportion of the current should be allocated for the amplifier circuit for good performance. Since we have about 7 branches in the biasing circuit, we allocate each branch with  $5\mu A$ . This gives us a total  $35\mu A$  current being allocated to the biasing circuit. Determine the overdrive voltage ( $\Delta V$ ) this parameter is constrained by output swing; we assume it to be  $0.2V$ .

Points to remember while sizing.

1. Size (W/L) of M7 is 4 times size (W/L) of M6.
2. PMOS should be made 2-3 times larger than corresponding NMOS.
3. Maintain all transistors in saturation.
4. The less the amount of current the biasing circuit consumes the better.
5. The voltage drops across  $R_1$  is  $(\Delta V/2)$  while that of  $R_2$  and  $R_3$  is  $(\Delta V)$  ideally when we ignore body bias effects.
6. The value of  $R_0$  the larger the better hence we choose  $30K\Omega$  that keep M0 and M1 in saturation.

Table 3: Transistor Sizing information of Biasing Circuit

NMOS	W/L( $\mu m$ )	M	PMOS	W/L( $\mu m$ )	M
M3,M4,M6	0.555/0.72	1	M1	1.110/0.72	4
M7	2.22/0.72	1	M0	2.220/0.72	1
M9, M14,M18	2.775/1.44	1	M2	0.445/0.72	1
M10,M15,M19	0.555/0.72	1	M5,M8	2.220/0.72	1
M31	1.4/0.6	1	M12,M16	2.220/0.72	2
M35, M36	4.8/0.6	1	M13, M17	11.10/0.72	1
M39, M40, M41	4.8/0.6	1	M11	1.000/15.8	1

\* M stands for multiplier

Table 4: Resistor Values in Biasing Circuit

Resistor	Value ( $\Omega$ )
$R_0$	30K
$R_1$	20K
$R_2$	40K
$R_3$	62K

Table 5: Current Consumption (Branch wise)

Branch	Current ( $\mu\text{A}$ )
B1	5.9099
B2	0.7338
B3	4.0158
B4	4.0363
B5	0.9653
B6	5.0024
B7	5.0019

Current consumption of entire biasing circuit is  $25.6654\mu\text{A}$ .

### 3.3 Transistor Sizing of Class AB Amplifier Circuit

Similar to the sizing of biasing circuit, we need to allocated currents to each branch, as the total current consumption is limited to  $2\text{mA}$  and  $35\mu\text{A}$  was used in the biasing circuit current of about  $1.96\text{mA}$  is available for the Class AB Amplifier. We size the transistors stages wise. We must remember the M46, M47 is a power transistor and of M22 and M23 should have high gain so that (W/L) is huge. We should keep the biasing transistors in the amplifiers the same (W/L) and increase multiplier to meet the current requirement. We can also calculate the (W/L) of the power transistors solving the equations of the translinear loops. Translinear loop has a voltage gain of 1 and a huge current gain. The capacitors C1 and C2 perform Ahuja compensation.

Table 6: Transistor Sizing information of Amplifier Circuit

NMOS	W/L( $\mu\text{m}$ )	M	PMOS	W/L( $\mu\text{m}$ )	M
M26, M30	2.775/1.440	8	M20	2.220/0.720	36
M27, M31	0.555/0.720	16	M21	11.10/0.720	36
M34	0.555/0.720	38	M22, M23	2.220/0.400	66
M35	4.400/0.200	48	M24, M28,	2.220/0.720	16
M38	2.775/1.440	16	M25, M29	11.10/0.720	16
M39	0.555/0.720	20	M32	2.220/0.720	24
M40	6.660/0.720	16	M33	11.10/0.720	12
M43	0.555/0.720	48	M36	8.400/0.200	44
M44	2.775/1.440	4	M37	2.220/0.720	44
M47	48.00/0.200	32	M41	2.220/0.720	16
			M42	11.10/0.720	16
			M45	2.220/0.720	8
			M46	64.00/0.200	64

\* M stands for multiplier.

Table 7: Current Consumption (Branch wise)

Branch	Current ( $\mu$ A)
B8	90.4796
B9	34.9996
B10	35.0053
B11	60.0242
B12	99.4164
B13	40.1964
B14	904.732

Current consumption of Audio Amplifier is 1.2648535mA.

Total current consumption of the entire circuit is equal to 1.2905189mA.

### 3.4 Testbench Design

Using the symbols generated from the biasing circuit and class AB audio amplifier we connect the biasing pins VCN, VBN, VCP, VBP between the two circuit and generate the Op-Amp symbol. We now use the Op-Amp symbol and built the test bench circuit.

Table 8: Values of the components used in the testbench circuit

Component	Value
$R_L$	16 $\Omega$
$C_L$	470u F
$R_F$	500 $\Omega$
$R_{FN}$	5 $\Omega$
$C_F$	5p F
$R_I$	125 $\Omega$

1.  $R_I$  and  $R_F$  are to set the gain of the audio amplifier. The ratio  $R_F/R_I = 4$ .
2.  $C_F$  and  $R_{FN}$  part of feedback network for frequency compensation, they limit the bandwidth of amplifier ensuring stability and reducing noise.
3.  $C_L$  coupling capacitor that blocks DC signals and allows AC signals to pass to load  $R_L$ .
4. ZIMP is the impedance seen by the operational amplifier at both inputs. It's crucial for maintaining balance and linearity of amplifiers response. Matching impedance help in common mode rejection ratio which is essential for differential amplifiers.
5. For the  $V_{out} = 0.8$ ,  $V_{ICM} = 160mV$ . Based on the resistor divider formula  $V_{ICM} = (0.8/5) = 0.16V$ .

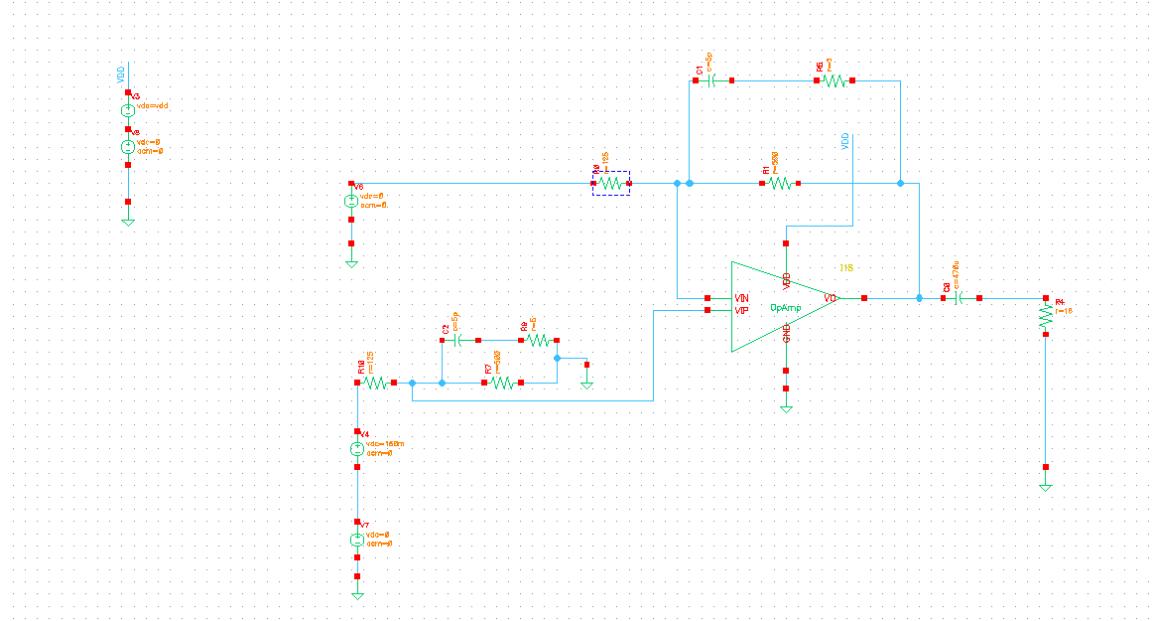


Figure 6: Test Bench Circuit

# Chapter 4: Pre-simulation and Performance Analysis

## 4.1 Closed Loop Gain and Unity Gain Bandwidth

These parameters determine the amplifier's ability to maintain a desired gain over a specific frequency range and its capability to amplify input signals without introducing significant distortion. To evaluate the closed-loop gain, an AC analysis is performed by applying a small-signal input voltage (typically 1V AC) to the amplifier's input stage. The closed-loop gain is then calculated as the ratio of the output voltage to the input voltage, expressed in decibels (dB). The desired closed-loop gain for this amplifier is set to 12 dB ( $\pm 5\%$ ), which corresponds to a voltage gain of approximately 4. The unity gain bandwidth, on the other hand, represents the frequency at which the amplifier's closed-loop gain drops to unity (0 dB). This parameter is crucial for determining the amplifier's ability to faithfully amplify high-frequency signals without significant attenuation. For audio applications, a unity gain bandwidth of at least 300 kHz is desired to ensure adequate reproduction of high-frequency audio content. The simulation result is shown in Figure 7 and Figure 8.

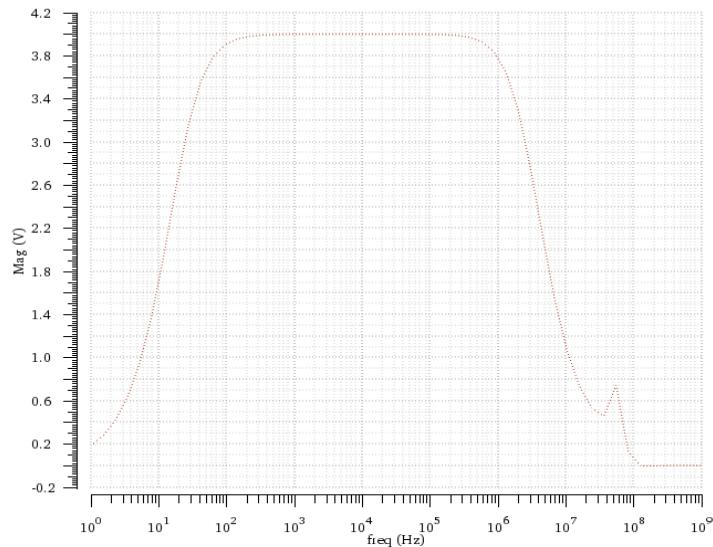


Figure 7: Closed Loop Gain

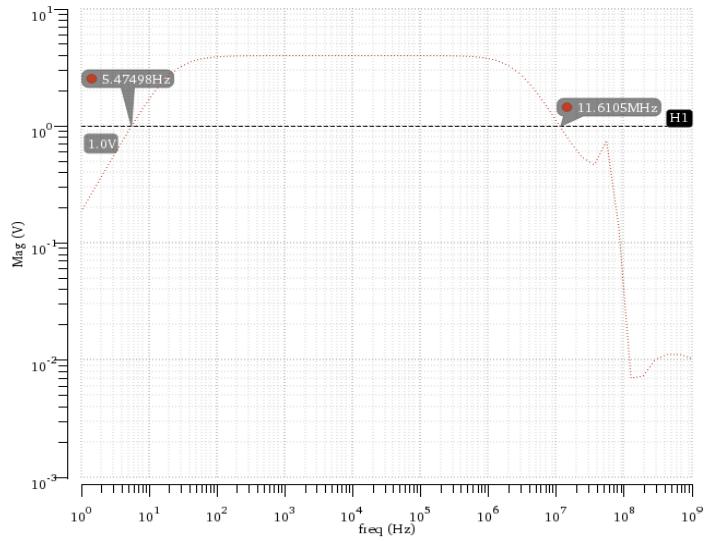


Figure 8: Unity Gain Bandwidth

#### 4.2 Common-mode Gain

It represents the amplifier's ability to reject common-mode signals, which are signals present simultaneously on both inputs with the same amplitude and phase.

In an ideal differential amplifier, the common-mode signal should be completely rejected, resulting in a common-mode gain of zero. However, due to practical limitations and non-idealities in the circuit, a finite common-mode gain is observed. The lower the common-mode gain, the better the amplifier's ability to suppress common-mode signals, thereby improving its overall performance and signal integrity.

To evaluate the common-mode gain, an AC analysis is performed by applying a common-mode signal (typically 1V AC) to both inputs of the amplifier simultaneously. The common-mode gain is then calculated as the ratio of the output voltage to the common-mode input voltage, expressed in decibels (dB). The target specification for the common-mode gain of this amplifier is to be less than or equal to -75dB. The simulation result is shown in Figure 9.

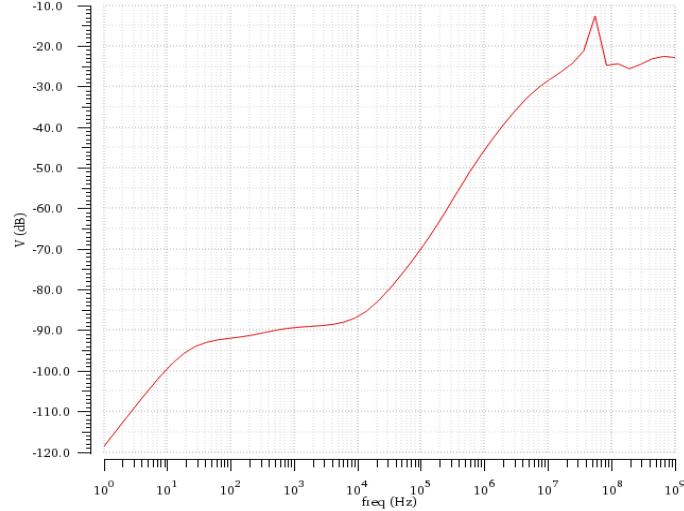


Figure 9: Common-mode Gain

### 4.3 Feedback Loop Gain and Phase Margin

The feedback loop gain represents the amount of signal amplification within the feedback loop, ensuring sufficient loop gain for effective feedback control. A higher feedback loop gain is desirable, with a typical target of at least 80 dB for this amplifier design.

The phase margin, on the other hand, quantifies the phase shift in the feedback loop at the unity gain frequency. A higher phase margin indicates a greater stability margin, reducing the risk of oscillations or ringing in the amplifier's output. The desired phase margin for this amplifier is 60 degrees or higher, ensuring a stable and well-damped closed-loop response. The following Figure 10 shows feedback loop gain and Phase Margin

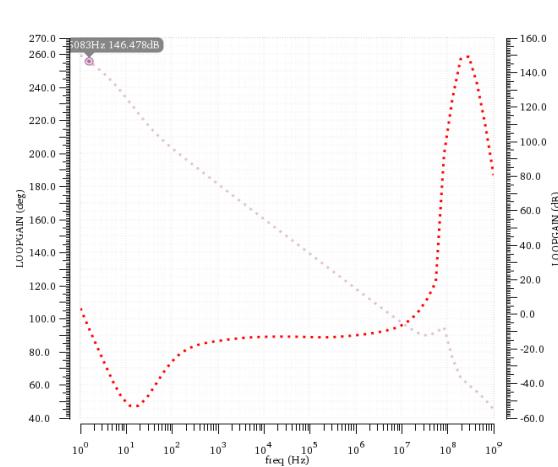


Figure 10: Feedback Loop Gain and Phase Margin

#### 4.4 Power Supply Rejection Ratio

A high PSRR is desirable, as it reduces the impact of power supply variations on the amplifier's output, improving signal integrity and overall performance.

To evaluate the PSRR, a small-signal AC voltage is applied to the power supply lines, and the resulting output voltage is measured. The PSRR is then calculated as the ratio of the input power supply signal to the output voltage, expressed in decibels (dB). The target specification for the PSRR of this amplifier is less than or equal to -70dB. Figure 11 plots UGBW for typical case.

$$\text{PSRR} = 20\log_{10}\left(\frac{\Delta V_{\text{supply}}}{\Delta V_{\text{out}}}\cdot A_V\right) \text{ dB}$$

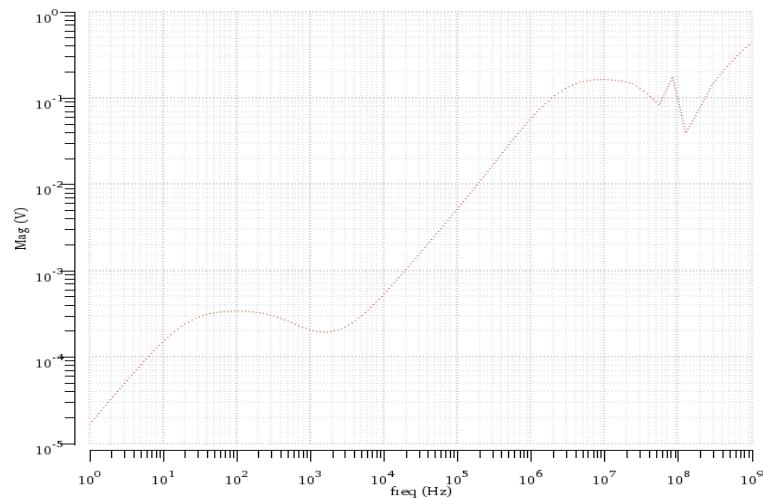


Figure 11: Power Supply Rejection Ratio

#### 4.5 Quiescent Current Consumption

For this amplifier design, the target specification is to maintain a quiescent current consumption of less than or equal to 2 mA.

Minimizing current consumption is essential for achieving power-efficient operation, particularly in portable or battery-powered applications. However, it is crucial to strike a balance between low current consumption and maintaining sufficient bias currents to ensure proper operation and meet other performance specifications.

## 4.6 Total Harmonic Distortion

The Total Harmonic Distortion (THD) is a measure of the amplifier's linearity and its ability to faithfully reproduce the input signal without introducing significant distortion. A lower THD value indicates better linearity and signal fidelity.

To evaluate the THD, a sinusoidal input signal (typically 1 kHz or 10 kHz) is applied to the amplifier, and the output signal is analysed for harmonic content. The THD is then calculated as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency component, expressed in decibels (dB). The target specification for the THD of this amplifier is less than or equal to -80dB.

$$\text{THD} = \frac{\sqrt{{V_2}^2 + {V_3}^2 + {V_4}^2 + \dots}}{V_1}$$

where  $V_n$  stands for the RMS voltage of  $n^{\text{th}}$  harmonic. When  $n=1$ , it refers to the fundamental frequency.

## 4.7 Settling Time

The settling time is a measure of the amplifier's transient response and its ability to settle to a stable output value after a step change in the input signal. A lower settling time is desirable, as it ensures a faster response and minimizes the time required for the output to reach its final value within a specified tolerance.

To evaluate the settling time, a step input signal is applied to the amplifier, and the time taken for the output to settle within a specified tolerance (typically 0.2% or 0.1% of the final value) is measured. The target specification for the settling time of this amplifier is less than or equal to 0.45 microseconds.

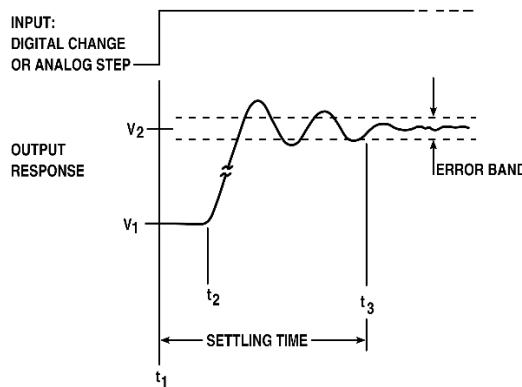


Figure 12: settling time definition

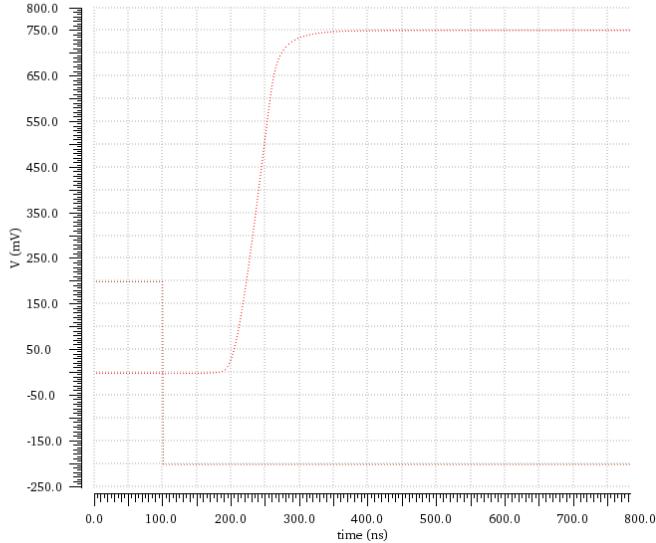


Figure 13: Settling Time and Slew Rate

#### 4.8 Slew Rate

The slew rate is a measure of the maximum rate of change of the amplifier's output voltage, typically expressed in volts per second (V/s). A higher slew rate is desirable, as it enables the amplifier to track rapid changes in the input signal without introducing significant distortion or limiting.

To evaluate the slew rate, a step input signal or a large-amplitude sinusoidal signal is applied to the amplifier, and the maximum rate of change of the output voltage is measured during the rising and falling edges or peaks.

The target specification for the slew rate of this amplifier is greater than or equal to 4 V/ $\mu$ s.

$$SR = \max \left( \left| \frac{dv_{out}(t)}{dt} \right| \right)$$

Here  $v_{out}(t)$  is the output of the amplifier.

#### 4.9 Output Swing

The voltage swing represents the maximum output voltage range that the amplifier can produce without introducing significant distortion or clipping. A larger voltage swing is desirable, as it allows the amplifier to handle a wider range of input signals without clipping or compression.

To evaluate the voltage swing, a large-amplitude sinusoidal input signal is applied to the amplifier, and the maximum peak-to-peak output voltage is measured before significant distortion or clipping occurs.

The target specification for the voltage swing of this amplifier, when operating at a supply voltage of 1.5V, is to have an output voltage range between 0.1V and 1.4V, ensuring sufficient headroom and avoiding clipping or compression. Figure 14 shows simulation results of output swing.

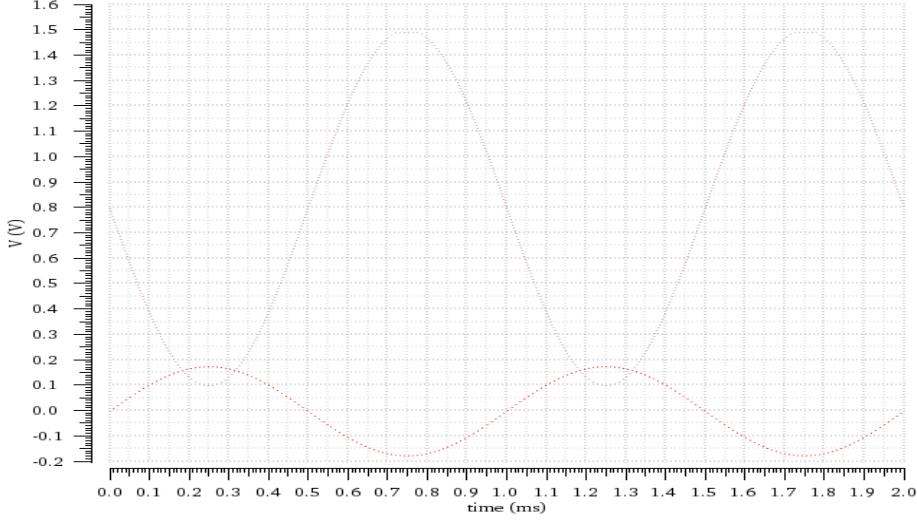


Figure 14: Power Supply Rejection Ratio

#### 4.10 Pre-simulation across process corners

To ensure robust performance and reliability, it is crucial to simulate the amplifier design across various process corners, accounting for manufacturing variations and extremes in device characteristics. The five process corners commonly considered are:

1. Typical-Typical (TT): This corner represents the nominal process parameters, where the transistor models are based on the typical values specified by the foundry.
2. Fast-Fast (FF): In this corner, the transistor models assume faster switching speeds and higher drive currents, representing the best-case scenario for device performance.
3. Slow-Slow (SS): Conversely, the slow-slow corner models slower switching speeds and lower drive currents, representing the worst-case scenario for device performance.
4. Fast-Slow (FS): This corner combines fast NMOS transistors with slow PMOS transistors, leading to potential imbalances and asymmetries in the circuit behaviour.
5. Slow-Fast (SF): Similar to the FS corner, this corner combines slow NMOS transistors with fast PMOS transistors, introducing further potential imbalances.

Simulating the amplifier design across these five process corners is essential to ensure that it meets the specified performance requirements, such as closed-loop gain, common-mode gain, and total harmonic distortion, under various manufacturing variations. This process involves adjusting the transistor models in the simulation environment to match the

respective corner conditions and analysing the results. The overall pre-simulation results are shown in the following table.

Table 9: Pre-simulation across five process corners

Output	Nominal	Spec	Min	Max	Typical 60 1.5	Typical 60 1.6	Typical 60 1.7	Typical 60 1.8	Typical -40 1.6	Typical 60 1.6	Typical 100 1.6	ff 60 1.6	fs 60 1.6	sf 60 1.6	
Closed Loop Gain	12.04	11.4-12.6	12.04	12.06	12.04	12.04	12.04	12.04	12.04	12.04	12.05	12.04	12.04	12.04	12.06
Unity Gain BW	19.5M	>300k	14.07M	25.68M	18.6M	19.5M	20.45M	21.39M	14.07M	19.5M	25.68M	20.37M	14.63M	22.02M	
Common Mode Gain	-90.8	<-73	-96.88	-85.83	-91.88	-90.8	-89.94	-89.23	-96.88	-90.8	-85.83	-86.11	-91.45	-89.68	
Feedback Loop Gain	115.1	>75	89.39	137.5	115.5	115.1	114.7	114.3	137.5	115.1	89.39	90.72	97.33	111.5	
Phase Margin	77.04	>60	72.91	79.08	77.51	77.04	76.64	76.29	72.91	77.04	78.35	77.67	75.03	79.08	
PSRR	-73.84	<-65	-81.31	-66.13	-72.55	-73.84	-74.91	-75.79	-81.31	-73.84	-66.13	-67.5	-75.56	-74.09	
Slew Rate	23.4M	>4M	13.43M	32.05M	21.67M	23.4M	25.01M	26.46M	31.11M	23.4M	18.38M	18.76M	13.43M	32.05M	
THD	-96.26	<-77	-98.48	-92.87	-96.62	-96.26	-96.37	-96.66	-92.87	-96.26	-98.48	-97.06	-96.96	-97.28	

# Chapter 5: Layout and Verification

## 5.1 General Considerations

### Considerations Before Creating the Class AB Amplifier Layout

Here are some key points to consider when designing the layout for your Class AB amplifier circuit:

#### Matching Input Transistors:

- To achieve excellent matching between the input transistors (critical for performance), utilize a **common centroid layout**.
- If your input transistors have a unit size multiplier of 12 (meaning they consist of 12 minimum-sized transistors connected in parallel), arrange them in a repeating pattern like this:

N M N M N M N M N M N  
M N M N M N M N M N M

Here, "M" and "N" represent the different transistors.

#### Minimizing Contact Resistance:

- Reduce the contact resistance of Vias (connections between metal layers) by increasing their contact area. This can be achieved by incorporating more contacts whenever feasible.

#### Protecting Resistors and Capacitors:

- Avoid routing metal layers directly over integrated resistors and capacitors. The signal running on the metal layer can modulate and alter the intended resistance and capacitance values of these components.

#### Guard Rings for Isolation:

- Enclose all NMOS and PMOS transistors within separate **guard rings**. These are essentially arrays of substrate contacts surrounding each transistor. Guard rings minimize parasitic resistance and effectively prevent latch-up (a destructive condition) in the CMOS circuit.

#### Metal Layer Usage:

- While the design allows for using three metal layers for wiring, prioritize using the first two metal layers (M1 and M2) whenever possible, especially for initial routing. This simplifies connections between the biasing circuit and the amplifier circuit itself.

#### Matching Resistors:

- Ensure that the input resistor (R1) and the output resistor (R2) are well-matched to maintain optimal circuit performance.

#### Long Channel PMOS Placement:

- Position the two long-channel PMOS transistors as close as possible to each other. Additionally, exclude the lower PMOS from the overall PMOS guard ring since its body and source are already shorted together.

#### Symmetry:

- Maintaining symmetry in the layout can help mitigate the effects of process gradients and improve common-mode rejection and power supply rejection ratios.

### **Power and Ground Distribution:**

- Proper power and ground distribution networks should be implemented to ensure stable and consistent power delivery throughout the circuit, minimizing supply noise and voltage drops.

## **5.2 Layout of Biasing Circuit**

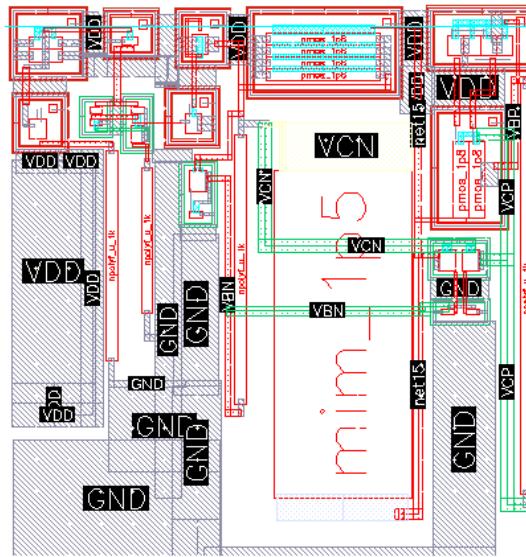


Figure 15: Layout of Biasing Circuit

### 5.2.1 Design Rule Check (DRC) of Biasing Circuit

The Design Rule Check (DRC) is a crucial step in the layout verification process. It involves running a tool that performs thorough checks of the layout to check if the layout is in accordance with foundry design rules and to identifies any violations or potential issues that could impact the manufacturability or functionality of the circuit.

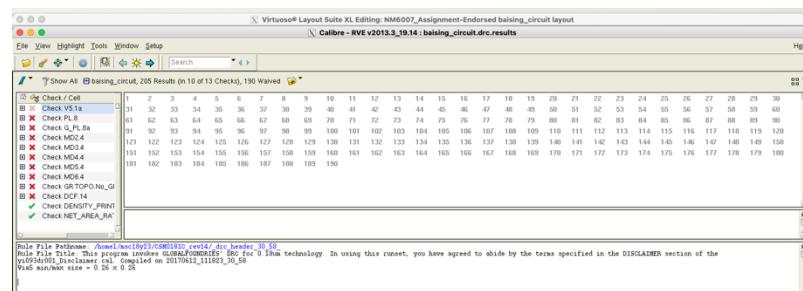


Figure 16: DRC Report of Biasing Circuit

## 5.2.2 Layout Versus Schematic Check (LVS) of Biasing Circuit

The Layout Versus Schematic (LVS) check is another critical verification step that ensures the consistency and correctness of the layout with respect to the original schematic design. It involves comparing the extracted layout netlist, which represents the physical layout, against the schematic netlist, which represents the intended circuit connectivity and device properties.

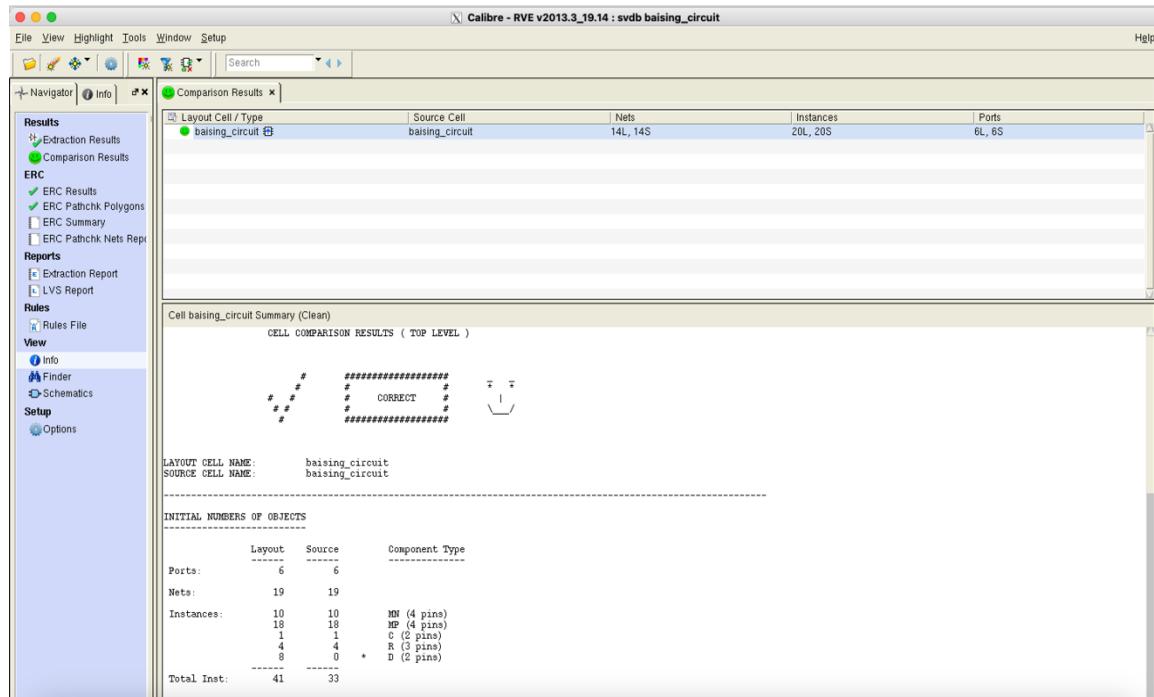


Figure 17: LVS Report of Biasing Circuit

### 5.3 Layout of Amplifier Circuit

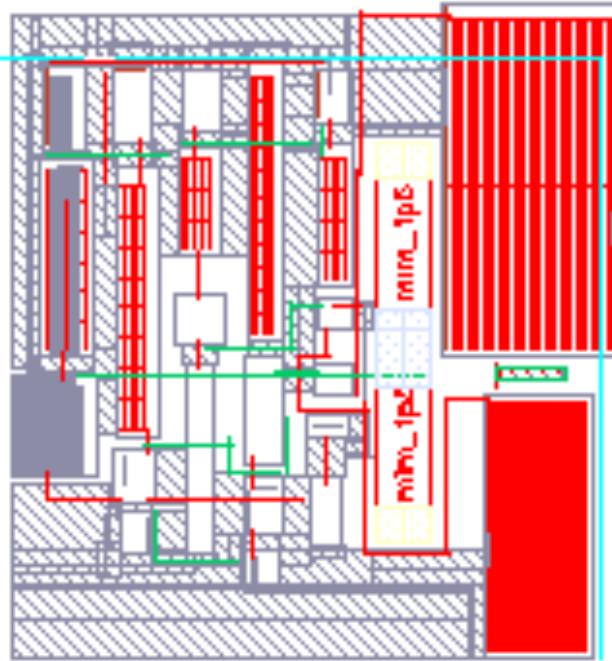


Figure 18: Layout: Amplifier Circuit

#### 5.3.1 Design Rule Check (DRC) of Amplifier Circuit

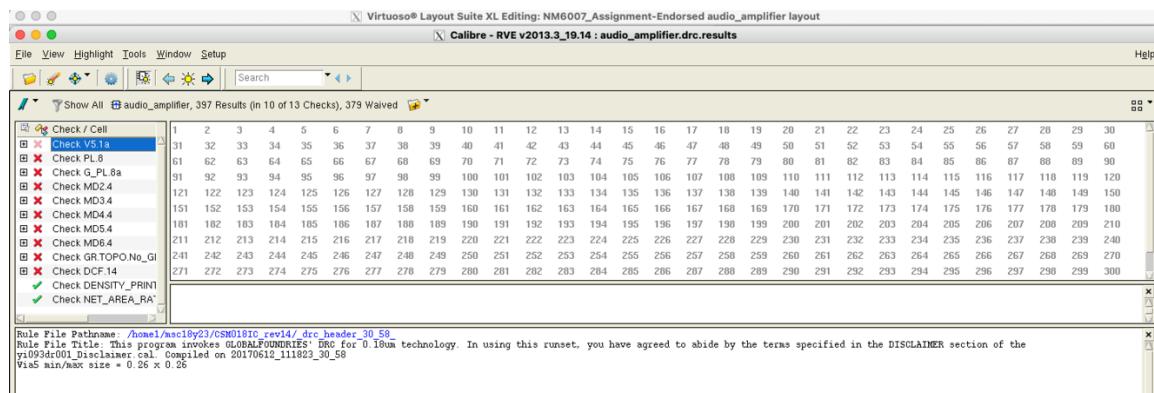


Figure 19: Design Rule Check of Amplifier Circuit

### 5.3.2 Layout Versus Schematic Check (LVS) of Amplifier Circuit

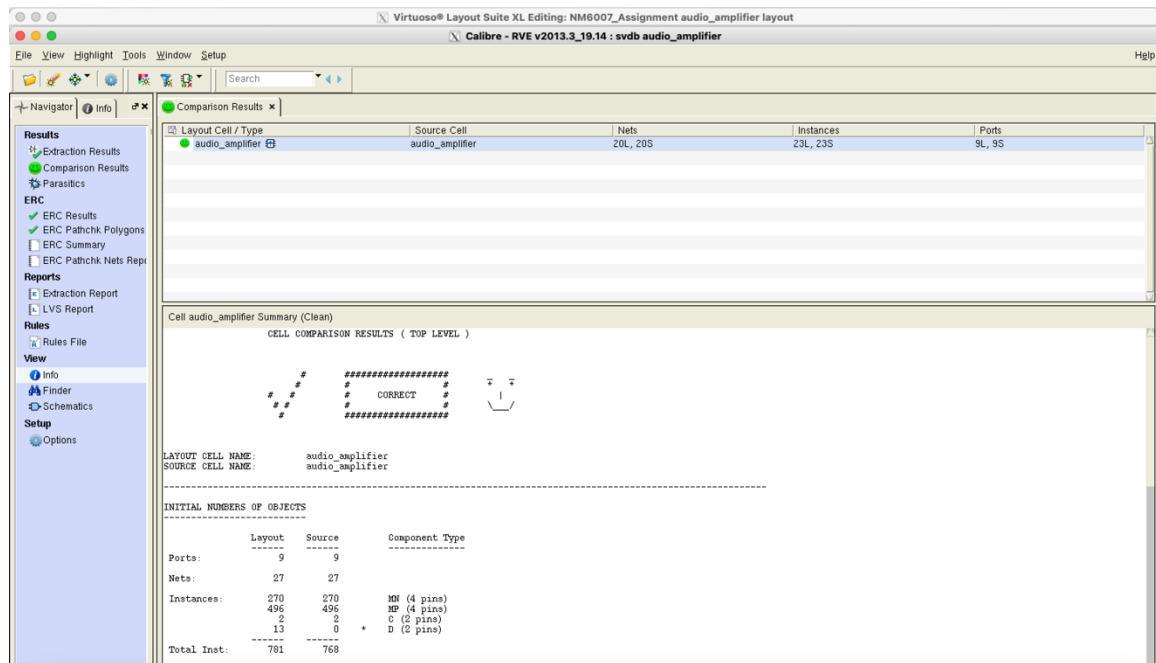


Figure 20: Layout VS Schematic Report of Amplifier Circuit

# Chapter 6: Post-layout Simulation

## 6.1 Parasitic Extraction (PEX)

Parasitic extraction (PEX) is the process of analyzing the physical layout and extracting the parasitic resistances, capacitances, and inductances associated with the interconnects and devices. These parasitic elements can have a significant impact on the performance and behavior of the circuit, particularly at high frequencies or in sensitive analog designs.



Figure 21: Parasitic Extraction

## 6.2 Post-layout simulation results

Table 10: Post-simulation across five corners

Output	Nominal	Spec	Min	Max	Typical 60 1.5	Typical 60 1.6	Typical 60 1.7	Typical 60 1.8	Typical -40 1.6	Typical 60 1.6	Typical 100 1.6	ff 60 1.6	fs 60 1.6	sf 60 1.6	ss 60 1.6
Closed Loop Gain	12.04	11.4-12.6	12.04	12.23	12.04	12.04	12.04	12.23	12.04	12.05	12.04	12.04	12.05	12.04	12.04
Unity Gain BW	14.71M	>300k	3.28K	17.84M	14.25M	14.71M	15.2M	15.68M	3.285K	14.71M	17.84M	15.06M	11.59M	16.76M	14.66M
Common Mode Gain	-101.8	<-73	-109.5	-37.73	-104.7	-101.8	-104.7	-97.71	-37.73	-101.8	-93.68	-91.88	-96.24	-109.5	-103.1
Feedback Loop Gain	74.03	>75	63.03	75.94	73.84	74.03	74.22	74.39	63.03	74.03	71.91	73.12	75.94	73.58	74.23
Phase Margin	73.58	>60	67.87	74.89	74.15	73.58	72.85	72.29	67.87	73.58	74.1	74.17	72.11	74.89	71.72
PSRR	-73.9	<-65	-77.04	-8.038	-72.94	-73.9	-70.64	-75.08	-8.038	-73.9	-67.8	-67.07	-77.04	-74.16	-72.38
Slew Rate	9.799M	>4M	300.7	13.28M	9.28M	9.79M	10.28M	10.74M	300.7	9.79M	7.59M	7.52M	5.70M	13.28M	10.81M
THD	-36.28	<-77	-69.88	-4.175	-26.08	-36.28	-68.51	-61.83	-4.175	-36.28	-35.52	-37.05	-35.38	-37.03	-35.31

Since the checklist was signed improvements suggested were made, leading to reach closer to the desired specifications. Though some have continued to stay out the desired range but the difference between the desired and achieved has been greatly reduced.

# **Chapter 7: Conclusions**

## **7.1 Conclusions**

The Analog IC Design lab provided an invaluable opportunity in designing a Class AB Audio Amplifier having a gain of 12dB and a UGBW of 300KHz. The journey began with characterizing the transistors, followed by schematic design and pre-simulations to meet the specifications across all five process corners. The next phase involved meticulously drawing the layout while ensuring clear DRC and LVS checks. After completing layout, I performed Parasitic Extraction (PEX) to account for the parasitic elements introduced by the physical implementation. Subsequently, I conducted post-layout simulations to validate the amplifier's performance, incorporating the extracted parasitic components. I must admit that the entire process was challenging, but it provided me with a great insight and a solid foundation for working on analog projects.

Through this project, I gained a better understanding of the underlying concepts and practical design aspects. It was an interesting and enriching experience to work on the layout, as it was the first time I had the chance to undertake such a comprehensive project. Although I encountered some errors along the way, I learned invaluable lessons with the guidance and support of Prof. Siek and the teaching assistant Mr. Lim Wu Cong. I am truly grateful to Prof. Siek for his patience, expertise, and dedication in helping me understand where I went wrong, suggesting improvements, and guiding me through the process of enhancing my project. This experience has not only strengthened my knowledge but also instilled in me a deep appreciation for the complexities and intricacies involved in analog IC design.

## **7.2 Future Considerations**

### **7.2.1 Do's**

- Choose feedback resistors with sufficient resistance to minimize their influence on the output stage. This selection ensures the current driving the output has a negligible effect on the resistors themselves. Consequently, minimal voltage variations are introduced at the input terminals, reducing the likelihood of offset issues.
- The Biasing circuit resistors R1, R2, R3 are matched.
- Employ transistor multipliers strategically to achieve a balance between maintaining transistor saturation and ensuring adequate current flow through the MOS devices. This optimization ensures both proper transistor operation and sufficient current for optimal circuit performance.
- Position the amplifier's output voltage ( $V_{out}$ ) at a bias point around 0.8V. This allows the output signal to swing freely in both positive and negative directions.

- Design the PMOS transistor with a width approximately twice that of the NMOS transistor in the output stage. This sizing ratio ensures proper current matching between the PMOS and NMOS devices.
- Characterize the transistors properly enough and proceed to W calculations.
- Prioritize efficient layout design to minimize overall circuit area. Since area constraints are critical, optimizing the layout to achieve a compact footprint is crucial.
- Layout of both biasing and class AB should be done together to make use of the area in a better way. As placement and routing needs of both sections simultaneously. This can lead to a more compact and efficient overall layout.
- Minimize the use of unnecessary empty spaces (voids) within the layout. While some spacing is essential for component isolation and routing, excessive void areas can significantly increase the overall circuit footprint.
- Do routing such a way it is minimizing the overall length of metal routing paths, especially for polysilicon (poly) layers. Since poly has a significantly higher resistance compared to other metals.
- Incorporate multiple contacts whenever possible, especially between different metal layers (VIAs) and transistor diffusion areas. This approach reduces the overall resistance as they are in parallel.
- Maintain consistent wire width throughout the layout whenever possible. Avoid abrupt transitions from thicker to thinner wires during routing. These abrupt changes in width introduce discontinuities that can cause unwanted localized increases in resistance.
- Prioritize metal routing over polysilicon (poly) routing whenever possible. Due to the significantly higher resistance of poly compared to metal.
- Employ multiple contacts when stacking transistors . Position these contacts between individual transistors within the stack. This approach minimizes the impact of resistance-induced voltage drops (IR drops). By ensuring transistors connect to points with similar potentials, leading to uniform current distribution across all stacked devices. This allows them to fully utilize their effective width (W) for optimal circuit performance.
- Place guard rings around individual transistors. This ensures effective isolation of the transistor's body region (VSB) from the surrounding substrate. By maintaining the intended body bias voltage (VDD for PMOS, GND for NMOS), you minimize variations in the threshold voltage (VT). Consistent VT helps maintain the desired  $\Delta V$  and I of the transistors. This prevents the creation of unwanted positive feedback loops within the circuit.
- Contact should be put closer to the gate rather than farther.
- Layout of power transistors should be done properly.

### 7.2.2 Don'ts

- Don't design with feedback resistors that have very low resistance values. Low resistance can cause a substantial portion of the output current to flow through them. Altering the voltages at the input terminals, potentially creating unwanted offset voltages within the circuit.
- Don't use different resistance values of resistance for R1, R2 and R3 as they should be matched since the current flowing through them and the voltage drop across them are equal.
- Don't overly prioritize transistor saturation by using excessive multipliers. While saturation is important, excessively large multipliers can restrict current flow through the MOS devices. This current limitation can hinder the circuit's functionality.
- Don't set the amplifier's output voltage ( $V_{out}$ ) at an improper bias point. Especially one significantly different from 0.8 V in this case, can restrict the output signal's swing in both positive and negative directions. This limitation, can lead to clipping, can distort the amplified signal.
- Don't use arbitrary widths for the PMOS and NMOS transistors in a branch. Selecting random widths can lead to mismatched currents flowing through these devices. This mismatch can distort the output signal and hinder the amplifier's performance.
- Don't proceed with W calculations without proper transistor characterization.
- Don't neglect layout area optimization during the design process. Failing to prioritize area efficiency can lead to an unnecessarily large circuit footprint.
- Don't design the biasing circuit and Class AB amplifier layouts independently. Separate layouts might not effectively utilize the available space.
- Don't leave large pockets of unused space (voids) in the layout. Excessive void spaces contribute to layout inefficiency, especially with stringent area constraints.
- Don't neglect the impact of poly resistance during routing. Excessively long poly routing paths can introduce parasitic resistance.
- Don't rely solely on single contacts for connections. A single contact point introduces inherent resistance that can impede signal flow. Utilizing multiple contacts in parallel offers a lower overall resistance path, improving circuit efficiency.
- Don't employ abrupt changes in wire width during routing. Sudden transitions from thick to thin wires create impedance mismatches. These mismatches can lead to localized resistance variations, hindering optimal signal transmission.
- Don't overly rely on poly routing paths. The high resistance of poly can weaken signals as they travel through the circuit. Opt for metal routing whenever possible to maintain strong signal integrity and optimal circuit performance.
- Don't rely on a single contact point at the top of a stacked transistor configuration. This setup can create potential variations between transistors due to IR drops. Transistors closer to the contact will experience a higher voltage compared to those further away. This can lead to unequal current flow, where transistors closer to the contact receive more current and potentially don't utilize their full W effectively.

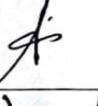
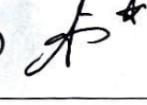
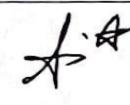
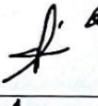
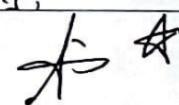
- Don't utilize a single, shared guard ring for multiple transistors. This configuration can lead to body bias variations (V<sub>SB</sub> not at zero for NMOS and V<sub>DD</sub> for PMOS) due to parasitic coupling between transistors. These variations can cause unintended changes in threshold voltage (V<sub>T</sub>), potentially affecting the  $\Delta V$  and drain current I of the transistors. In turn, this can create positive feedback loops that disrupt circuit performance.
- Don't Position gate contacts far away from the transistor gate.
- Don't Neglect layout of Power Transistor.

NM6007 Assignment: Class-AB Audio Amplifier

Personal Score Sheet

Name: P. VARUN SRINIVAS

Date: 12<sup>th</sup> March '24

Specification	Signature
<b>Closed Loop Gain</b> $11.4 - 12.6$	Min $12.04 (T, 60, 1.6)$ Max $12.96 (T, -40, 1.6)$ 
<b>Closed Loop Unity Gain Bandwidth</b> $> 300\text{K}$	Min $531.8 \text{ (T, -40, 1.6)}$ Max $7.515 \text{ M (T, 100, 1.6)}$ 
<b>Common-mode Gain</b> $< -73$	Min $-107.9 (\text{FS}, 60, 1.6)$ Max $-43.6 (T, -40, 1.6)$ 
<b>Feedback Loop Gain</b> $> 75$	Min $49.89 (T, -40, 1.6)$ Max $67.21 (\text{FS}, 60, 1.6)$ 
<b>Feedback Loop Phase Margin</b> $> 60$	Min $88.51 (\text{FS}, 60, 1.6)$ Max $89.47 (T, -40, 1.6)$ 
<b>Power Supply Rejection Ratio</b> $< -85$	Min $-77.11 (\text{FS}, 60, 1.6)$ Max $-80.78 (T, -40, 1.6)$ 
<b>Current Consumption</b>	$871.464 \mu\text{A}$ 
<b>Total Harmonic Distortion</b> $< -77$	Min $-69.77 (T, 60, 1.6)$ Max $-24.59 (T, 60, 1.5)$ 
<b>Settling Time</b> (Highest only $680 \text{ mV}$ )	$T_s = 172.39 \text{ ns}$ $T_s = 141.00 \text{ ns}$ 
<b>Slew Rate</b> $> 4\text{M}$	Min $7.951 \text{ M (\text{FS}, 60, 1.6)}$ Max $18.05 \text{ M (T, -40, 1.6)}$ $T_s = 13.764 \text{ V/ms}$ $T_s = 4.82 \text{ V/ms}$ 
<b>Chip Area</b>	$329 \times 256.21$ $\text{mm}^2$ 

  $-40^\circ\text{C}$  A(1) got problem (not meets spec)

Please scan a copy of this page which must be included in the appendix of the final report.