NTU-TUM MSc (IC Design) Programme
NM6008 - Digital IC Design

Consider a hypothetical processor that is designed to do arithmetic operation in a very humanistic manner. The special purpose processor carries out multiplication of two 3-digit numbers through the long multiplication process, just like a human doing manual multiplication on paper. An illustration of this multiplication process involving two operands A = 333 and B = 222 is as shown in Table 1. Do note that unlike multiplication on paper, here our accumulation step is done in stages rather than all at once.

A generic block architecture of the processor is as shown in Figure 1. The block architecture is intentionally general so that you will have the full flexibility to design your chip accordingly. Clearly, regardless of how you design your processor chip, the important point to note is that the functional objective of the chip is to calculate the results of AxB after being initiated by the *Start* input and upon completion, the *Ready* signal is asserted to indicate that the results is valid.

Table 1: Illustration of long multiplication process.

Operation	Value	Accumulated Sum
Load A	333	
Load B	222	
1st digit multiplication	666	666
2nd digit multiplication	666	7326
3rd digit multiplication	666	73926

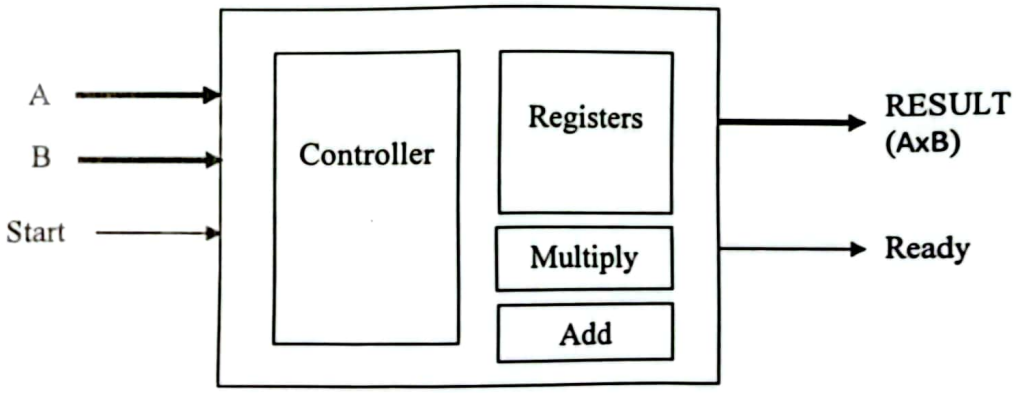

Fig 1: A generic block architecture of a 3-digit multiplier.

1. Your tasks in this exercise are as follow:
   a. Design the processor using HDL modeling.
   b. To write a test bench to simulate the multiplication function.
   c. Provide test bench that include simulation of sample inputs.
   d. State clearly your assumptions (if any) for your design.
   e. To synthesize the counter, providing a short summary of the synthesized circuit.

2. Compile a report of what you accomplished in this exercise. Among other things, your report submission should include the following.
   a. The printout of the HDL code for the counter.
   b. The printout of the test bench.
   c. The printout of the simulation waveform clearly indicating on the waveforms the validity of your simulation results.
   d. Block or functional flow diagrams to explain your approach.
   e. Written descriptions of your design methodology and testing approach.
   f. Any other points or analytical discussion.

Notes on Submission

All results or documents (except for parts 2d, 2e and 2f) should be submitted by emailing to emhlim.nm6008@gmail.com. The format for your submission is "pdf" format. It is much preferred that all files are combined as one pdf document rather than a collection of individual files when emailing your submission. DO NOT compress/zip the documents when emailing your submission. When emailing your submission, use your full name to name the file attachment.
Submission for parts 2d, 2e and 2f should be in handwritten or typewritten format. Physical printouts of these 3 parts are required. As a general guide, do not exceed 3 pages for the physical printouts.

Discussion Point (Optional)

Consider the processor you designed as a single core processing unit. You are now tasked with developing a massively parallel multi-core processor for the multiplication process. The idea is to be able to do multiplication involving a long string of numbers. Assuming that the size or area of the chip is not a primary concern, discuss and propose ideas on how you may go about achieving this assignment. If you attempt this part of the test assignment, you may email this as a separate pdf document. Name your file attachment as "your_full_name(optional)"

ALL submissions are due by 12.30pm, 7 October 2022 (Friday).