ADC SPI MASTER TIMING PARAMETER – SINGLE SLAVE

Parameters		**Required**	**Designed**
Conversion Time	**<=**	**12 CLK Cycles**	**12**
Analog Input Sample Time	**<=**	**1.5 CLK Cycles**	**1.5**
Throughput Rate	**<=**	**50 KSPS**	**50 KSPS**
Clock Frequency	**<=**	**1 MHz**	**50 KHz**
Clock High Time	**>=**	**250 ns**	**10,000 ns**
Clock Low Time	**>=**	**250 ns**	**10,000 ns**
CS Fall To First Rising CLK Edge	**>=**	**100 ns**	**20,000 ns**
Data Input Setup Time	**>=**	**50 ns**	**-**
Data Input Hold Time	**>=**	**50 ns**	**-**
CLK Fall To Output Data Valid	**<=**	**200 ns**	**-**
CLK Fall To Output Enable	**<=**	**200 ns**	**-**
CS Rise To Output Disable	**<=**	**200 ns**	**-**
CS Disable Time	**>=**	**500 ns**	**10,000 ns**