VLSI DESIGN

(ECE3006)

LAB RECORD

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Code: ECE3006

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Sem: Winter Inter Semester (Phase 1)

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Lab Record Link: github.com/varunram2001/VLSI-Design-Lab-Experiments

Experiment No. 1

Date: 27 Jan 2023

Output and transfer characteristics of n-channel MOSFET

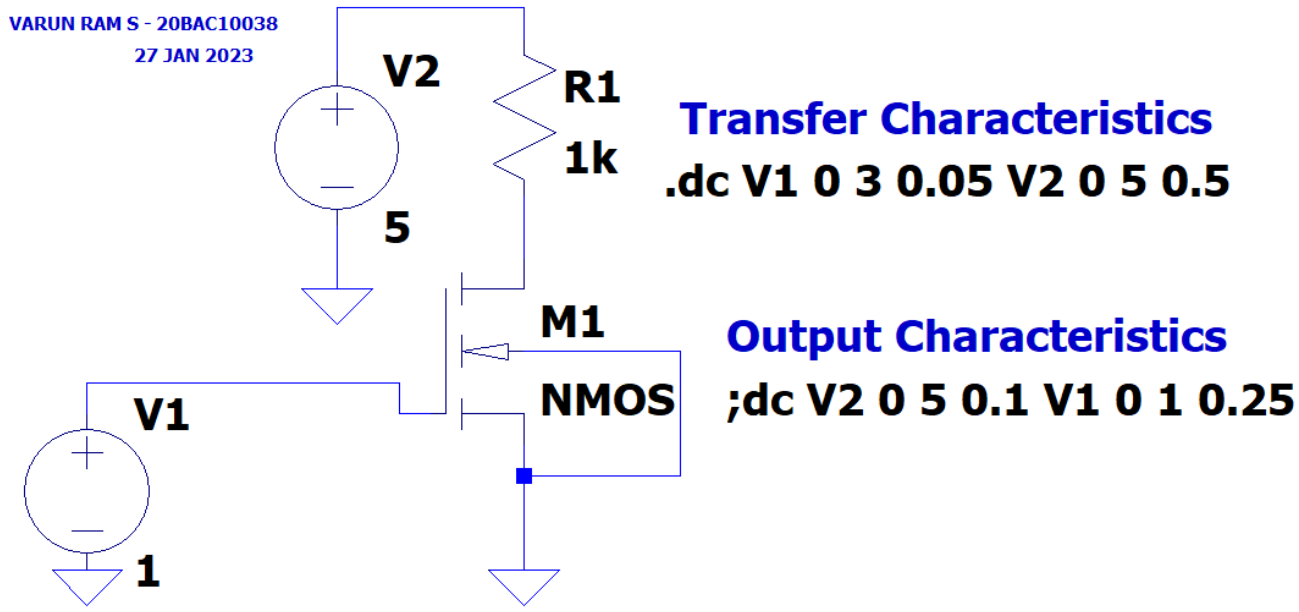
Aim:

This experiment aims to investigate the output and transfer characteristics of an n channel MOSFET.

Software Required:

LT Spice

Schematic:



Simulation Results:

Output Characteristics:

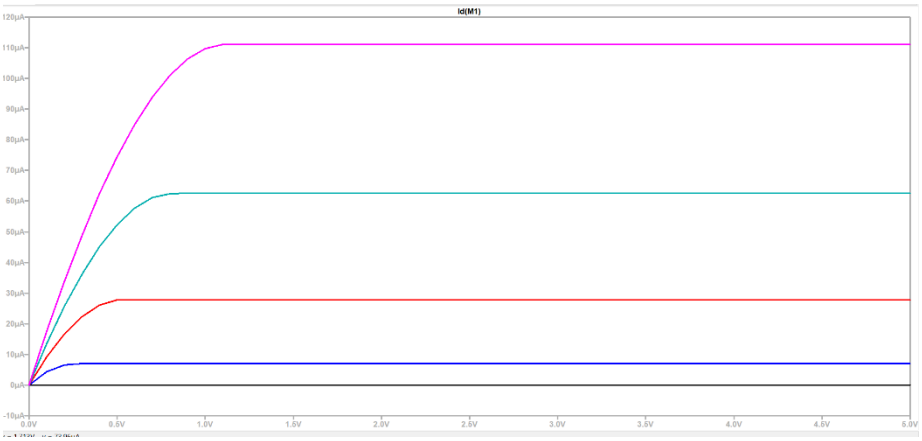


Fig: Output Characteristics (I_{ds} by V_{ds})

Transfer Characteristics:

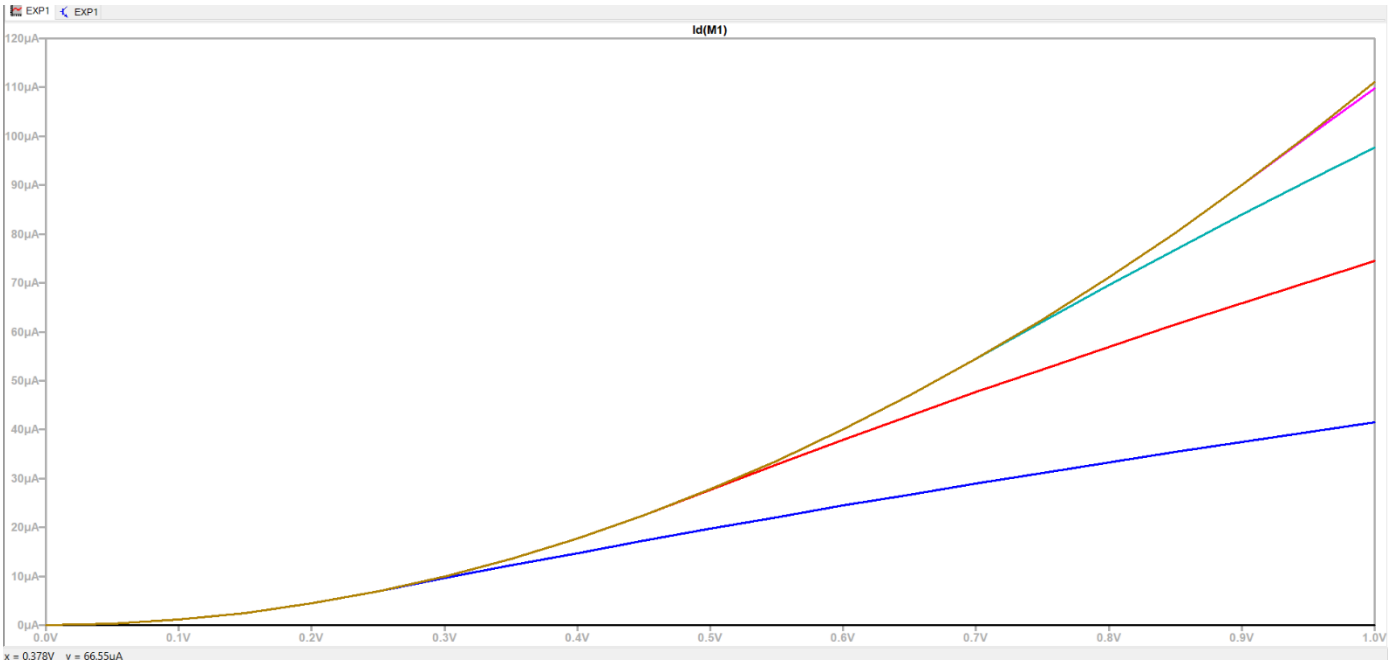


Fig: Transfer Characteristics (I_{ds} by V_{gs})

Observation:

Through this experiment, the basic understanding that MOSFET has three different regions is understood. They are:

1) Cut off Region
2) Linear Region
3) Saturation Region

We can also observe two differently shaped graphs for the Output and Transfer Characteristics.

Inference:

Some common inferences for the above observation can be:

1) MOSFET's behaviour depends upon the Gate-Source Voltage and above three regions defined are a direct consequence of this.
2) In the saturation region, the drain current is becoming close to constant and is kind of independent of the gate source voltage. This behaviour is similar to that of a Current Controlled Switch.
3) In the triode or linear region, drain current is kind of proportional to gate source voltage. Primary inference of this behaviour can be related to it being a Voltage Controlled Resistor.

Result:

The experiment has been carried out successfully.

Link: github.com/varunram2001/VLSI-Design-Lab-Experiments/tree/main/Lab%201%20-%20Output%20and%20Transfer%20Characteristics%20of%20an%20N%20channel%20MOSFET

Experiment No. 2

Date: 02 Feb 2023

Design a Simulation of CMOS Inverter Transfer Characteristics

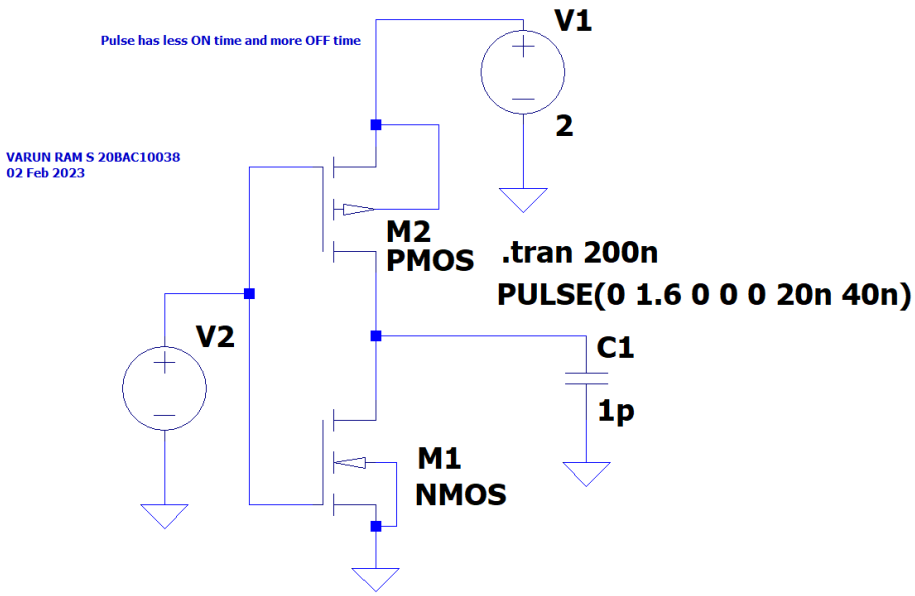
Aim:

This experiment aims to investigate the output and transfer characteristics of an n channel MOSFET.

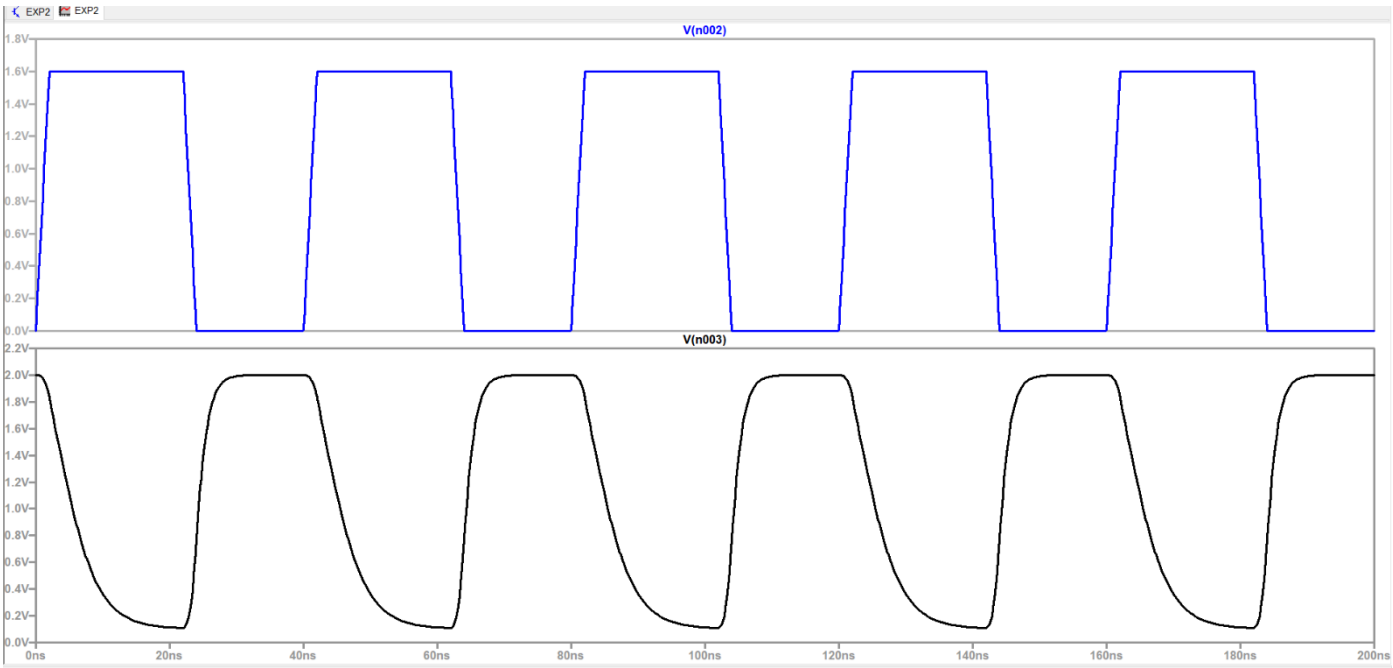
Software Required:

LT Spice

Schematic:



Simulation Results:



Observation:

1) The circuit has a PMOS and an NMOS.
2) When the input is high, NMOS is ON and PMOS shall be OFF. Vice versa trends for low input
3) The output is almost an inverted signal with a slight lag.

Inference:

Based on the above observations, the following inferences can be drawn:

1) CMOS has a lower power consumption. This is because when NMOS is ON and PMOS is OFF for the same signal, then power will be consumed only during the switching transitions and that is also pretty short.
2) Switching speed of this CMOS inverter is kind of relatively fast because they can switch quickly between ON and OFF states. There will be no current flow between ground and power supply during the switching transitions which is the reason for it being fast. This actually reduces switching delay.
3) We can also infer that the Output voltage swings between power supply voltage and ground by observing the symmetrical output.

Results:

The experiment has been carried out successfully.

Link: github.com/varunram2001/VLSI-Design-Lab-Experiments/tree/main/Lab%202%20-%20Simulation%20Design%20of%20CMOS%20Inverter%20Transfer%20Characteristics

Experiment No. 3

Date: 04 Feb 2023

Investigation of VTC Characteristics of a CMOS Inverter

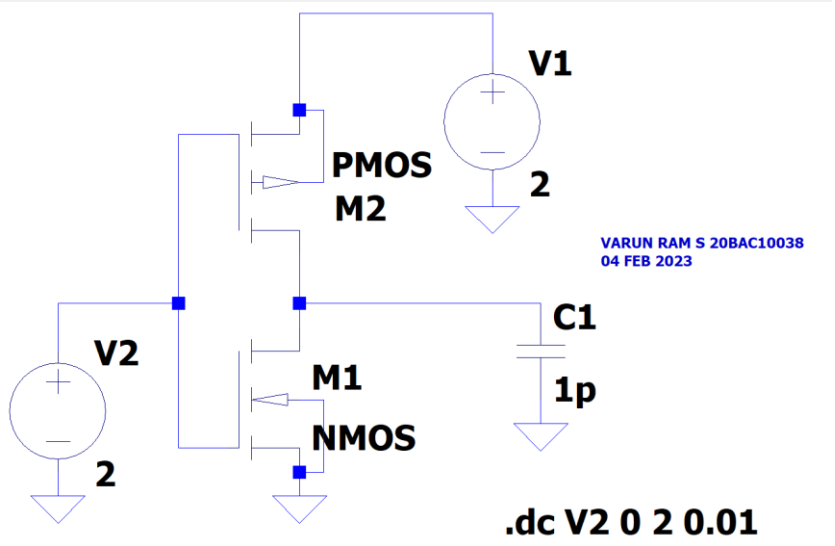
Aim:

This experiment aims to investigate the Voltage transfer characteristics of a CMOS Inverter.

Software Required:

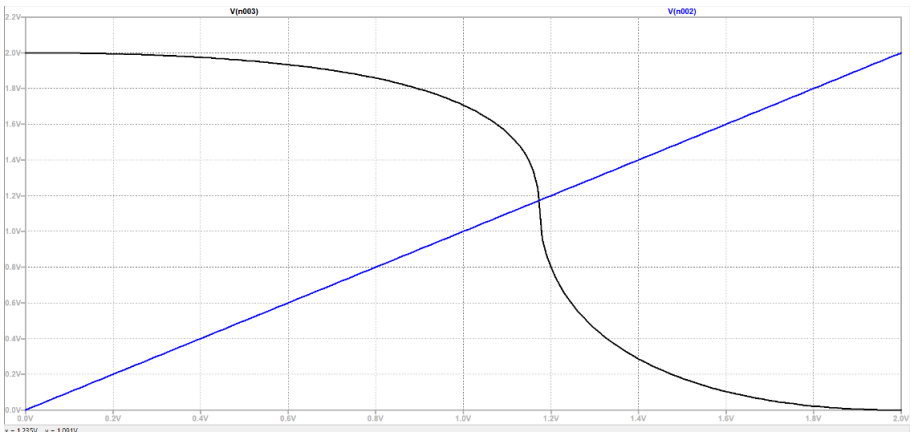
LT Spice

Schematic:

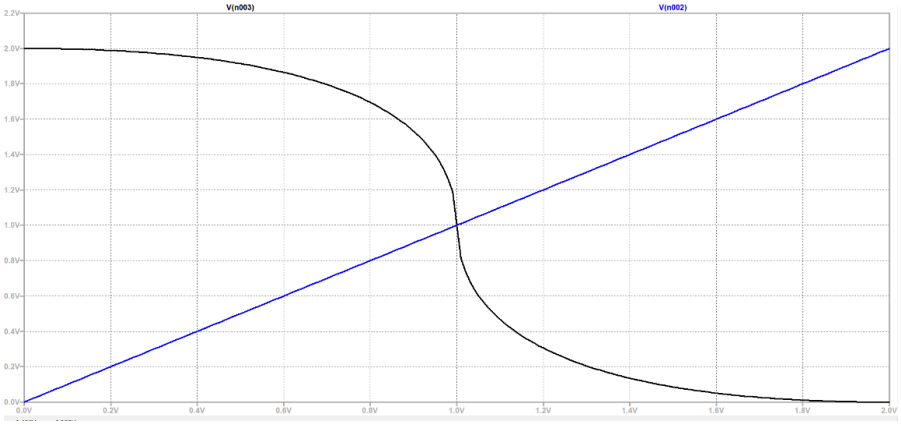


Simulation Results:

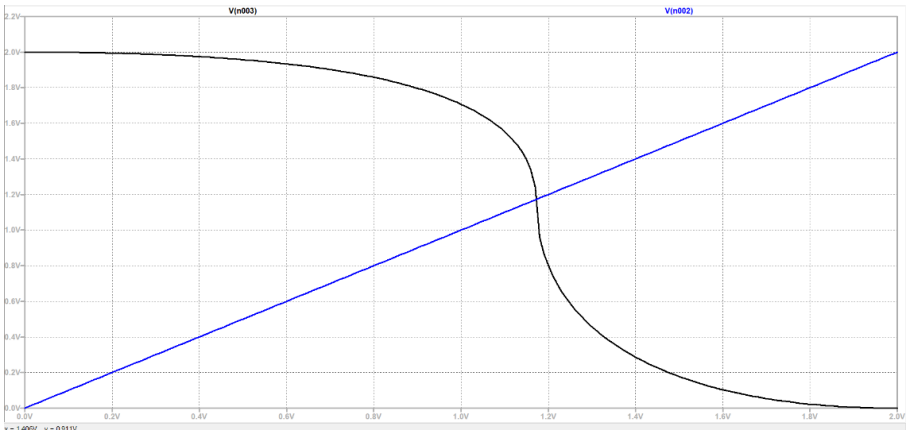
i) W_n=2u, W_p=4u, β= 2:1



ii) W_n=4u, W_p=4u, β= 1:1



iii) W_n=2u, W_p=4u, β= 3:1



Observation:

L=180nm

Observation No.	Wp	Wn	Beta Ratio	Vm
1	4u	2u	2	1.170V
2	4u	4u	1	1.000V
3	6u	2u	3	1.268V
4	8u	2u	4	1.333V

Inference:

1) If β is greater than 1 ie. If we keep increasing w_p, then the value of V_m keeps shifting to the right of the graph.

2) It is better to avoid β=2 should be avoided as the power dissipation is highest at this ratio. Basically this is the case where W_p=W_n

Results:

The experiment has been carried out successfully.

Link: github.com/varunram2001/VLSI-Design-Lab-Experiments/tree/main/Lab%203%20-%20VTC%20Characterstics%20of%20CMOS%20Inverter

Experiment No. 4

Date: 25 Feb 2023

Transient Response of CMOS Inverter and Ratioed Circuit (NMOS Load)

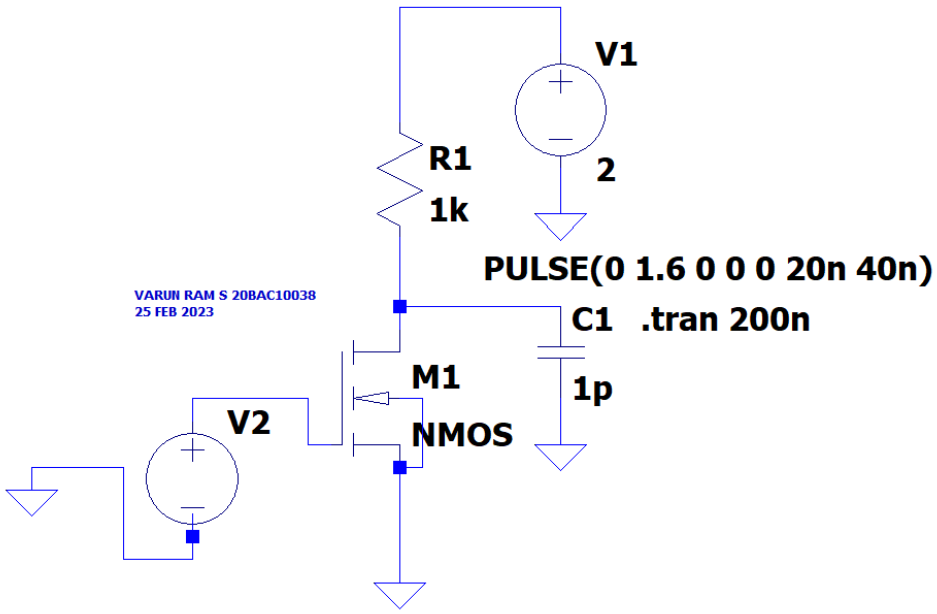
Aim:

This experiment aims to compare the transient response of a CMOS Inverter and a Ratioed Circuit with NMOS load.

Software Required:

LT Spice

Schematic:



Simulation Results:

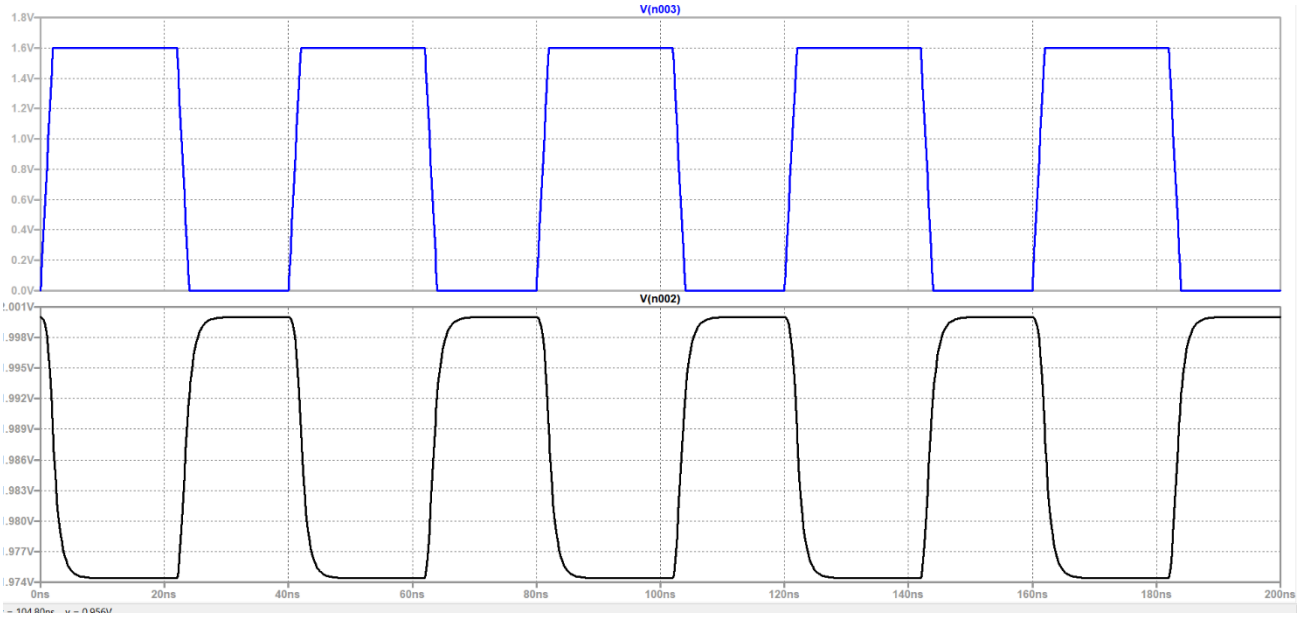


Fig: Simulation Results for the experiment

Observations:

- Max value: 2.00V
- Min value: 1.97V
- Pull Up Network has a resistor.
- Output is always connected to V_{DD}.

Inference:

Based on the observations, the following inferences can be drawn:

1) Output voltage swing of the circuit is likely to be larger than that of a non-ratioed circuit, as the load transistor's larger W/L ratio allows it to handle larger currents and produce a larger output voltage.
2) Improved performance in terms of gain and noise figure.
3) Reduced number of transistors as compared to traditional CMOS inverter.

Result:

The experiment has been carried out successfully

Link: github.com/varunram2001/VLSI-Design-Lab-Experiments/tree/main/Lab%204

Date: 25 Feb 2023

Experiment No. 5

Transient Response of CMOS Inverter and Ratioed Circuit (PMOS Load)

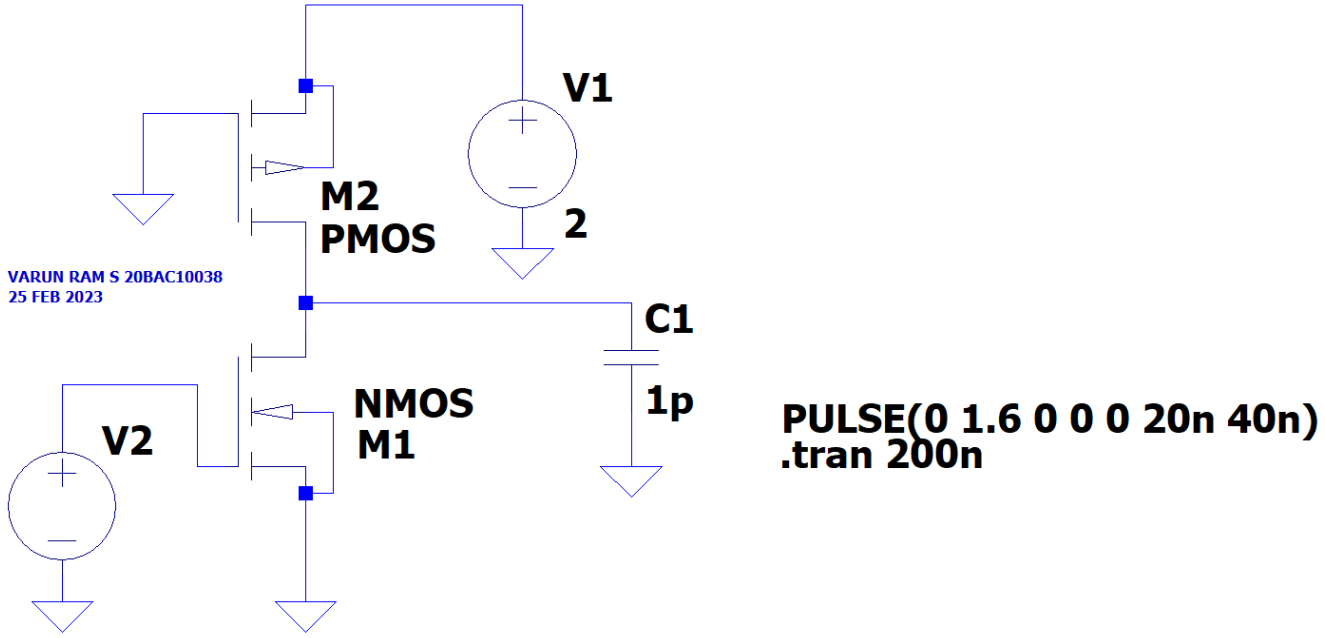
Aim:

This experiment aims to investigate the output and transfer characteristics of an n channel MOSFET.

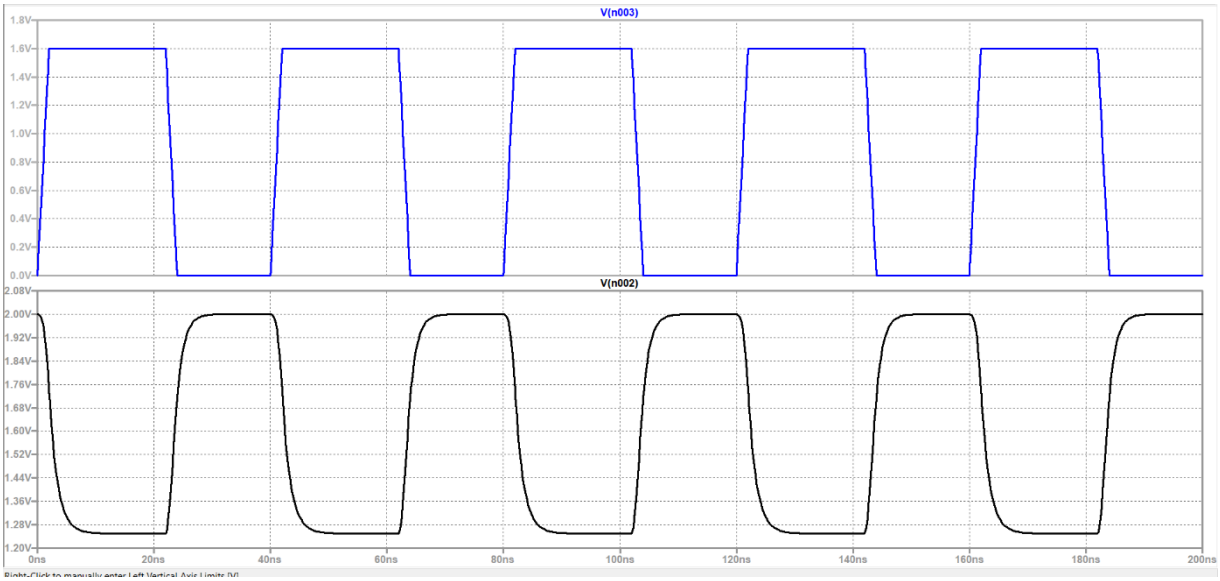
Software Required:

LT Spice

Schematic:



Simulation Results:



Observation:

- Max value:2.00V
- Min value:1.97V
- Pull up network has a grounded PMOS.
- Output is always connected to V_{DD} in the circuit.

Inference:

1) Lower number of transistors compared to the traditional CMOS inverter.
2) Lower power consumption leads to Slightly better efficiency compared to non-ratioed CMOS inverter.

Result:

The experiment has been carried out successfully

Link: github.com/varunram2001/VLSI-Design-Lab-Experiments/tree/main/Lab%205

Experiment No. 6

Date: 10 Mar 2023

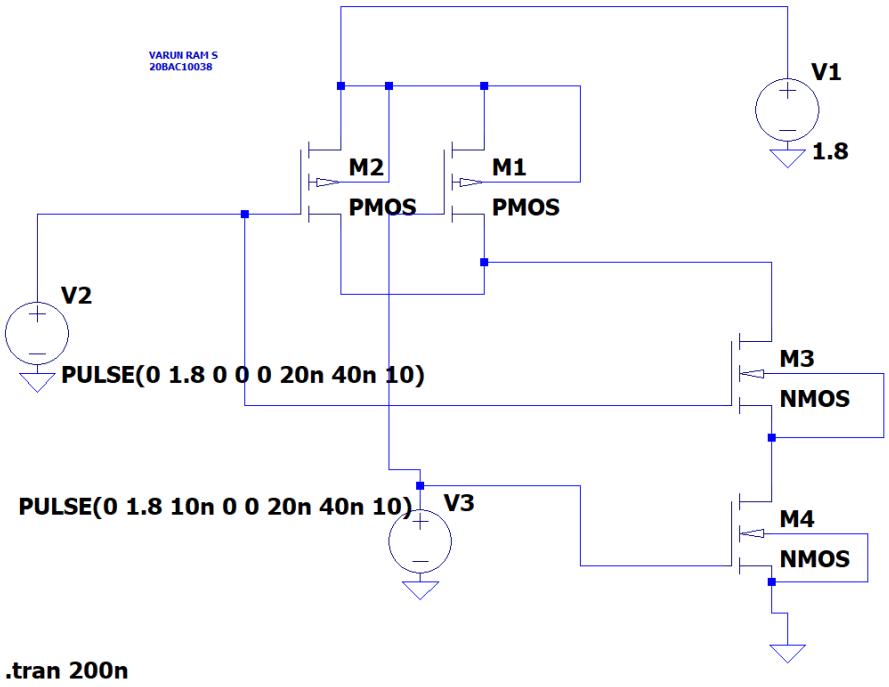
Functionality of a 2 input NAND Gate

Aim: This experiment aims to investigate the functionality of a 2 input NAND Gate.

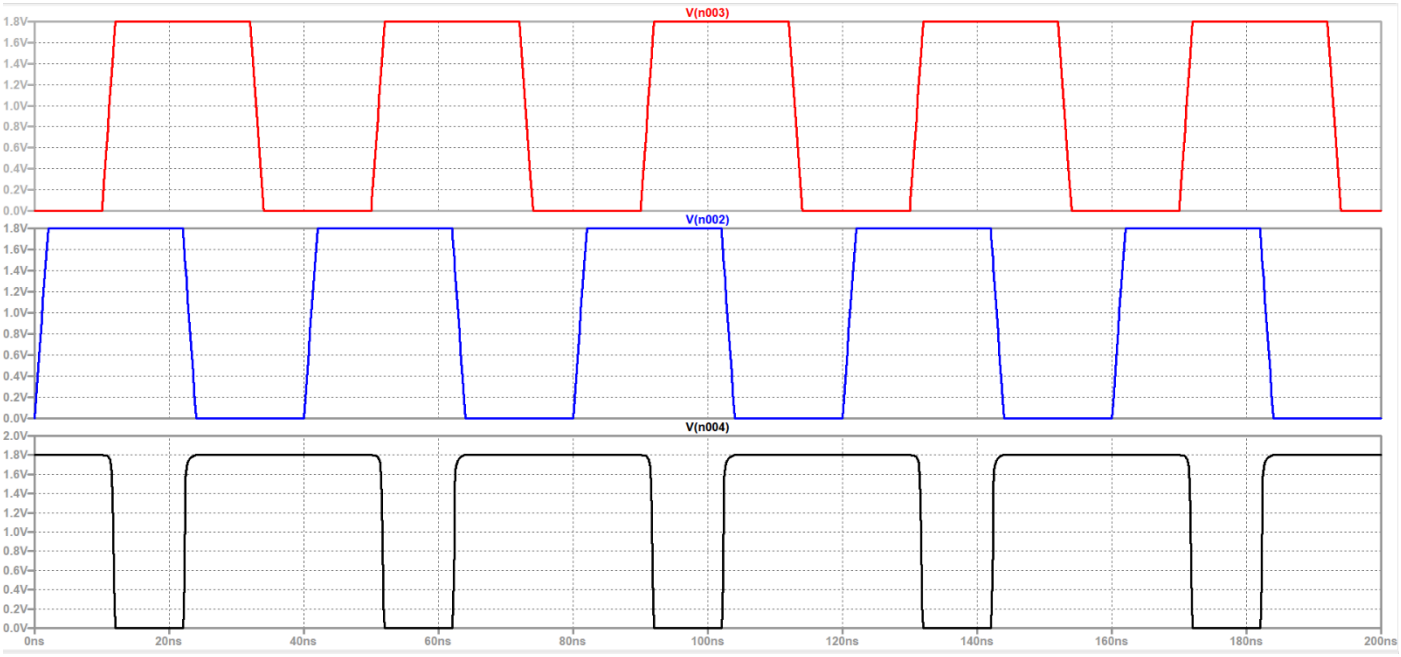
Software Required:

LT Spice

Schematic:



Simulation Results:



Observation:

Case number	A	B	Output
1	0	0	1
2	0	1	0
3	1	0	0
4	1	1	0

Inference:

Based on the above observations, the following inferences can be drawn:

1) NMOS when connected in series can be equivalent to multiplication and same is the case for PMOS in parallel.
2) When A and B are both logic 1, both NMOS transistors are ON, this creates a low resistance path from the output to ground. This results in a logic 0 output.

Result:

The experiment has been carried out successfully

Link: github.com/varunram2001/VLSI-Design-Lab-Experiments/tree/main/Lab%206%20-%20Functionality%20of%20a%202%20input%20%20NAND%20gate

Experiment No. 7

Date: 10 Mar 2023

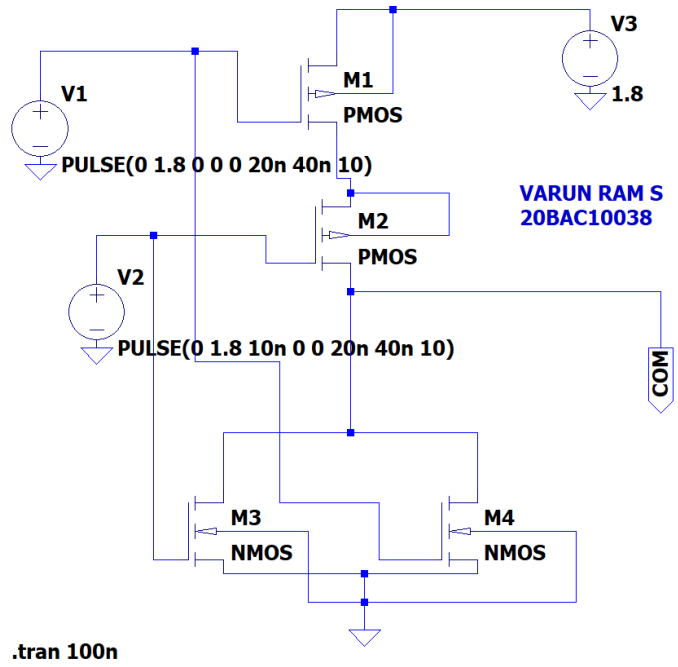
Functionality of a 2 input NOR Gate

Aim: This experiment aims to investigate the functionality of a 2 input NAND Gate.

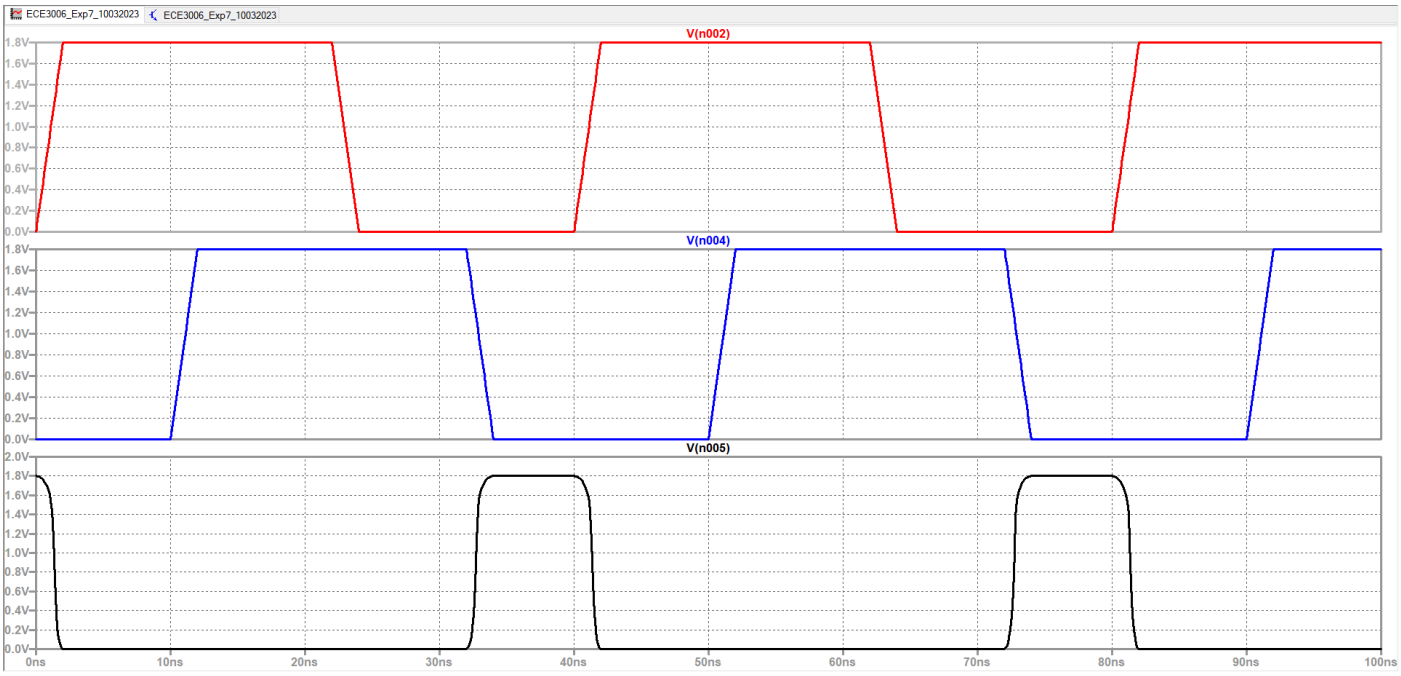
Software Required:

LT Spice

Schematic:



Simulation Results:



Observation:

Case number	A	B	Output
1	0	0	1
2	0	1	1
3	1	0	1
4	1	1	0

Inference:

Based on the above observations, the following inferences can be drawn:

1) NMOS when connected in parallel can be equivalent to an addition and same is the case for PMOS in series.
2) The delay in output for the given inputs is pretty large.
3) When either A or B is logic 1, the corresponding transistor is turned off, and this creating a high resistance path from the output Y to VDD. This results in a logic 0 output.

Result:

The experiment has been carried out successfully

Link: github.com/varunram2001/VLSI-Design-Lab-Experiments/tree/main/Lab%207%20-%20Functionality%20of%20a%202%20input%20NOR%20Gate