



Gowin DDS IP

User Guide

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Revision History

Date	Version	Description
06/30/2020	1.0E	Initial version published.
02/01/2021	1.1E	Descriptions of chapter 4 Functional Description updated.
08/19/2022	1.2E	<ul style="list-style-type: none">● Triangle and square waveforms added.● Taylor correction added.
12/20/2022	1.3E	Descriptions of chapter 4 Functional Description updated.
10/17/2025	1.3.1E	<ul style="list-style-type: none">● Section 1.2 Related Documents updated.● The formula for calculating the frequency of sine and triangle waveforms modified in section 4.1 The Structure and Function of Gowin DDS IP.

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1 About This Guide

1.1 Purpose

Gowin DDS IP User Guide mainly includes the descriptions of the functions features, ports, timing, configuration call, and reference design, etc. It mainly helps you quickly understand the characteristics, and usage of Gowin DDS IP.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X &9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DDS	Direct Digital Frequency Synthesizer
DSP	Digital Signal Processing
IP	Intellectual Property
LUT	Look-up Table
RAM	Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin DDS IP is a direct digital frequency synthesizer that enables direct synthesis of the expected sinusoidal waveform from the phase concept. The IP can be configured with multiple independent time-division multiplexed channels, output data bit width, frequency, and phase offsets, thus providing flexibility and ease of use.

Table 2-1 Gowin DDS IP Overview

Gowin DDS IP	
Logic Resource	Please refer to Table 3-1
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.6Beta and above)

Note!

For the devices supported, you can click [here](#) to get the information.

3 Features and Performance

3.1 Features

- Number of configurable output channels (1 to 16 channels)
- Configurable output phase offset
- Configurable output waveform phase increment
- Configurable look-up table depth (2^4 - 2^{16})
- Dynamically configures output phase and frequency
- Support sine, triangle, sawtooth, pulse square, and custom waveforms

3.2 System Clock Frequency

The maximum system clock frequency of Gowin DDS IP is primarily determined by the device used and speed grade thereof. Take the Gowin GW2A-LV18 series of FPGA for an instance. The system clock frequency reaches up to 175MHz.

3.3 Latency

The latency of Gowin DDS IP is determined by the configuration parameters.

$T_D = T_{clk} * (6 + \text{Channel_Num})$, where TD is the delay clock, Tclk is the system clock, and Channel_Num is the number of channels.

3.4 Resource Utilization

Gowin DDS IP can be implemented by Verilog language. Its performance and resource utilization may vary when the design is employed in different devices, or at different density, speed, grade or the different modes of IP configuration.

Taking Gowin GW2A-18 series of FPGA for an instance, the resource utilization of Gowin DDS IP in single-channel mode is shown in Table 3-1. For application verification on other Gowin FPGA, please pay attention to the later release information.

Table 3-1 Gowin DDS IP Resource Utilization

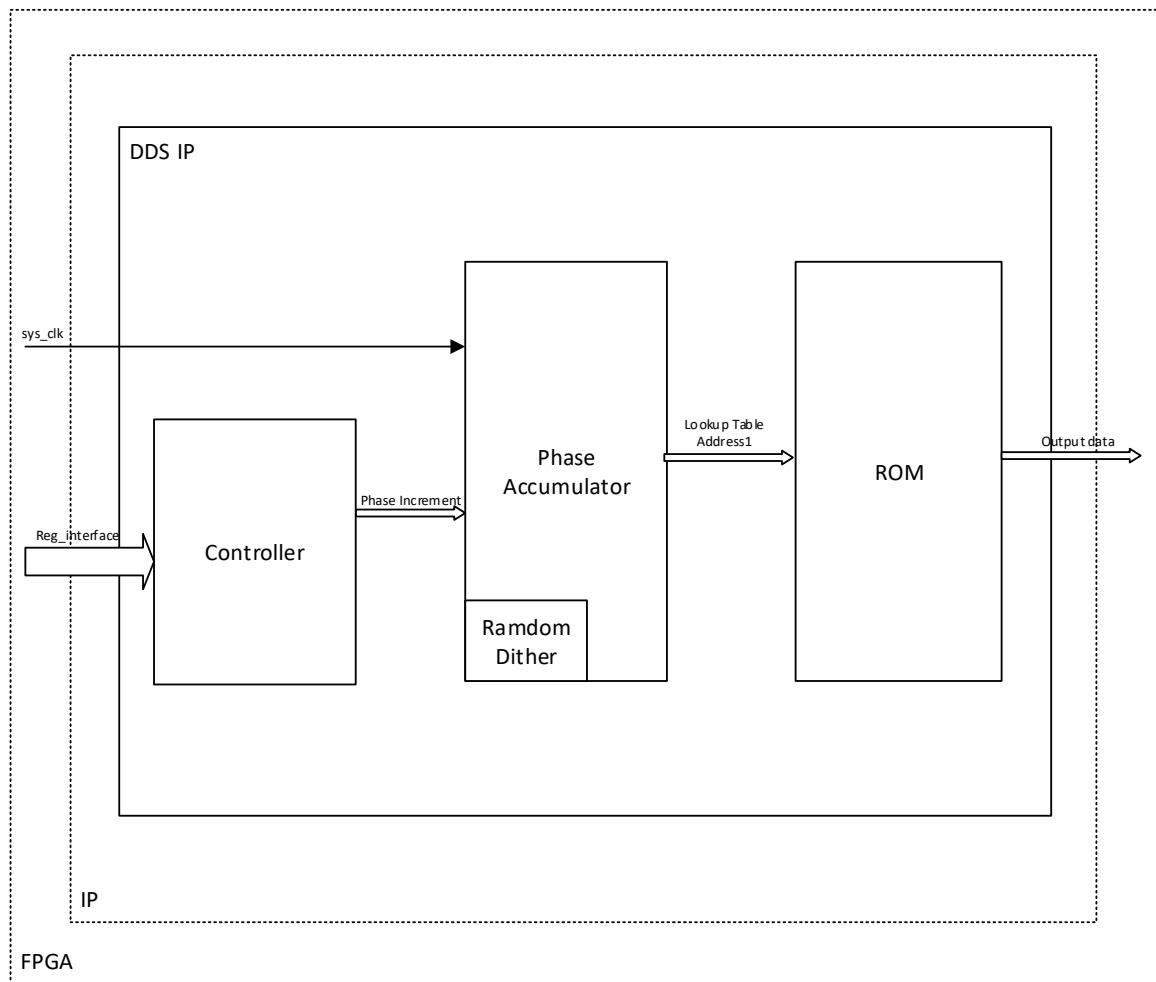
Device Series	Speed Grade	Name	Resource Utilization	Notes
GW2A-18	-7	LUT	58	-
		ALU	32	
		REG	133	
		BSRAM	2	
		DSP	0	
		PLL	0	

4 Functional Description

4.1 The Structure and Function of Gowin DDS IP

Gowin DDS IP is mainly composed of controller, phase generator, and memory, as shown in Figure 4-1.

Figure 4-1 DDS IP Implementation Block Diagram



The basic principle of Gowin DDS IP is as follows: under the control of the system clock, the internal phase generator generates a continuous uniform phase according to the selected phase increment, and then reads the LUT according to the generated phase and outputs the values corresponding to the phase to obtain the waveform with fixed frequency.

By providing the CLK clock signal and configuring the corresponding parameters, you can make Gowin DDS IP output a wave signal with a certain frequency. Different waveforms have different calculation formulas.

The formula for calculating the frequency of sine and triangle waveforms is:

$$f_{out} = \frac{f_{clk} \times PINC}{2^{(Pw+1)}}$$

f_{out} is the frequency which outputs sine waveform; f_{clk} is the system clock frequency; PINC is the phase increment; and Pw is the sum of LUT depth and truncation width. PINC and Pw can be freely adjusted through the configuration options Phase Increment and Lookup Table Depth.

Pw determines the minimum phase resolution. The larger the value is, the higher the phase resolution the system can achieve and the better the quality of the waveform is. PINC determines the actual phase increment, which represents the multiple each output value spans the minimum phase increment. And increasing this value results in outputting a higher wave frequency with a reduced quality.

When DDS is configured to $f_{clk} = 100 \times 10^6 \text{Hz}$, Lookup Table Depth=12, Truncation Width=4, Pw= 16, PINC= 4, then:

$$\begin{aligned} f_{out} &= \frac{f_{clk} \times PINC}{2^{(Pw+1)}} \\ &= \frac{100 \times 10^6 \times 4}{2^{17}} \\ &= 3051.76 \text{Hz} \end{aligned}$$

For multi-channel configuration, the output signal frequency is reduced to 1/C times the original. (C is the number of channels)

$$f_{out} = \frac{f_{clk} \times PINC}{2^{(Pw+1)}C}$$

When DDS is configured to $f_{clk} = 100 \times 10^6 \text{Hz}$, C=4, Lookup Table Depth=12, Truncation Width=4, Pw= 16, PINC= 4, then:

$$\begin{aligned}
 f_{out} &= \frac{f_{clk} \times PINC}{2^{(Pw+1)}} \\
 &= \frac{100 \times 10^6 \times 4}{2^{17} \times 4} \\
 &= 762.94\text{Hz}
 \end{aligned}$$

The frequency of the user-defined waveform is calculated as:

$$f_{out} = \frac{f_{clk} \times PINC}{Modulus}$$

The Modulus here is the user-defined modulus.

4.2 Gowin DDS IP Control Register Description

You can reconfigure the phase offset and phase increment by means of controlling word writes, as well as turning channels on and off.

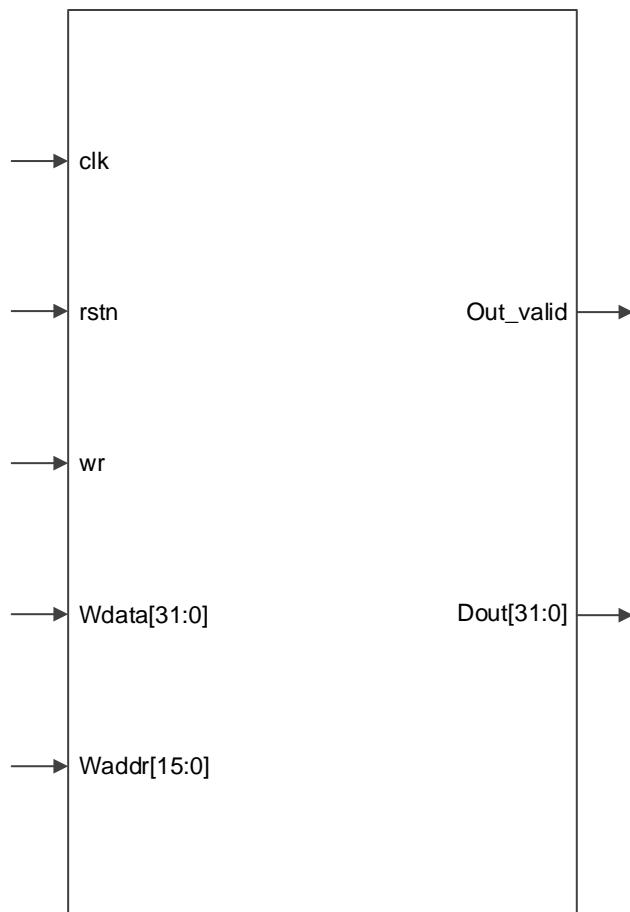
Table 4-1 Gowin DDS IP Control Register

Register	Address	Bit Width	Description
Waveforms	0x10	[3: 0]	4'b0000 --- Sin/Cos waveforms 4'b0001 --- Triangle waveforms 4'b0010 --- Sawtooth waveforms 4'b0011 --- Square/Square with duty waveforms 4'b0100 --- User Defined waveforms
POFF	0x20	[31:0]	Phase offset register, used for writing phase offset.
PINC	0x30	[31:0]	Phase incremental register, used for writing phase increment.
Square Duty	0x40	[31:0]	Square wave weight control register, used for writing square wave weight. The range is 0~2^(Pw+1). 0 is all-1. 1 is the pulse waveform. 2^(Pw)-1 is the square waveform. 2^(Pw+1) and outside the range are all 1. Pw=Lookup Table Depth + Truncation Width
CHN	0x50	[15:0]	Channel controller register, used to select the channels that need to change phase increments or offsets. For instance, if you write 4'b0100 to 0x0050 in 4-channel mode, the phase offset or phase increment of channel 2 can be configured dynamically, and the other channels remain unchanged.

5 Port Description

The IO port of Gowin DDS IP is shown in Figure 5-1.

Figure 5-1 Gowin DDS IP Port Diagram



For Gowin DDS IP IO port descriptions, you can see Table 5-1.

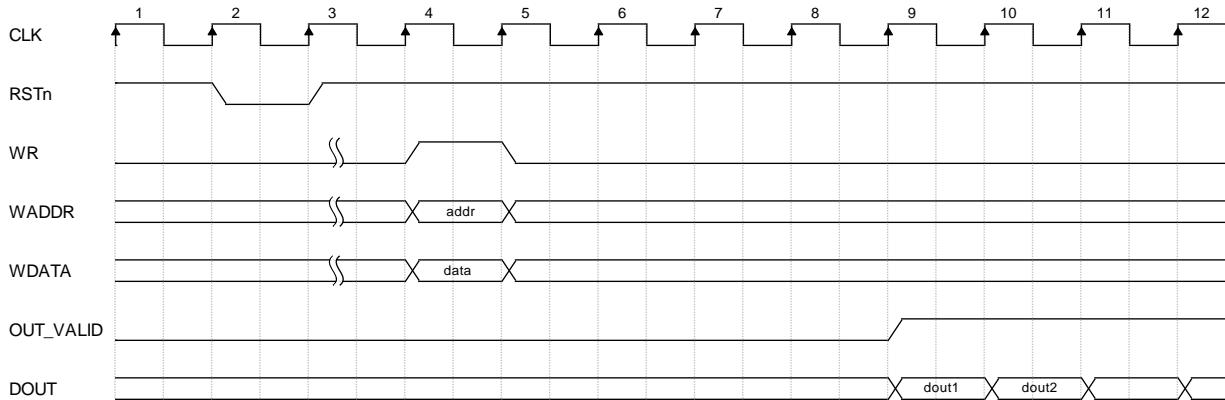
Table 5-1 List of Gowin DDS IP IO Ports

Signal	I/O	Description
clk	I	Clock signal
rstn	I	Reset signal, active-low.
wr	I	Write Enable Signal
wdata	I	Input data
waddr	I	Input address
out_valid	O	Output valid signal
dout	O	Output data

6 Timing Description

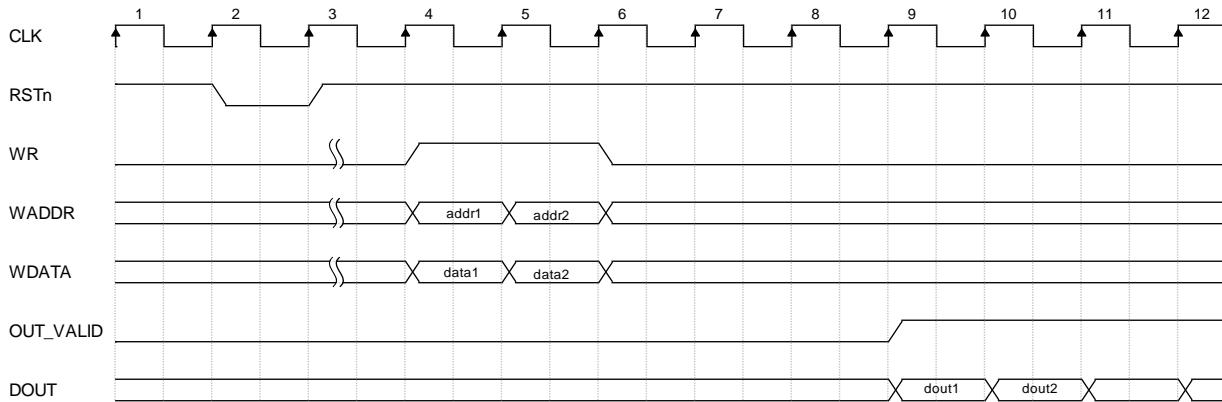
This chapter describes Gowin DDS IP timing. The timing diagram of Gowin DDS IP data write is shown in Figure 6-1.

Figure 6-1 Timing Diagram of Gowin DDS IP Data Write (Single-channel)



In single-channel mode, data can be output directly through IP configuration without writing control words; or phase increment and phase offset can be changed by writing data through register interface (WR, WADDR, WDATA).

The WR signal needs to be pulled up when writing data, and pulled down when writing completed.

Figure 6-2 Timing Diagram of Gowin DDS IP Data Write (Multi-channel)

In multi-channel mode, phase increments and phase offsets must be changed by writing data through the register interfaces (WR, WADDR, WDATA).

1. The WR signal needs to be pulled up when writing data, and pulled down when writing completed.
2. After power-on reset, it is necessary to write data to address 0x50, select a channel, and then configure the channel phase. For instance, if the phase increment of channel 2 is set to 8, 4'b0100 should be written to address 0x50, and then 16'h0008 should be written to address 0x30.
3. The data output adopts time-sharing multiplexing to output data 1 of channel 0, data 1 of channel 1, data 1 of channel 2... data n of channel 0, data n of channel 1, data n of channel 2....

7 Call & Configuration

Start "IP Core Generator" from the "Tools" menu in Gowin Software and then call and configure DDS IP.

Figure 7-1 Open the IP Configuration Interface Via Toolbar Icon

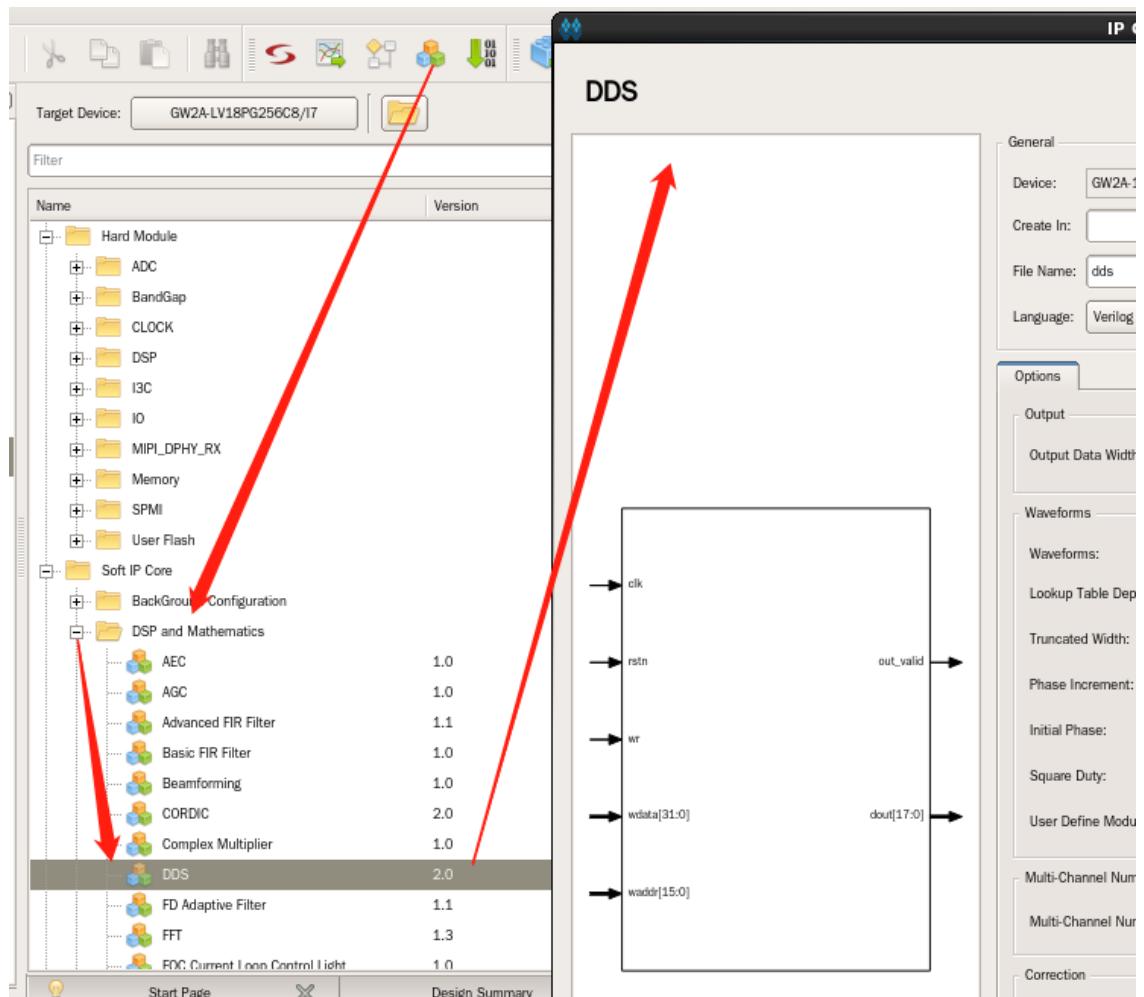
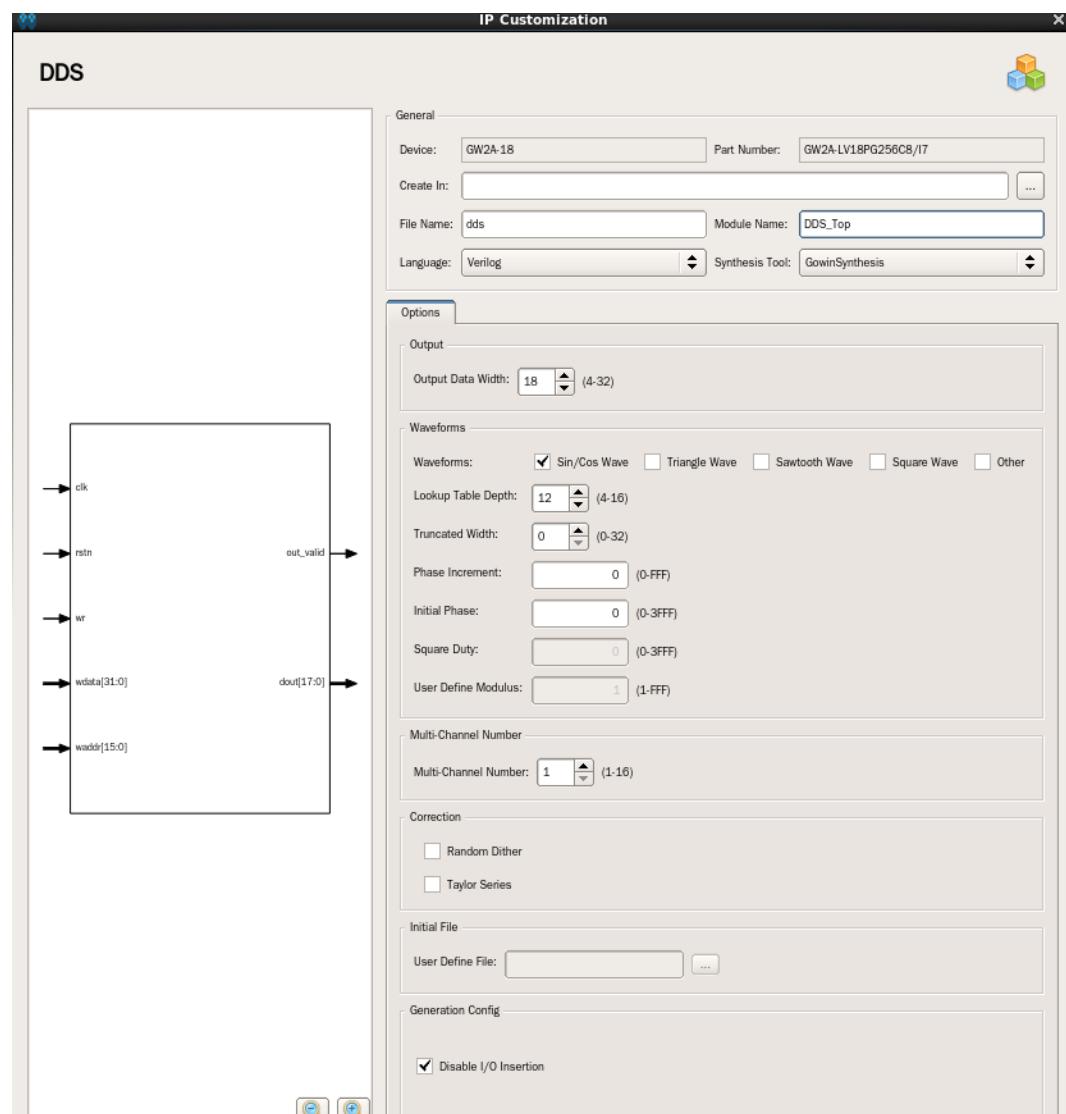


Figure 7-2 DDS IP Configuration

1. You can configure the generated file name by modifying the "File Name" text box.
 2. You can configure the module name by modifying the "Module Name" text box.
 3. You can configure IP working mode and other options by "Options".
- The configuration options of Gowin DDS IP are shown in Table 7-1.

Table 7-1 Gowin DDS IP Configuration Options

Option	Description
Output Data Width	Output data width, 4~32 bits.
Waveform	Sine, triangle, sawtooth, pulse square or custom waveform.
Lookup Table Depth	Look-up table depth, 4-16 bits.
Truncated Width	Truncated width, 0-32 bits.
Phase Increment	Phase increment, maximum configurable range determined by look-up table depth and truncated width.
Initial Phase	Initial phase, maximum configurable range determined by look-up table depth and truncated width.
Square Duty	Square wave weight, maximum configurable range determined by look-up table depth and truncated width.
User Define Modulus	User-defined waveform modulus, maximum configurable range determined by look-up table depth.
Multi-Channel Number	The number of channels, 1~16.
Random Dither	Random dither
Taylor Series	Taylor series
User Define File	User-defined wave file loading

8 Reference Design

This chapter focuses on the usage and structure of the reference design instance of Gowin DDS IP. The DDS design example has only one module. Please refer to Gowin DDS IP [reference design](#) for details.

In the design instance, the steps are as follows:

1. Generate Gowin DDS IP after selecting the appropriate configuration options.
2. The output is calculated by Gowin DDS IP and compared to the simulation data.

Application

Gowin DDS IP functions can be verified quickly using this design example. When the reference design is applied to board level test, the users need to provide appropriate incentive to the reference design and use an on-line logic analyzer or oscilloscope to observe the signals.

