**Title**: *Design and Implementation of a Traffic Light Controller using Finite State Machine (FSM) in Verilog HDL*

**Abstract**:  
Traffic management is one of the key challenges in urban areas. Traffic light controllers play a vital role in ensuring smooth flow of vehicles and reducing congestion at road intersections. In this project, a Traffic Light Controller is designed and implemented using a Finite State Machine (FSM) approach in Verilog HDL.

The controller operates with three states: **Green**, **Yellow**, and **Red**, which transition sequentially based on a clock-driven counter. The design models a simple two-way intersection where each road is given a specific time duration for green, yellow, and red signals. The FSM ensures safe transitions by preventing conflicting green lights.

The Verilog RTL design is simulated using ModelSim/Vivado to verify functional correctness. Further, the design is synthesized and implemented on an FPGA using the Xilinx Vivado tool, generating timing and power analysis reports. This project demonstrates how FSM-based digital design principles can be applied to real-world traffic control systems with possibilities of extension to pedestrian signals, adaptive timers, or multi-way intersections.

**Keywords**: Traffic Light Controller, FSM, Verilog HDL, FPGA, Synthesis, Timing Analysis, Power Analysis.