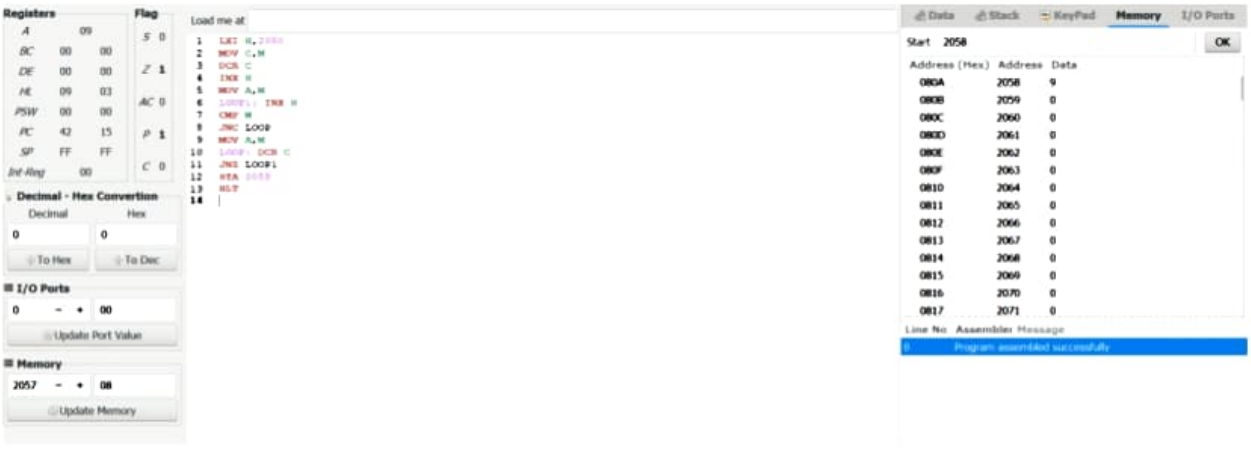
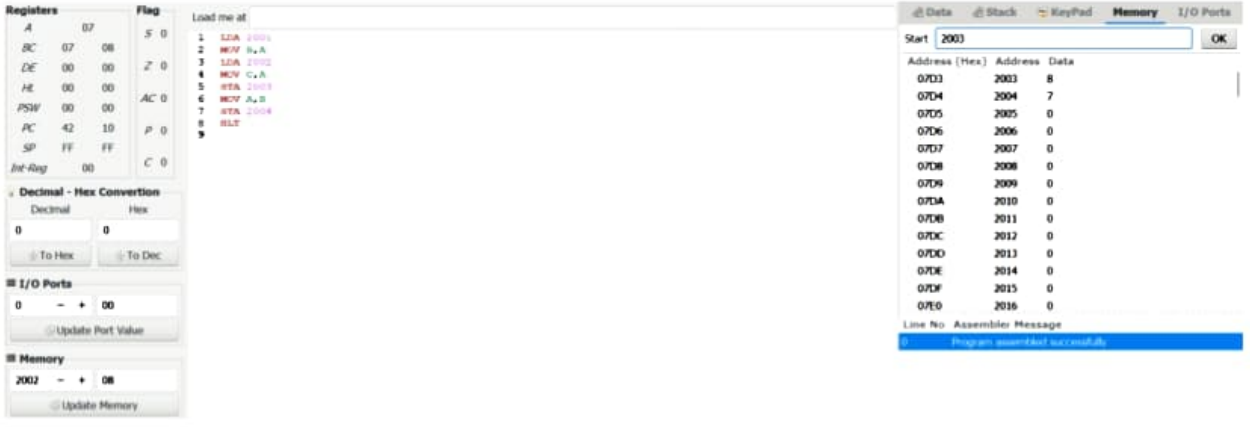
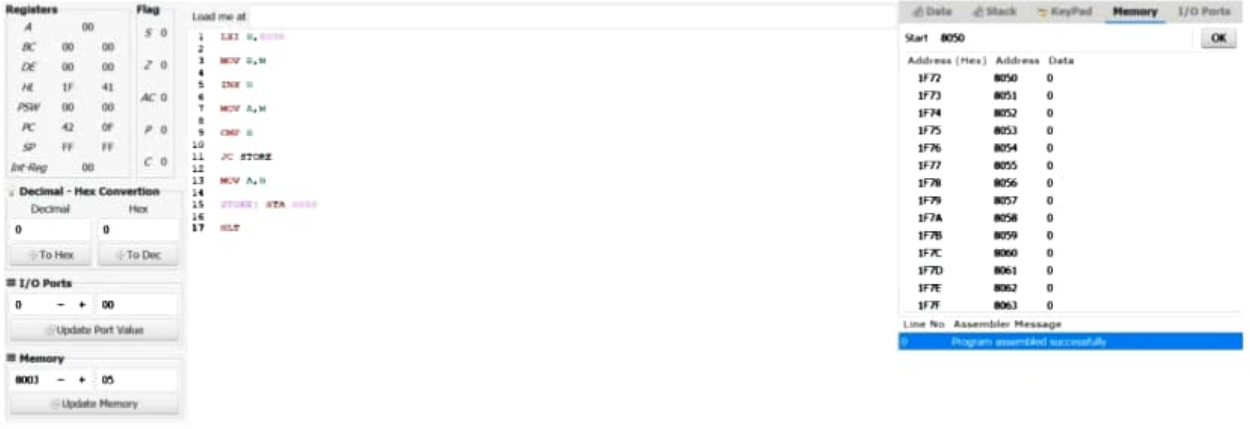
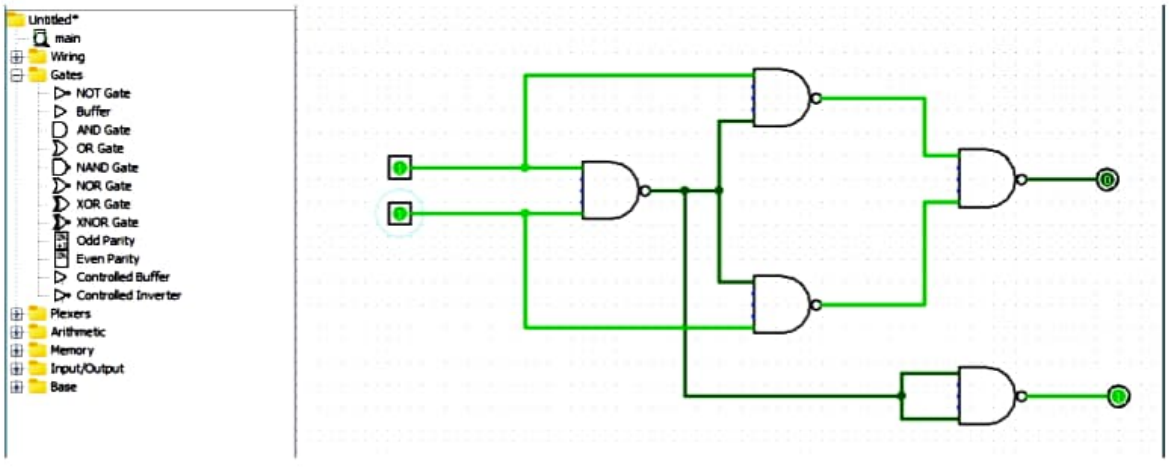
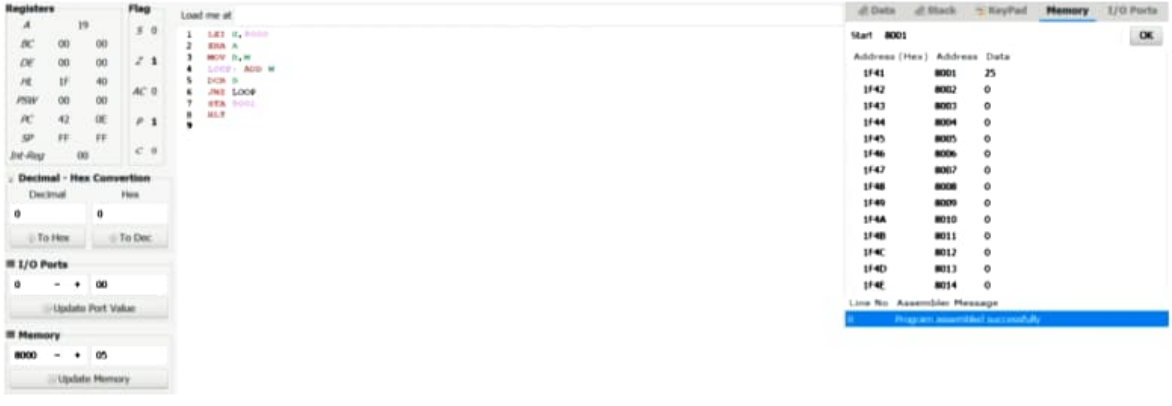
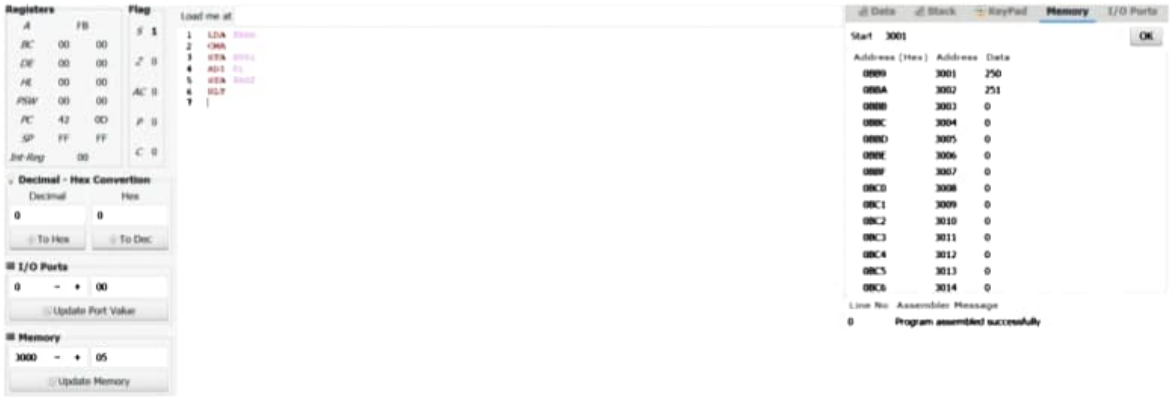

Registers
Flag
A 09
BC 00 00
DE 00 00
HL 09 03
PSW 00 00
PC 42 15
SP FF FF
Int-Reg 00
S 0
Z 1
AC 0
P 1
C 0
Decimal - Hex Convertion
Decimal
Hex
0
0
To Hex
To Dec
I/O Ports
0 - + 00
Update Port Value
Memory
2057 - + 08
Update Memory
Load me at
1 LXI H,2058
2 MOV C,M
3 DCR C
4 INX H
5 MOV A,M
6 LOOP: INR M
7 CMP M
8 JNC LOOP
9 MOV A,M
10 LOOP: DCR C
11 JNZ LOOP1
12 STA 3050
13 HLT
14
Data
Stack
KeyPad
Memory
I/O Ports
Start 2058
OK
Address (Hex) Address Data
080A 2058 9
080B 2059 0
080C 2060 0
080D 2061 0
080E 2062 0
080F 2063 0
0810 2064 0
0811 2065 0
0812 2066 0
0813 2067 0
0814 2068 0
0815 2069 0
0816 2070 0
0817 2071 0
Line No Assembler Message
0 Program assembled successfully

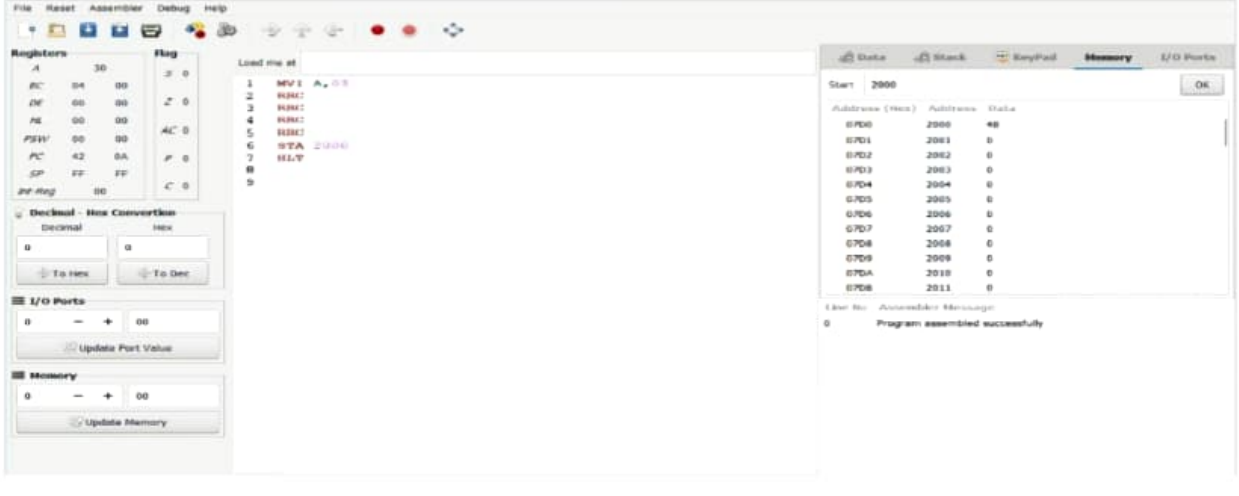

Registers
Flag
A 07
BC 07 08
DE 00 00
HL 00 00
PSW 00 00
PC 42 10
SP FF FF
Int-Reg 00
S 0
Z 0
AC 0
P 0
C 0
Decimal - Hex Convertion
Decimal
Hex
0
0
To Hex
To Dec
I/O Ports
0 - + 00
Update Port Value
Memory
2002 - + 08
Update Memory
Load me at
1 LDA 2001
2 MOV B,A
3 LDA 2002
4 MOV C,A
5 STA 2003
6 MOV A,B
7 STA 2004
8 HLT
9
Data
Stack
KeyPad
Memory
I/O Ports
Start 2003
OK
Address (Hex) Address Data
07D3 2003 8
07D4 2004 7
07D5 2005 0
07D6 2006 0
07D7 2007 0
07D8 2008 0
07D9 2009 0
07DA 2010 0
07DB 2011 0
07DC 2012 0
07DD 2013 0
07DE 2014 0
07DF 2015 0
07E0 2016 0
Line No Assembler Message
0 Program assembled successfully

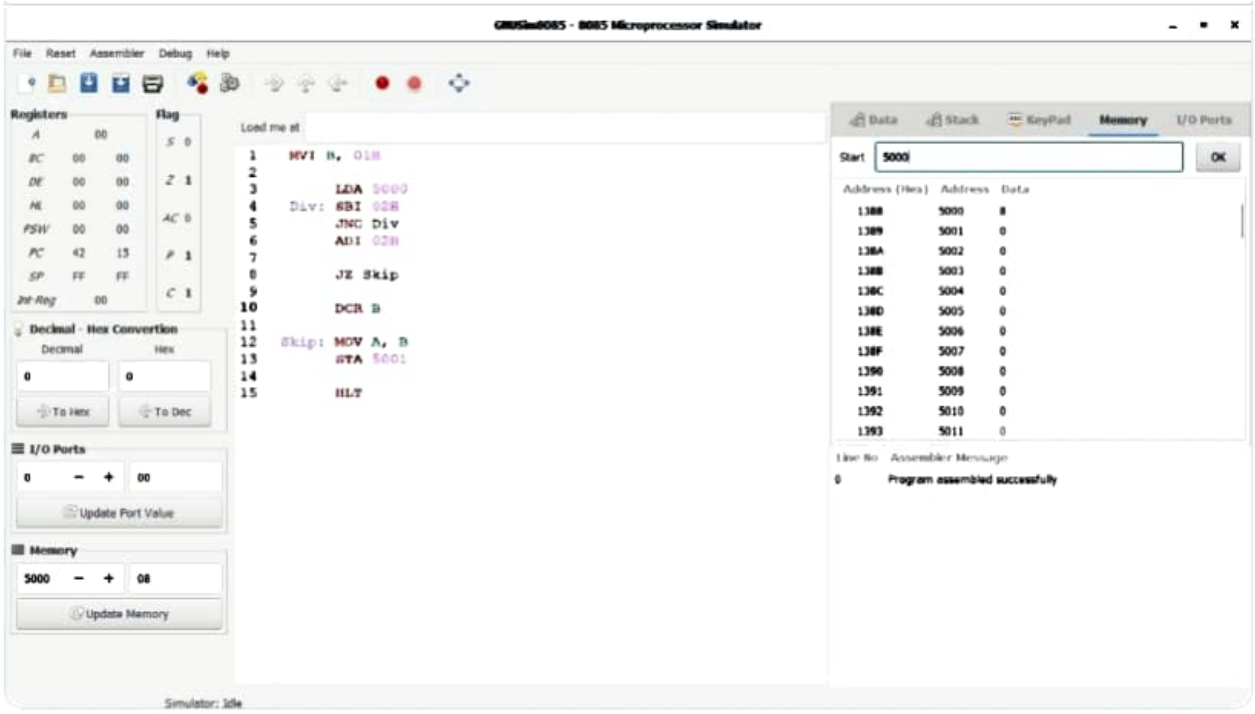

Registers
Flag
A 00
BC 00 00
DE 00 00
HL 1F 41
PSW 00 00
PC 42 0F
SP FF FF
Int-Reg 00
S 0
Z 0
AC 0
P 0
C 0
Decimal - Hex Convertion
Decimal
Hex
0
0
To Hex
To Dec
I/O Ports
0 - + 00
Update Port Value
Memory
8003 - + 05
Update Memory
Load me at
1 LXI H,8050
2
3 MOV B,M
4
5 INX H
6
7 MOV A,M
8
9 CMP B
10
11 JC STORE
12
13 MOV A,B
14
15 STORE: STA 8050
16
17 HLT
Data
Stack
KeyPad
Memory
I/O Ports
Start 8050
OK
Address (Hex) Address Data
1F72 8050 0
1F73 8051 0
1F74 8052 0
1F75 8053 0
1F76 8054 0
1F77 8055 0
1F78 8056 0
1F79 8057 0
1F7A 8058 0
1F7B 8059 0
1F7C 8060 0
1F7D 8061 0
1F7E 8062 0
1F7F 8063 0
Line No Assembler Message
0 Program assembled successfully

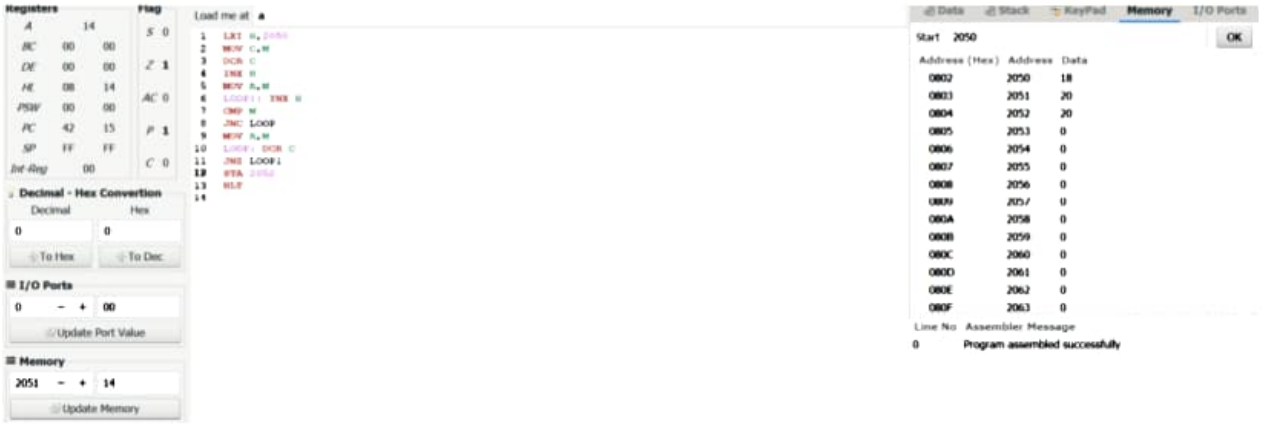

Untitled*
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Memory
Input/Output
Base

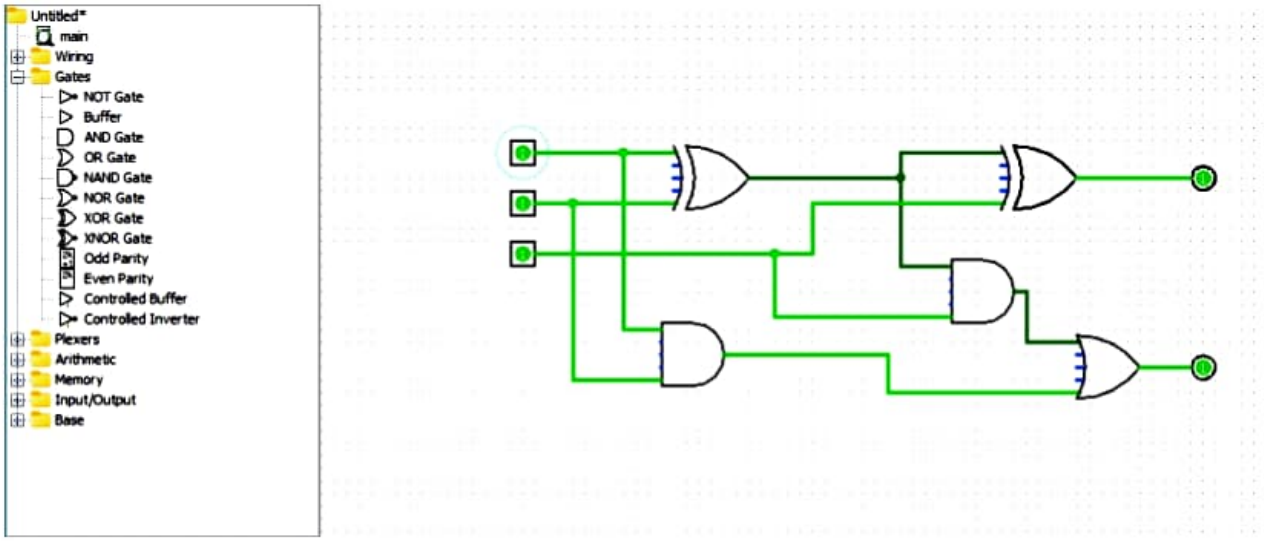

Registers
Flag
Load me at
Data
Stack
KeyPad
Memory
I/O Ports
Start 8001
OK
Address (Hex) Address Data
Decimal - Hex Convertion
I/O Ports
Memory
Update Memory
Program assembled successfully

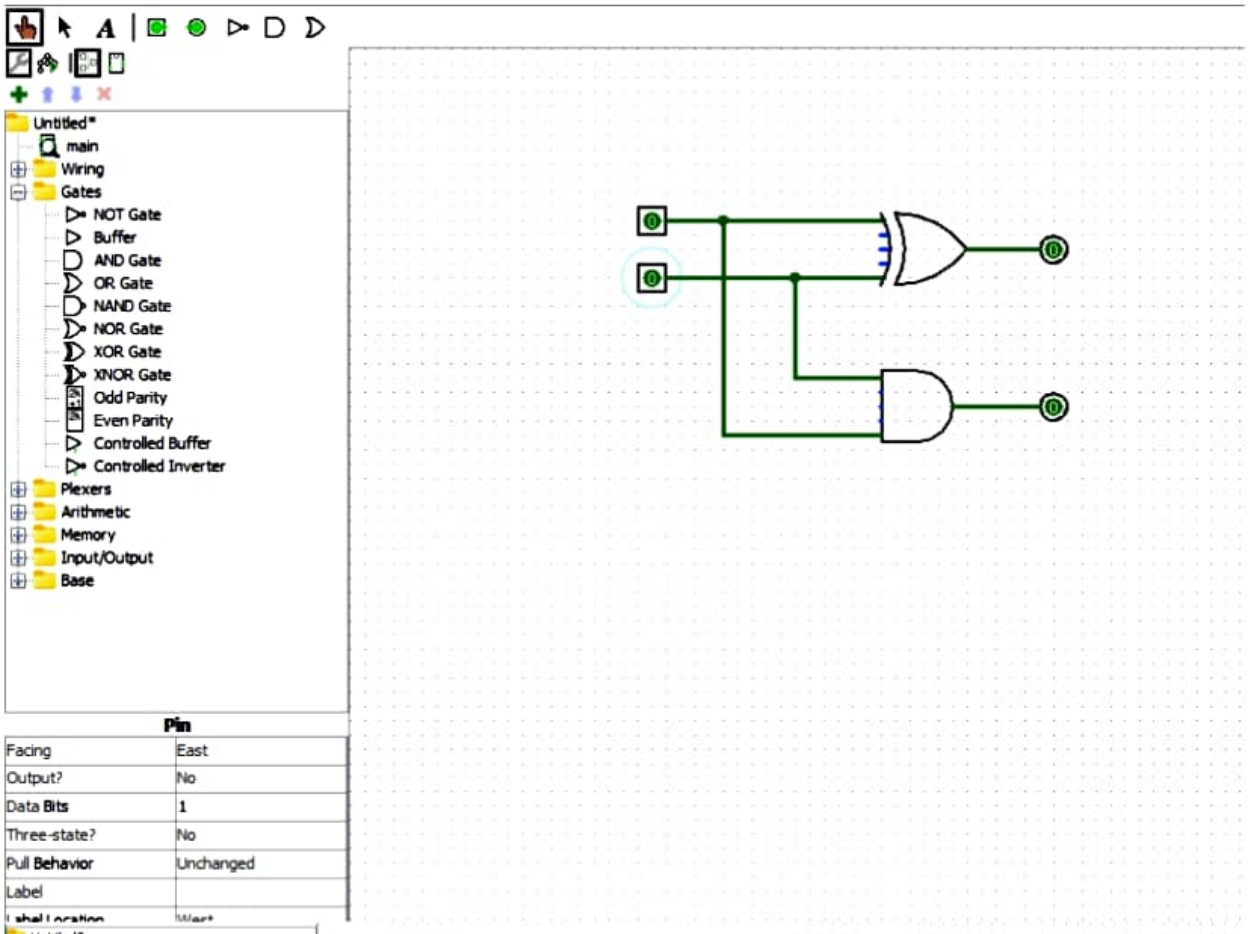

Registers
Flag
Load me at
Data
Stack
KeyPad
Memory
I/O Ports
Start 3001
OK
Address (Hex) Address Data
Decimal - Hex Convertion
I/O Ports
Memory
Update Memory
Program assembled successfully

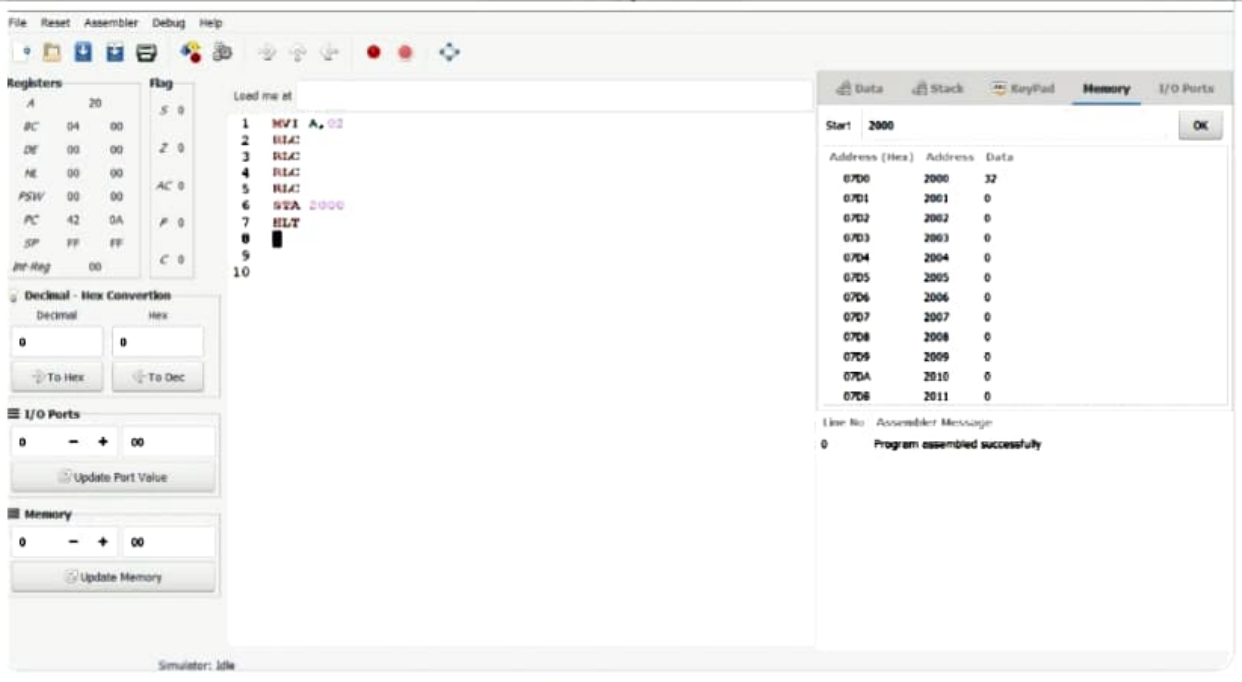

File Reset Assembler Debug Help
Registers
Flag
Load me at
Data
Stack
KeyPad
Memory
I/O Ports
Start 2000
OK
Decimal - Hex Convertion
I/O Ports
Memory
Update Memory
Program assembled successfully

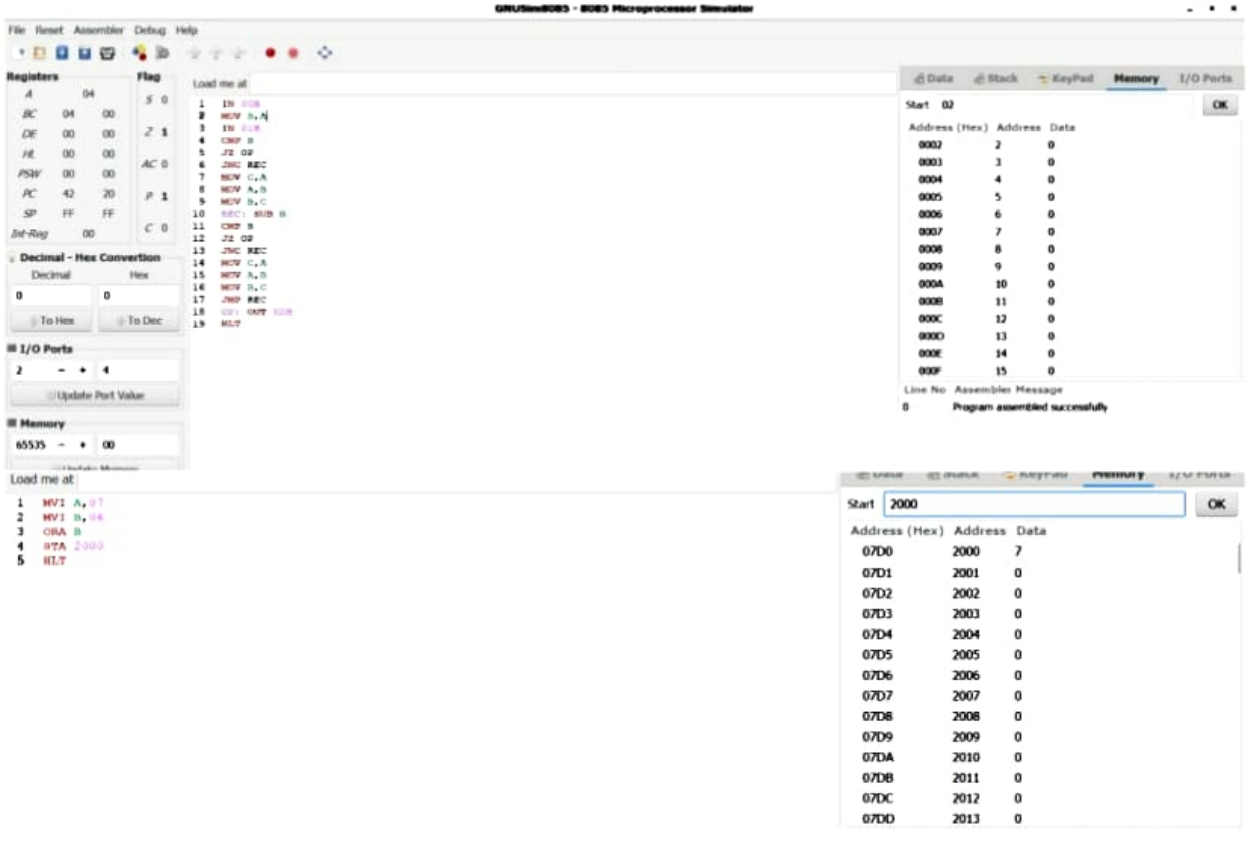

GNUSim8085 - 8085 Microprocessor Simulator
File Reset Assembler Debug Help
Registers
Flag
Load me at
1 MVI B, 01H
2
3 LDA 5000
4 Div: SBI 02H
5 JNC Div
6 ADI 02H
7
8 JZ Skip
9
10 DCR B
11
12 Skip: MOV A, B
13 STA 5001
14
15 HLT
Data Stack KeyPad Memory I/O Ports
Start 5000 OK
Address (Hex) Address Data
1388 5000 8
1389 5001 0
138A 5002 0
138B 5003 0
138C 5004 0
138D 5005 0
138E 5006 0
138F 5007 0
1390 5008 0
1391 5009 0
1392 5010 0
1393 5011 0
Line No Assembler Message
0 Program assembled successfully
Decimal - Hex Convertion
I/O Ports
Update Port Value
Memory
Update Memory
Simulator: Idle


Registers
Flag
Load me at
1 LXI H,2050
2 MOV C,M
3 DCR C
4 INX H
5 MOV A,M
6 LOOP1: INX H
7 CMP M
8 JNC LOOP
9 MOV A,M
10 LOOP: DCR C
11 JNZ LOOP1
12 STA 2052
13 HLT
14
Data Stack KeyPad Memory I/O Ports
Start 2050 OK
Address (Hex) Address Data
0802 2050 18
0803 2051 20
0804 2052 20
0805 2053 0
0806 2054 0
0807 2055 0
0808 2056 0
0809 2057 0
080A 2058 0
080B 2059 0
080C 2060 0
080D 2061 0
080E 2062 0
080F 2063 0
Line No Assembler Message
0 Program assembled successfully
Decimal - Hex Convertion
I/O Ports
Update Port Value
Memory
Update Memory


Untitled*
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Memory
Input/Output
Base


Untitled*
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing East
Output? No
Data Bits 1
Three-state? No
Pull Behavior Unchanged
Label
Untitled*
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Memory
Input/Output
Base


File Reset Assembler Debug Help
Registers
Flag
Load me at
1 MVI A,02
2 RLC
3 RLC
4 RLC
5 RLC
6 STA 2000
7 HLT
8
Data Stack KeyPad Memory I/O Ports
Start 2000
OK
Address (Hex) Address Data
07D0 2000 32
07D1 2001 0
07D2 2002 0
07D3 2003 0
07D4 2004 0
07D5 2005 0
07D6 2006 0
07D7 2007 0
07D8 2008 0
07D9 2009 0
07DA 2010 0
07DB 2011 0
Line No Assembler Message
0 Program assembled successfully
Decimal - Hex Convertion
Decimal
Hex
To Hex
To Dec
I/O Ports
Update Port Value
Memory
Update Memory
Simulator: Idle


GNUSim8085 - 8085 Microprocessor Simulator
File Reset Assembler Debug Help
Registers
Flag
Load me at
1 IN 00H
2 MOV B,A
3 IN 01H
4 CMP B
5 JZ 02
6 JNC REC
7 MOV C,A
8 MOV A,B
9 MOV B,C
10 REC: SUB B
11 CMP B
12 JZ 02
13 JNC REC
14 MOV C,A
15 MOV A,B
16 MOV B,C
17 JMP REC
18 02: OUT 02H
19 HLT
Data Stack KeyPad Memory I/O Ports
Start 02
OK
Address (Hex) Address Data
0002 2 0
0003 3 0
0004 4 0
0005 5 0
0006 6 0
0007 7 0
0008 8 0
0009 9 0
000A 10 0
000B 11 0
000C 12 0
000D 13 0
000E 14 0
000F 15 0
Line No Assembler Message
0 Program assembled successfully
Decimal - Hex Convertion
I/O Ports
Memory
Load me at
1 MVI A,07
2 MVI B,06
3 ORA B
4 STA 2000
5 HLT
Start 2000
OK
Address (Hex) Address Data
07D0 2000 7
07D1 2001 0
07D2 2002 0
07D3 2003 0
07D4 2004 0
07D5 2005 0
07D6 2006 0
07D7 2007 0
07D8 2008 0
07D9 2009 0
07DA 2010 0
07DB 2011 0
07DC 2012 0
07DD 2013 0

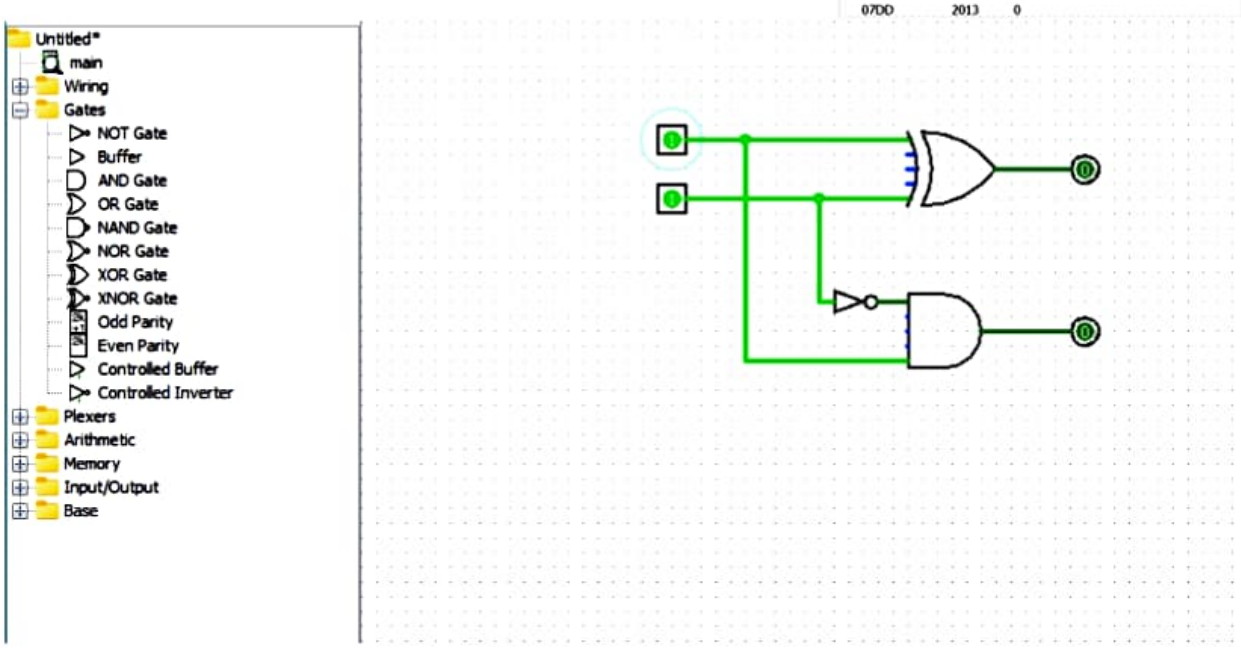
Load me at

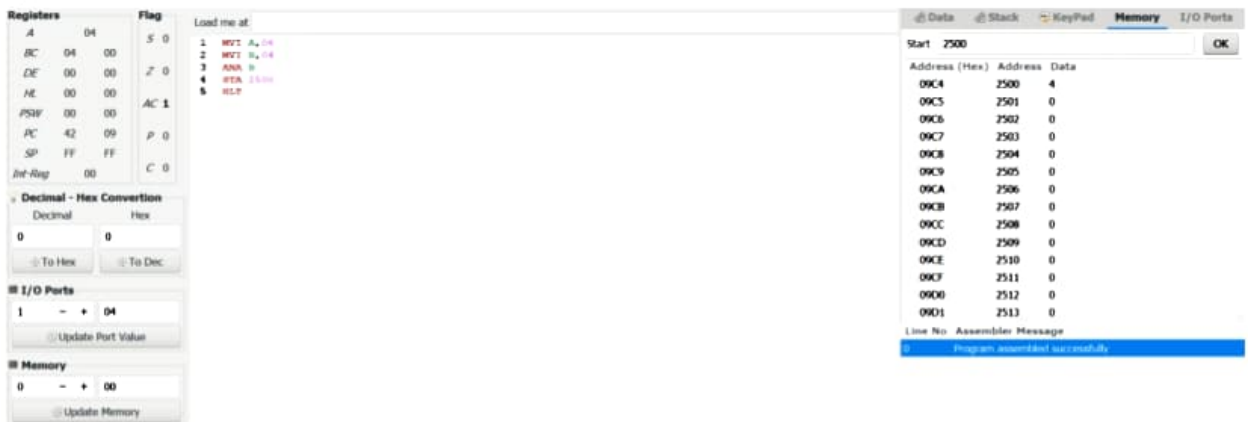
```
1  MVI A,07
2  MVI B,06
3  XRA B
4  STA 2000
5  HLT
```

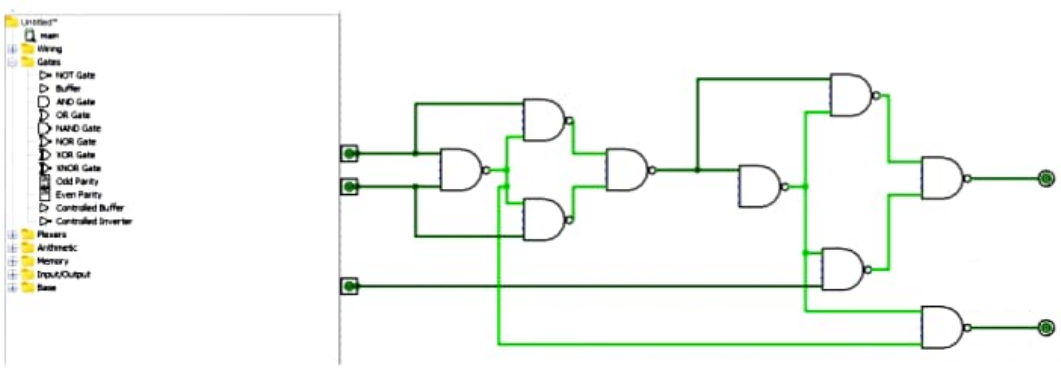
Data | Stack | KeyPad | **Memory** | I/O Ports

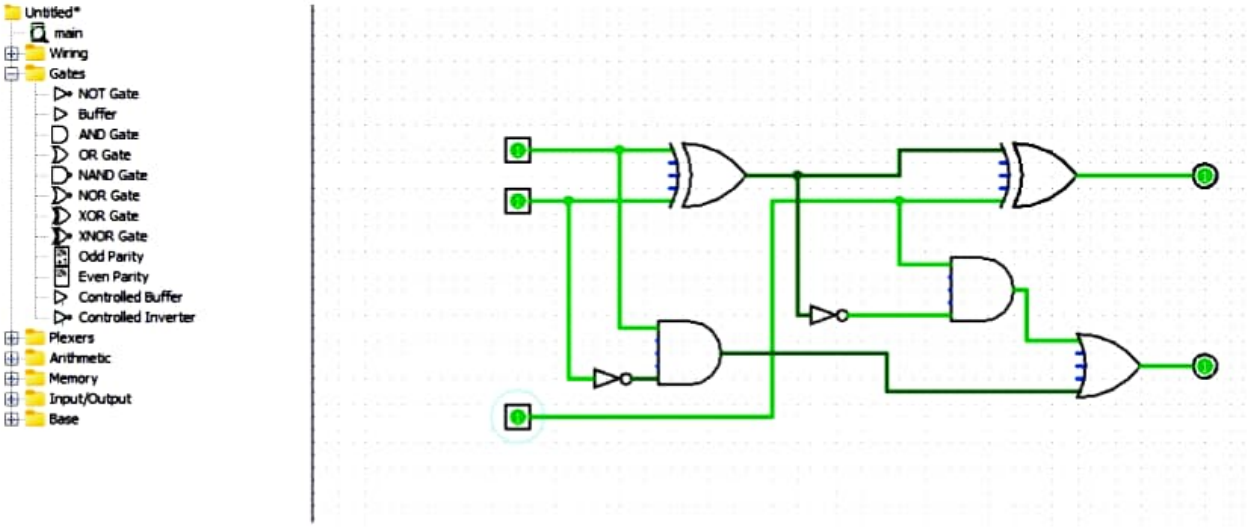
Start 2000 OK

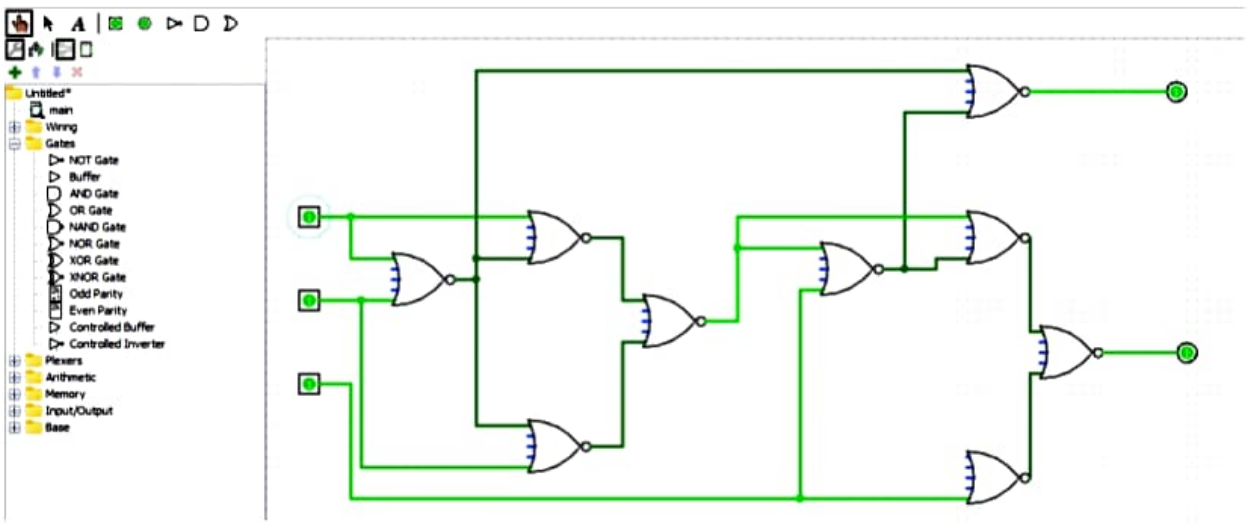
Address (Hex)	Address	Data
07D0	2000	1
07D1	2001	0
07D2	2002	0
07D3	2003	0
07D4	2004	0
07D5	2005	0
07D6	2006	0
07D7	2007	0
07D8	2008	0
07D9	2009	0
07DA	2010	0
07DB	2011	0
07DC	2012	0
07DD	2013	0

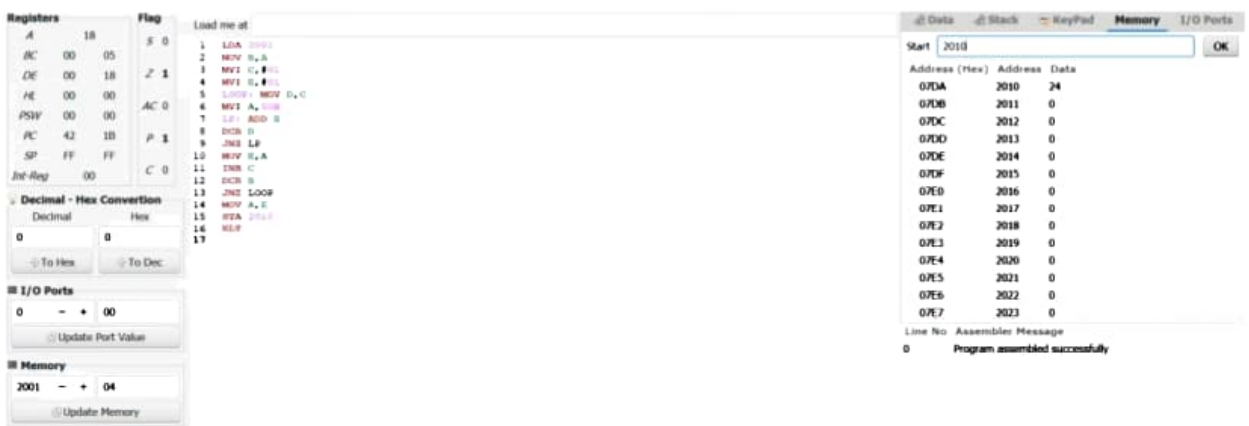


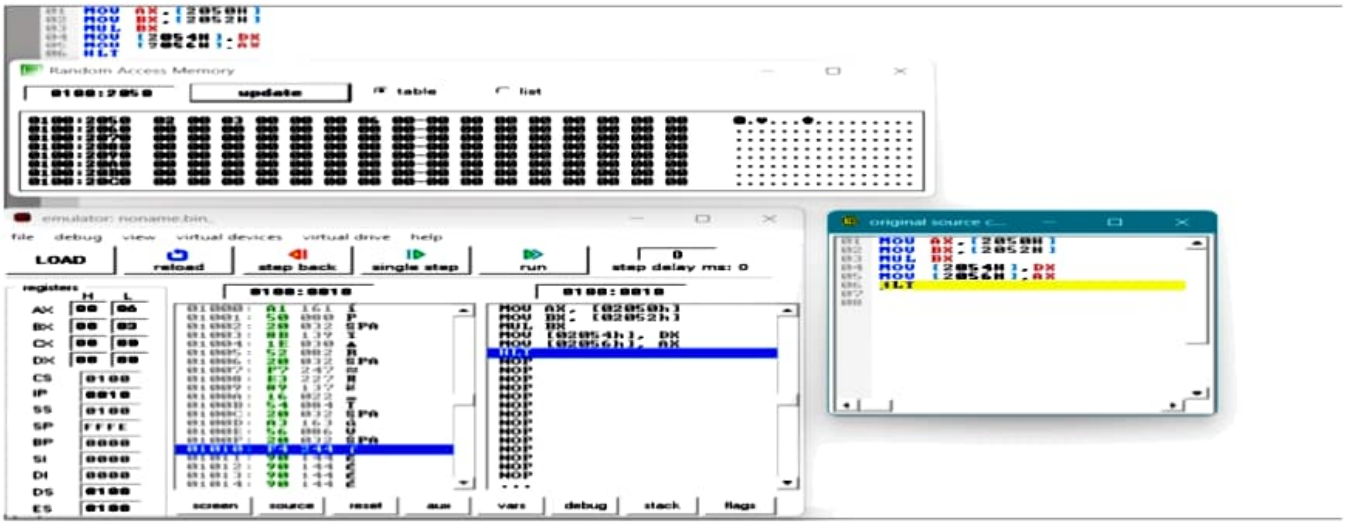





Untitled*
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Memory
Input/Output
Base


Untitled*
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Controlled Inverter
Plexers
Arithmetic
Memory
Input/Output
Base


Registers
Flag
Load me at
Data
Stack
KeyPad
Memory
I/O Ports
Start
OK
Address (Hex)
Address
Data
Decimal - Hex Convertion
Decimal
Hex
To Hex
To Dec
I/O Ports
Update Port Value
Memory
Update Memory
Line No
Assembler Message
Program assembled successfully

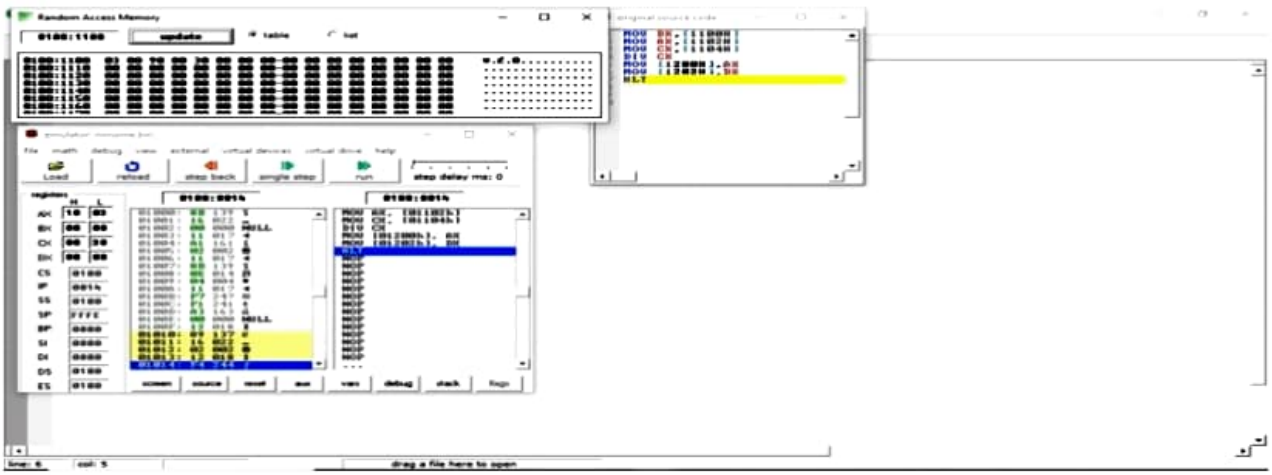


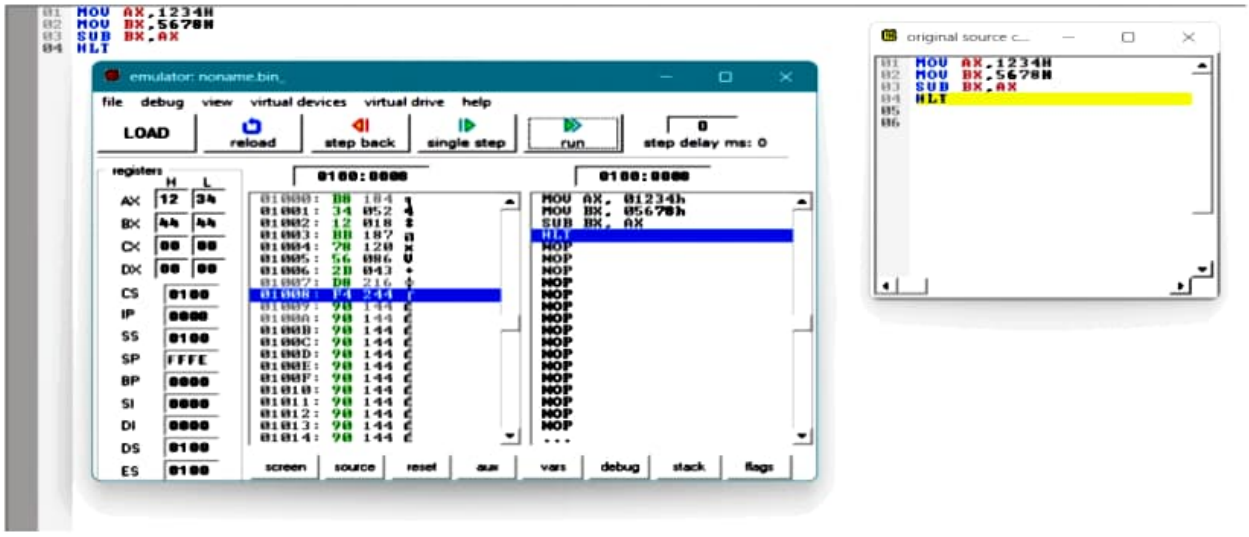

```
1   LOOP: LXI H,3500
2   MVI D,00
3   MVI C,05
4   LOOP1: MOV A,M
5   INX H
6   CMP M
7   JC LOOP2
8   MOV B,M
9   MOV M,A
10  DCX H
11  MOV M,B
12  INX H
13  MVI D,01
14  LOOP2: DCR C
15  JNZ LOOP1
16  MOV A,D
17  RRC
18  JC LOOP
19  HLT
```

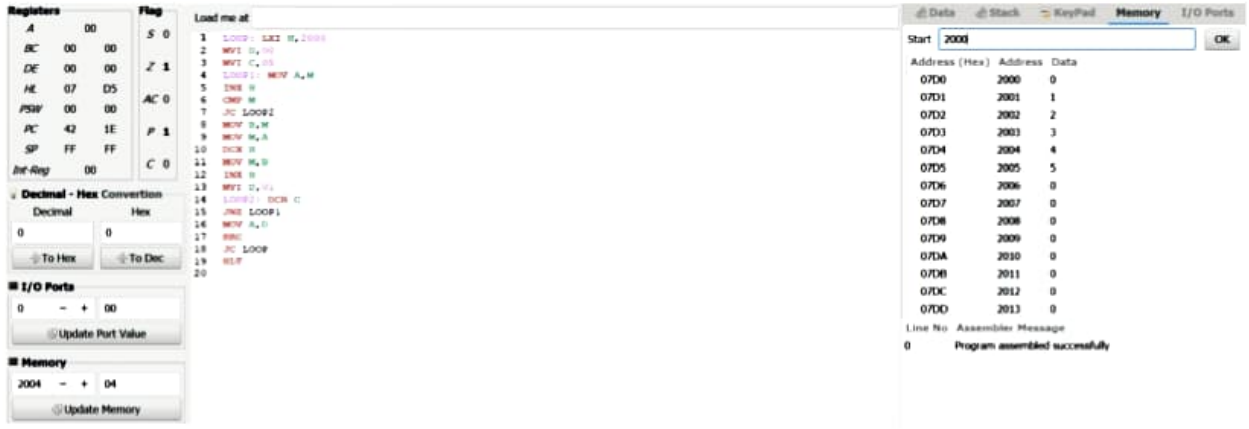
Start 3500 OK

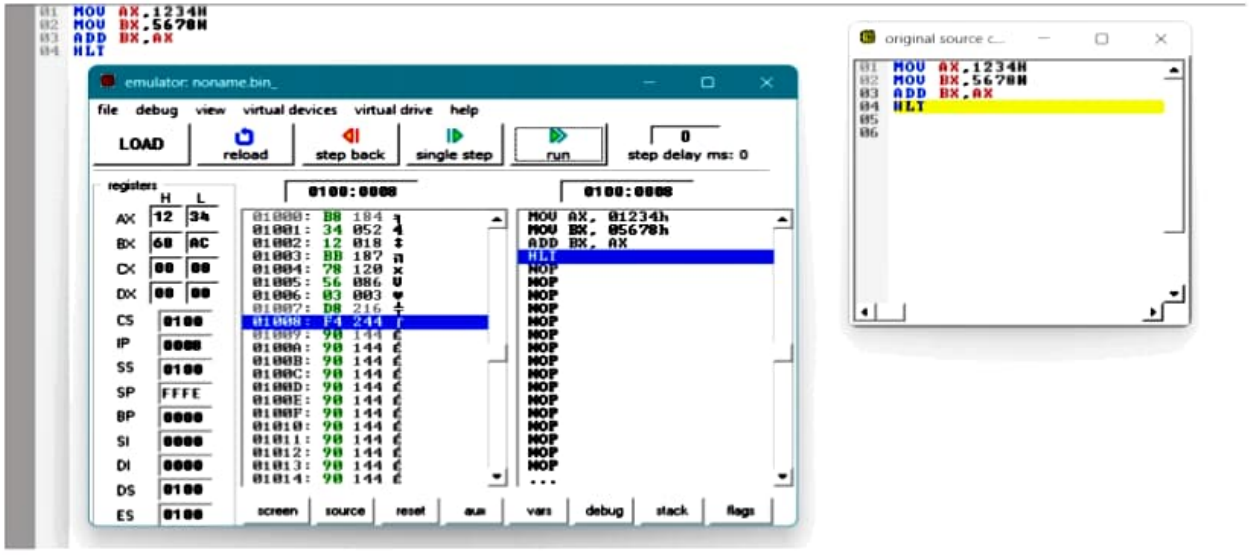
Address (Hex)	Address	Data
0DAC	3500	2
0DAD	3501	5
0DAE	3502	9
0DAF	3503	0
0DB0	3504	0
0DB1	3505	0
0DB2	3506	0
0DB3	3507	0
0DB4	3508	0
0DB5	3509	0
0DB6	3510	0
0DB7	3511	0

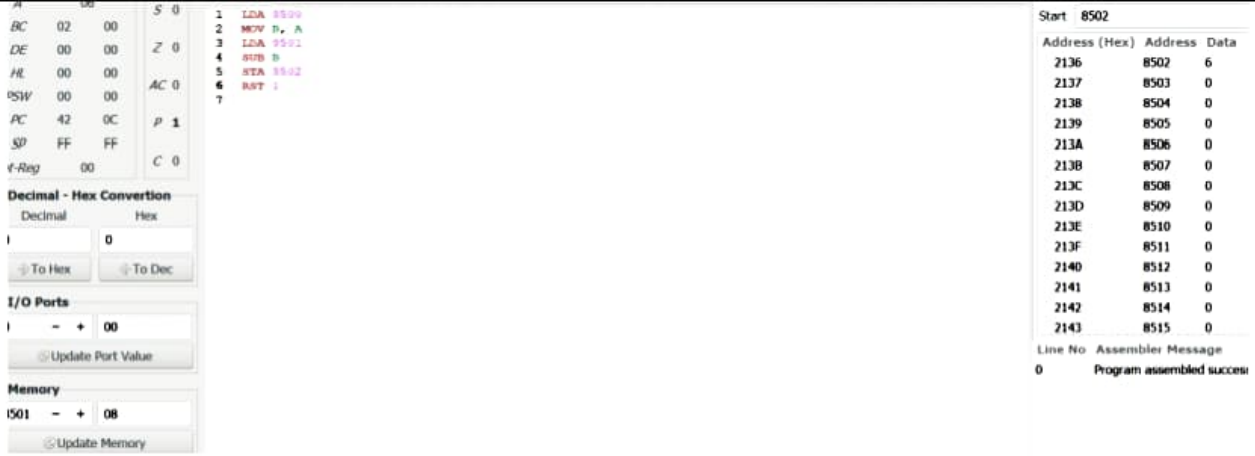
Line No Assembler Message

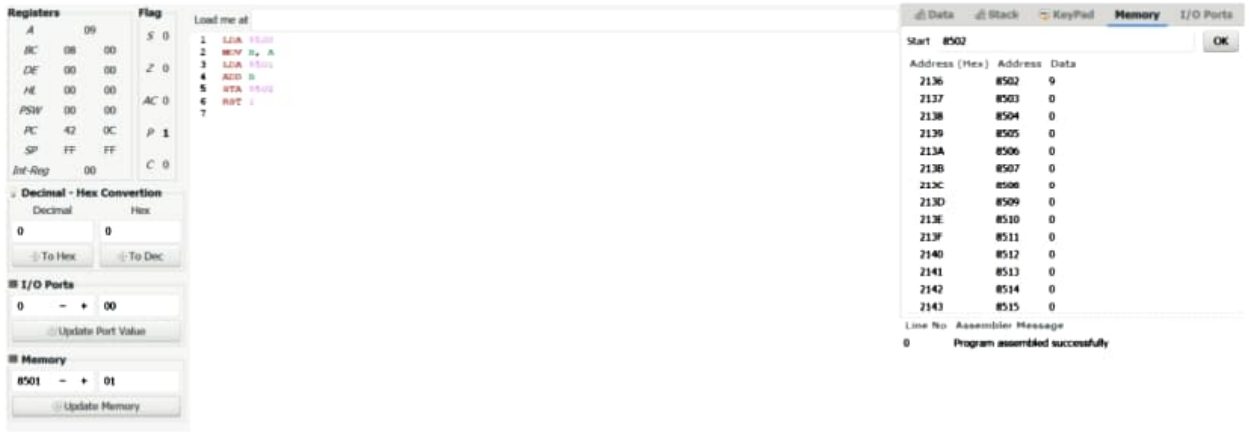



MOV AX,1234H
MOV BX,5678H
SUB BX,AX
HLT
emulator: noname.bin_
file debug view virtual devices virtual drive help
LOAD
reload
step back
single step
run
step delay ms: 0
registers
AX 12 34
BX 56 78
CX 00 00
DX 00 00
CS 0100
IP 0000
SS 0100
SP FFFE
BP 0000
SI 0000
DI 0000
DS 0100
ES 0100
0100:0000
0100:0000
MOV AX, 01234h
MOV BX, 05678h
SUB BX, AX
HLT
NOP
screen source reset aux vars debug stack flags
original source c...

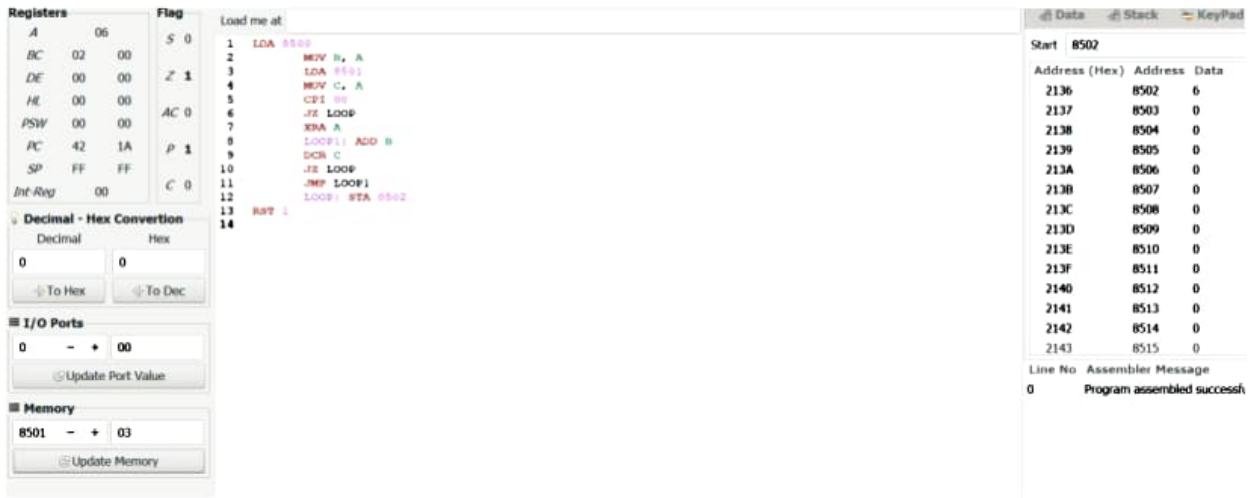

Registers
Flag
Decimal - Hex Convertion
Decimal
Hex
To Hex
To Dec
I/O Ports
Update Port Value
Memory
Update Memory
Load me at
Data
Stack
KeyPad
Memory
I/O Ports
Start 2000
OK
Address (Hex) Address Data
Line No Assembler Message
Program assembled successfully


MOV AX,1234H
MOV BX,5678H
ADD BX,AX
HLT
emulator: noname.bin_
file debug view virtual devices virtual drive help
LOAD
reload
step back
single step
run
step delay ms: 0
registers
AX 12 34
BX 68 AC
CX 00 00
DX 00 00
CS 0100
IP 0000
SS 0100
SP FFFE
BP 0000
SI 0000
DI 0000
DS 0100
ES 0100
0100:0000
0100:0000
MOV AX, 01234h
MOV BX, 05678h
ADD BX, AX
HLT
NOP
screen source reset aux vars debug stack flags
original source c...


Registers
Flag
Decimal - Hex Convertion
I/O Ports
Memory
Update Port Value
Update Memory
To Hex
To Dec
Load me at
Start 8502
Address (Hex) Address Data
Line No Assembler Message
Program assembled succes


Registers
Flag
Decimal - Hex Convertion
I/O Ports
Memory
Update Port Value
Update Memory
To Hex
To Dec
Load me at
Data
Stack
KeyPad
Memory
I/O Ports
Start 8502
OK
Address (Hex) Address Data
Line No Assembler Message
Program assembled successfully


Registers
Flag
Decimal - Hex Convertion
I/O Ports
Memory
Update Port Value
Update Memory
To Hex
To Dec
Load me at
Data
Stack
KeyPad
Memory
I/O Ports
Start 5002
OK
Address (Hex) Address Data
Line No Assembler Message
Program assembled successfully


Registers
Flag
Decimal - Hex Convertion
I/O Ports
Memory
Update Port Value
Update Memory
To Hex
To Dec
Load me at
Data
Stack
KeyPad
Start 8502
Address (Hex) Address Data
Line No Assembler Message
Program assembled successfu