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APPROXIMATE VEDIC MULTIPLIER USING LOW ORDER COMPRESSORS

A MINOR PROJECT - III REPORT

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**M.KUMARASAMY COLLEGE OF ENGINEERING,
KARUR**

BONAFIDE CERTIFICATE

Certified that this **18ECP105L - Minor Project III** report “**APPROXIMATE VEDIC MULTIPLIER USING LOW ORDER COMPRESSORS**” is the bonafide work of “**VASANTH P (927621BEC234), SIBI V B (927621BEC199), VISHAL G (927621BEC242), YUVASARAVANAN S (927621BEC248)**” who carried out the project work under my supervision in the academic year **2021-2025-ODD**.

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PROJECT COORDINATOR

INSTITUTION VISION AND MISSION

Vision

To emerge as a leader among the top institutions in the field of technical education.

Mission

M1: Produce smart technocrats with empirical knowledge who can surmount the global challenges.

M2: Create a diverse, fully -engaged, learner -centric campus environment to provide quality education to the students.

M3: Maintain mutually beneficial partnerships with our alumni, industry and professional associations

DEPARTMENT VISION, MISSION, PEO, PO AND PSO

Vision

To empower the Electronics and Communication Engineering students with emerging technologies, professionalism, innovative research and social responsibility.

Mission

M1: Attain the academic excellence through innovative teaching learning process, research areas & laboratories and Consultancy projects.

M2: Inculcate the students in problem solving and lifelong learning ability.

M3: Provide entrepreneurial skills and leadership qualities.

M4: Render the technical knowledge and skills of faculty members.

Program Educational Objectives

- PEO1: Core Competence:** Graduates will have a successful career in academia or industry associated with Electronics and Communication Engineering
- PEO2: Professionalism:** Graduates will provide feasible solutions for the challenging problems through comprehensive research and innovation in the allied areas of Electronics and Communication Engineering.
- PEO3: Lifelong Learning:** Graduates will contribute to the social needs through lifelong learning, practicing professional ethics and leadership quality

Program Outcomes

- PO 1: Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- PO 2: Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- PO 3: Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- PO 4: Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- PO 5: Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO 6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO 10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO 12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes

PSO1: Applying knowledge in various areas, like Electronics, Communications, Signal processing, VLSI, Embedded systems etc., in the design and implementation of Engineering application.

PSO2: Able to solve complex problems in Electronics and Communication Engineering with analytical and managerial skills either independently or in team using latest hardware and software tools to fulfil the industrial expectations.

Abstract	Matching with POs, PSOs
Multiplier, compressor, Approximation Multiplier, Vedic Multiplier	PO1, PO2, PO3, PO4, PO5, PO6, PO7, PO9, PO10, PO11, PO12, PSO1, PSO2

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ABSTRACT

In the ever-evolving landscape of digital computation, efficient multiplication remains a critical operation. This paper introduces an innovative approach to accelerate multiplication processes by combining the ancient wisdom of Vedic mathematics with modern low-order compressors. We propose an approximate Vedic multiplier that balances computational speed and resource efficiency, making it ideal for applications where precise multiplication results can be modestly compromised. The Vedic multiplication system, originating from ancient Indian mathematical texts, offers a range of multiplication techniques known for their efficiency and versatility. However, their direct application to contemporary digital hardware may pose challenges, especially in resource-constrained environments. Our research addresses this challenge by introducing a novel approximation technique that leverages low-order compressors. These compressors have proven to be valuable tools for designing efficient hardware implementations and are particularly well-suited for our purpose. In this paper a new approximate low compressor model is proposed for less complex multiplication process. The proposed compressor design uses less hardware resources and less energy as compared to existing compressors. When compared with other existing multipliers with bit size of 4×4 . The proposed multiplier gives approximately 20% reduction in area and Delay

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LIST OF ABBREVIATIONS

ACRONYM		ABBREVIATION
DSP	-	Digital Signal Processor
ALU	-	Arithmetic and logic unit
MAC	-	Multiply and Accumulate
LSB	-	Least Significant Bits
MSB	-	Most Significant Bits

CHAPTER 1

INTRODUCTION

While using computers and smart phones sometimes we face a situation where the device (hangs) stops responding. One of the reasons behind it is processor speed that motivated us to go for a high-speed multiplier design. Multiplier in special application processors like Digital Signal Processor (DSPs) improves the speed of operation since the entire signal and data processing operations involve multiplication. Multiplication plays a vital role in DSP applications (like DFT, convolution, FFT etc.), Arithmetic and logic unit (ALU), and Multiply and Accumulate (MAC) unit. High Speed Multiplication thus becomes a necessity to increase the performance of processor. Quite a few multipliers have been designed and proposed over last few decades but for multiplication these designs need several intermediate stages to calculate the final result due to which critical path length increases hence cause more delay. Moreover, the intermediate stages need additional hardware which becomes reason for increased area and power consumption. and a new approach for multiplier design based on Vedic Mathematics is explored to overcome these disadvantages. Vedic Mathematics is an ancient and prominent approach that serves as base to solve many mathematical challenges experienced nowadays. A Vedic multiplier is a type of digital multiplier that is based on ancient Indian multiplication techniques described in Vedic mathematics. Vedic multiplication methods are known for their efficiency and speed, making them a popular choice for designing hardware multipliers in digital circuits. One of the key techniques used in Vedic multiplication is the use of compressors, particularly low-order compressors, to perform multiplication operations.

1.1 PROJECT DETAILS

Designing an approximate Vedic multiplier using low-order compressors is a complex project that involves both digital circuit design and a solid understanding of Vedic mathematics principles. Here are the project details broken down into steps

Design an efficient and fast multiplier using Vedic mathematics techniques and low-order compressors to perform approximate multiplication. The project aims to balance speed, area, and power consumption in the design. Balancing approximation accuracy with speed and efficiency. Optimizing the use of low-order compressors to minimize delay. Selecting appropriate approximation techniques. Ensuring proper testing and verification of the multiplier's functionality

The timeline for the project will depend on the complexity of the design and the resources available, but it can range from several weeks to several months. Remember to consult with a project advisor or supervisor for guidance and to refine the project details based on the available resources and project goals. In this project, you will design and implement a digital multiplier based on Vedic mathematics techniques. The multiplier will employ low-order compressors to approximate the multiplication operation. The main objective is to achieve faster multiplication while minimizing hardware resource usage. The success of your project can be evaluated based on the accuracy and efficiency of the approximate Vedic multiplier, as well as its performance compared to traditional multiplication methods. You can also assess how well the low-order compressors contribute to reducing delay and resource consumption.

1.2 VEDIC MULTIPLIER

A Vedic multiplier is a type of digital multiplier based on ancient Indian multiplication techniques described in Vedic mathematics. It is a hardware-based approach to perform fast multiplication operations. The term "Vedic" is derived from the ancient Indian scripture called the Vedas, where these multiplication techniques are documented. The key feature of Vedic multiplication is its efficiency and speed. Vedic mathematics offers various methods to perform arithmetic operations mentally or using minimal steps. In the context of multiplication, Vedic multiplication techniques can be applied to design hardware circuits for efficient multiplication. The primary method used in Vedic multiplication is called "Nikhilam Sutra." It is based on a series of rules and techniques for multiplying two numbers together. The Nikhilam Sutra method is particularly useful for hardware implementation because it reduces the number of additions and subtractions, making the multiplication process faster. Vedic multiplication decomposes the multiplication process into a set of partial products, which are easier to compute. Each partial product corresponds to a digit in one of the operands. Vedic multiplication uses specific rules for adding the partial products together and handling carries efficiently. These rules are designed to minimize the number of additions required. Compressors are used to combine the partial products efficiently. Low-order compressors and higher-order compressors are employed to merge the least significant bits and reduce the number of adder stages. The advantages of Vedic multipliers include their speed and efficiency compared to traditional multiplication methods. They are often used in digital signal processing, cryptography, and other applications where multiplication is a critical operation. Therefore, they are typically used in applications where speed is more critical than absolute precision.

1.2.1 DESCRIPTION

The project aims to develop a digital multiplier that approximates multiplication using Vedic mathematics techniques, with a focus on low-order compressors. The goal is to achieve faster multiplication while sacrificing some precision when compared to traditional multiplication methods. This project is ideal for applications where speed and efficiency are more critical than precise results.

1. **Vedic Mathematics Principles:** The project will be based on the principles of Vedic mathematics, emphasizing fast and efficient multiplication techniques that decompose the multiplication process into manageable steps.
2. **Low-Order Compressors:** Low-order compressors are at the heart of this design. These compressors will be used to merge the least significant bits of partial products generated during the multiplication process. This reduces the number of adder stages and minimizes the critical path delay, leading to faster multiplication.
3. **Partial Products:** The multiplication process will involve breaking down the operands into smaller parts, creating partial products that will be merged using low-order compressors.
4. **Approximation Techniques:** To increase speed, some approximation techniques may be employed. This could involve truncating or rounding results to minimize the time required for precision calculations.
5. **Parallel Processing:** The project may implement parallel processing to compute partial products simultaneously, reducing the overall multiplication time.
6. **Accuracy vs. Speed Trade-off:** It's essential to understand that this multiplier will not provide the same level of accuracy as traditional multiplication methods.

CHAPTER 2

LITERATURE SURVEY

2.1 The analysis and design two new approximate 4:2 compressors

These designs rely on different features of compression, such that imprecision in computation can meet with respect to circuit-based figures of merit of a design. Different schemes for utilizing the proposed approximate compressors are proposed and analyzed for a Dada multiplier. The results show that the proposed designs accomplish significant reductions in power dissipation, delay and transistor count compared to an exact design. Multipliers are key arithmetic circuits in many such applications such as digital signal processing (DSP). Approximate computing has received significant attention as a promising strategy to decrease power consumption of inherently error tolerant applications. Here we focus on hardware- level approximation by introducing the partial product perforation technique for designing approximate multiplication circuits. The partial product tree of the multiplier is approximated by the proposed tree compressor. In this paper, an approximate multiply-and-accumulate (MAC) unit is introduced. The MAC partial product terms are compressed by using simple OR gates as approximate counters; moreover, to further save energy, selected columns of the partial product terms are not formed. A compensation term is introduced in the proposed MAC, to reduce the overall approximation error. Approximate/inexact computing has become an attractive approach for designing high performance and low power arithmetic circuits. Floating-point (FLP) arithmetic is required in many applications, such as digital signal processing, image processing and machine learning. Approximate FLP multipliers with variable accuracy are proposed in this paper; the accuracy and the circuit requirements of these designs are analyzed and assessed according to different 8 metrics.

2.2 VEDIC MULTIPLICATION TECHNIQUE

The ancient Vedic multiplication techniques are equally applicable for binary numbers also. The Vedic mathematics reduces the cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. The proposed multiplier is based on Urdhvatiryakbhyam - (Vertically and crosswise) sutra. The Urdhva-tiryakbhyam sutra is basically vertically and crosswise. In this method the partial products are generated simultaneously which itself reduces the delay makes this method fast. The method is explained below for two, three-bit numbers A and B where $A = a_2a_1a_0$ and $B = b_2b_1b_0$ as shown in Figure 1. Firstly, the least significant bits are multiplied which gives the least significant bit of the product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum, which is obtained by processing the three bits with crosswise and vertical multiplication and addition to give the sum and carry. The sum is the corresponding bit of the product and the carry is again added to the next stage multiplication and addition of two bits except the LSB. The same operation continues until the multiplication of the two MSBs to give the MSB of the product. The implementation of Vedic Multiplier is done using VHDL and the functionality of each block is verified using simulation software, Model Sim and ISE. The basic building blocks are two input AND gate and Adder, so the structural modeling style is used for the implementation of Vedic Multiplier.

2.3 VEDIC FORMULA – URDHVA TIRYAKBHYAM

Vedic mathematics is not only limited to India but has become an interesting topic of research abroad because of the fact that it reduces the calculations which appears complex to us in conventional mathematics to a very simple one. The reason behind this is the Vedic formulae are claimed to be based on the natural principles of the working of human mind. Among these 16 formulae, Urdhva Tiryakbhyam proves to be quite useful concept through which all partial products are generated concurrently and applicable to all cases of multiplication. Urdhva Tiryakbhyam is term in Sanskrit language that literally means Vertically and Crosswise [5]. Fig.1 gives the clear picture of the method in which the black dots at tops and bottoms of each steps represent multiplier and multiplicand bits, and the two-way arrows are indication for the bits to be multiplied to get the individual bits of the final product. Each step shown in the figure results in individual bits of the final 16-bit product. If we consider two 8-bit numbers A7-A0 and B7-B0 then step 1 shows that we have to multiply A0 and B0 to get P0. In step 2 the second bit of product P1 will be calculated by adding (A1*B0) and (A0*B1) as given in equation (2). they carry will be added to the next step. The process continues till we get all the bits of final product. The final computed product is represented by P0 to P15 which are calculated by adding partial products obtained earlier using logical AND operation.

$$P_0 = A_0 * B_0 \quad (1)$$

$$C_1 P_1 = (A_1 * B_0) + (A_0 * B_1) \quad (2) \quad C_3 C_2 P_2 = (A_2 * B_0) + (A_0 * B_2) + (A_1 * B_1) + C_1 \quad (3)$$

$$C_5 C_4 P_3 = (A_3 * B_0) + (A_2 * B_1) + (A_1 * B_2) + (A_0 * B_3) + C_2 \quad (4)$$

$$C_7 C_6 P_4 = (A_4 * B_0) + (A_3 * B_1) + (A_2 * B_2) + (A_1 * B_3) + (A_0 * B_4) + C_3 + C_4 \quad (5)$$

$$C10C9C8P5 = (A5 * B0) + (A4 * B1) + (A3 * B2) + (A2 * B3) + (A1 * B4) + (A0 * B5) + C5 + C6 \quad (6)$$

$$C13C12C11P6 = (A6 * B0) + (A5 * B1) + (A4 * B2) + (A3 * B3) + (A2 * B4) + (A1 * B5) + (A0 * B6) + C7 + C8 \quad (7)$$

$$C16C15C14P7 = (A7 * B0) + (A6 * B1) + (A5 * B2) + (A4 * B3) + (A3 * B4) + (A2 * B5) + (A1 * B6) + (A0 * B7) + C9 + C11 \quad (8)$$

$$C19C18C17P8 = (A7 * B1) + (A6 * B2) + (A5 * B3) + (A4 * B4) + (A3 * B5) + (A2 * B6) + (A1 * B7) + C10 + C12 + C14 \quad (9)$$

$$C22C21C20P9 = (A7 * B2) + (A6 * B3) + (A5 * B4) + (A4 * B5) + (A3 * B6) + (A2 * B7) + C13 + C15 + C17 \quad (10)$$

$$C25C24C23P10 = (A7 * B3) + (A6 * B4) + (A5 * B5) + (A4 * B6) + (A3 * B7) + C16 + C18 + C20 \quad (11)$$

$$C27C26P11 = (A7 * B4) + (A6 * B5) + (A5 * B6) + (A4 * B7) + C19 + C21 + C23 \quad (12)$$

$$C29C28P12 = (A7 * B5) + (A5 * B6) + (A5 * B7) + C22 + C24 + C26 \quad (13)$$

$$C31C30P13 = (A7 * B6) + (A6 * B7) + C25 + C27 + C28 \quad (14)$$

$$C32P14 = (A7 * B7) + C29 + C30 \quad (15)$$

$$P15 = C31 + C32 \quad (16)$$

CHAPTER-3

EXISTING SYSTEM

The compressors are used to design the high speed multipliers, to minimize the delay in the summation part of the partial product. Therefore, the compressors improve the multiplier circuits and overall systems performance. The 4-2 compressor is implemented using XOR-XNOR gates and 2:1 multiplexers. This 4-2 compressor has five inputs in which one carry input and two outputs. The 3-2 compressor has three inputs and two outputs; it is similar to FA(full adder).

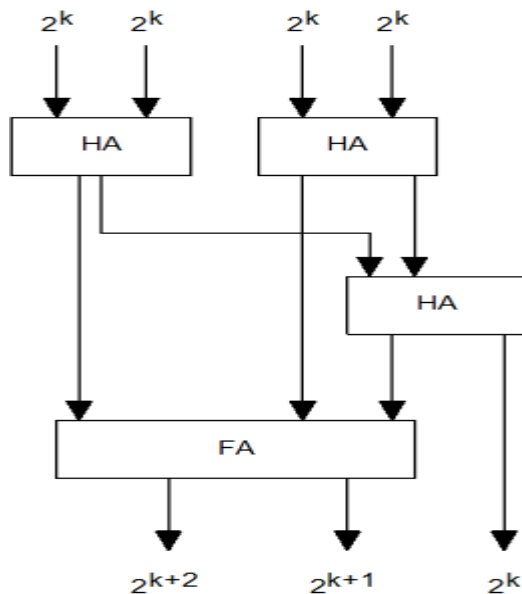


Figure 3.1 Existing 4:3 compressor

The existing 4:3 compressor is shown in Figure 3.1 (Mehrabi et al. 2017), and it consists of three half adders and one full adder. The cout (2^{k+2}) is the critical path and, it is fed into the input as next level partial product tree reduction in the multiplication process. Therefore, delay reduction in the critical path (cout) increases the performance of the multiplier. The proposed compressors are focused on reducing the critical path delay.

$$\text{SUM} = X1 \oplus X2 \oplus X3 \oplus X4 \oplus \text{Cin} \dots\dots\dots (1)$$

$$\text{CARRY} = ((X1 \oplus X2 \oplus X3 \oplus X4) \& \text{Cin}) \mid ((\sim(X1 \oplus X2 \oplus X3 \oplus X4)) \& X4) \dots\dots\dots (2)$$

$$C_{out} = ((X_1 \wedge X_2) \wedge X_3) \vee ((\neg(X_1 \wedge X_2)) \wedge X_1) \dots\dots\dots (3)$$

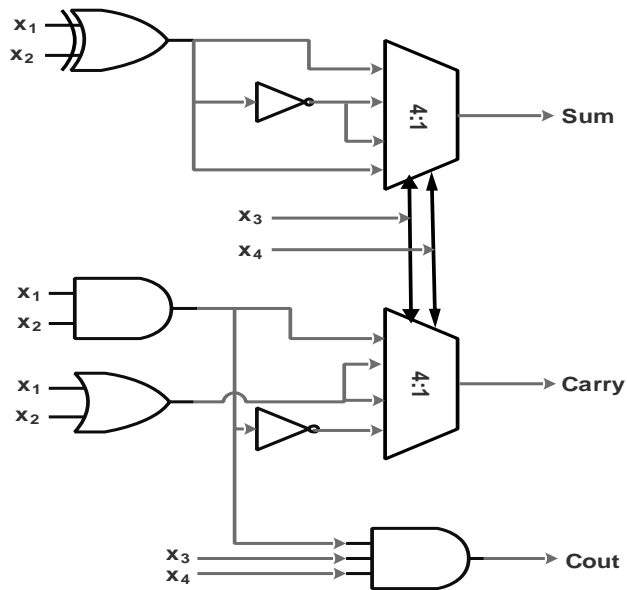


Figure 3.2 The proposed 3-1-1-2 compressor with 4:1 multiplexer

CHAPTER-4

PROPOSED SYSTEM

4.1 VEDIC MULTIPLIER DESIGN FOR 8x8 WITH PROPOSED COMPRESSORS

The proposed compressors are designed and discussed in chapter 3.3. The proposed compressors are utilized in the 8x8 Vedic multiplier, and its partial product tree compressions are discussed with the help of the dot diagram.

4.1.1 Vedic Multiplier Design for 8x8 with Proposed 3-1-1-2 Compressor

The proposed 3-1-1-2 compressor is used in the 8x8 Vedic multiplier designs. Figure shows a dot diagram for the proposed 3-1-1-2 compressor-based 8x8 multiplier. The PPterms are reduced using a 3-1-1-2 compressor with the minimum usage of full adders and half adders in the step-by-step PP tree reduction process. The final product result is assigned as Z0 to Z15. In Figure, the PPs are reduced to two PPs in each column. After this point ripple carry, adder is used to compute the end product result of the 8x8 multiplier. The proposed 3-1-1-2 compressor is used to compute four available bits in the column itself or to compute the three available bits in a column and the remaining one bit as carry from the previous column. The carry bit is needed to feed as x3 or x4 because x3 and x4 are processed with one unit gate delay.

4.1.2 Vedic Multiplier Design for 8x8 with Proposed 4-1-2 Compressor

The proposed 4-1-2 compressor is used in the 8x8 Vedic multiplier designs. The dot diagram for the proposed 4-1-2 compressor-based 8x8 multiplier is the same as shown in Figure 3.11. The proposed 3-1-1-2 compressor and the proposed 4-1-2 compressor have consisted of same the number of inputs and outputs. But the

proposed 4-1-2 compressor is used to compute four available bits at the initial time, and it cannot be used with the previous column carry like 3-1-1-2 compressor because x_3 and x_4 need to feed through from the initial stage gate.

4.1.3 Vedic Multiplier Design for 8x8 with Proposed 5-3 Multi-Column Compressor

The proposed 5-3 multi-column compressor is used in the 8x8 Vedic multiplier designs to analyse the performance of the compressor. Figure 3.13 shows a dot diagram for the proposed 5-3 compressor-based 8x8 multiplier. The PP terms are reduced using a 5-3 compressor with the minimum usage of full adders and half adders in the step-by-step PP tree reduction process. The final product result is assigned as Z_0 to Z_{15} . The 5-3 multi-column compressor gets five partial product inputs. Three partial products get from the first column, and two partial products get from the second column. Figure 3.12 shows the dot diagram for the 5-3 multi-column compressor.

4.1.4 Logical Component Analysis of Proposed 8x8 Multiplier Designs with Conventional Design

The 8-bit Vedic multiplier is implemented using the proposed compressors and implemented the 8-bit Vedic multiplier using conventional full adders and half adders. The logical components count is given in Table 3.2. The components are required logic gates to implement the 8-bit multiplier architecture. The area and delay comparison are discussed in chapter 3.6 and chapter 3.7 in detail.

Table 4.1 Components requirement for 8-bit multiplier with various compressors

S.No.	Multiplier architecture	Components	
		Name of the Component	Count
	Conventional structure using HA and FA	Half Adder	8
		Full Adder	48

Using proposed 3-1-1-2 compressor with 4:1 mux	XOR	30
	AND	45
	OR	15
	NOT	30
	4:1 Mux	30
Using proposed 3-1-1-2 compressor with 2:1 mux	XOR	30
	AND	45
	OR	15
	NOT	30
	4:1 Mux	15
	2:1 Mux	15
Using proposed 4-1-2 compressor	4-1-2	15
	FA	31
	HA	9
	XOR	1
Using existing multicolumn 5-3 compressor	4:1 Mux	80
	NOT	40
	HA	8
	FA	8
Using proposed multicolumn 5-3 compressor	4:1 Mux	40
	2:1 Mux	40
	NOT	40
	XOR	40
	HA	8
	FA	8

4.2 VEDIC MULTIPLIER DESIGN FOR 16x16 WITH PROPOSED COMPRESSORS

The proposed compressors are used in the 16x16 Vedic multiplier and, its partial product tree compressions are discussed with the help of the dot diagram.

4.2.1 Vedic Multiplier Design for 16x16 with Half Adders and Full Adders

The traditional partial product tree compression is considered to design a 16x16 Vedic multiplier using half adders and full adders. Figure 3.14 shows the dot diagram of the 16x16 multiplier design.

In the 16x16 multiplier, initially, 256 partial product terms are generated and assigned as P1 to P256. The PP terms are reduced using full adders and half adders in the step-by-step PP tree reduction process. The final product result is assigned as Z0 to Z31. In Figure 3.14, the PPs are reduced to two PPs in each column. After this step, the ripple carry adder is used to compute the end product result of the 16x16 multiplier.

4.2.2 Vedic Multiplier Design for 16x16 with Proposed 3-1-1-2 Compressor

The proposed 3-1-1-2 compressor is used in 16x16 Vedic multiplier designs. Figure 3.15 shows the dot diagram representation for a 16x16 multiplier with the proposed 3-1-1-2 compressor. The PP terms are reduced using a 3-1-1-2 compressor with the minimum usage of full adders and half adders in the step-by-step PP tree reduction process. The final product result is assigned as Z0 to Z31. In Figure 3.15, the PPs are reduced to two PPs in each column. After this step, the ripple carry adder is used to compute the end product result of the 16x16 multiplier.

4.2.3 Vedic Multiplier Design for 16x16 with Proposed 4-1-2 Compressor

The proposed 4-1-2 compressor is used in 16x16 Vedic multiplier designs. The dot diagram for the proposed 4-1-2 compressor based 16x16 multiplier is the same as shown in Figure 3.15. The proposed 3-1-1-2 compressor and the proposed 4-1-2 compressor have consisted of the same number of inputs and outputs. But the

proposed 4-1-2 compressor is used to compute four available bits initially, and it cannot be used with the previous column carry like 3-1-1-2 compressor because x_3 and x_4 need to feed through the initial stage gate.

4.2.4 Vedic Multiplier Design for 16x16 with Proposed 5-3 Multi-Column Compressor

The proposed 5-3 multi-column compressor is used in a 16x16 Vedic multiplier design to analyse the performance of the compressor. Figure shows the dot diagram of the proposed 5-3 compressor-based 16x16 multiplier. The PP terms are reduced using a 5-3 compressor with the minimum usage of full adders and half adders in the step-by-step PP tree reduction process. The final product result is assigned as Z_0 to Z_{31} . The 5-3 multi-column compressor gets five partial product inputs. Three partial products are received from the first column, and two partial products are received from the second column.

4.2.5 Logical Component Analysis of Proposed 16x16 Multiplier Designs with Conventional Design

The 16-bit Vedic multiplier is implemented using the proposed compressors and using conventional full adders and half adders. The logical components count is given in Table 3.3. The components are required logic gates to implement the 16-bit multiplier architecture. The area and delay comparison are discussed in chapter 3.6 and chapter 3.7 in detail.

Table 4.2 Components requirement of 16-bit multiplier with various compressors

S.No.	Multiplier architecture	Components	
		Name of the Component	Count
	Conventional using HA and FA	Half Adder	6
		Full Adder	223
		XOR	250

Using proposed 3-1-1-2 compressor with 4:1 mux	AND	375
	OR	125
	NOT	250
	4:1 Mux	250
Using proposed 3-1-1-2 compressor with 2:1 mux	XOR	250
	AND	375
	OR	125
	NOT	250
	4:1 Mux	125
	2:1 Mux	125
Using proposed 4-1-2 compressor	4-1-2	125
	FA	96
	HA	15
	XOR	1
Using existing multicolumn 5-3 compressor	4:1 Mux	388
	NOT	194
	HA	15
	FA	29
Using proposed multicolumn 5-3 compressor	4:1 Mux	194
	2:1 Mux	194
	NOT	194
	XOR	194
	HA	15
	FA	29

CHAPTER-5

APPROXIMATE VEDIC MULTIPLIER USING LOW ORDER COMPRESSORS

An approximate Vedic multiplier using low-order compressors is a digital circuit design that performs multiplication operations using the principles of the Vedic mathematics and incorporates low-order compressors to reduce hardware complexity and power consumption. Let's break down this concept:

1. **Vedic Multiplier:** Vedic mathematics is an ancient Indian system of mathematics that uses various techniques to simplify arithmetic operations. Vedic multipliers are based on these techniques and are designed to multiply two numbers efficiently. They often consist of a series of stages, each performing partial products and accumulating the final result.
2. **Low-Order Compressors:** A low-order compressor is a digital circuit that is used to compress binary numbers. It takes multiple binary inputs and generates a compressed output, reducing the number of bits required to represent the sum of those inputs. Common types of low-order compressors include Half Adders, Full Adders, and other similar logic gates.

To create an approximate Vedic multiplier using low-order compressors, you would typically follow these steps:

Partitioning: Divide the numbers you want to multiply into smaller parts, based on the principles of Vedic mathematics. These smaller parts can be processed in parallel or in a sequence. **Partial Product Generation:** Calculate partial products for each partitioned pair of bits in the input numbers. This can be done using bitwise AND operations. **Partial Product Accumulation:** Use low-order compressors, like Full Adders, to accumulate the partial products. You may also use other compressors like Carry Look-Ahead Adders or Carry Save Adders, depending on your design requirements.

5.1 High Order Compressor

The critical path of a multiplier is often related to the maximum height of PPM (partial product matrix). Thus, there is a need to compress the PPM. A $n:2$ compressor is a slice of a multiplier that reduces n numbers (i.e., product terms) to two numbers when properly replicated. The 4:2 compressor has 4 inputs X_1, X_2, X_3 and X_4 and 2 outputs Sum and Carry along with a Carry-in (C_{in}) and a Carry-out (C_{out}). The input C_{in} is the output from the previous lower significant compressor. The C_{out} is the output to the compressor in the next significant stage.

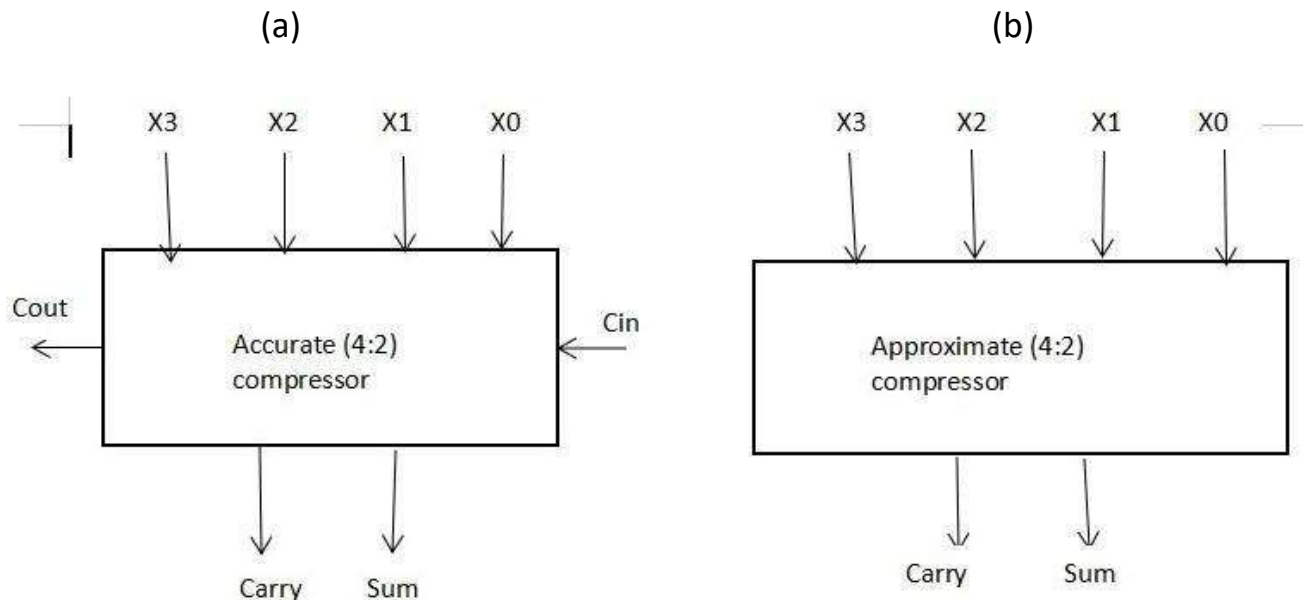


Fig. 5.1: (a) Accurate 4:2 Compressor (b) Approximate 4:2 Compressor

5.1.1 Approximation of carry

Half adder, the carry bit C_h is defined as $C_h(X_0, X_1) = X_0 \cdot X_1$

Full adder, the carry bit C_f is defined as $C_f(X_0, X_1, X_2) = X_0 \cdot X_1 + X_1 \cdot X_2 + X_0 \cdot X_2$. The Carry output of our approximate 5:2 compressor is $C_f(X_0, X_1, X_2) + C_h(X_3, X_4) + C_h(X_0 + X_1 + X_2, X_3 + X_4)$. The Carry output of our approximate 8:2 compressor is as $C_f(X_0, X_1, X_2) + C_f(X_3, X_4, X_5) + C_h(X_6, X_7) + C_f(X_0 + X_1 + X_2, X_3 + X_4 + X_5, X_6 + X_7)$.

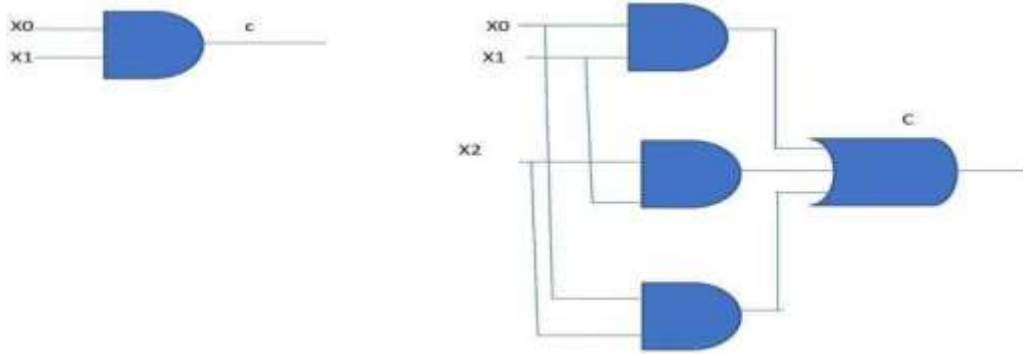


Fig. 5.2: Modified Half adder And Modified Full adder

5.1.2 Approximation of sum

Here, we study the approximation of the logic of Sum output. Conventionally, the tree of XOR gates are used to produce the output Sum. However, compared with other logic gates, XOR gate often has larger design overheads. We use the logic gates in SAED 32nm cell library as an example. We find that XOR gate has the largest power, the largest area, and the largest delay. Thus, if we can replace XOR gates with other logic gates, all the design overheads (including the power, the area and the delay) can be reduced.

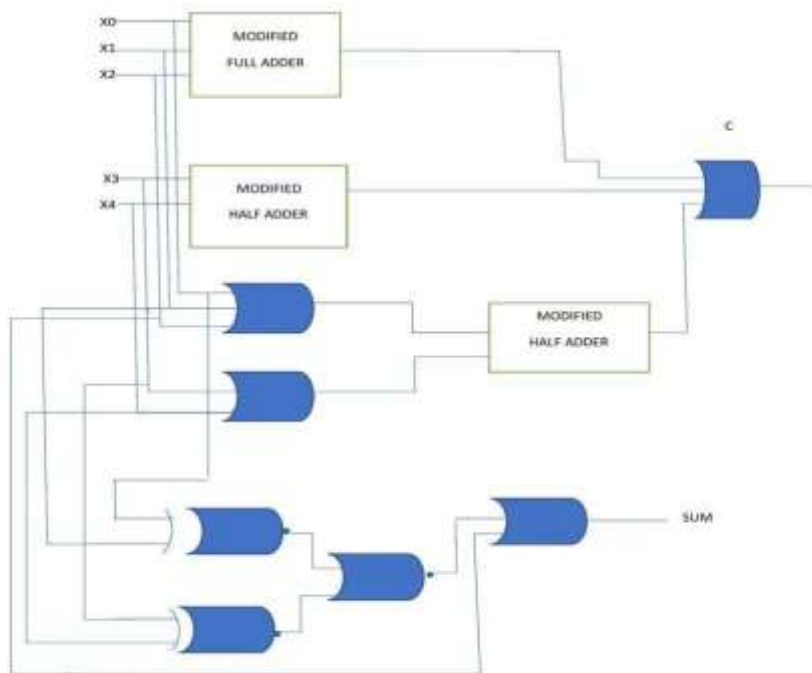


Fig. 5.3: Sum And Carry Output For 5:2 Compressor

5.2 Approximate Multiplier Design

To reduce the power consumption with a small error, our PPM reduction circuitry applies the significance driven logic compression technique as below: the higher significance weights use accurate (i.e., exact) 4:2 compressors; the middle significance weights use approximate high-order compressors; the lower significance weights use inaccurate compressors (OR-tree based approximation).

PPM reduction circuitry has two stages. The first stage is for all the weights

For each lower significance weight, we use a simple OR tree based approximation for power saving. Suppose that the number of inputs is n . If $n \leq 2$, no action is performed. On the other hand, if $n > 2$, we use an OR tree for $n-1$ inputs to approximate the accumulation result of these $n-1$ inputs. Thus, after the first stage is done, each lower significance weight has at most two product terms. For each middle significance weight, we use our approximate $n:2$ compressor for power saving, where n is the number of product terms in this weight.

The second stage is only for the higher significance weights. In order to achieve high accuracy, we use accurate (i.e., exact) 4:2 compressors to reduce the maximum height of the PPM. The carry bit C_{in} of the rightmost accurate 4:2 compressor is set to be 0. As shown in Fig. 5, after the second stage is completed, each highsignificance weight has two product terms.

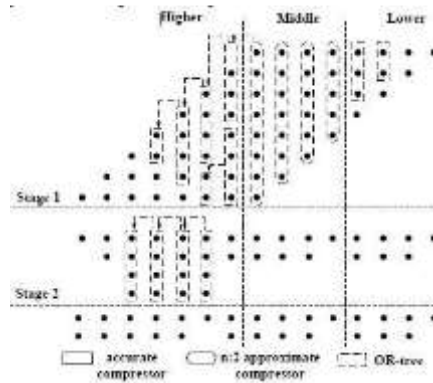


Fig. 5.4: PPM Reduction In Approximate Multiplier

CHAPTER-6

RESULT AND DISCUSSION

The performance of the proposed compressors, the 8x8 and 16x16 Vedic multipliers using the proposed compressors, are analyzed in both FPGA and ASIC technologies. The critical path delay, area, power, area delay product, power delay product, and energy delay product are compared with the existing architectures.

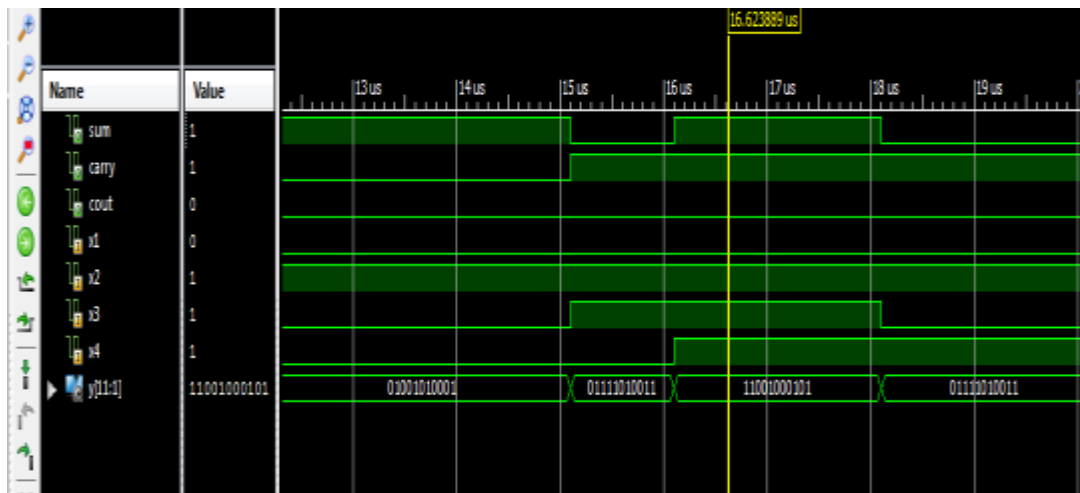


Figure 6.1 Functionality verification output for 4-1-2 compressor architecture

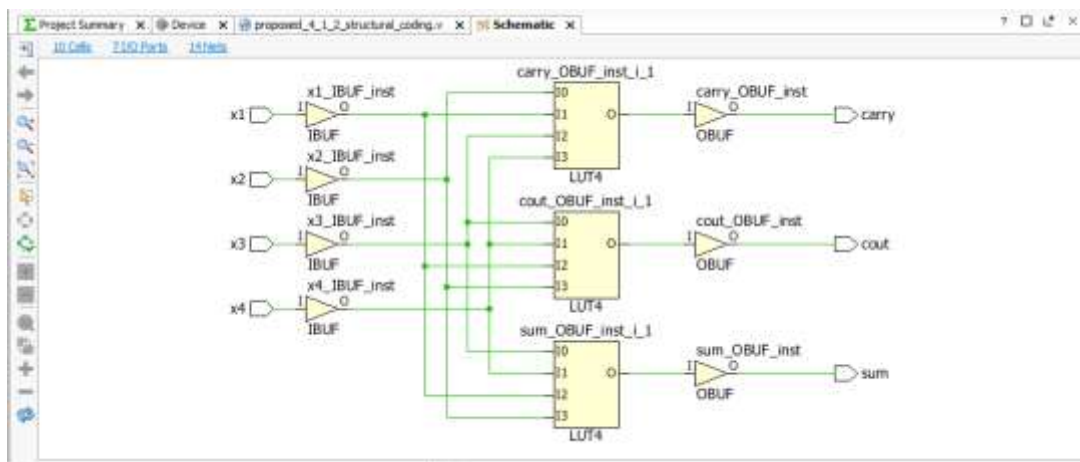


Figure 6.2 Technology schematic view of 4-1-2 compressor architecture

The technology schematic view of the proposed 3-1-1-2 compressor using 4:1 mux architecture is shown in Figure 3.19. The 4-1-2 compressor is required three LUT4. The 3-1-1-2 compressor using 4:1 mux architecture is required two LUT4 and one LUT3.

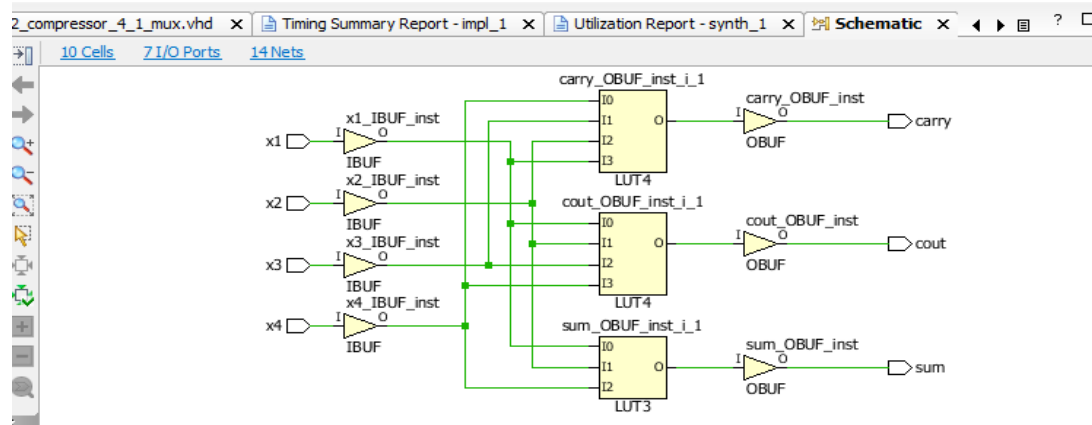


Figure 6.3 Technology schematic view of 3-1-1-2 compressor using 4:1 Mux architecture

Table 6.1 Combinational delay for various 4:3 compressors

Types	Output Bit position	Logic delay (ns)	Net delay (ns)	Path delay (ns)	Normalized path delay
Existing 4:3	2k	3.721	3.183	6.904	1.031
Ghumre et al. (2010)	2k+1	3.813	3.280	7.093	1.054
	2k+2	3.948	3.402	7.350	1.038
Existing 4:3	2k	3.639	3.059	6.698	1.000
Mehrabi et al. (2017)	2k+1	3.618	3.110	6.728	1.000
	2k+2	3.869	3.211	7.080	1.000
Proposed 3- 1-1-2 using 4:1 Mux	2k	3.703	3.047	6.750	1.008
	2k+1	3.547	2.900	6.447	0.958
	2k+2	3.350	3.187	6.537	0.923
Proposed 3- 1-1-2 using 2:1 Mux	2k	3.680	2.925	6.605	0.986
	2k+1	3.522	2.860	6.382	0.949
	2k+2	3.350	3.187	6.537	0.923
Proposed 4- 1-2	2k	3.933	3.056	6.989	1.043
	2k+1	3.563	3.082	6.645	0.988
	2k+2	3.639	3.060	6.699	0.946

6.1 Performance Analysis of Vedic 8x8 Multiplier in FPGA Technology

The Vedic 8x8 multiplier is designed using various proposed and existing compressors and coded in VHDL. The functionality verification, logic synthesis, and physical implementation of the proposed multiplier architectures are performed using Xilinx Vivado 16.4 software using the Zynq-7000 (xc7z020clg484) device. The functionality verification output and path delay characteristics view of 8x8 Vedic multiplier architecture using proposed 4-1-2 compressor architecture is shown in Figures respectively.

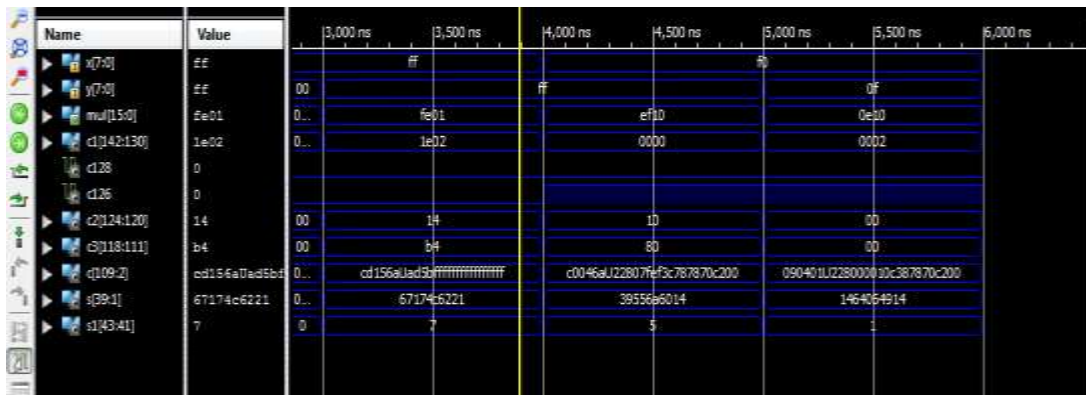


Figure 6.4 Functionality verification output for 8x8 Vedic Multiplier using proposed 4-1-2 compressor

The critical path delays for the 8x8 Vedic multiplier using various existing and proposed compressors are given in Table 3.10. The 8x8 Vedic multiplier using half adder and full adder is normalized to unity. From Figure 3.29, the normalized critical path delay is reduced by 7.47% in the proposed 4-1-2 compressor. The normalized critical path delay reduction in the proposed 3-1-1-2 compressor using 4:1 mux is 7.18%. The normalized critical path delay is reduced by 11.23% in the proposed 3-1-1-2 compressor using 2:1 mux. Similarly, the normalized critical path delay is reduced by 7.72% in the proposed 5-3 multi-column compressor, and the normalized critical path delay reduction in the proposed 8-1-3 compressor using 4-1-2 is 1.72%.

Table6.2 Combinational delay for various 8x8 Vedic multipliers

Types	Logic delay (ns)	Net delay (ns)	Path delay (ns)	Normalized critical path delay
Using HA and FA	5.706	12.499	18.205	1.000
Using existing 4-3 compressor	5.440	8.689	14.129	0.776
Existing 5:3 multicolumn	5.140	8.359	13.499	0.741
Existing 8:3	5.363	8.241	13.604	0.747
Using proposed 4-1-2 compressor	4.661	8.413	13.074	0.718
Using proposed 3-1-1-2 compressor with 4:1 mux	4.966	8.148	13.114	0.720
Using proposed 3-1-1-2 compressor with 2:1 mux	4.708	7.834	12.542	0.689
Using proposed 5:3 multicolumn	4.834	7.623	12.457	0.684
Using proposed 8-1-3 using 4- 1-2	5.245	8.125	13.370	0.734

6.2 Performance Analysis of Vedic 16x16 Multiplier in FPGA Technology

The Vedic 16x16 multiplier is designed using various proposed and existing compressors and coded in VHDL. The functionality verification, logic synthesis, and physical implementation of the proposed multiplier architectures are performed using the Zynq-7000 device.

The critical path delays for the 16x16 Vedic multiplier using various existing and proposed compressors are given in Table 3.11. The 16x16 Vedic multiplier using half adder and full adder is normalized to unity. From Figure 3.30, the normalized critical path delay is reduced by 7.96% in the proposed 4-1-2 compressor. The normalized critical path delay is reduced by 9.47% in the proposed 3-1-1-2 compressor using 4:1 mux. The normalized critical path delay reduction in the proposed 3-1-1-2 compressor using 2:1 mux is 16.23%. Similarly, the normalized

critical path delay is reduced by 13.09% in the proposed 5-3 multi-column compressor, and the reduction in the proposed 8-1-3 compressor using 4-1-2 is 8.64%.

Table6.3 Combinational delay for various 16x16 Vedic multipliers

Types	Logic delay (ns)	Net delay (ns)	Path delay (ns)	Normalized path delay
Using HA and FA	22.82	50.00	72.82	1.000
Using existing 4-3 compressor	21.76	34.76	56.52	0.776
Existing 5:3 multicolumn	20.56	33.44	54.00	0.741
Existing 8:3	21.45	32.96	54.42	0.747
Using proposed 4-1-2 compressor	18.36	33.65	52.02	0.714
Using proposed 3-1-1-2 compressor with 4:1 mux	18.57	32.59	51.16	0.703
Using proposed 3-1-1-2 compressor with 2:1 mux	16.01	31.34	47.34	0.650
Using proposed 5:3 multicolumn	16.44	30.49	46.93	0.644
Using proposed 8-1-3 using 4-1-2	20.14	29.58	49.72	0.683

CHAPTER-7

CONCLUSION

All approximate multipliers are designed for $n = 8$. The multipliers are simulated using Verilog code in Model Sim tool and synthesized using Xilinx ISE 9.1i. This paper has presented a partial product array based 4×4 ($M \times A \& L \times A$) multipliers using a probabilistic analysis. High performance NOR based Half Adder ($N \times HA$) and Full Adder ($N \times FA$) cells have been proposed for using 4×4 Multiplier. Mainly this proposal was done to reduce the time and increasing the speed of processing of the error tolerant application likes compressing files to the minimum bytes or in image processing applications, because in our recent days the researchers are trying to minimize speed of processing work to compensate the time of finishing the work. We know that whenever increasing the speed and reducing the time of the work the error of calculation also increases, to reduce that, we using compensate circuit the proposed approximate multiplier can be used in the image processing, due to the error distance close to 23.8 percentage. There are many compensations circuit compressor based, rounding based but here only we adding mean error to the output so this a mean error compensating circuit. By using this 4×4 approximate multiplier we can built large multipliers, which is also have the maximum lust close to 15 percentage. Advantage of this approximate multiplier is we can add the whatever mean value while compensation according the requirements of the user. Whenever we reducing the wires, adders the area of the design.

REFERENCES

- [1] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie and C. Lucas, "BioInspired Imprecise Computational Blocks for Efficient VLSI Implementation of Soft-Computing Applications," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 4, pp. 850-862, April 2010, doi: 10.1109/TCSI.2009.2027626.
- [2] Jiangmin Gu and Chip-Hong Chang, "Low voltage, low power (5:2) compressor cell for fast arithmetic circuits," 2003 IEEE International Conference on Acoustics, Speech, and Signal Processing, 2003. Proceedings. (ICASSP '03)., Hong Kong, China, 2003, pp. II-661, doi: 10.1109/ICASSP.2003.1202453.
- [3] Chip-Hong Chang, Jiangmin Gu and Mingyan Zhang, "Ultra lowvoltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 10, pp. 1985-1997, Oct. 2004, doi: 10.1109/TCSI.2004.835683.
- [4] A. G. M. Strollo, E. Napoli, D. De Caro, N. Petra, G. Saggese and G. Di Meo, "Approximate Multipliers Using Static Segmentation: Error Analysis and Improvements," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 6, pp. 2449-2462, June 2022, doi: 10.1109/TCSI.2022.3152921.
- [5] A. G. M. Strollo, E. Napoli, D. De Caro, N. Petra, G. Saggese and G. Di Meo, "Approximate Multipliers Using Static Segmentation: Error Analysis and Improvements," in IEEE Transactions on Circuits and 23 Systems I: Regular Papers, vol. 69, no. 6, pp. 2449-2462, June 2022, doi: 10.1109/TCSI.2022.3152921.

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