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Approximate vedic multiplier using low order compressors

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Abstract- In the ever-evolving landscape of digital computation, efficient multiplication remains a critical operation. This paper introduces an innovative approach to accelerate multiplication processes by combining the ancient wisdom of Vedic mathematics with modern low-order compressors. We propose an approximate Vedic multiplier that balances computational speed and resource efficiency, making it ideal for applications where precise multiplication results can be modestly compromised. The Vedic multiplication system, originating from ancient Indian mathematical texts, offers a range of multiplication techniques known for their efficiency and versatility. However, their direct application to contemporary digital hardware may pose challenges, especially in resource-constrained environments. Our research addresses this challenge by introducing a novel approximation technique that leverages low-order compressors. These compressors have proven to be valuable tools for designing efficient hardware implementations and are particularly well-suited for our purpose. In this paper a new approximate low compressor model is proposed for less complex multiplication process. The proposed compressor design uses less hardware resources and less energy as compared to existing compressors. When compared with other existing multipliers with bit size of 4×4. The proposed multiplier gives approximately 20% reduction in area and Delay.

Keywords: Approximation Modules, Low-Order Compressors Integration, Vedic Multiplier.

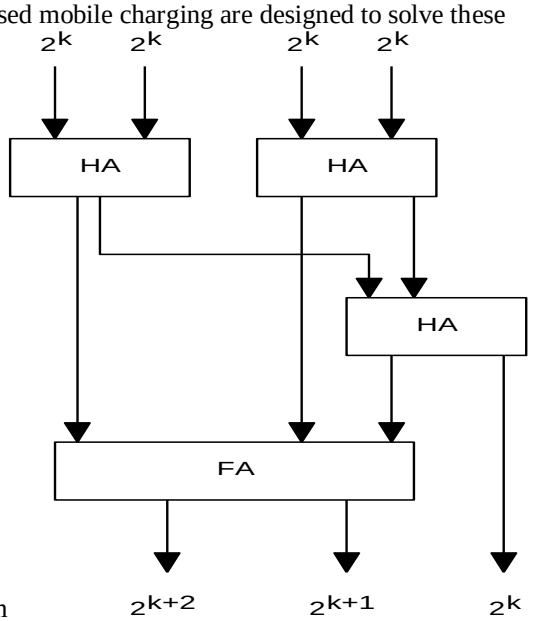
1. INTRODUCTION

While using computers and smart phones sometimes we face a situation where the device (hangs) stops responding. One of the reasons behind it is processor speed that motivated us to go for a high speed multiplier design. Multiplier in special application processors like Digital Signal Processor (DSPs) improves the speed of operation since the entire signal and data processing operations involve multiplication. Multiplication plays a vital role in DSP applications (like DFT, convolution, FFT etc.), Arithmetic and logic unit (ALU), and Multiply and Accumulate (MAC) unit. High Speed Multiplication thus becomes a necessity to increase the performance of processor. Quite a few multipliers have been designed and proposed over last few decades but for multiplication these designs need several intermediate stages to calculate the final result due to which critical path length increases hence cause more delay. Moreover, the intermediate stages need additional hardware which becomes reason for increased area and power consumption. and a new approach for multiplier design based on Vedic Mathematics is explored to overcome these disadvantages. Vedic Mathematics is an ancient and prominent approach that serves as base to solve many mathematical challenges experienced nowadays.

2. RESEARCH METHODLOGY

2.1: Existing Compressor:

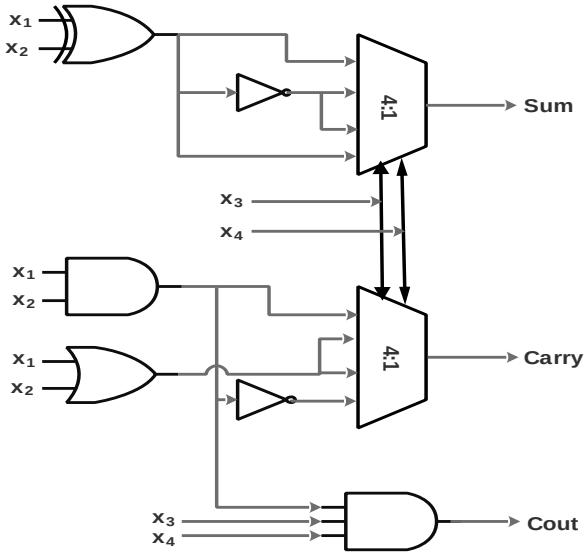
Now a days students and many other people use the public transportation ,people who are making every long journey in order attend business conventions ,conferences, or for any private purpose don't know their battery level is low and they often forget their charger at home or it in hotel room. Many critics argued that long distance travelling vehicles provides power points. Even through one or two power points are provided at a particular place in the vehicles it is not all sufficient for all passengers, therefore need to provide a public charging service is essential and coin based mobile charging are designed to solve these problem

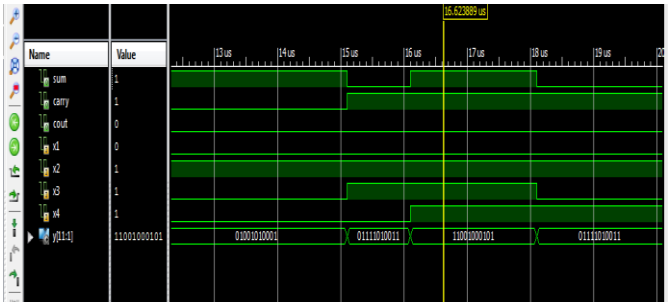


2.2: Proposed Compressor:

The proposed high speed area-efficient approximate 3-1-1-2 compressor is implemented in this section. The existing 3-1-1-2 compressor consumes more area and power in order to minimize the resources utilization. Approximation is introduced in the design. The approximate compressor accepts four inputs and produce two outputs are sum and carry. The compressor inputs are X1, X2, X3 and X4, outputs are Carry' and Sum. In the design of approximate 3-1-1–2 compressor Sum and carry can be generated using a multiplexer (MUX) based design approach. Output of XOR gate(X3 XOR X4) acts as the select line for the MUXes.

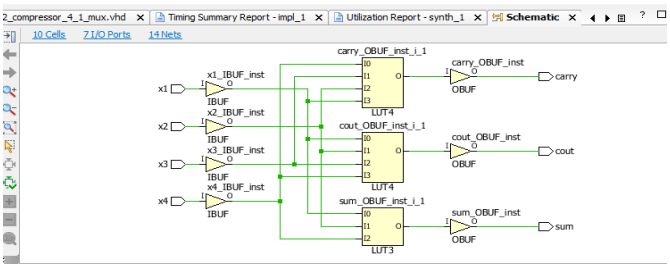
When select line goes high, (X1 XOR X2) is selected and when it goes low, (X1 XNOR X2) is selected for sum operation. For carry operation when select line goes high, (X1 OR X2) is selected and when it goes low, (X1 AND X2) is selected.

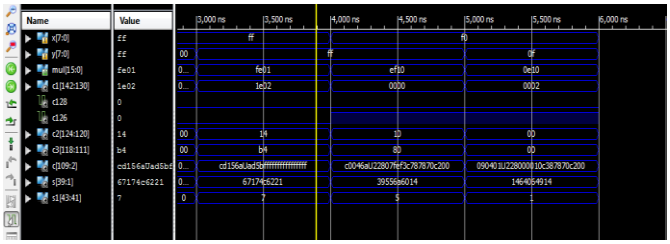




3.Software implementation

In this section proposed approximate compressor and multiplier is simulated and synthesis by Xilinx ISE 14.7 and vivado 2019.2 are discussed. For the better comparison propose between existing Vedic multiplier in [14] and proposed multiplier is implemented using Xilinx ISE 14.7





From the synthesis report it is observed that Existing Vedic [1] multiplier takes 20 LUTs for the designing the system but Proposed Vedic multiplier is designed using 17 LUTs ,so 15% area efficient than the existing multiplier and Existing Vedic multiplier Delay is 3.501ns for the system but Proposed Vedic multiplier Delay is 2.62ns ,so 25% Delay is reduced in proposed system when compared with existing system. From that it is noticed proposed system is faster than existing system. From the overall report proposed system is optimized in aspect of Area and Delay as compared to existing system.

4. CONCLUSION

In this paper, we proposed a method to design approximate 3-1-1-2 compressor. by using proposed compressor Vedic multiplier is designed. This approach minimize the active logic gate count compared with the exact 3-1-1-2 compressor, the proposed compressor designs achieve a significant reduction in power consumption, area utilization, and delay. From Simulation results and synthesis report it is indicate that the utilization of the proposed models brings significant improvement to the resource performance of multipliers. At the same time, the proposed multipliers keep a tolerable error performance. In conclusion, this work has shown that multiplier can be used for approximate computing by an approximate design of a compressor; this proposed multiplier gives better results in terms of design parameters compared to existing multipliers, and in terms of accuracy metrics, critical path delay, area and power.

5.REFERENCES

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