TDC mezzanine | Performance testing

The document describes different tests on the TDC mezzanine that aim at assessing its performance. You could also consult the [TDC precision documentation](http://www.ohwr.org/projects/fmc-tdc/repository/changes/board_testing/TDCprecision.pdf).[1]

**Test Setup 1 | Cable Length**

We use the PCIE\_FMC\_TESTBENCH5 front end in the 864-1-A17 lab where we plug two SPEC carrier boards as Figure 1 indicates.

SPEC 1 carries a Fine Delay mezzanine, used as pulse generator. SPEC 2 carries the TDC mezzanine under test. The CLOCK FAN\_OUT board is also used. Figure 2 shows how pulses should be arriving to each one of the TDC channels.

A dedicated python testing program is responsible for the continuous retrieval of the timestamps and their manipulation: only timestamps corresponding to rising edges are kept and they are subtracted by pairs. This way the delay introduced by the coaxial cable is the constant value on which the precision testing is based.

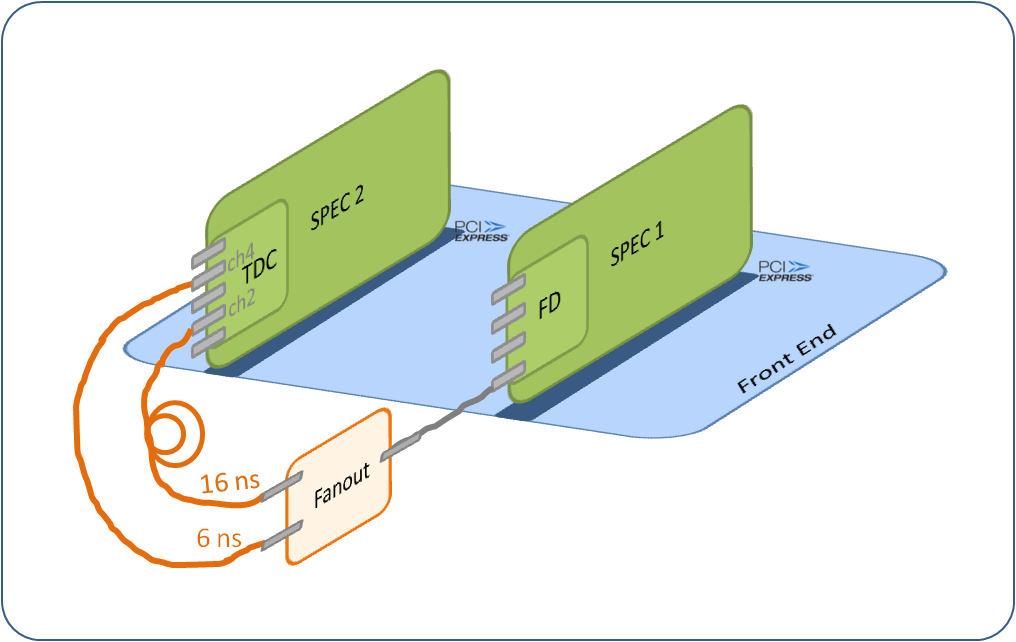


Figure : Test setup 1

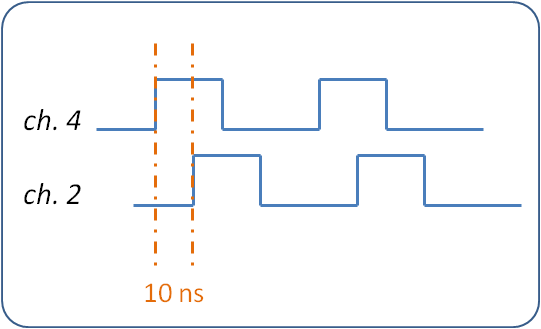


Figure : Pulses arriving to the TDC input channels 2 and 4

[1]: Note that in this documentation, the +-4ns spikes were removed for the data processing in order to focus on the precision definition.

The board #007 was tested at two different moments. 10 M measurements were acquired per test. Figures 3 and 4 show the 10 M data for the two tests.

Note in Figure 3 the 14 spikes and in Figure 4 the 9 spikes at around mean\_value +-4 ns. This 4 ns offset comes from the ACAM fine time; we believe it is caused by a bug in the ACAM chip. The error rate is ~1 wrong timestamp per 2 M. We have remarked that this issue could be related with Tomasz Wlostowski issue on ACAM R-mode, where he was seeing wrong measurements of around +-1.5ns every few millions. The resolution in R-mode is 3 times higher than in I-mode and the errors seen in I-mode (~4ns) are 3 times the ones in in R-mode (~1.5\*3 = ~4ns). We are in contact with ACAM for the clarification of the issue.

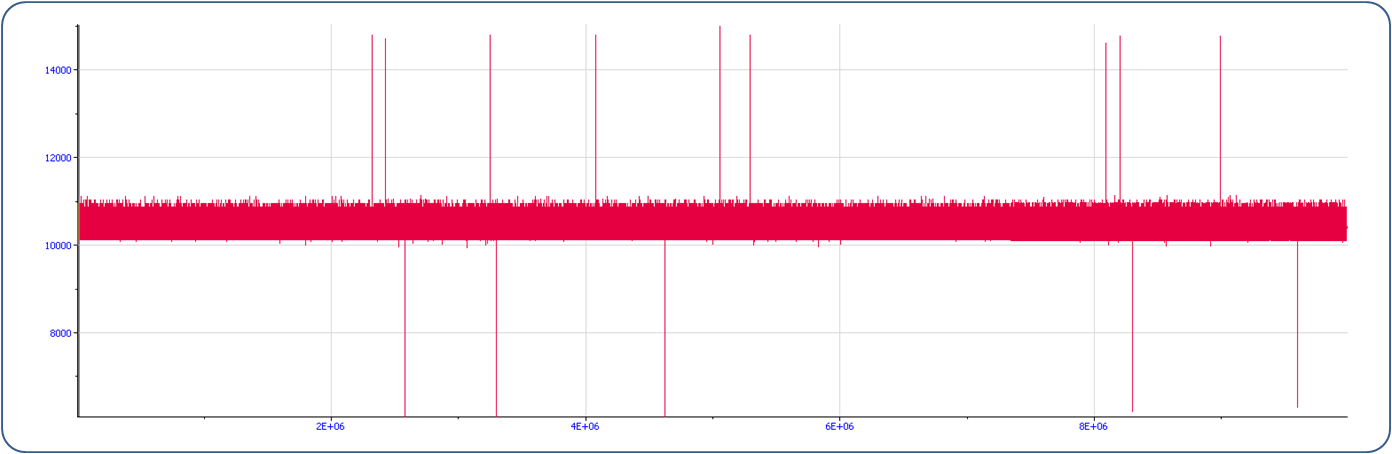


Figure : Test Setup 1 Test#1 measurements

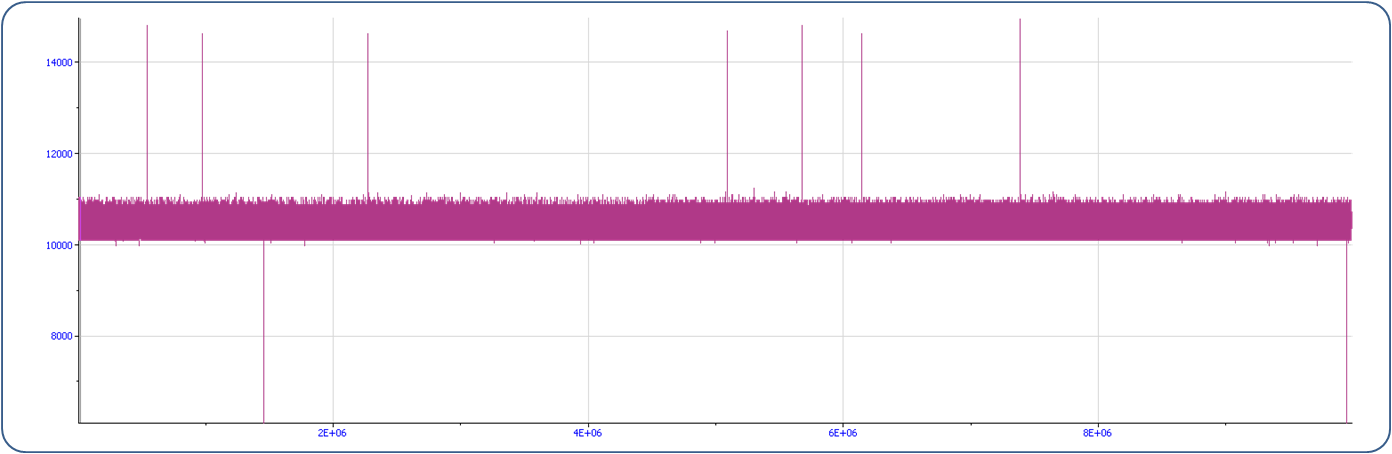


Figure : Test Setup 1 Test#2 measurements

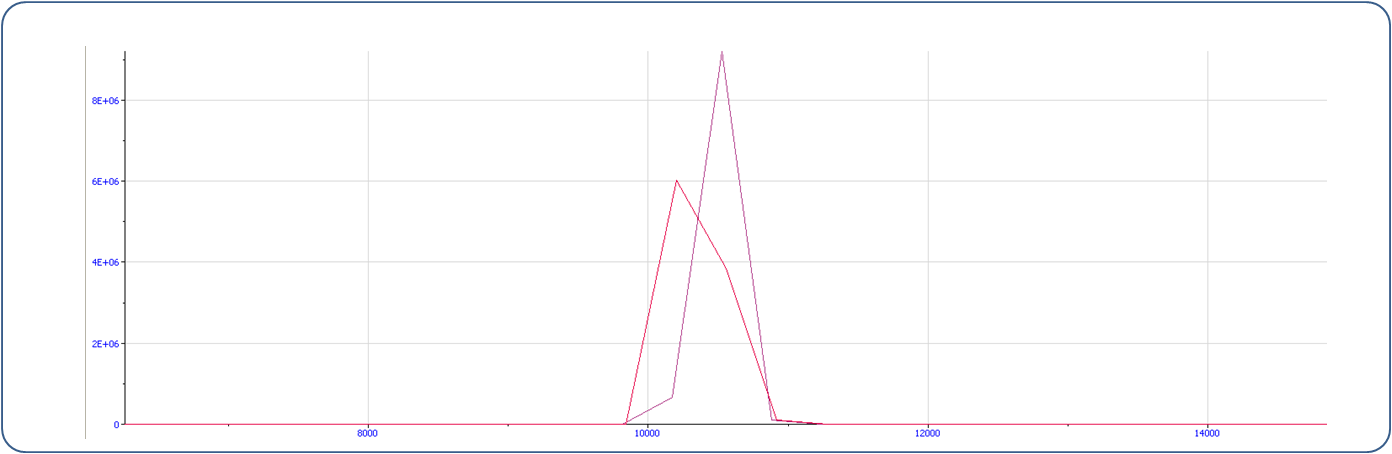


Figure : Histograms from measurements of Figures 3 and 4

Table 1 summarizes the measurements main statistics.

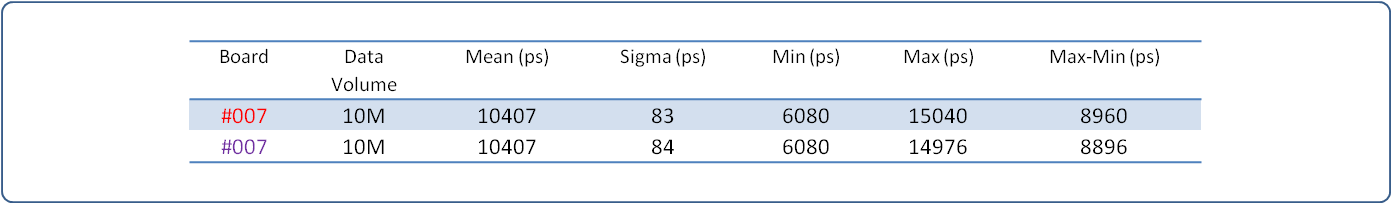


Table : Summary from measurements of Figures 3 and 4

Removing the +-4 ns spikes, gives the following clean measurements.

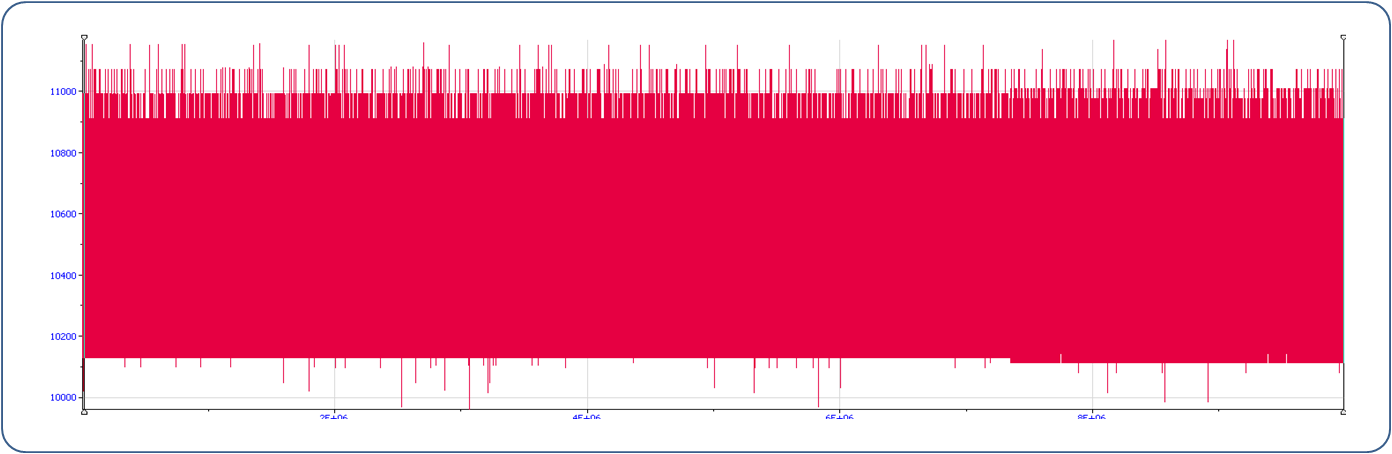


Figure : Test Setup 1 Test#1 measurements without 4 ns spikes

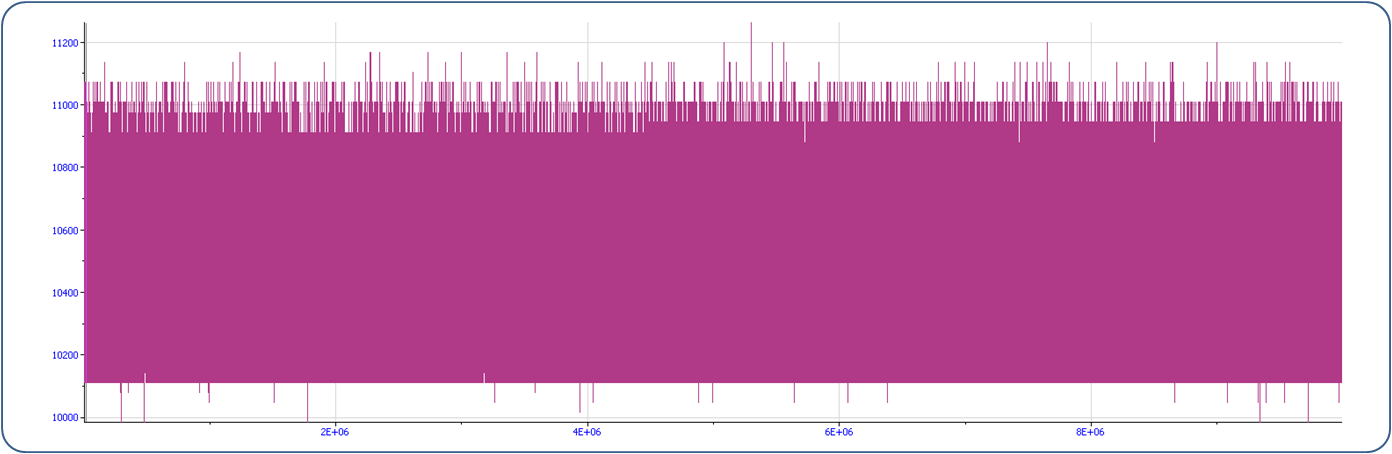


Figure : Test Setup 1 Test#2 measurements without 4 ns spikes

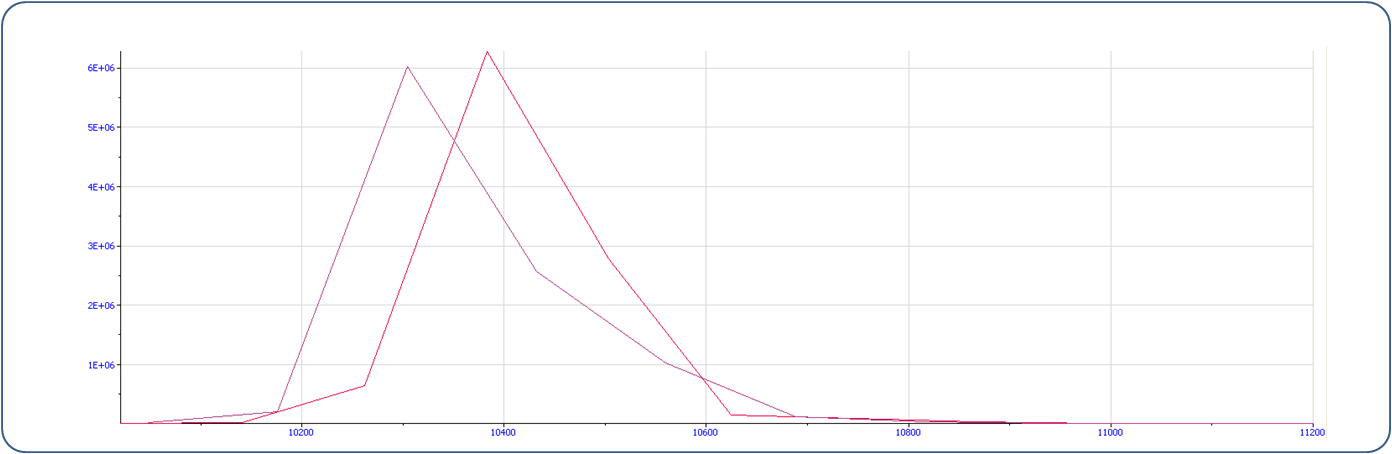


Figure : Histograms from measurements of Figures 6 and 7

Table 2 summarizes the main statistics without the 4ns spikes.

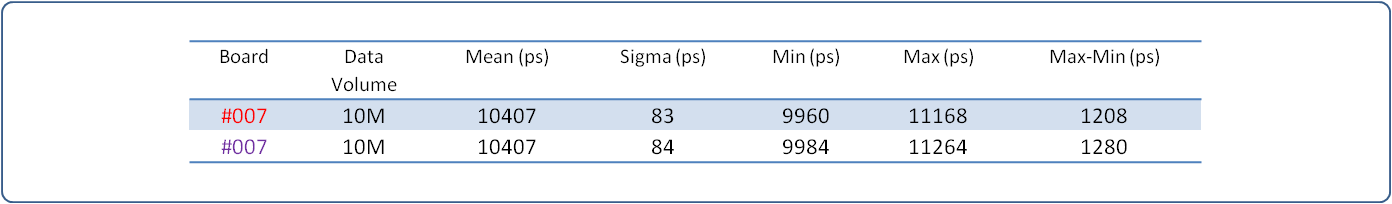


Table : Summary from measurements of Figures 6 and 7

Regarding the accuracy of the measurements, note that instead of 10’000 ps, which is the difference in cable length, we are measuring 10’407 ps; this comes from the part-to-part skew of the channels input buffers and the different path delays on the board. The calibration procedure will eliminate this offset.

**Test Setup 2 | Cesium 1 PPS**

We use the PCIE\_FMC\_TESTBENCH7 front end in the 864-1-A19 lab where we plug one SPEC carrier board. As pulse generator we use the 1 PPS output of the Cesium Clock. Figure 9 shows the setup and Figure 10 the pulses arriving to the TDC input channel.

A dedicated python testing program is responsible for the continuous retrieval of the timestamps and their manipulation: only timestamps corresponding to rising edges are kept and they are subtracted by pairs. This way we are expecting constantly measurements of 1 second.

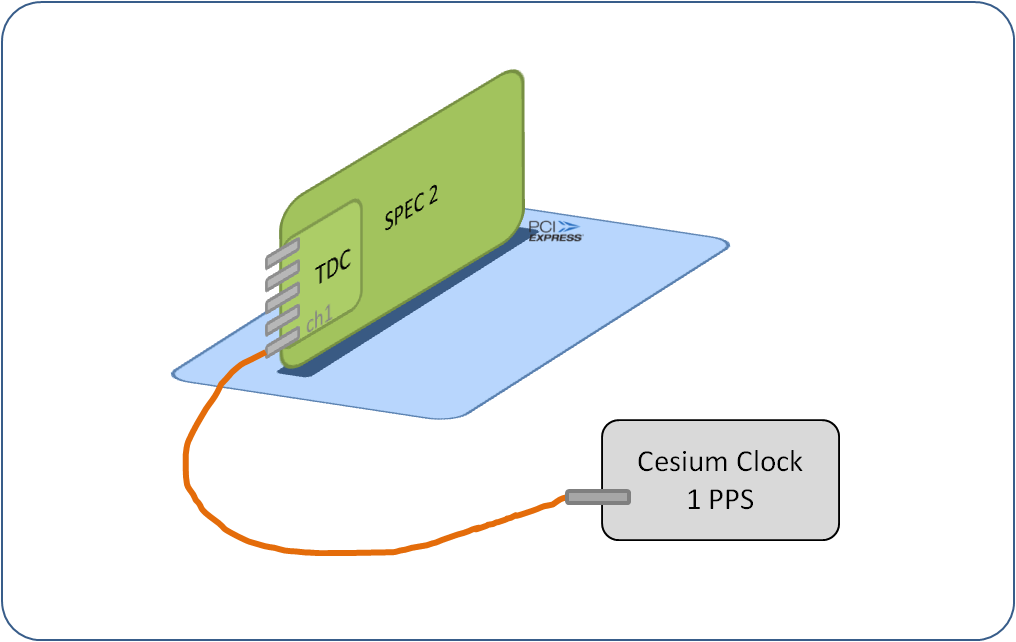
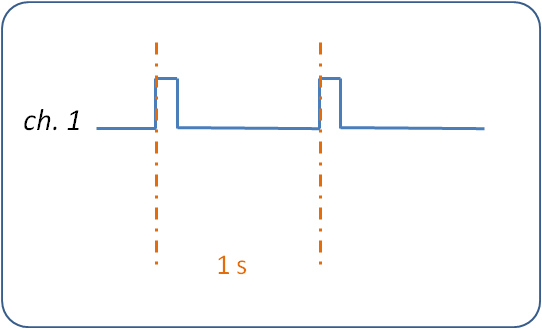


Figure : Test Setup 2



# Figure 10: Pulses arriving to the TDC input channel 1

Figure 11 shows in blue the 400 K measurements that were acquired during ~10 days. In green are the temperature measurements from the One-Wire temperature sensor on the TDC board.

Note that the timebase accuracy of the TDC application is by specification +-4 ppm; for a measurement of   
1 s this translates to a margin of +-4’000’000 ps. From Table 3, the span of our measurements was limited to  
< 200’000 ps.

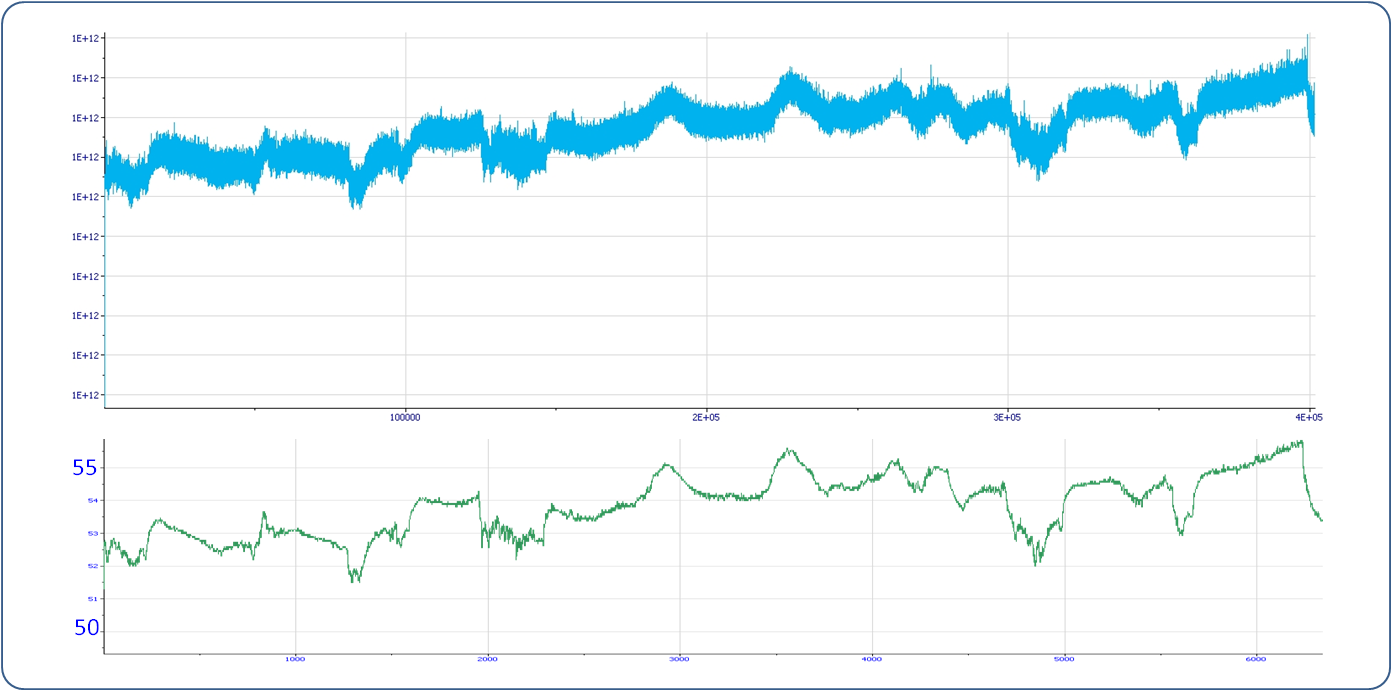


Figure : Test Setup 2 timestamp measurements (in blue) and temperature measurements (in green)

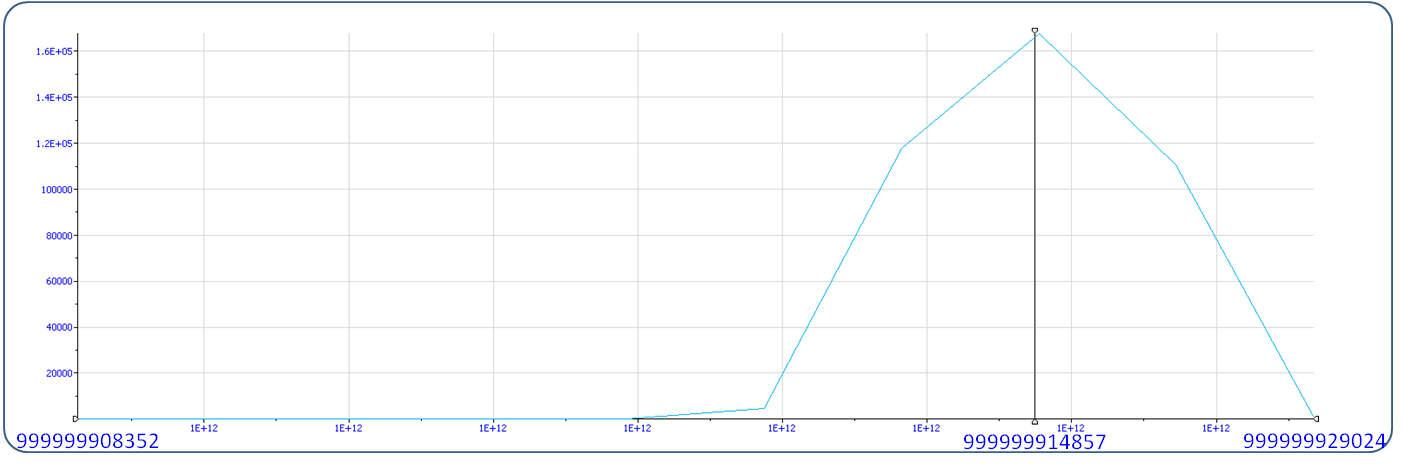


Figure : Histogram from timestamp measurements of Figure 11

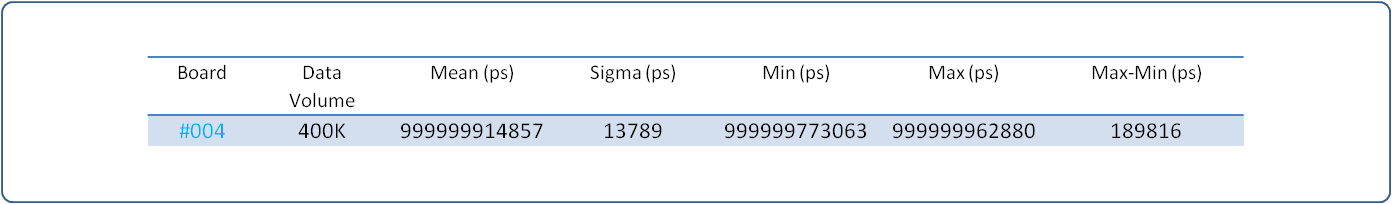


Table : Summary from timestamp measurements of Figure 11

Note that in these measurements because of the +-4ppm span, the eventual +-4ns spikes cannot be distinguished.

Changing the DAC from 1V65 (DAC word 0xA8F5) to 1V66 (DAC word 0xAA00) shifts the measurements to higher values. Figure 13 shows both data spanning over around 6 hours at a relatively stable temperature. Note though that since the tests took place at different moments, the temperature has not been the same for the two versions.

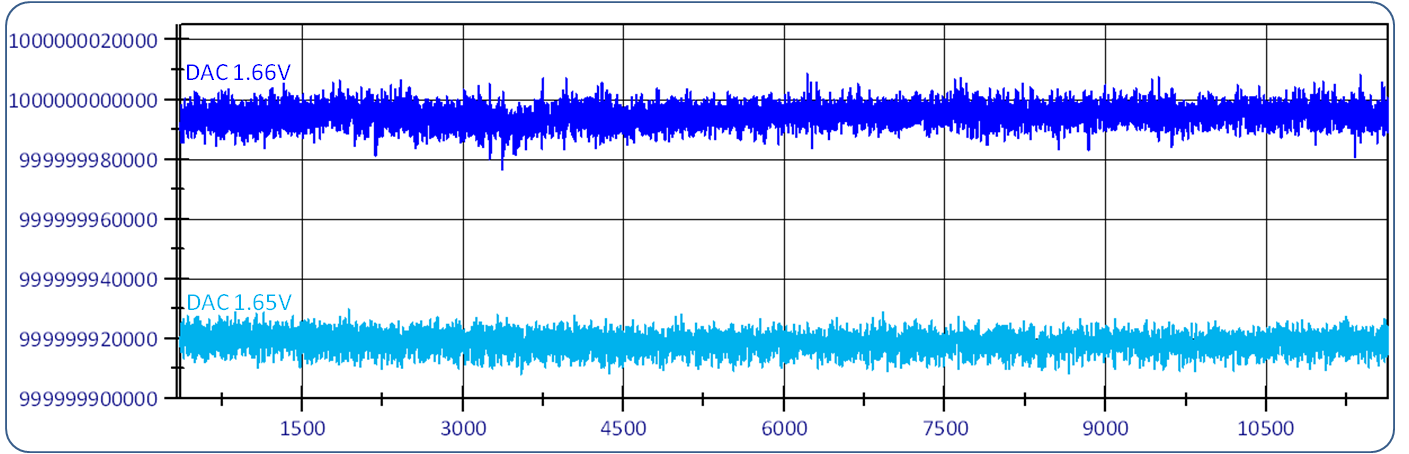


Figure : Test Setup 2 measurements with different DAC values

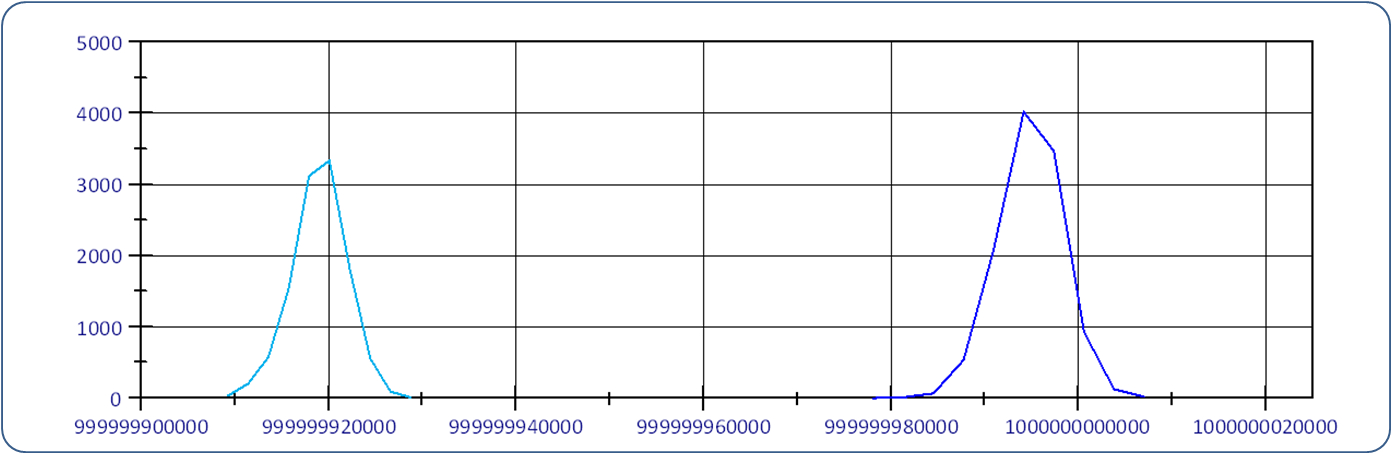


Figure : Histogram from measurements of Figure 14

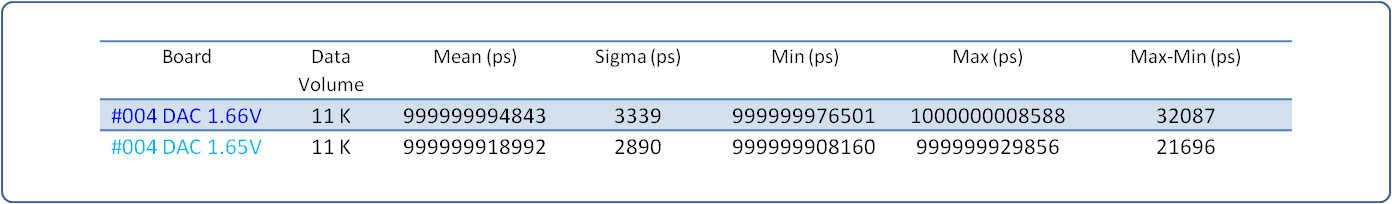


Table : Summary from measurements of Figure 14

Regarding the accuracy of the measurements, the calibration procedure will set the DAC to its optimal value.

# Test Setup 3 | Sweeping

We use the PCIE\_FMC\_TESTBENCH5 front end in the 864-1-A17 lab where we plug two SPEC carrier boards as Figure 15 indicates.

SPEC 1 carries a Fine Delay mezzanine, used as pulse generator at different frequencies. SPEC 2 carries the TDC mezzanine under test.

A dedicated python testing program is responsible for setting the fine delay output period to a range of values from 100 ns to 150 us with steps of 20 ns [2]. For each period value, 128 pulses are sent. The TDC timestamps are retrieved and manipulated: only timestamps corresponding to rising edges are kept and they are subtracted by pairs.

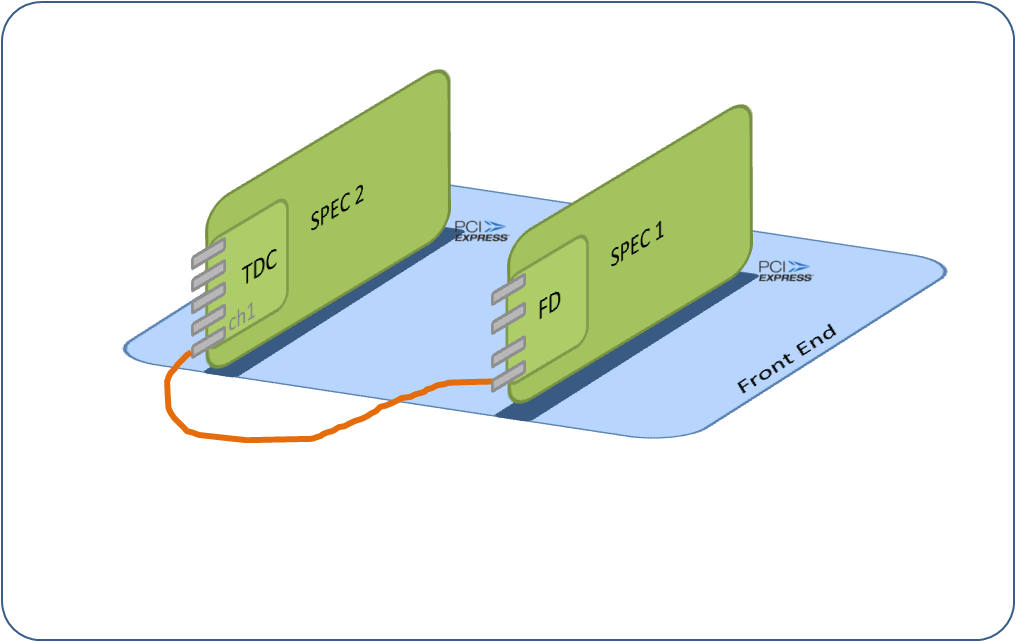


Figure : Test Setup 2

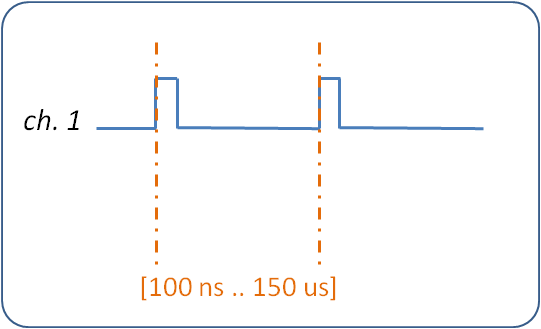


Figure : Pulses arriving to the TDC input channel 1

[2] Because of system limitations the sweeping above 150us is currently not possible. In detail because of the TDC and FD drivers incompatibility, the FD board is used uncalibrated; this makes the values above 150us giving errors > 4ppm, so there would be no reliable reference for our testing.

Figure 17 shows the 500 K data ranging from 100 ns to 150 us.

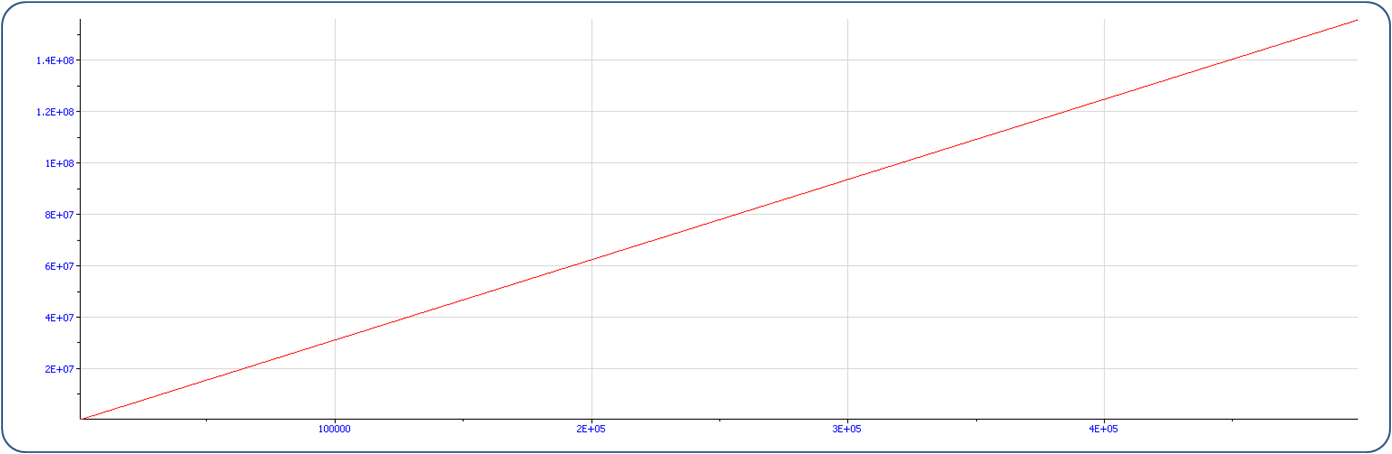


Figure : Test Setup 3 measurements

Zooming into Figure 17 brings us to Figure 18 that shows the first steps of this test. Note the 64 measurements per step.

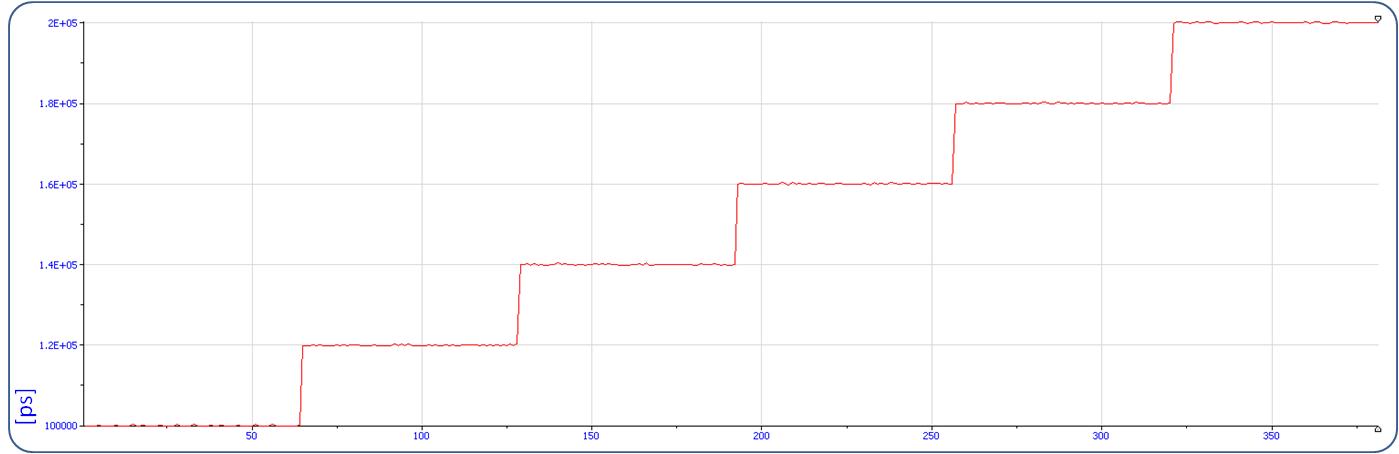


Figure : Zoom in Figure 15

The measurements stayed within the range of the accuracy of the TDC plus the FD:

[+-700 ps +- 4 ppm] + [+-500 ps +- 4 ppm].

With different DAC values, the higher the measurements, the bigger the difference in measurements.

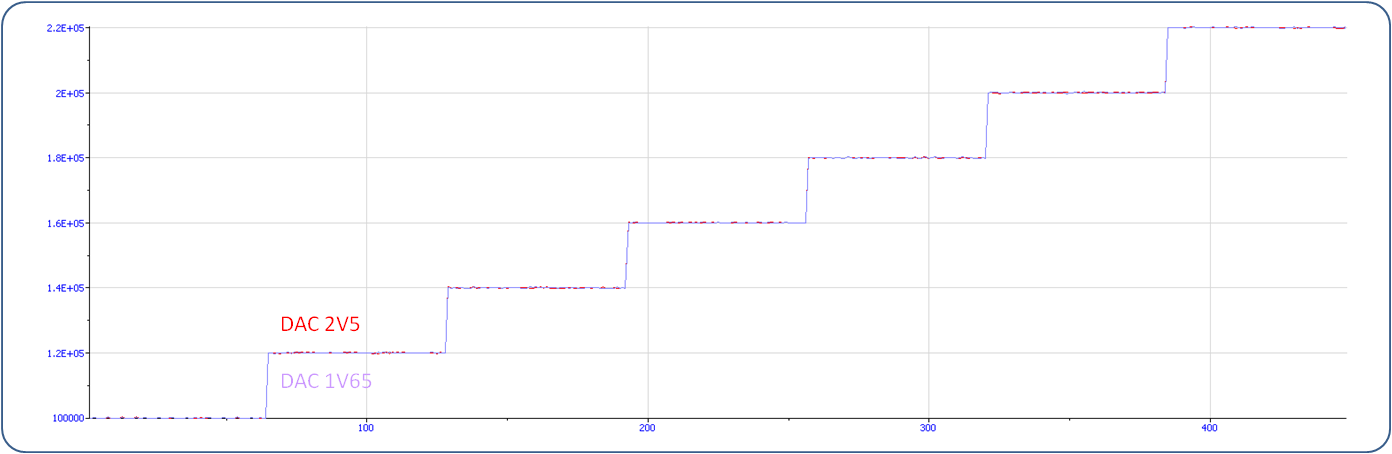


Figure : Measurements at around 100 ns with different DAC values

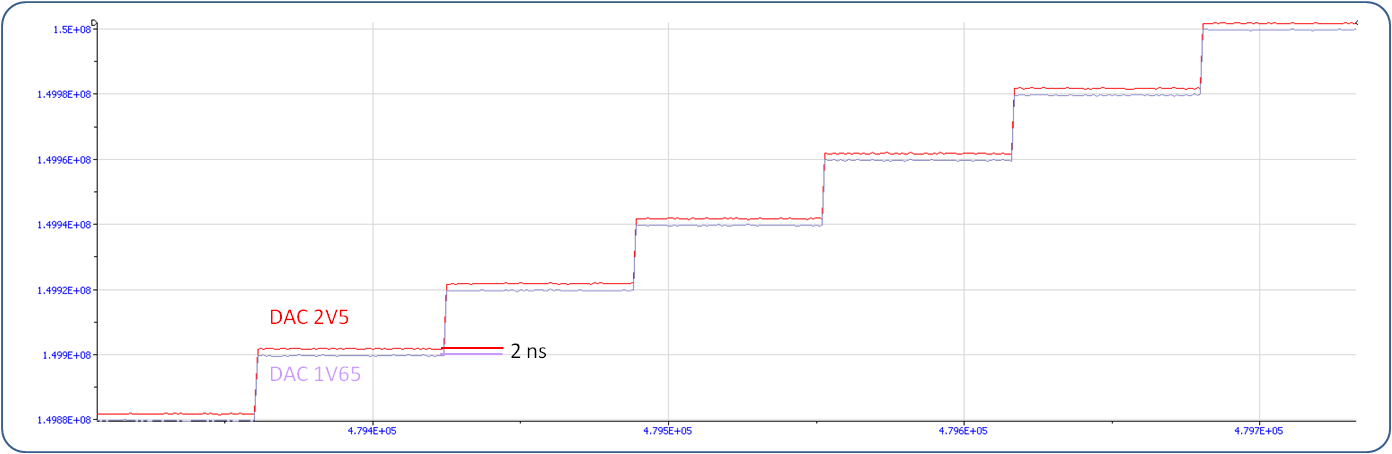


Figure : Measurements at around 150 us with different DAC values

**Conclusions**

The tests have confirmed the general reliability of the TDC board. Its precision is within the +-700ps +-4ppm specification. The issue of the +-4ns spikes with 0.5ppm occurrence however would need to be clarified in collaboration with the ACAM engineers.

The calibration procedure would eliminate the offsets coming from the different channel paths.

The calibration procedure would also seek for the optimal DAC value.