IP CORE

CPU

AXI LITE

AXI LITE

BRAM CTRL

AXI Lite CTRL

MEMORY SUBSYSTEM

READY

START

GR

CH

BLOCK_TYPE

4-bit

IMDCT

ROM 32x144

sine_block [0]

sine_block [143]

BRAM 32x36

sample_block[0]

sample_block[35]

BRAM 32x1152

prev_samples[0]

prev_samples[1151]

BRAM 32x4608

samples_in [0]

samples_in [2303]

samples_out [2304]

samples_out [4607]

BRAM inteface

IMDCT

READY
START
GR
CH
BLOCK_TYPE

addrb
doutb
dinb
en
web

sine_addr_o
sine_data_i
sine_en

sb_addr_o
sb_data_i
sb_data_o
sine_en
sine_wen

ps_addr_o
ps_data_i
ps_data_o
ps_en
ps_wen