Brake System Plausibility Device

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1 Introduction

With electronic throttle control systems becoming mandatory for FSAE competitions so are BSPDs . Brake System Plausibility Device (BSPD) is a standalone non-programmable circuit, witch must stop the current provision when hard braking occurs and the throttle position is more than 25 percent over the idle position for more than 500ms . Furthermore throttle and brake sensors must be able to be disconnected separately .

2 Regulator

As a circuit BSPD works with a 5 volts V_{DD} but the cars battery provides 12 volts in order to reduce the voltage an LM340MP regulator was selected with 3 decoupling capacitors as shown in Fig. 1. Because the car battery is positioned away from the PCB, in case of a momentary high load there is a chance of a voltage drop due to the wiring. In that case the input capacitor of the regulator C_1 provides the circuit the mandatory load for a small period of time. The regulators output capacitor improve stability, the time response of the regulator and filter part of the noise of the bandwidth. The values of the capacitors were selected according to the data sheet.

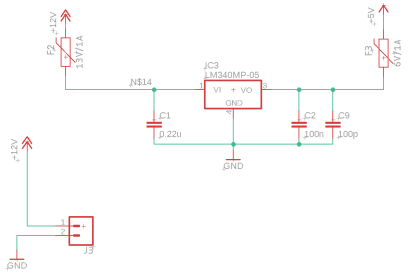

Figure 1: Regulator circuit

3 Comparisons and Implausibility Verification

In order to disconnect the sensor separately at any given time they must not be in the PCB and they are connected with it with a pin connector. In both sensor signal a 50K pull down resistance is connected thus when disconnecting the sensors the input signal will not be floating . The value of those resistances must be much higher of the sensor resistance in order not to interfere with the input signal. The signal from both sensor passes through an operational amplifier comparing the signals voltage with a threshold set by the user via a potentiometer in order do detect hard breaking and the throttle position. When the signal voltage is higher than the threshold op-amp is triggered providing 5 volts at the output. A 5K ohm pull up resistor is placed on output in case of an op-amp failure to provide 5V output. Both signals are connected with 2 nand gates (making an AND gate) to pass a high signal only if both throttle and brake signal are high. As set by the rules in order to trigger shut down both signal must be high for more than 500ms as such an rc filter with values 100uf for the capacitor and 5.1k(5.1 because nand gates are not ideal and the output wont be exactly 5 volts) for the resistor accompanied by an op-amp are connected with the set of nand gates . The rc filter has a time constant of 510ms given the equation for the capacitor's charging :

$$V_c = V_{in} - (V * \exp(-t/(R * C))) \tag{1}$$

we get an estimated 3.15 volts for the potentiometer on the other terminal of the op-amp. Finally if an implausibility happens for less than 500ms a diode is placed in order to discharge the capacitor. The capacitor is discharged to 0.7 through the diode and the 100ohm resistor and from 0.7 to 0 through the 5.1 kohm resistor. We can see all this in Fig .2

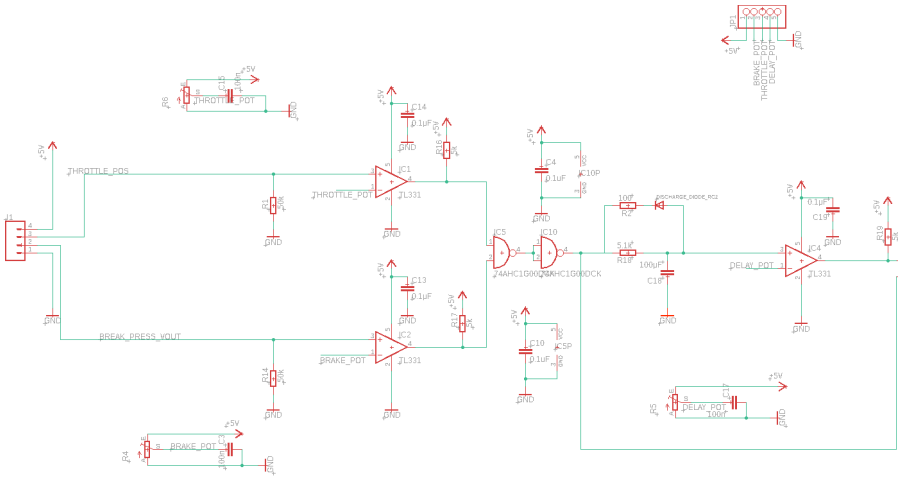

Figure 2: 1st part of the circuit

4 Reset Mechanisms

In order to understand the reset mechanisms first comprehend the working principle of the lm555. As shown in Fig .3 both trigger and threshold are sorted and the capacitor is connected directly to 5V so when the car powers up the capacitor instantly goes to 5V in order to avoid any false triggers. So when no implausibilities are present the bjt is open and the trigger threshold node is an open circuit, as a result its has a voltage of 5V . When VDD is present in both trigger and threshold the SR flip flop inside the lm555 goes high but the output driver inside the lm555 takes it back down to 0 so in order for the circuit to work correctly an inverter is placed on the output of the lm555. As we saw in the previous chapter when an implausibility is present for more than 500ms the bjt closes driving the trigger threshold node to GND thus the lm555 is now generating 0volts and the inverter drives it to 5volts. As stated by the rules the reset must trigger when the implausibility is aspsent for more than 10 seconds or when there is a power cycle. As for the power cycle rule when the car's power is shut down the capacitor is immediately discharged by the diode thus reseting the lm555 output back to 0 volts. As for the 10 second rule the voltage on the trigger threshold node must reached 2/3 V_{DD} in order to change the lm555 state thus a 100uF capacitor and a 92 kohm resistor were selected making for a timing constant of 9.2 seconds and 10 second delay for the capacitor to reach 2/3 V_{DD}, using the equation: (1)

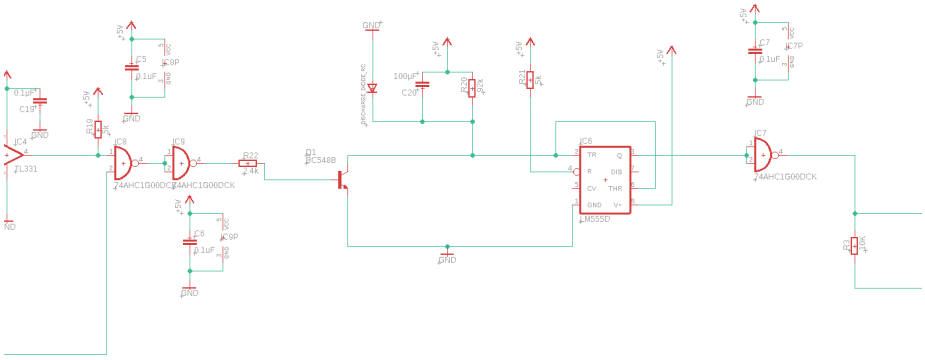

Figure 3: 2nd part of the circuit

5 Relay Trigeer

Finally when an implausibility is present the output of the the inverter is high thus closing the MOSFET and dragging the one terminal of the relay to 0 volts . As a results the voltage difference between the 2 terminals of the relay is 12 Volts triggering the shut down. When no implausibility is present both terminals stands at 12 volts thus not triggering the relay. Furthermore a flyback diode is placed in orded to avoid any spices due to the triggering of the coil inside the relay and a 10k pull down resistor is placed between the gate opf the MOSFET and the ground insuring that the gate can be discharged through that resistor as shown in Fig .3.

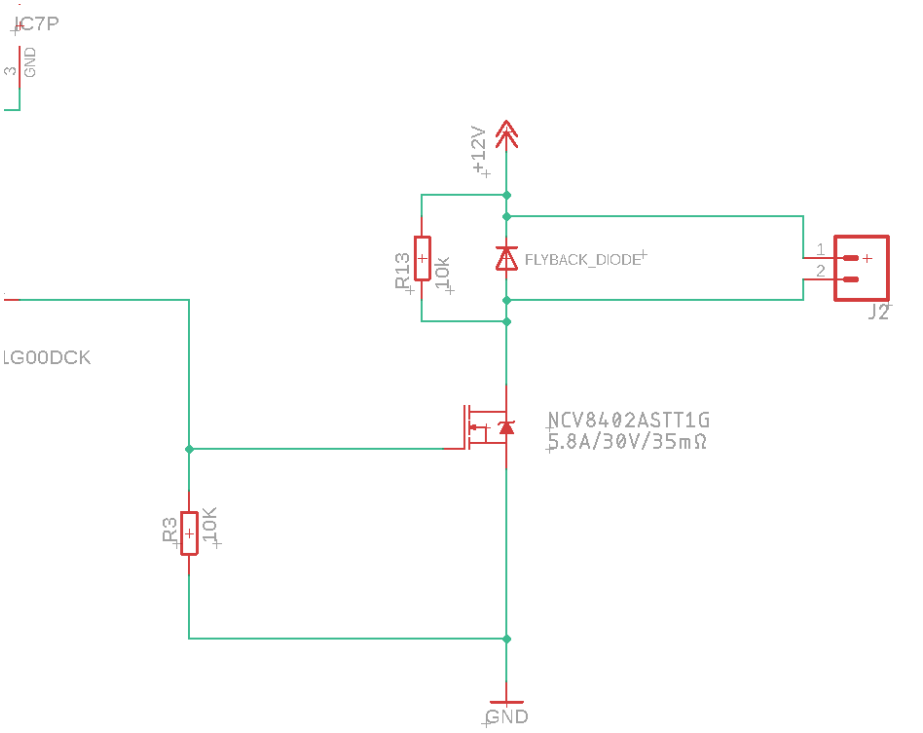

Figure 4: 3rd part of the circuit

6 Full circuit

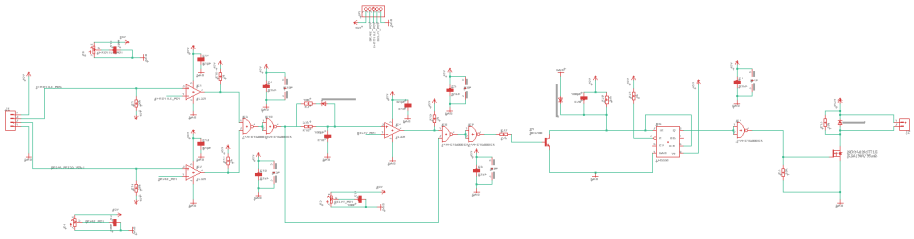

Figure 5: Full circuit

7 Simulation results

The proposed circuit was designed using autodesk EAGLE and simulated with ltspice . As shown in Fig .6 when the implausbility lasts for 500ms or less there is no trigger of the relay and the capacitor is almost immediately discharged. When an 8 sec implausibility as present the relay stays always open as shown in Fig .7. Finally when analyzing a 10 second or longer implausibility or a power cycle reset occurs as shown in Fig .8 and Fig .9 working as demonstrated in the previous sections.

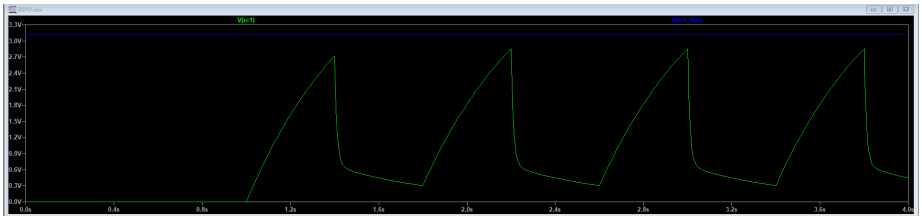

Figure 6: Full circuit

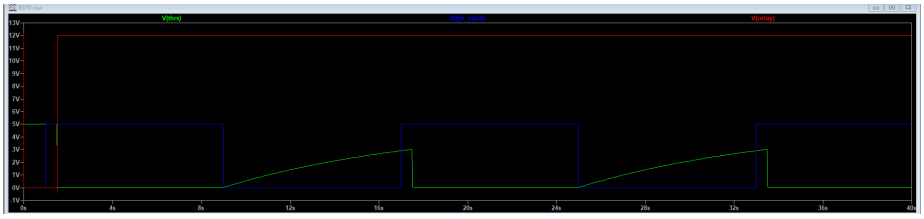

Figure 7: Full circuit

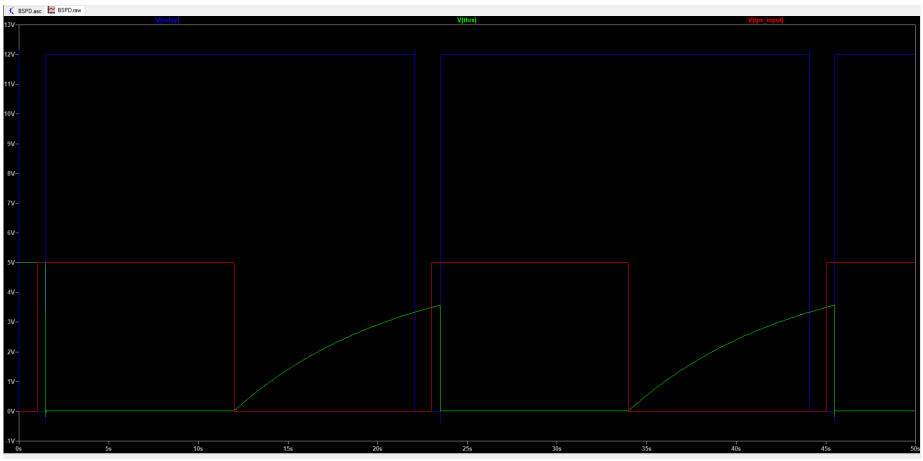

Figure 8: Full circuit

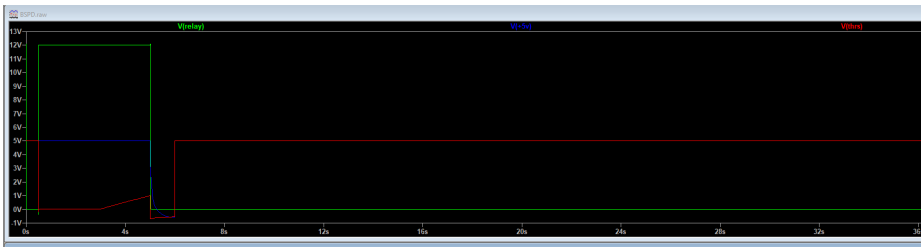

Figure 9: Full circuit

8 PCB

When designing the PCB decoupling components were placed as close as possible to their respective components so in case of voltage drop they could instantly provide the necessary voltage to those components. The PCB is a layer design with vias to connect them and when 2 traces are crossing each other they do it in a 90 degree angle in order to avoid electromagnetic interferences. As much of the interconnects as possible were placed on the top layer. This is where the pins of the parts are already anyway, so is the logical layer to use to connect them. Then bottom plane is used for short "jumpers" only when needed to make the routing work. The bottom plane is otherwise ground. Further more in order to reduce to resistance in power lines their width is higher so the efficiency becomes greater . Finally to reduce the EMI crossing between top and bottom layer traces happens in a 90 degree angle so the interference is minimized and a top group plane was added this means there is no need for a separate via for the ground side of the bypass cap. As a result power loop connects directly to the ground pin on the top side, then net is connected to the ground plane with a via at a single point.

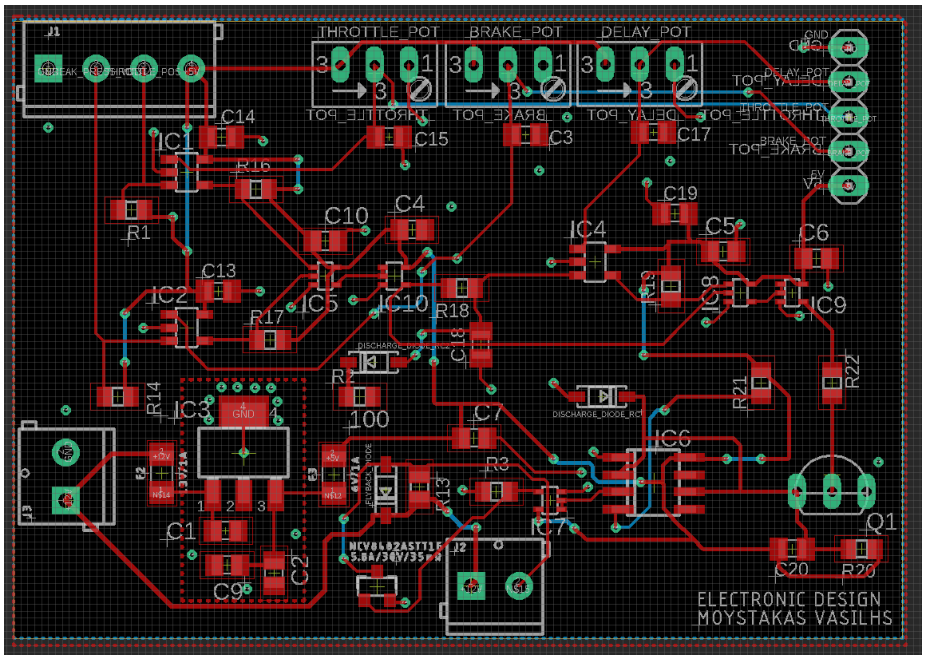

Figure 10: PCB

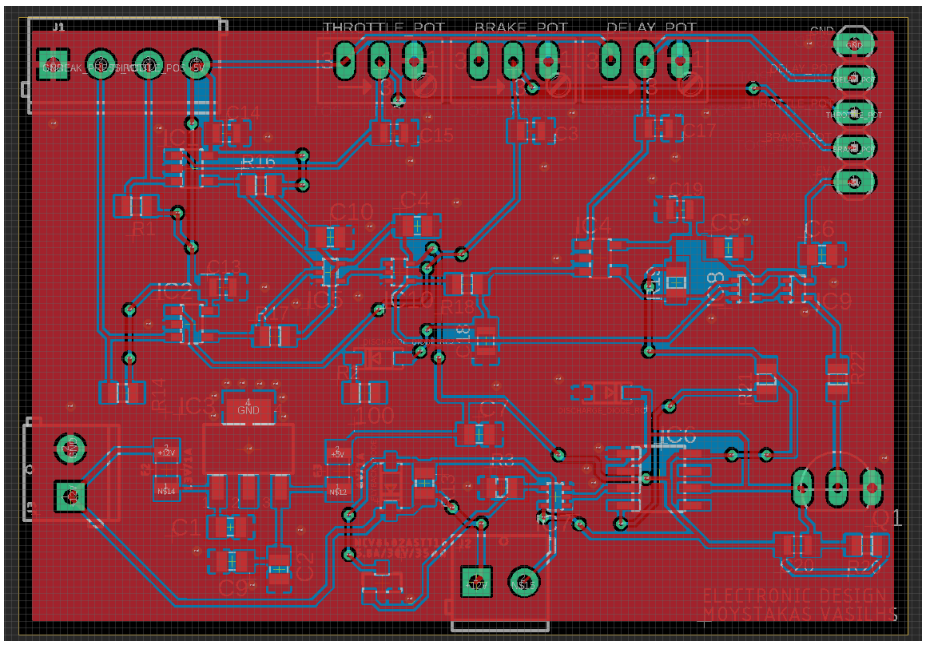

Figure 11: PCB with ground planes