Design of high efficiency low noise charge pump topologies for mobile applications

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Abstract

In this report we review the basic working principles of charge pumps, their evolution over the years, their improvement in preventing power loses and simulating the most widely used topologies using the Advanced Design System(ADS) software from keysight.

1 Introduction

A charge pump is a circuit that converts the supply voltage V_{DD} to a several times higher voltage V_{out} by the principle of switched-capacitors. Charge pumps are also know as an inductorless DC to DC converter is a special type of converter that is only using capacitors as its charging elements.

2 Working Principle

In order to understand the working principle let as consider a basic one step ideal charge pump topology.

As shown in Figure 1 an ideal charge pump comprises of two switches driven by opposite phases a charging capacitor and a clock with amplitude equal to V_{DD} . In the first half period when the clock is low, switch (SwitchV1) closes charging the capacitor to V_{DD} as the clock rises and reaches V_{DD}. The charging capacitor's voltage rises to $2V_{DD}$ and switch (SwtichV2) closes thus part of the charge stored in the charging capacitor is transferred to the load and the output capacitor. After several cycles the output voltage is equal to.

$$V_{out} = 2V_{DD} - \frac{I_{load} * T}{C} \tag{1}$$

I_{load} referring to the output load, T to the period and, C to the charging capacitor.

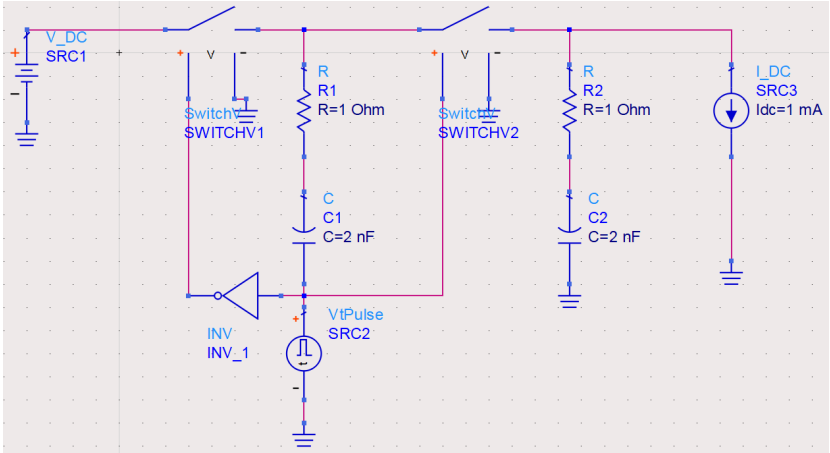


Figure 1: Ideal one stage charge pump

3 Power Loses Mechanisms

3.1 Redistribution loss

A very important part of a charge pump is it's efficiency and in order to understand that we must first comprehend the power loses of the circuit. We can separate loses in 4 basic categories. First of all redistribution is caused when two capacitors are shorted and charge transfers between them. When referring to charge pumps V_{out} is lower than $2V_{DD}$ because I_{load} is constantly discharging the output capacitor. When switches change their state, output and charging capacitors are shorted thus leading to redistribution loss.The main way of counteracting redistribution loss is by reducing the ripple at the output making the difference of V_b-V_{out} (V_{out} referring to the charging capacitors voltage) very small. The following equation describes redistribution loss :

$$Redistribution = \frac{1}{2} f_s C_b (V_b - V_{DD})^2 + \frac{1}{2} f_s C_{out} V_{out}^2 - \frac{1}{2} f_s \frac{C_b V_b + C_{out} V_{out}}{C_b + C_{out}} \quad (2)$$

Where f_s is the switching frequency of the charge pump, C_b is the pumping capacitor in the power stage, C_{out} is the filtering capacitor at the output load.

3.2 Conduction loss

Most commonly charge pumps are implemented using CMOS technologies swapping power switches with MOSFETS . We can describe MOSFETS as variable resistors controlled by voltage as the voltage on its gate increases and passes a certain threshold the resistance between drain and source drops dramatically but a really small resistance still exists thus triggering Conduction loss in the power stage. The conduction loss can be reduced by increasing the aspect ratio

of the transistor W/L. A common technique used to reduce the resistance of the transistor is using a number of transistors parallel to each other at the cost of increasing the capacitance of the switching mechanism. The equation that describes the conduction loss is:

$$Conduction = R_{on} f_S \int_0^{DT} I^2(t)\, dt \tag{3}$$

Where W and L are the MOSFET width and effective channel length of the transistor as a power switch, respectively.

3.3 Switching loss

As mentioned before MOSFETS are voltage controlled devices meaning that its states are controlled by a control voltage V_{gs} . The voltage changes on V_{gs} are accomplished by charging and discharging the gate capacitor of the transistor , which is proportional to the to product of the transistors width and length $W * L$.In order to reduce the switching loss, the size of the transistor is preferred to be small. It is obvious that conduction and switching loss are contradicting so its a challenge to find the optimal point for the width of the transistor , W , where the sum of conduction and switching loss reaches the minimum. The mathematical expression describing the switching loss is:

$$Switching = \frac{1}{2} f_s C_{ox} W L V_{gs}^2 \tag{4}$$

Where C_{ox} is the gate oxide capacitance per unit area and V_{gs} is the gate-source voltage swing of the corresponding power transistor.

3.4 Reversion loss

Finally, reversion loss is most commonly found in cross-coupled charge pumps and occurs when sorting a higher voltage node to a lower one forming a reversion current from the original power flow, resulting in power transfer from the output to charging capacitors thus degrading the efficiency of the charge pump. Reversion loss is described by the following equation :

$$Reversion = \frac{1}{2} f_s \frac{C_b C_{out} (V_{out} - V_b)^2}{C_b + C_{out}} \tag{5}$$

4 Diode Topology

In order to make the transition to the CMOS technology charge pumps its essential to first understand the workings of a diode model charge pump.Let us consider an one stage diode topology without load equipped with small capacitors in the range of NanoFarads. This topology consist of the charging capacitor, the output capacitor C_1, a 5volts V_{DD}, a clock with a period of 2 uSeconds and 2 diodes.

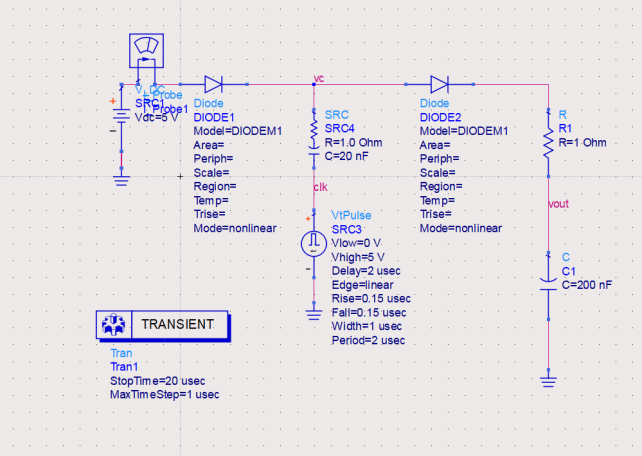


Figure 2: Diode charge pump without load

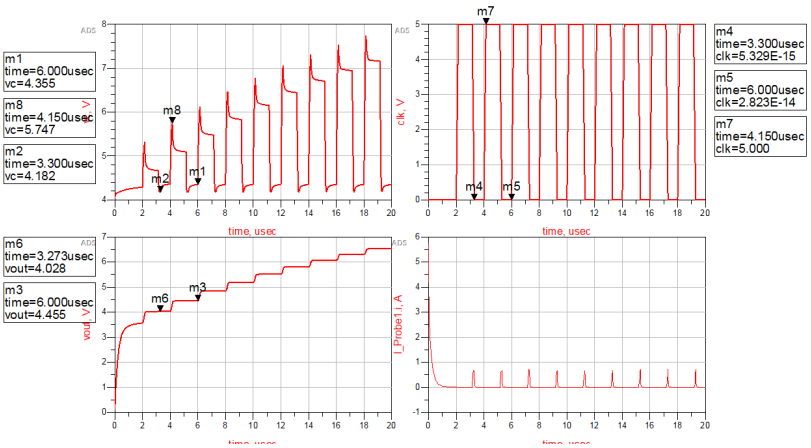


Figure 3: Charging stages between 0-20us

Let start by analyzing a charging cycle in figure:3 starting at 3.3u sec we observe that the clock is low as a result the diode D_1 is closed charging the capacitor C_4 until we reach 4.15u at this point the clock obtains its high value (V_{DD}) thus diode D_1 opens and diode D_2 closes (because anode is 0.6V higher than the cathode) transferring energy from the charging capacitor to the output capacitor.We can observe the discharging effect in V_c between the points m8 and m9 and the rise of the output at point m3.

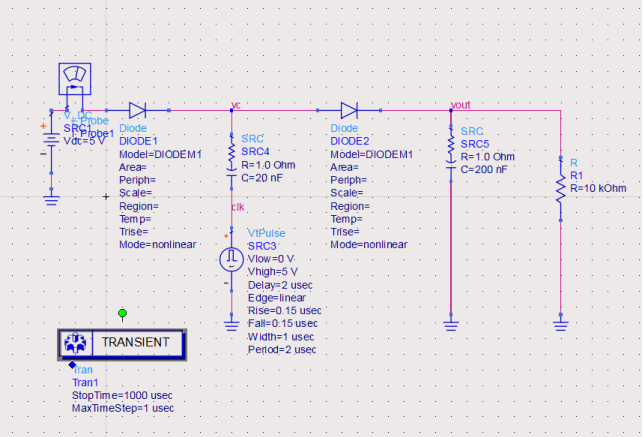


Figure 4: Diode charge pump with load

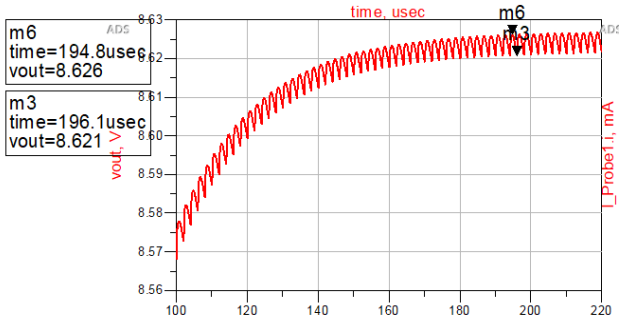


Figure 5: Ripple Effect

Having already analyzed the charging mechanism of the diode topology charge pump the next step is to comprehend the ripple effect in figure:5 under a load of 1mA.The steady output of the Charge pump follows the equation:

$$V_{out} = 2V_{DD} - \frac{I_{load} * T}{C} - 2V_{diode} \tag{6}$$

As we see the diode topology has a major weaknesses 0.7 volts are lost in every stage due to the existence of the diode.That might not sound much

but with charge pumps usage in low voltage applications becoming more more popular those loses must be mitigated.

5 Dickson Topology

Similarly to the diode model Dickson charge pump is implemented with MOS diodes. In this topologies although we get rid of the diode's voltage drop we still have to consider the V_{TH} of the transistor as a loss.In this specific scenario in figure: 6 our V_{TH} is 2V witch makes this circuit a bit worse than the diode one but that introduces us to CMOS charge pumps.

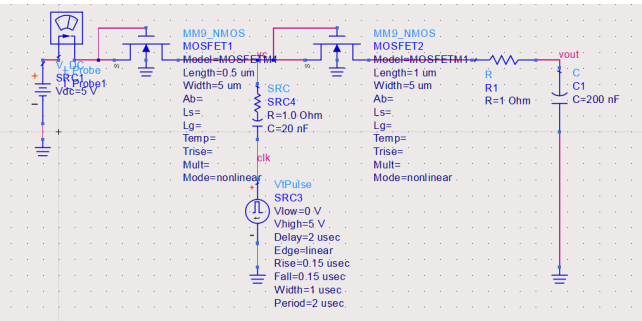


Figure 6: Dickson charge pump with no load

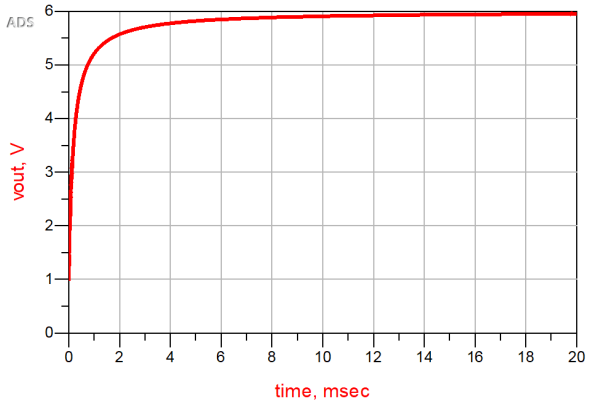


Figure 7: Dickson charge pump V_{out} wave form

The V_{out} waveform makes it clear that with no load and with 2 NMOS vout equals 6V as we lose 2V from each transistor's threshold. So already the topology has some major flaws so lets try to take V_{TH} out of the equation.

6 Bootstrap Topology

A very common and attractive way to get rid of the V_{TH} confinements is the Bootstrap topology.Its a wildly used method that uses higher gate voltages in order to mitigate the loses related to threshold as shown in Fig.8. In order to understand the working principle of the Bootstrap charge pump lets analyze a basic state on its steady condition. First of all clocks have a high value of $2V_{DD}$ as seen in Fig. 9. When Fb1 goes high the gate voltage of charging MOSFET1 reaches $3V_{DD}(2V_{DD}$ due to the clock and V_{DD} due to the switching capacitor) as a result V_{gs} is much higher than $2V_{DD}$ subsequently there are no loses due to the transistors threshold and the charging MOSFET 1 closes charging the capacitor C1 to V_{DD}. As the clock f1 goes high and V_c reaches $2V_{DD}$ therefor the gate voltage of switching MOSFET goes to $2V_{DD}$ thus charging the switching capacitor to V_{DD} . Furthermore after a short delay Fb2 goes high and for the same reasons motioned before there are no drops due to threshold voltage and charging mos 2 closes so the output capacitor is charges through C1. At the small time left that only F1 is high V_{out} is close to $2V_{DD}$ so the switching MOSFET 2 closes and the capacitor CS2 is charged by the capacitor C1. Finally the MOSFET on the output is used as a switch to activate the load when output of the charge pump has reached its steady form.

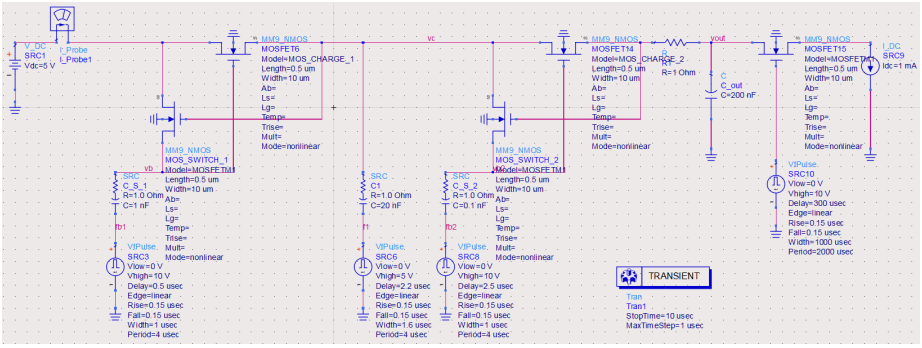


Figure 8: Bootstrap charge pump

As we see in Fig.10 m3 is the point that the load MOSFET closes and load is introduced to the circuit. We see that the peak voltage on the steady state is 9.973 volts and after the introduction of a 1mA load the voltage drops to 9.777 volts those numbers are really close to $2V_{DD}$ making the Bootstrap a suitable charge pump solution.

The wave-forms presented in Fig.11 verify our assumptions for the working principle of the Bootstrap. Furthermore it is shown that the peak Current is 300mA making a suitable current consumption.

Although Bootstrap is an efficient topology it comes with its problems.First of all, the $2V_{DD}$ required for the clocks has to be produced from a second charge pump or the input voltage must be reduced to $V_{DD}/2$ essentially making

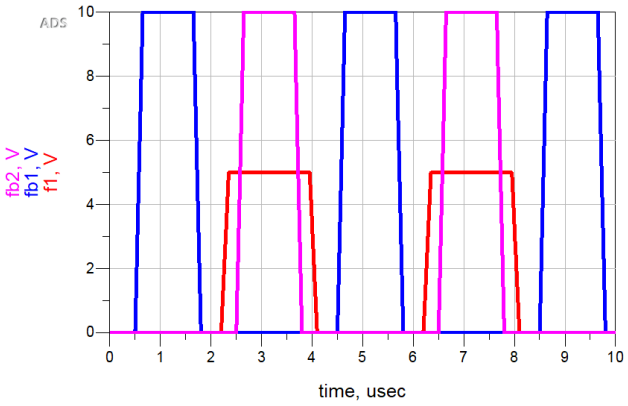


Figure 9: Bootstrap Clocks

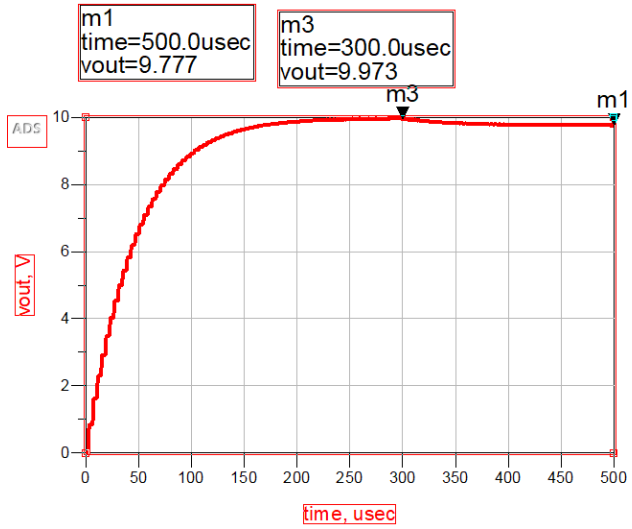


Figure 10: Bootstrap's V_{out} waveform

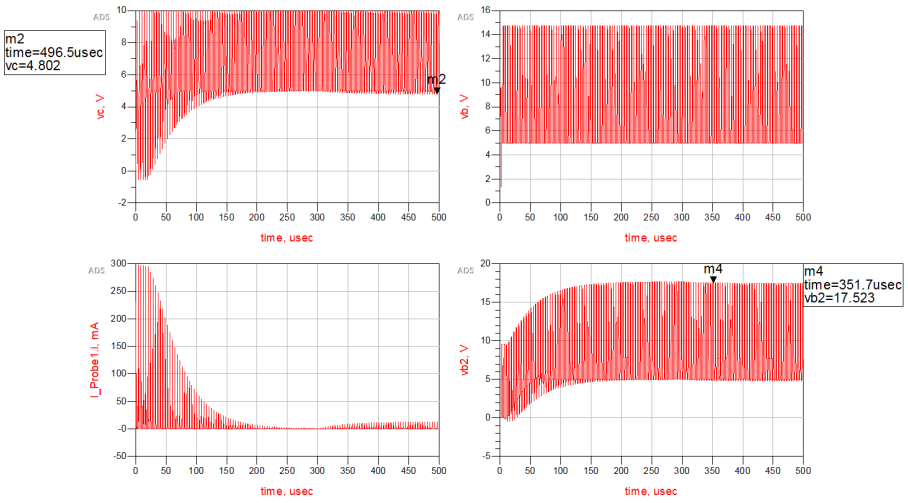


Figure 11: Bootstrap's wave forms

the $2V_{DD}$ that the clocks need the starting V_{DD}.The second solution its only viable on multi stage Bootstrap charge pumps because by cutting down the input voltage in half the output voltage will be V_{DD} so more stages are need to reach the needed result. As we can see in Fig.11 $VB2$ fluctuates between 5 and 17.5 volts those extra 2.5 volts are transferred from the charging capacitor C_1 when only F1 is high. That creates a problem when choosing the values for the switching capacitors they have to be much smaller than the charging capacitors in order not to compromise the efficiency of the circuit but not small enough to be discharged by the capacitance of the MOSFETS.

7 Cross Coupled Topology

As we have seen in the previous section although Bootstrap is a really efficient solution the clock's voltage remains a major problem and in order to resolve that we take a look at one of the most used charge pump topologies the Cross Coupled charge pump Fig.12. Lets start by analyzing its working principle at its steady state.As clock 1 goes high $NMOS_1$ closes charging the capacitor C3 to V_{DD} , simultaneously clock 2 is low so $PMOS_2$ closes charging C1 through C2. The same phenomenon is observed when the clocks switch their condition but with $NMOS_2$ and $PMOS_1$ respectively. As we see in Fig.13 between m2 and m6 both clocks have the same value (0 volts) making them overlap, this results in both PMOS been closed thus sorting a higher voltage node(vout) to a lower one(gate,gate2) forming a reversion current from the original power flow resulting in reversion loss as we can see in Fig.14.

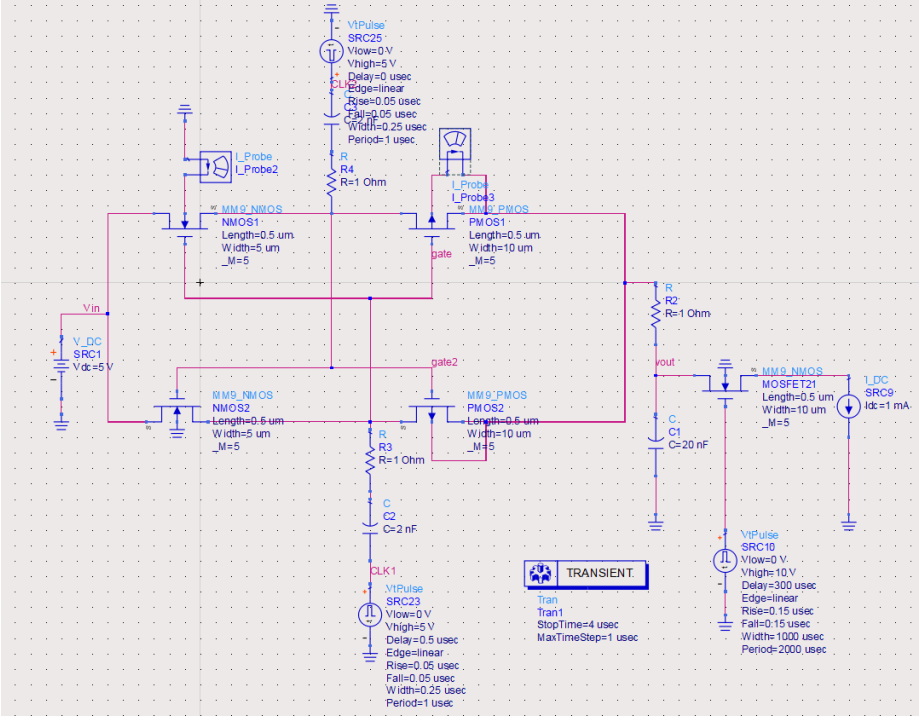


Figure 12: Cross Coupled Charge Pump

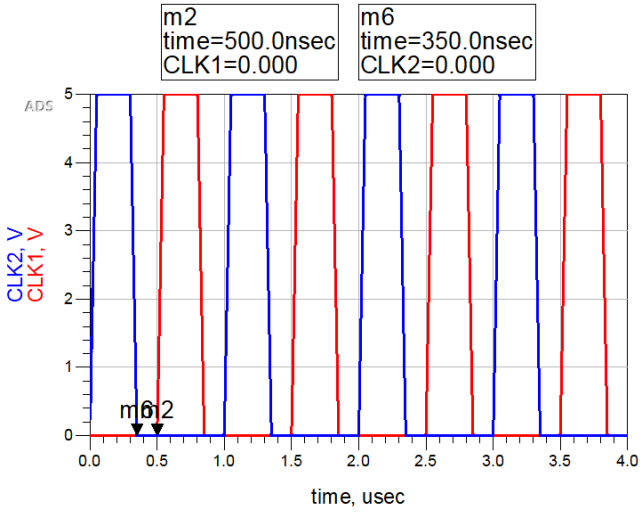


Figure 13: Overlapping clocks

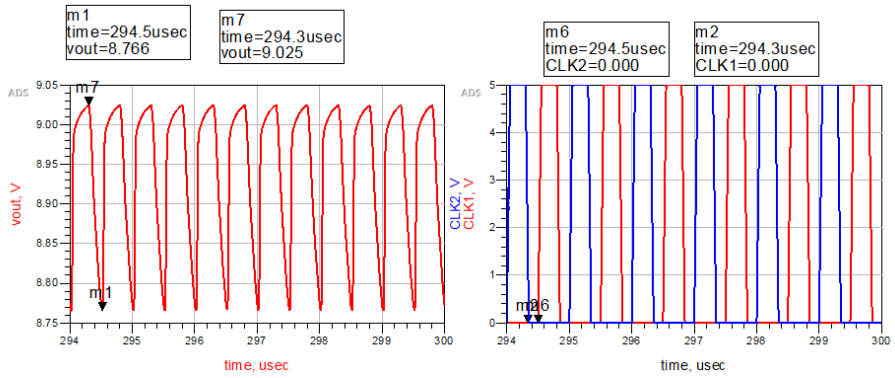
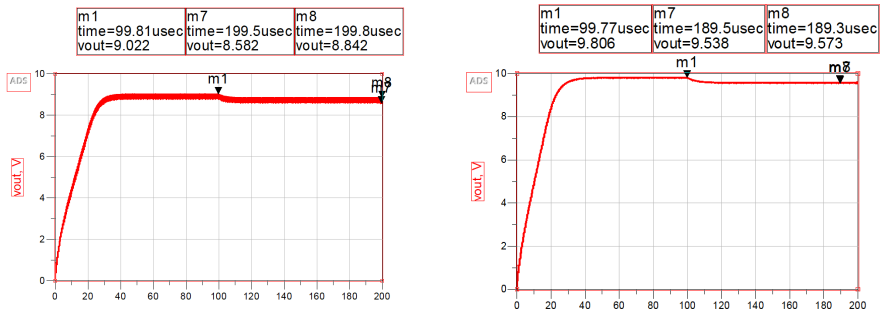


Figure 14: Reversion loss

As shown in Fig.13 the basic cross coupled charge pump under a load of 1mA is inefficient but lets compare Fig.15a with Fig.15b as demonstrated without the reversion losses V_{out} is 0.8V higher before the introduction of the load 1V higher after the load and the ripple has been reduced from 0.3V to 0.04V.Its clear that reversion is cross coupled charge pump's biggest problem.



(a) V_{out} with overlapping clocks

(b) V_{out} without overlapping clocks

Figure 15: Cross coupled V_{out} wave forms

8 Complimentary Cross Coupled Topology

As shown in the previous section cross coupled is an efficient topology and only when there is no reversion loss so to accomplish that there must be perfect non overlapping clocks(almost non existent rise and fall time) which is not possible so preventing reversion loss is the only viable way, for that purpose there is the complimentary cross coupled charge pump Fig.16.But lets analyze how this topology solves the reversion loss. As we see in Fig.16 the circuit composes of

two shells with only difference being the complimentary clocks on the side. As a result when both clk_1 and clk_2 are low their complimentary clocks are high subsequently both V_a2 and V_b2 are high and V_a1 , V_b1 are both high effectively making closing all transistors preventing reversion loss.

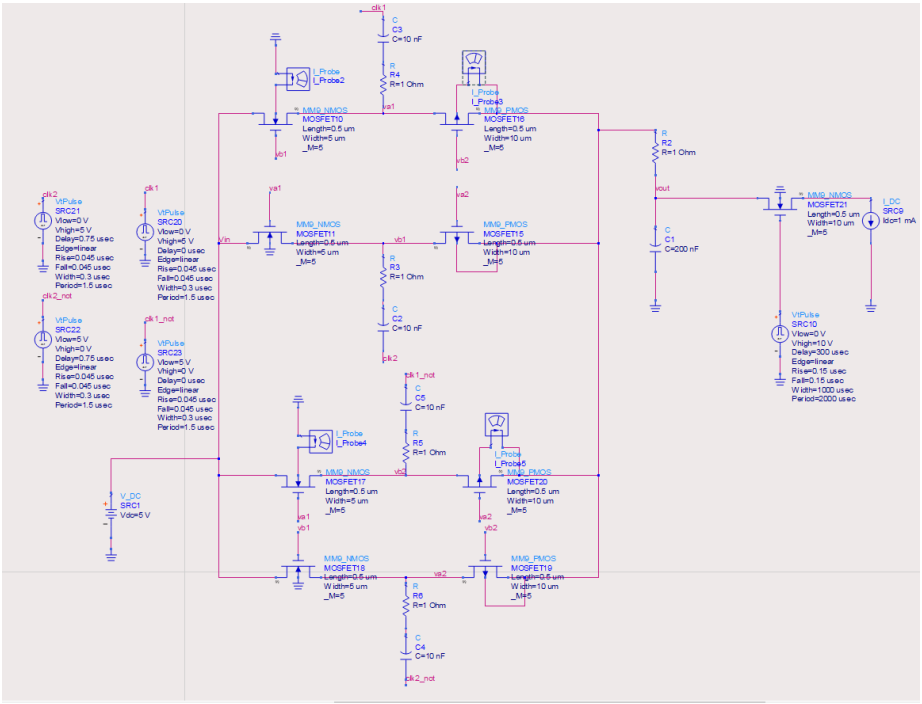


Figure 16: Complimentary Cross Coupled Charge Pump

Moving on to the wave form of the circuit , ripples are observed even if there is no load as seen in in Fig. 17. A voltage drop is observed when clk_1 rises and clk_{1not} drops. That voltage drop occurs because V_{gs} is higher than the transistors threshold before the clocks reaches its highest value effectively shorting the output to lower voltage node causing a small reversion but the ripple its so small that is negligible.And as we see when both clocks are low vout is stable so the reversion prevention is successful. Additionally by evaluating the bout waveform Fig.18 we can see that the efficiency has increased.

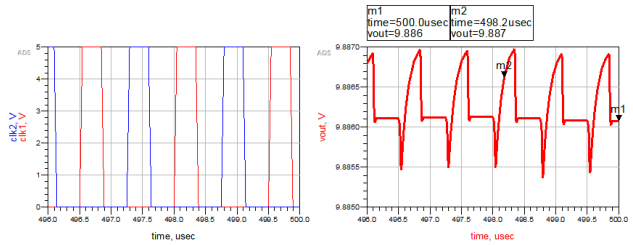


Figure 17: Complimentary Cross Coupled Charge Pump without load

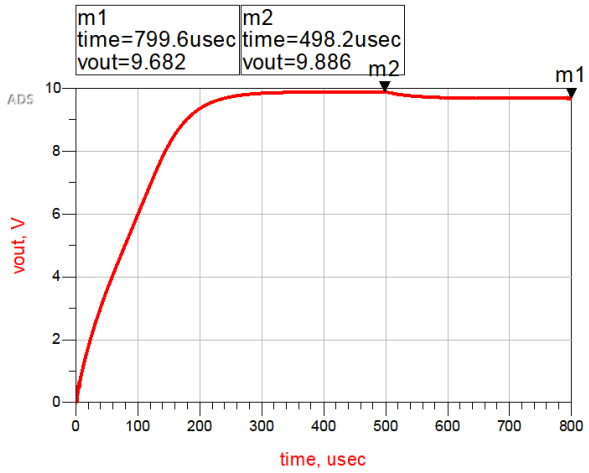


Figure 18: Complimentary Cross Coupled Charge Pump V_{out} waveform

9 Simulation Results

The proposed charge pump was designed and simulated with ADVANCED DESIGN SYSTEM(ADS) using a level 1 model for the transistors with W=5um and L=0.5 for NMOS transistors and W=10um and L=0.5 for PMOS transistors. The switching frequency of the charge pump is design as 1MHz . The total charging capacitance was set to 8nF and the output capacitor was set to 20nm. Finally all signals were overlapping.THe results can be seen at Fig.19

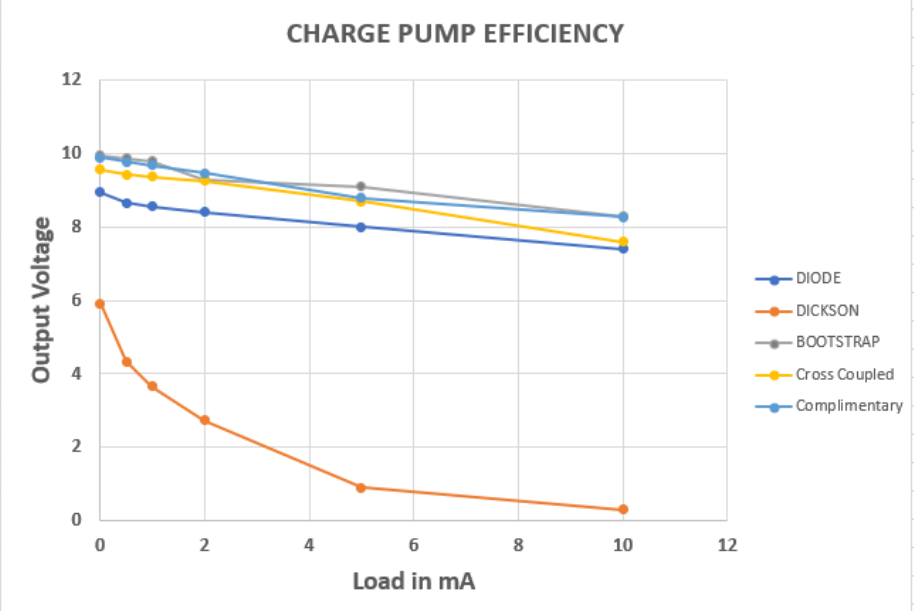


Figure 19: Output efficiencies comparison

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