Design of a Rail-to-Rail Operational Amplifier

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1 Introduction

The design of rail-to-rail operational amplifiers (op amps) is crucial in current analog circuits as it allows for precise signal processing throughout the whole supply voltage range. Traditional operational amplifiers have output voltage swing restrictions, limiting their applicability in applications needing signals to cover the whole voltage range. Rail-to-rail op amps solve this constraint by supplying output voltage close to the power supply rails, boosting dynamic range and signal quality. Firstly, this report explores the basic specifications of the op-amp, then provides a basic design of a two-stage op-amp, and closes with the design of a rail-to-rail Folded-Cascode Op Amp with class AB output using Cadence Virtuoso for the simulations.

2 Op-Amp Specifications

The presence of an Operational amplifier holds the utmost significance in the operation of various circuits such as integrated analog filters like switched-capacitor or Gm-C filters. Data converters, which include analog-to-digital and digital-to-analog converters, are another category in which the op-amps play a critical role in achieving the desired performance. In this instance, many system parameters heavily rely on the specifications of the op-amp. It is important to note that the criteria used for the design of an application-specific op-amp to those employed for creating general purpose op amps intended for standalone use. Generally, an op amp's behavior is characterized by an array of parameters some of which hold greater significance depending on the application.

Starting with one of the main parameters, the DC gain of an op-amp represents its amplifications factor in an open loop configuration, although ideally, its value is infinity. In reality, the voltage gain of the transistors within the op-amp limits the gain within the range of 40dB to 100dB depending on the design. The Dc gain indicates the op-amp's ability to amplify small input voltage differences. Typically op amps are used as linear amplifiers with a negative feedback loop to ensure stability and accurate signal amplification. In this configuration a high Dc gain is essential.

The open loop gain of an op-amp declines as the frequency increases. This occurs due to the internal parasitic capacitance of the op-amp circuit. As a result, the frequency bandwidth of an op-amp defines the range of frequencies over which the op-amp can accurately amplify signals. At some frequency, known as the unity gain bandwidth (denoted as LM), the op amp's open-loop gain drops to unity (1). This frequency represents the upper limit of the op amp's frequency response.

An op amp's slew rate represents its maximum output voltage change rate particularly in large input signals while settling time indicates the time it takes for the output to reach a steady state after the input changes. Both characteristics influence the speed and accuracy of numerous applications, particularly those involving large-signal processing and analog-to-digital conversion. A typical value for the slew rate is $\geq$ 50 V/us.

An op amp's phase margin is a measure of its stability in a closed-loop setup. It indicates the difference between the actual phase shift and a critical phase shift, beyond which the system becomes unstable. A bigger phase margin implies more stability and offers a safety margin against output signal instability and oscillations.

3 CMOS two-stage Op-Amp

The circuit of a two-stage op-amp as its name suggests consists of two cascaded stages. In the first stage, a differential pair with a current mirror as active load, and in the second stage is a common-source amplifier with a compensation capacitor to provide the necessary voltage gain and stability. A CMOS two-stage op-amp is shown in Figure 1. In Figure 1 the symmetrical pair of (N0, N1) and (P2, P0) forces the DC voltage at the drain of N0 to be the same as the voltage at the drain of N1. The diode connected to P2 makes the voltage at the drain of N0 equal to VDD-Vgs. The Vds and Vgs of P2 and P0 are equal to the Vgs of P1. To ensure stability and prevent oscillations C0, a compensation capacitor is introduced in the circuit. N3 acts as the current source of the differential pair and N2 is the active load of the common source amplifier in the second stage. Finally, N4 acts as a mirror biasing N3 and N2.

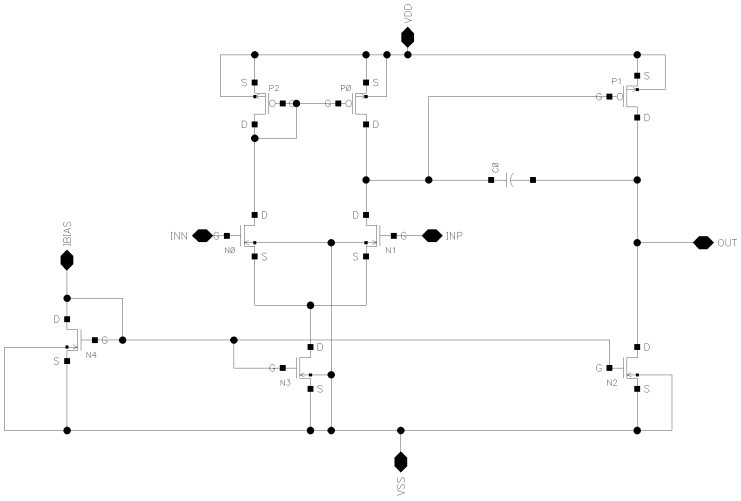

Figure 1: CMOS two-stage op-amp schematic

3.1 Results

The results of the table can be confirmed by the following simulation made with the Cadence Virtuoso tool.

Parameter	Value
UGF	155.1Mhz
Phase-Margain	63.3°
Power consumption	55.95uW
Supply voltage	0-0.9V
DC GAIN	43.5dB

Table 1: Two stage OP-AMP specs

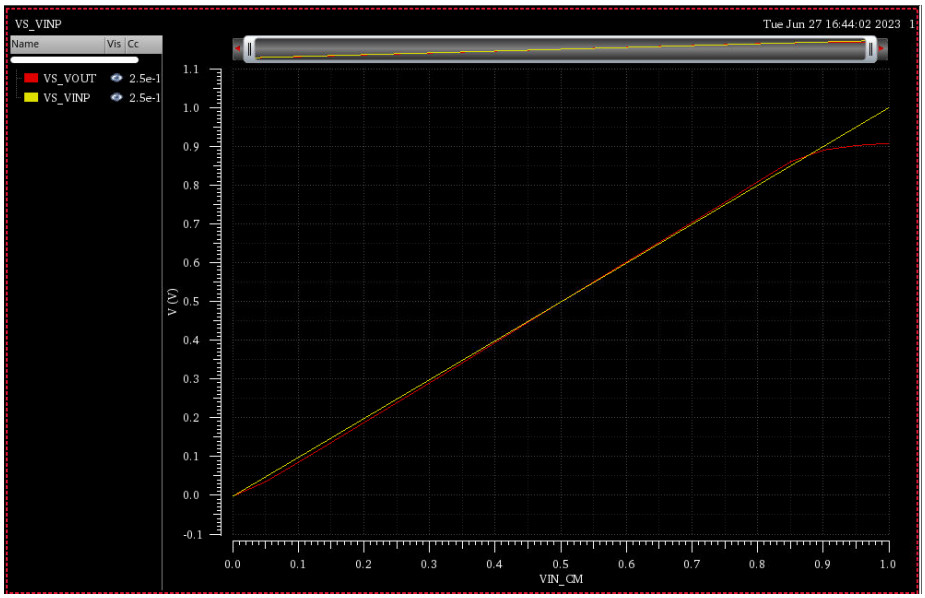

Figure 2: Vsupply range

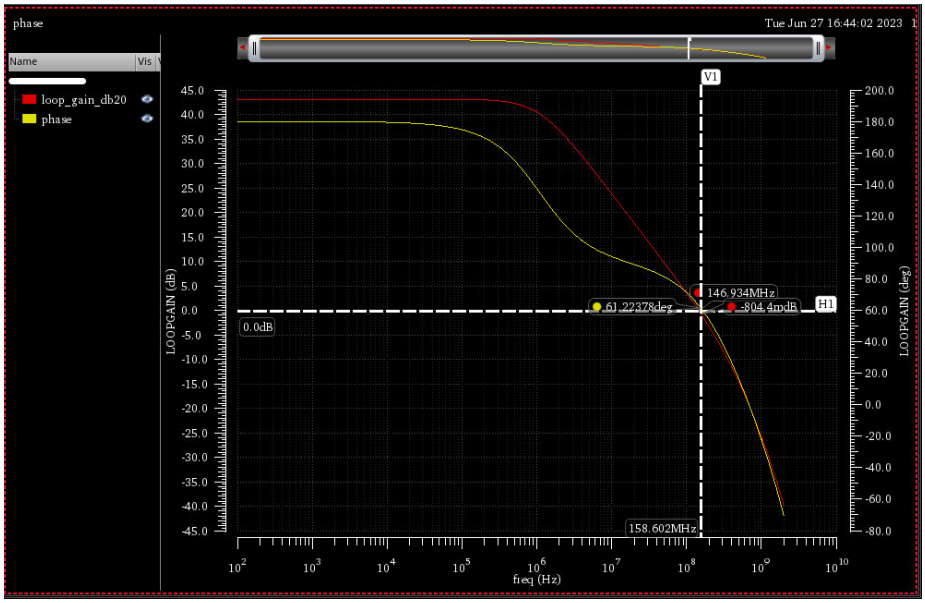

Figure 3: Phase margin

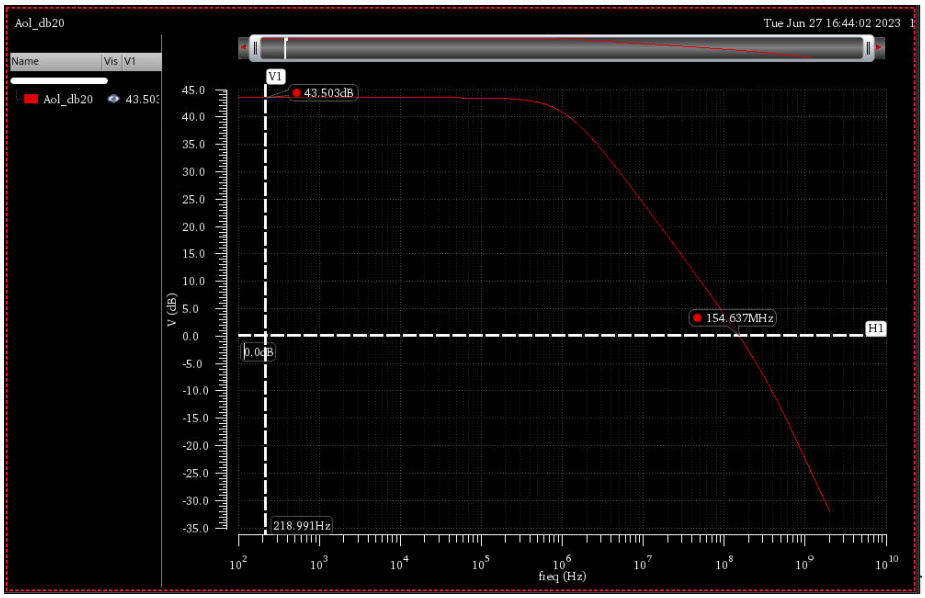

Figure 4: Gain and UGF

4 CMOS rail to rail folded cascode Op-Amp with class AB output

Single differential pair op amps use either NMOS or PMOS transistors in a setup that limits the input common-mode voltage to a threshold below the V_{DD} or above the V_{SS} depending on the differential pair. In the NMOS differential pair, the input common-mode voltage can reach values close to V_{DD} but is restricted from reaching values below a certain threshold which is equal to equation (1). Here V_{gs} describes the gate-source voltage of the NMOS. When the input voltage goes below the threshold, the current source transistor enters the triode region causing a drop in the transconductance of the input stage. On the other hand when the differential pair consists of PMOS transistors the input common-mode voltage levels can reach values close to V_{SS}, but its limitation lies in getting above a threshold close to V_{DD} and the threshold is equal to equation (2). Where V_{gs} is the gate-source voltage of the PMOS and V_{od} is the overdrive voltage. In order to ensure a stable voltage gain and bandwidth, it is important to maintain a constant input transconductance even when the input common-mode voltage (Vic) varies. The most common approach to address this is the parallel combination of PMOS and NMOS differential pairs. However, this topology has a problem, the total transconductance of the circuit in the region where both pairs are active doubles, assuming the two differential pairs have the same transconductance in the midrange of Vic as shown in Figure 5. The complete design of the rail-to-rail op-amp can be seen in Figure 6. This design

consists of two stages. The first stage consists of the rail-to-rail differential pairs connected with a folded cascode. In order to provide higher gain while keeping the input and output swing high and the output stage that consists of a class AB amplifier. In this design, the transistors N2 and N3 make up the NMOS differential pair and the PMOS P1 and P2 are the PMOS differential pair. The current mirrors N0 N1 and P5 supply the current of the tail transistors N4, N8, N10, N14, and P4, P17. The Transistors (P7, N6) and (N11, P12) are used to provide the cascode bias voltage for the gates of (N7, N9) and (P10, P11) respectively. The transistors (P6, P9, P10, P11, N7, N9, N8, N10) together with the differential pairs form the folded cascode with transistors N8 and N10 acting as the tail current source and P6 and P9 as the current mirror. In order to increase the gain of the op-amp and make efficient use of the supply voltage a class-AB amplifier is used as the output stage. The class Ab amplifier consists of two common source-connected transistors (P19) (N19) driven by the outputs of the cascode. The floating class AB control is formed by (P14)(N13). In order to bias the gates of the transistors (P19)(N19) this topology utilizes stacked diode-connected transistors, namely (P15, P16) and (N16, N17), this configuration ensures the proper operation of the output stage. The minimum required voltage is limited by the rail-to-rail common mode input range, as a result, two stacked V_{gs} voltages are stacked in the output stage. The quiescent current of the output transistors is determined by two KVL loops formed by (P15, P16, P14, 19) and (N13, N17, N16, N19). The class AB amplifier is achieved by keeping the gates of the output transistors constant. Consider the output stage performs a pull action the voltage of (N13) increases while the voltage of (P14) decreases by the same amount, as a result, the V_{gs} of both output transistors decreases. Thus the output stage pulls a current to the output node. A similar analysis can be performed for the P-channel output transistor. Finally, a compensation RC circuit is utilized to move to the dominant pole further in order to ensure high bandwidth and stability.

$$V_{icmin} = Vgsn + Vod \tag{1}$$

$$V_{icmax} = VDD - Vsgp - Vod \tag{2}$$

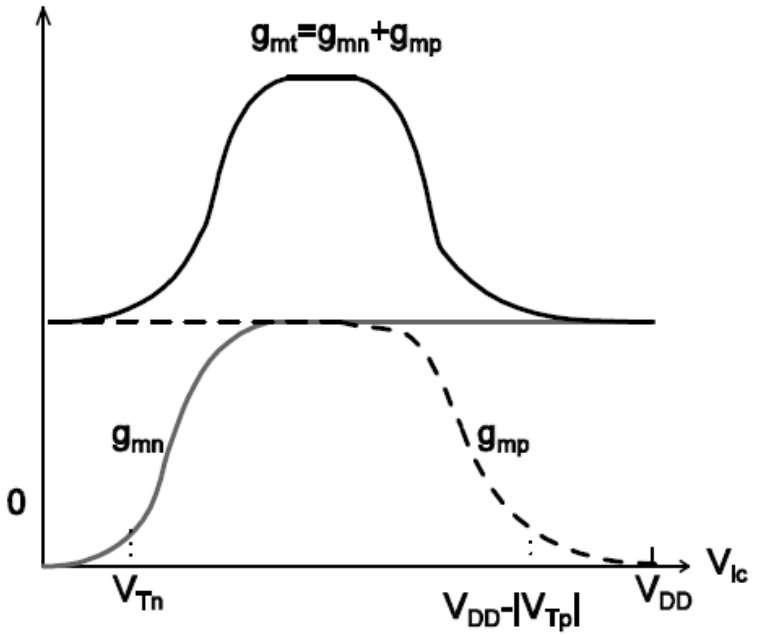

Figure 5: Rail to Rail transconductance

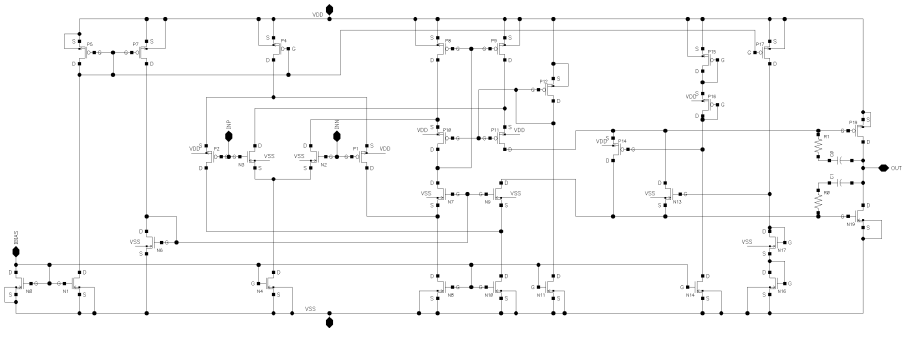

Figure 6: CMOS rail to rail folded cascode Op-Amp with class AB output

4.1 Results

The results of the table can be confirmed by the following simulation made with the Cadence Virtuoso tool.

Parameter	Value
UGF	73.4Mhz
Phase-Margain	61.3°
Power consumption	151.2uW
Supply voltage	0-1V
DC GAIN	85.3dB

Table 2: R2R OP-AMP specs

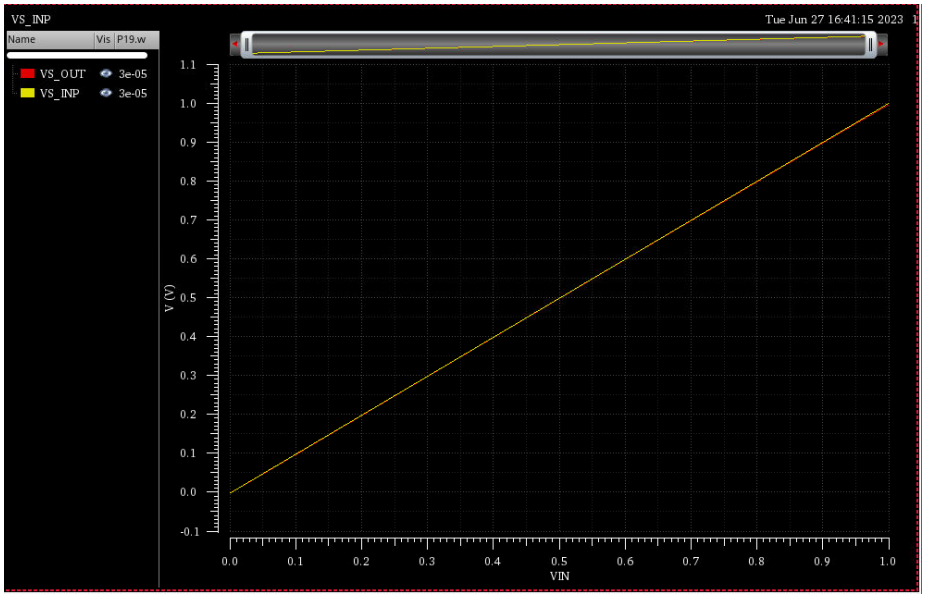

Figure 7: Vsupply range

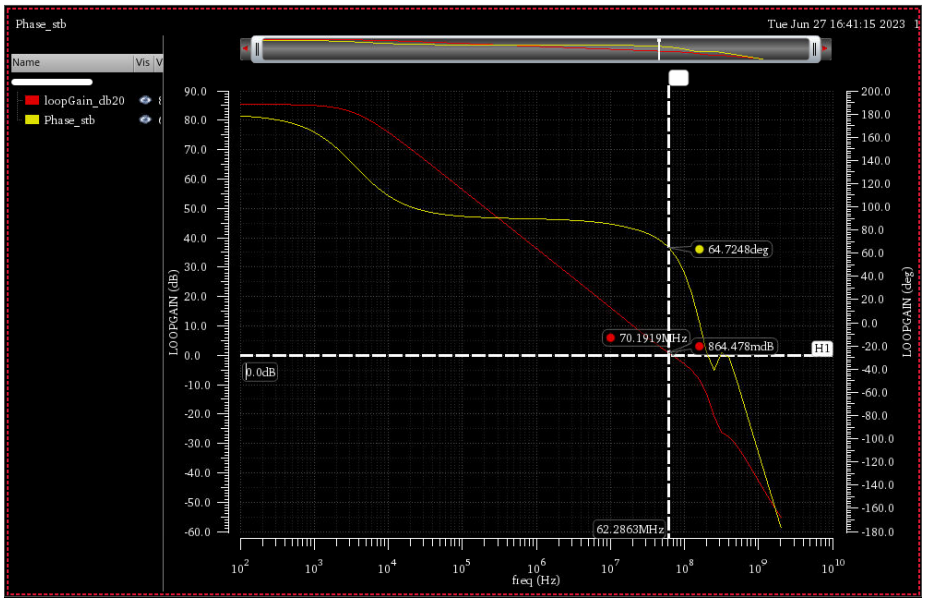

Figure 8: Phase margin

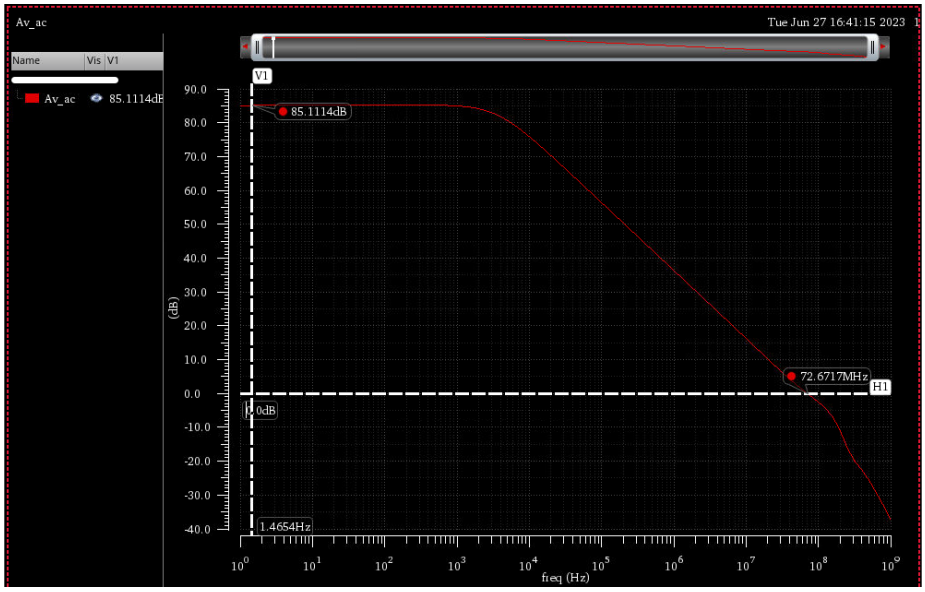

Figure 9: Gain and UGF