Project designation

OWL 640 Cooled (Ninox) Camera

Document title

Instructions and Manual of Use

DOCUMENT VALIDATION

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DOCUMENT CHANGE RECORD

Issue	Date	Name	Pages/sections affected	Comment
1.0	09/01/15			First release

TABLE OF CONTENTS

1 SCOPE

This document details the design for the OWL 640 Cooled (Ninox) camera model NX1.7-VS-CL-640.

Details of the camera electrical interfaces and communication protocols are also provided.

A model of the complete camera module is shown below.

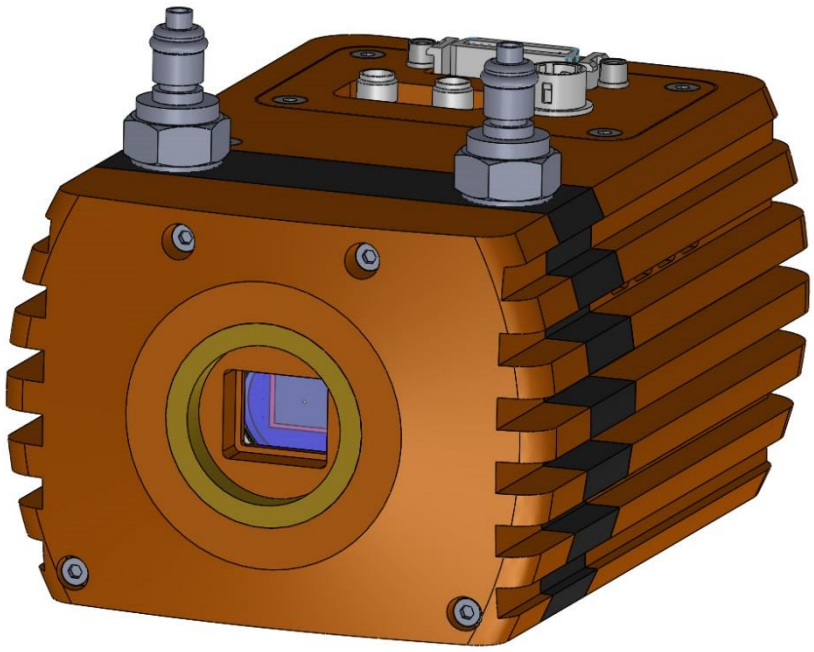
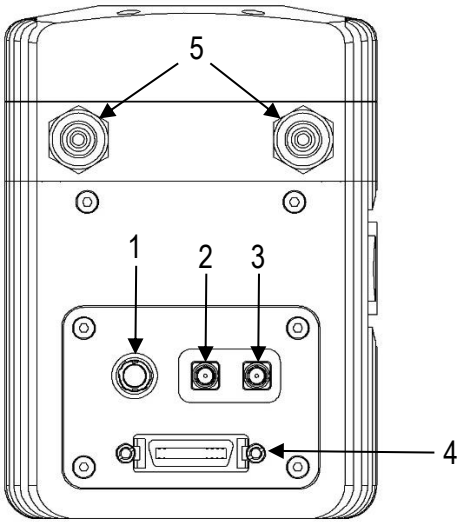


Figure 1: Complete Camera Module.

2 DESIGN OVERVIEW

2.1 Physical Interfaces

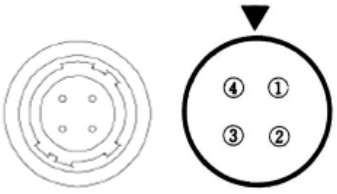


1. **4 Pin Hirose connector**
   Part #: HR10A-7R-4PB (73)
2. **SMA connector**: Trigger In.
   Single ended, termination impedance = 510 Ω, capacitive load = 200 pF, TTL compatible.
3. **SMA connector**: Trigger Out.
   Single ended, source impedance = 51 Ω, capable of sinking and sourcing 32mA and will have an output voltage of 3.3v i.e. TTL compatible.
4. **3M CameraLink connector**
   Part #: 10226-6212PC
5. **Liquid cooling inlet/outlet valved coupling:** CPC P/N MCD2404

Figure 2: Physical Interfaces.

2.1.1 4 pin Hirose

The camera has a 4-pin Hirose multi-connector for power input and signal integration.
The pin-out table is shown in Figure 3 (image seen from rear of camera). The associated male connector part # is: HR10-7P-4S (73).



Pin out	I/O	Signal name
1	IN	12V
2	IN	12V
3	IN	GND
4	IN	GND

Figure 3: Hirose Connector.

2.1.2 SMA Connectors

The camera has 2 SMA connectors on the rear panel. One is for trigger out to allow the user to trigger other equipment such as a laser and the other is a trigger in. The trigger is used when a laser, for example, is in control of the timings and wishes to trigger the camera.

2.1.3 Camera Link Connector

Camera link connector is compliant with the Camera Link® Version 2.0 standard Ref. http://www.visiononline.org/vision-standards-details.cfm?id=171&type=6.

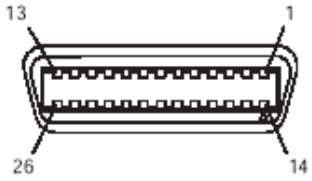


Figure 4: Camera Link Connector.

Medium and Full Configurations				Base Configuration (with Camera Control and Serial Communications)		
Camera Connector	Frame Grabber Connector	Channel Link Signal	Cable Name	Camera Connector	Frame Grabber Connector	Channel Link Signal
1	1	inner shield	Inner Shield	1	1	inner shield
14	14	inner shield	Inner Shield	14	14	inner shield
2	25	Y0-	PAIR1-	2	25	X0-
15	12	Y0+	PAIR1+	15	12	X0+
3	24	Y1-	PAIR2-	3	24	X1-
16	11	Y1+	PAIR2+	16	11	X1+
4	23	Y2-	PAIR3-	4	23	X2-
17	10	Y2+	PAIR3+	17	10	X2+
5	22	Yclk-	PAIR4-	5	22	Xclk-
18	9	Yclk+	PAIR4+	18	9	Xclk+
6	21	Y3-	PAIR5-	6	21	X3-
19	8	Y3+	PAIR5+	19	8	X3+
7	20	100 Ω	PAIR6+	7	20	SerTC+
20	7	terminated	PAIR6-	20	7	SerTC-
8	19	Z0-	PAIR7-	8	19	SerTFG-
21	6	Z0+	PAIR7+	21	6	SerTFG+
9	18	Z1-	PAIR8-	9	18	CC1-
22	5	Z1+	PAIR8+	22	5	CC1+
10	17	Z2-	PAIR9+	10	17	CC2+
23	4	Z2+	PAIR9-	23	4	CC2-
23	4	Z2+	PAIR9-	23	4	CC2-
11	16	Zclk-	PAIR10-	11	16	CC3-
24	3	Zclk+	PAIR10+	24	3	CC3+
12	15	Z3-	PAIR11+	12	15	CC4+
25	2	Z3+	PAIR11-	25	2	CC4-
13	13	inner shield	Inner Shield	13	13	inner shield
26	26	inner shield	Inner Shield	26	26	inner shield

Table 1: Camera Link Pin Description.

2.1.4 Liquid cooling quick release couplings

The camera electronics drive a ThermoElectric Cooler (TEC) to cool the sensor. The Hot side of the TEC is cooled via either circulating coolant or forced air. Connection to the coolant channel is made via two quick release, valved coupling bodies (Colder Products Co. P/N MCD2404). Please ensure compatibility with these connectors on the camera module before attempting to connect the coolant supply. ¼" Hose barb valved in-line coupling body P/N MCD 1704 is a typical choice.

2.2 Mechanical Profile

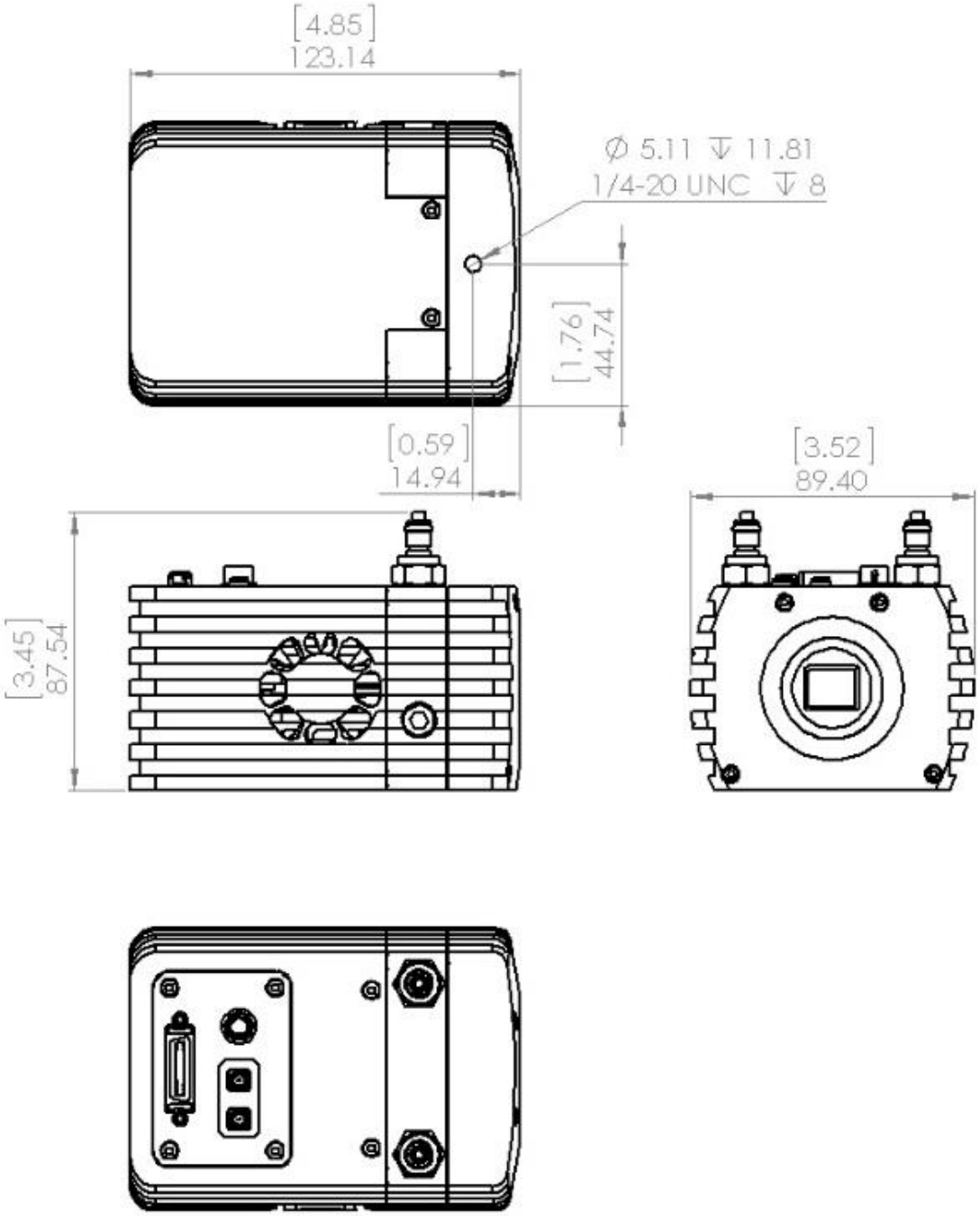


Figure 5: Owl Ninox 640 Mechanical Profile Drawing (SolidWorks Model).

3 DESIGN DETAILS

3.1 Electrical Design

3.1.1 Power Supplies and TEC

Unit input power specification is +12V +/- 0.5V with a maximum of 5 Watts power dissipation when the TEC is disabled. An additional 5W may be required if the full drive to the TEC is required. This will be dependent on environmental conditions and the TEC temperature set point. On power up, the peak power due to inrush current will be less than 12 Watts.

3.1.2 ROIC and Set Point Temperature Calibration

The temperature of the ROIC is determined from a platinum resistor on the ROIC. The resistor voltage varies linearly with temperature. This voltage is read via an Analogue to Digital (ADC) converter.

For calibration two ADC count values for the ROIC temperature are determined during acceptance testing for each camera i.e. at 0degC and at +40degC. These two points are stored in the cameras EPROM. A straight line graph can then be used to determine temperature for any given ADC count value.

Straight line eqn. Y = M*X+C, becomes
where the slope, M = (Y1-Y2)/(X1-X2) -- two known points from calibration
Constant offset, C = Y2 - M*(X2)

For any ADC value, ADC temp.(degC) = M*(ADC counts) + C

For example, using the calibration values from the example given in section 4.5.1
ADC cal. 0degC = 1226 counts, ADC cal. +40degC = 788 counts. See the graph Table 2 for more information.

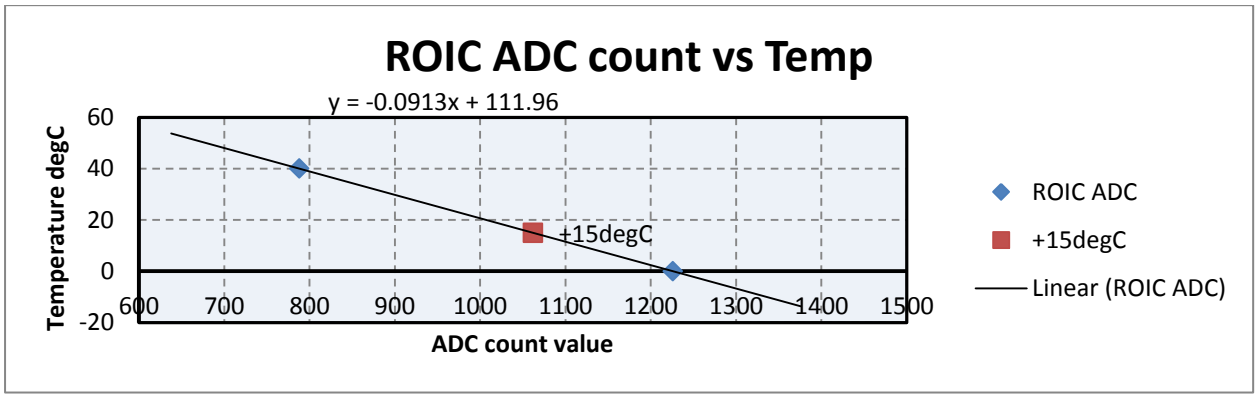


Table 2: ROIC ADC vs Temp.

In the above example a reading from the ADC of 1062 counts would equate to +15degC

Likewise a Digital to Analogue Converter (DAC) is used to produce a voltage for the set point of the TEC control loop. Two values are determined for 0degC and +40degC for each camera during acceptance testing and stored in the cameras EPROM.

The relationship of DAC counts to set point temperature is linear and therefore a straight line graph can be used to determine the set point temperature from the DAC count value.

3.1.3 Sensor Cooling

The default/power up set point for the TEC cooling is approximately +15 degC, however the NUC tables are calculated and stored into the camera based on a cooling set point of -15 degC. Therefore, for optimum performance it is essential that the user ensures the set point of -15degC is calculated from the DAC calibration values and is written into the camera as per section 3.1.2.

The TEC power is automatically adjusted to try and achieve the set point temperature, with a limit of approx. 5 Watt drive. A cooling set point of -15degC is achievable with either water cooling (+20degC water) or forced air (in an ambient of +25degC) options. The fan can be switched on or off via a serial command.

3.1.4 Digital Video Out

The camera produces mono, progressive scan, digital video output to Camera Link® standard. Raw 14 bit parallel video data is clocked at a continuous 80MHz clock. This clock and data along with FRAME VALID, LINE VALID, DATA VALID are embedded within the Camera Link® signals that are exposed on the cameras 26 pin Camera Link® connector.

The SWIR Sensor has 640 x 512 active pixels.

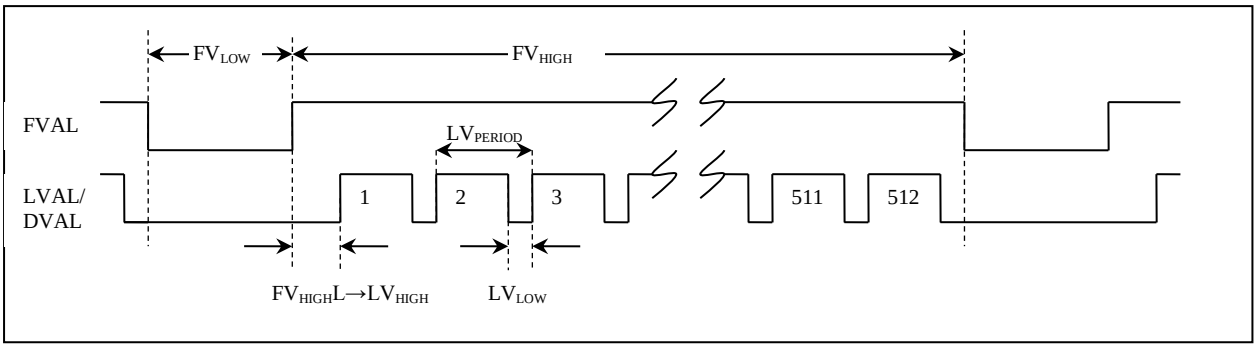


Figure 6: Digital Video Timing.

FV_{HIGH} = Frame Valid High
High Gain Mode = 4.479 msec = 358320 clks@80MHz
Low Gain Mode = 6.238 msec = 499040 clks@80MHz

FV_{LOW} = Frame Valid low
= Frame period - FV_{HIGH}
Frame period determined by either external trigger or by user setting, see Table 3 for more information.

LV_{PERIOD} **= Line Valid period**
≥ 643 clks@80MHz

LV_{LOW} **= Line Valid low**
≥ 3 clks@80MHz

FV_{HIGH}→LV_{HIGH} **= Rising edge of Frame valid to rising edge of line 1 Line Valid**
≥ 3 clks@80MHz

Video Latency = 2 line periods

Notes:
- The camera link signals LVAL and DVAL have identical timing

3.1.5 Internal Frame Synchronisation

When internal trigger is selected the frame rate is determined using a set of 4 8-bit internal registers that make up a 32 bit number. Each count in the 32bit register equates to a 1*40MHz clock period i.e. 25ns.

Example frame rates are given below:

Frame Rate (Hz)	Period (ms)	Count value
25	40.000	1,600,000
29.97	33.367	1,334,668
30	33.333	1,333,333
50	20.000	800,000
59.94	16.683	667334
60	16.667	666667

Table 3: Example Internal Trigger Frame Rate Values.

3.1.6 External Frame synchronisation

When external trigger is selected the camera may be triggered from an external source via the trigger in SMA as detailed in section 2.1. The external trigger may be configured as either rising (+ve) or falling (-ve) edge sensitive. See the definition of register 0xF2 in section 4.3 for more information.

A programmable delay may also be used to delay the start of the exposure of the camera.

The Trigger Out SMA provides a TTL compliant signal which follows the exposure time. The signal goes high to indicate when the exposure is active.

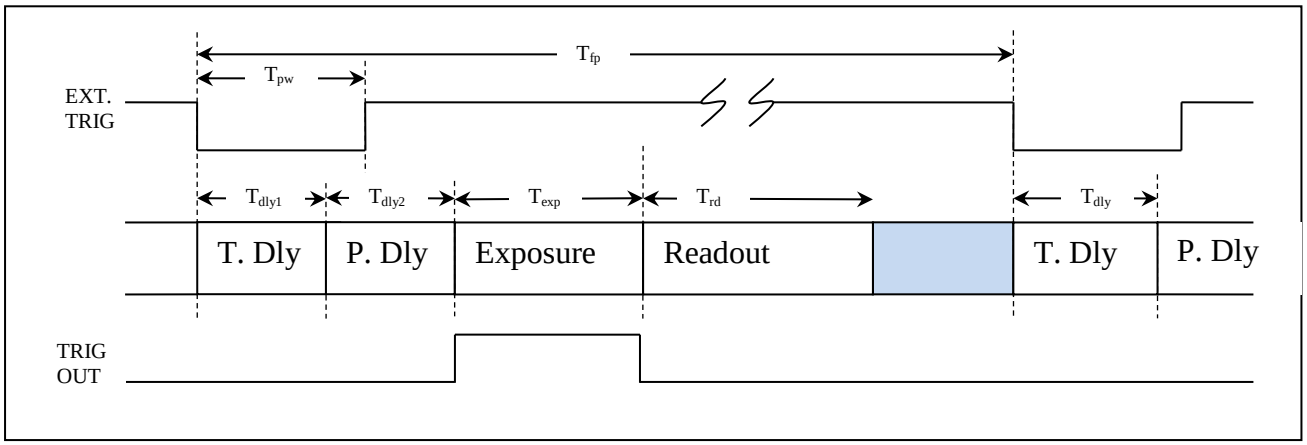


Figure 7: External Trigger timing.

T_{fp} = Frame period, set by external trigger or by internal registers (see Table 3).
T_{pw} = Trigger pulse width, min width > 50ns.
T_{dly1} = Fixed Delay from falling edge of trigger to start of exposure.
T_{dly2} = Programmable Delay from falling edge of trigger to start of exposure.
T_{rd} = Readout time for 1 progressive frame.
T_{exp} = Exposure time of sensor.
Notes;
- External trigger, triggers the start of a new exposure.
- Camera is set to external trigger –ve edge for the above times.
- T_{dly1} = 245ns +/-12.5ns Jitter for Low gain mode.
- T_{dly1} = 378us +/-12.5ns Jitter for High gain mode 1* (Register 0xF2 bit 4 = '0') (default).
- T_{dly1} = 245ns +/-12.5ns Jitter for High gain mode 2* (Register 0xF2 bit 4 = '1').
- T_{dly1} will be the time from the rising edge if selected.
- T_{dly2} may be increased from 0ns in steps of 25 ns by setting the trigger delay register.
- In Low gain mode the sensor will exhibit some sensitivity to light during the T_{dly1} and T_{dly2} phases. This is due to charge lag/charge clearing time constants when in Low gain mode. The responsivity during these phases is non-linear in nature.

*Other than the Tdly1 differences there are no other functional differences between High gain mode 1 and High gain mode 2.

3.1.7 Region Of Interest (ROI)

A Region Of Interest within the main active region of 640*512 may be defined. This region may be used to calculate Peak and Average settings for the Automatic Light control function of the camera.

The ROI offset and sizes are outlined below:

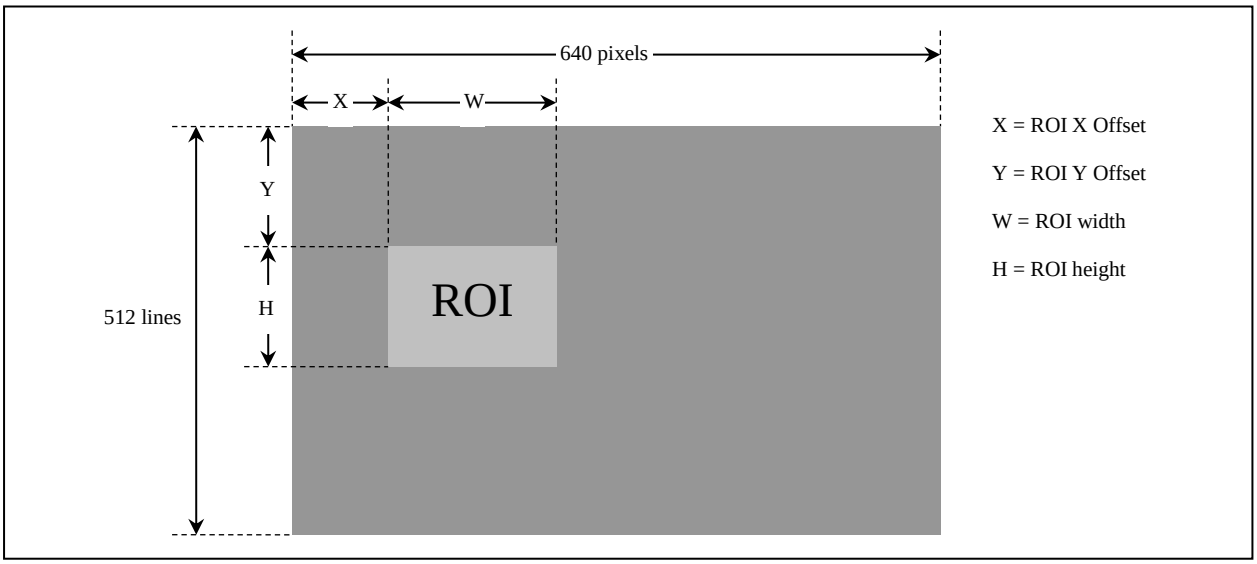


Figure 8: ROI size and offset.

8-bit values are used to store X, Y, W and H.

The 8-bit values sent to the camera for X, Y, W and H will be multiplied by 4 in the camera, to give the required number pixels for the offset/size for the ROI i.e. the ROI can be moved to within a resolution of 4 pixels in the X and Y, and the ROI size will have a resolution of 4 pixels

Note that the ROI may only be moved within a region 632*504 region, with a min offset of 4,4.
If (X+W)>632 then X will be internally limited to make sure (X+W) = 632
If (Y+H)>504 then Y will be internally limited to make sure (Y+H) = 504

ROI highlighting is also provided. When selected, the pixels within the ROI will have a gain of unity. Those pixels outside the ROI may either have 0.75 gain or x1 gain applied.

An optional ROI outline feature is also included that if enabled will draw a 1pixel wide box around the ROI.

3.1.8 Average Video Level Detection

An average video level is calculated for active ROI. This value will be calculated in real time, i.e. as pixel data in the ROI is captured from the sensor it is fed directly to an Accumulator. At the end of frame the Accumulator is divided to give a true average. This average can be read from internal registers in the camera.

3.1.9 Peak Video level detection

Peak video is determined from a rolling average of 4 pixels. Current pixel + 3 previous pixels are used to derive peak value. This peak value is monitored for the ROI and latched at the end of frame. The peak value may be read from internal registers in the camera.

3.1.10 Automatic Light Control (ALC)

Exposure of the Sensor may be automatically controlled by using the "Set FPGA CTRL reg." command and setting bit 1 = 1 (default = 1 ie ALC Enabled).

Both peak and average for the video levels are derived and monitored for the ROI. The active video level used to compare to the set point can be adjusted from full average to full peak or a percentage of both.

Exposure will automatically be adjusted until the set point is reached. If the Exposure reaches its maximum value the camera will automatically increase the Digital gain applied to the image until the set point is reached.

When ALC is enabled, exposure is limited to a minimum value of 100usec and a maximum value determined by the frame rate of the camera.

Digital Gain is limited to a min of 256counts = gain of 1 so that the full well on the sensor may saturate the 14bit digital output. Maximum digital gain count = 65535 = gain of 256.

3.1.11 Bad Pixel

Bad pixels will be determined from Non Uniform Correction (NUC) values that are calibrated stored for each pixel during acceptance testing. Bad pixels will be determined as those which have gain and offset values outside a given threshold.

During the calibration of the NUC values, any pixels identified as bad will have their gain and offset values set to zero.

Bad pixels may be highlighted during live video by selecting the appropriate NUC state. See section 4.3, Set NUC State for more details.

3.1.12 ROIC Gain Modes

The camera has two modes of operation, high gain mode and low gain mode (default). Either mode may be manually selected by sending the appropriate command.

High gain mode provides the best noise performance and can provide better images for low scene illumination e.g. night time imaging.

Low gain mode provides the best dynamic range and can provide better images for high scene illumination e.g. day time imaging.

ROIC gain characteristics are detailed below:

	High Gain	**Low Gain**
Min Exposure	100us	1us
Max Exposure	Frame period (ms) - 10ms	Frame period (ms) - 6ms
Noise	45 electrons (typical)	180 electrons (typical)
Well depth	12,000 electrons	650,000 electrons

Table 4: ROIC Gain Characteristics.

3.1.13 Maximum Exposure Times

The camera operates at the following frame rates with corresponding maximum integration times:

Frame Rate (Hz)	**Max Integration Time, High-Gain Mode**	**Max Integration Time, Low-Gain Mode**
25	30 ms	33 ms
29.97	23 ms	26 ms
30	23 ms	26 ms
50	10 ms	13 ms
59.94	6 ms	10 ms
60	6 ms	10 ms

Table 5: Maximum Integration Times.

Note: With the ALC disabled the maximum exposure time can be increased to ≈ 26.8secs.

3.1.14 Video Inversion

Output video may be digitally inverted such that dark areas in the image will appear bright.

Video may be inverted by using the "Set FPGA CTRL reg." command and setting bit 6 = 1. (Set = 0 by default)

3.1.15 Horizontal Mirror

Output video may be mirrored horizontally such that left side of the image becomes the right side.

Video may be horizontally mirrored by using the "Set FPGA CTRL reg." command and setting bit 7 = 1. (Set =1 by default)

3.1.16 Image Sharpening

Output video may be digitally processed to provide image sharpening.

Sharpening may be enabled by using the "Set Convolve reg." command and setting the register(FD) value = 0x43.

Setting the register(FD) value = 0x22 returns the video to normal image data.

3.1.17 Unit Serial Number

The unit serial number may be read from the camera's EPROM by using either the "Get Unit Serial Number" or by the "Get manufacturers Data".

Before accessing the EPROM, if not already enabled, communications to the EPROM should be enabled via the "Set system state" command.

4 SERIAL COMMUNICATION (LVDS INTERFACE USING CAMERALINK)

4.1 Overview

For version 2.3 (or greater) of the Micro firmware, the Power on default settings for camera serial port are;

- 115200 baud
- 1 start bit
- 8 data bits
- 1 stop bit

UART message format from Host to camera

Command	Data 1	Data 2	.....	Data n	ETX	Chk_Sum

The first Byte is the command to the Microcontroller in the camera, following bytes contain data required by the command, the ETX byte terminates the command. 0x50 is always used to terminate the command. An additional check sum byte may also be required to be sent by the host if check sum mode is enabled.

UART message format from camera to Host

Data 1	Data 2	.....	Data n	ETX	Chk_Sum

all or none of the above bytes may be sent in response to commands from the host depending on the commands sent by the host.

An optional mode of operation is included in the firmware for command acknowledge. Once enabled the camera will respond to all commands send by the host. After the camera has received and processed the command from the host, a single command acknowledge byte will be sent at the end of transmission (ETX). i.e. should the host command require data to be sent from the camera then the ETX byte will be sent at the end of the requested data.

Another optional mode of operation is included in the firmware is for check sum operation, this mode should only be used when the command acknowledge mode is enabled. Once the check sum mode is enabled the camera will only act upon commands that are received with the correct check sum byte sent at the end of the command packet. Note that if the check sum feature is not enabled check sum bytes may still be sent at the end of a command packet, the command will be processed and the check sum will be ignored. The check sum byte should be the result of the Exclusive OR of all bytes in the Host command packet including the ETX byte.

When check sum mode is enabled data returned from the camera will include an echo of the checksum from the host command

By default the camera will boot up with both command acknowledge and check sum operation disabled.

It is intended that the camera be operated from a higher level perspective whereby complete UART messages or groups of UART messages are used to achieve required camera functionality.

Bits in registers that have not been identified in the documentation should be ignored.

Once a command has been received by the camera all subsequent commands from the host will be ignored until the command has been processed.

It is recommend that both command acknowledge and check sum operation be enabled at power up.

4.2 ETX/ERROR codes

Error codes will be sent as ETX characters by the camera in response to commands that have failed.

0x50	ETX	Command acknowledge - command processed successfully.
0x51	ETX_SER_TIMEOUT	Partial command packet received, camera timed out waiting for end of packet. Command not processed
0x52	ETX_CK_SUM_ERR	Check sum transmitted by host did not match that calculated for the packet. Command not processed
0x53	ETX_I2C_ERR	An I2C command has been received from the Host but failed internally in the camera.
0x54	ETX_UNKNOWN_CMD	Data was detected on serial line, command not recognized
0x55	ETX_DONE_LOW	Host Command to access the camera EPROM successfully received by camera but not processed as EPROM is busy. I.e. FPGA trying to boot.

Table 6: ETX Error Codes.

4.3 Set Commands

Set Command	Serial Packet	Comments
Set system state	0x4F 0xYY 0x50	YY Bits 7,5,3,2 = Reserved set to 0 YY Bit 6 = 1 to enable check sum mode YY Bit 4 = 1 to enable command ack YY Bit 1 = 0 to Hold FPGA in RESET YY Bit 0 = 1 to enable comms to FPGA EPROM
Micro RESET	0x55 0x99 0x66 0x11 0x50 0xEB	Will trap Micro causing watchdog and reset of Microcontroller firmware
Set exposure	0x53 0xE0 0x02 0xEE 0xY1 0x50 0x53 0xE0 0x02 0xEF 0xY2 0x50 0x53 0xE0 0x02 0xF0 0xY3 0x50 0x53 0xE0 0x02 0xF1 0xY4 0x50	30 bit value, 4 separate commands, 1 count = 1*40MHz period = 25nsecs Y1 = xxMMMMMM of 4 byte word :: Y4 = LLLLLLLL of 4 byte word Exposure updated on LSB write Min Exposure = 500nsec = 20counts Max Exposure = (2^30)*25ns ≈ 26.8secs
Set digital video gain	0x53 0xE0 0x02 0xC6 0xMM 0x50 0x53 0xE0 0x02 0xC7 0xLL 0x50	16bit value = gain*256 MM bits 7..0 = gain bits 15..8 LL bits 7..0 = level bits 7..0 Data updated on write to LSBs
Set trig delay	0x53 0xE2 0x02 0xE9 0xY1 0x50 0x53 0xE2 0x02 0xEA 0xY2 0x50 0x53 0xE2 0x02 0xEB 0xY3 0x50 0x53 0xE2 0x02 0xEC 0xY4 0x50	30 bit value, 4 separate commands, 1 count = 1*40MHz period = 25nsecs Y1 = xxMMMMMM of 4 byte word :: Y4 = LLLLLLLL of 4 byte word Trig Delay updated on LSB write
Set frame rate (Internal trig)	0x53 0xE0 0x02 0xDD 0xY1 0x50 0x53 0xE0 0x02 0xDE 0xY2 0x50 0x53 0xE0 0x02 0xDF 0xY3 0x50 0x53 0xE0 0x02 0xE0 0xY4 0x50	32 bit value, 4 separate commands, 1 count = 1*40MHz period = 25nsecs Y1 = MSB of 4 byte word Y4 = LSB of 4 byte word; Frame rate updated on LSB write
Set FPGA CTRL reg.	0x53 0xE0 0x02 0x00 0xYY 0x50	YY Bit 7 = 1 to enable horiz flip (default = 1) YY Bit 6 = 1 to invert video (default = 0) YY Bit 2 = 1 to enable the fan (default = 0, note this only applies to the Owl 640 cooled variant) YY Bit 1 = 1 to enable auto exposure (default = 1) YY Bit 0 = 1 to enable TEC (default = 0)

Set TEC set point	0x53 0xE0 0x02 0xFB 0xMM 0x50 0x53 0xE0 0x02 0xFA 0xLL 0x50	12 bit DAC value, LSB = LL byte, Lower nibble of MM = MSBs Reg 0xFB, bits 3..0 = set point bits 11..8 Reg 0xFA, bits 7..0 = set point bits 7..0 12 bit value to be converted to temperature from DAC calibration values (see " Get manufacturers Data")
Set NUC state	0x53 0xE0 0x02 0xF9 0xYY 0x50	Bit7 Bit6 Bit5 Bit4 (of YY) 0 0 0 1 Ramp test pattern 0 0 0 0 offset corrected 0 0 1 0 offset+gain corrected 0 1 0 0 Normal 0 1 1 0 offset +gain + Dark 1 0 0 0 8bit offset /32 1 0 1 0 8bit Dark *2^19 1 1 0 0 8bit gain /128 1 0 0 1 Reserved map YY Bit 3,2,1 = Reserved set = 0. YY Bit 0 = 1 to enable Bad Pixel show in any mode YY default value = 0x60
Set Gain/Trigger mode	0x53 0xE0 0x02 0xF2 0xYY 0x50	YY Bit 7 = 0, Reserved (default = 0) YY Bit 6 = 1 to enable Ext trig (default = 0) YY Bit 5 = 0 for –ve edge trig (default = 0) YY Bit 4 = 1 to enable High Gain Trigger mode 2 (default = 0) YY Bit 3 = 0, Reserved (default = 0) YY Bit 2 = 0 for low gain, 1 for high gain(default = 0) YY Bit 1 = 0 for low gain, 1 for high gain(default = 0) YY Bit 0 = 0, Reserved (default = 0) Note that bits 2 and 1 should be set to the same value.
Set Auto level	0x53 0xE0 0x02 0x23 0xMM 0x50 0x53 0xE0 0x02 0x24 0xLL 0x50	14 bit value – max 0x3FFF = White MM bits 7..0 = level bits 13..6 LL bits 7..2 = level bits 5..0
Set PEAK/Average	0x53 0xE0 0x02 0x2D 0xYY 0x50	YY 8-bit value 0 = Full Peak 255 = Full Average

Set AGC speed	0x53 0xE0 0x02 0x2F 0xYY 0x50	YY Bits 7..4 = GAIN speed(Default=7) YY Bits 3..0 = EXP speed(Default=7)
Set ROI appearance	0x53 0xE0 0x02 0x31 0xYY 0x50	Pixels within ROI always gain = 1 Bit 7 Bit 6 0 0 gain=1 outside ROI (Default) 1 0 gain=0.75 outside ROI 0 1 gain=1 + ROI BOX
Set ROI X offset	0x53 0xE0 0x02 0x32 0xYY 0x50	YY 8-bit value = 1/4 of X pixel offset
Set ROI Y offset	0x53 0xE0 0x02 0x33 0xYY 0x50	YY 8-bit value = 1/4 of Y pixel offset
Set ROI X Size	0x53 0xE0 0x02 0x35 0xYY 0x50	YY 8-bit value = 1/4 of X pixel offset
Set ROI Y Size	0x53 0xE0 0x02 0x36 0xYY 0x50	YY 8-bit value = 1/4 of Y pixel offset
Set Convolve reg.	0x53 0xE0 0x02 0xFD 0xYY 0x50	YY = 0x43 to enable image sharpening YY = 0x22 to provide normal image data

Table 7: Set Commands.

4.4 Query Commands

Query Command	Send Serial Packet	Comments
Get system status	0x49 0x50	Single byte will be transmitted from camera when command received. YY Bits 7,5,3= Reserved YY Bit 6 = 1 if check sum mode enabled YY Bit 4 = 1 if command ack enabled YY Bit 2 = 1 if FPGA booted successfully YY Bit 1 = 0 if FPGA is held in RESET YY Bit 0 = 1 if comms is enabled to FPGA EPROM
Get exposure value (May also be read during Auto Exposure)	0x53 0xE0 0x01 0xEE 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xEF 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xF0 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xF1 0x50 0x53 0xE1 0x01 0x50	Set address EE Read address EE ,(MSB) 1 byte Set address EF Read address EF ,(MIDU) 1 byte Set address F0 Read address F0, (MIDL)1 byte Set address F1 Read address F1 (LSB) , 1 byte 30 bit value, 4 bytes, 1 count = 1*40MHz period = 25nsecs 2 Upper bits of 0xEE are don't care's. Min Exposure = 500nsec = 20counts
Get Digital Gain	0x53 0xE0 0x01 0xC6 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xC7 0x50 0x53 0xE1 0x01 0x50	2 bytes returned MM,LL 16bit value = gain*256 Reg. C6 bits 7..0 = gain bits 15..8 Reg. C7 bits 7..0 = level bits 7..0
Get trig delay	0x53 0xE0 0x01 0xE9 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xEA 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xEB 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xEC 0x50 0x53 0xE1 0x01 0x50	30 bit value, 4 separate Registers, 1 count = 1*40MHz period =25nsecs 0xE9 = MSB of 4 byte word :: 0xEC = LSB of 4 byte word; 2 Upper bits of 0xE9 are don't care's.
Get Gain/Trigger mode	0x53 0xE0 0x01 0xF2 0x50 0x53 0xE1 0x01 0x50	1 byte returned Bit 7 = 0, Reserved Bit 6 = 1 Ext trig enabled Bit 5 = 0 –ve edge trig, 1 = +ve Bit 4 = 0, Reserved Bit 3 = 0, Reserved Bit 2 = 0 for low gain, 1 for high gain Bit 1 = 0 for low gain, 1 for high gain Bit 0 = 0, Reserved
Get frame rate	0x53 0xE0 0x01 0xDD 0x50	32 bit value, 4 separate Registers,

(Internal trig)	0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xDE 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xDF 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xE0 0x50 0x53 0xE1 0x01 0x50	1 count = 1*5MHz period = 200nsecs DD = MSB of 4 byte word : : : E0 = LSB of 4 byte word;
Get FPGA Status	0x53 0xE0 0x01 0x00 0x50 0x53 0xE1 0x01 0x50	Set address 00 (MSB) Read address 00 (MSB), 1 byte Bit 7 = 1 if horiz flip is enabled (default = 1) Bit 6 = 1 if video is inverted (default = 0) Bit 2 = 1 if the fan is enabled (default = 0, note this only applies to the Owl 640 cooled variant) Bit 1 = 1 if auto exposure is enabled (default = 0) Bit 0 = 1 if the TEC is enabled (default = 0)
Get TEC Setpoint	0x53 0xE0 0x01 0xFB 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0xFA 0x50 0x53 0xE1 0x01 0x50	Read 12 bit EM word; 2 bytes returned MM,LL Reg 0xFB, bits 3..0 = set point bits 11..8 Reg 0xFA, bits 7..0 = set point bits 7..0 12 bit value to be converted to temperature from DAC calibration values (see " Get manufacturers Data")
Get NUC state	0x53 0xE0 0x01 0xF9 0x50 0x53 0xE1 0x01 0x50	1 byte returned Bit7 Bit6 Bit5 Bit4 0 0 0 1 Ramp test pattern 0 0 0 0 offset corrected 0 0 1 0 offset+gain corrected 0 1 0 0 Normal 0 1 1 0 offset +gain + Dark 1 0 0 0 8bit offset /32 1 0 1 0 8bit Dark *2^19 1 1 0 0 8bit gain /128 1 0 0 1 Reserved map Bit 3,2,1 = Reserved set = 0. Bit 0 = 1 if Bad Pixel show is enabled
Get Auto level (Set point)	0x53 0xE0 0x01 0x23 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x24 0x50 0x53 0xE1 0x01 0x50	2 bytes returned MM,LL 14 bit value – max 0x3FFF = White Reg 23, bits 7..0 = level bits 13..6 Reg 24, bits 7..2 = level bits 5..0
Get PEAK/Average	0x53 0xE0 0x01 0x2D 0x50	1 byte returned, 8-bit value

setting	0x53 0xE1 0x01 0x50	0 = Full Peak 255 = Full Average
Get AGC speed	0x53 0xE0 0x01 0x2F 0x50 0x53 0xE1 0x01 0x50	1 byte returned Bits 7..4 = GAIN speed(Default=7) Bits 3..0 = EXP speed(Default=7)
Get ROI appearance	0x53 0xE0 0x01 0x31 0x50 0x53 0xE1 0x01 0x50	1 byte returned Pixels within ROI always gain = 1 Bit 7 Bit 6 0 0 gain=1 outside ROI (Default) 1 0 gain=0.75 outside ROI 0 1 gain=1 + ROI BOX
Get ROI X offset	0x53 0xE0 0x01 0x32 0x50 0x53 0xE1 0x01 0x50	1 byte returned 8-bit value = 1/4 of X pixel offset
Get ROI Y offset	0x53 0xE0 0x01 0x33 0x50 0x53 0xE1 0x01 0x50	1 byte returned 8-bit value = 1/4 of Y pixel offset
Get ROI X Size	0x53 0xE0 0x01 0x35 0x50 0x53 0xE1 0x01 0x50	1 byte returned 8-bit value = 1/4 of X pixel offset
Get ROI Y Size	0x53 0xE0 0x01 0x36 0x50 0x53 0xE1 0x01 0x50	1 byte returned 8-bit value = 1/4 of Y pixel offset
Get Convolve reg.	0x53 0xE0 0x01 0xFD 0x50 0x53 0xE1 0x01 0x50	1 byte returned = 0x43 image sharpening enabled = 0x22 normal image data
Get Video Peak value	0x53 0xE0 0x01 0x5E 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x5F 0x50 0x53 0xE1 0x01 0x50	14 bit value, 2 bytes returned Set address 5E Add 5E, bits 5..0 = Pk. level bits 13..8 Set address 5F Read Add 5F = Pk level bits 7..0
Get Video Average value	0x53 0xE0 0x01 0x60 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x61 0x50 0x53 0xE1 0x01 0x50	14 bit value, 2 bytes returned Set address 60 Add 60, bits 5..0 = Avg. bits 13..8 Set address 61 Read Add 61 = Avg. bits 7..0
Get sensor PCB temperature	0x53 0xE0 0x01 0x70 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x71 0x50 0x53 0xE1 0x01 0x50	12 bit signed number returned in 2 bytes Reg 70, bits 3..0 = temp bits 11..8 Reg 71, bits 7..0 = temp bits 7..0 Temp bits 11..4 is a signed number that represents the temperature in deg C. Temp bits 3..0 is a signed number that represents the fractional part of the temp in deg C. i.e. 1/16th of a degC e.g. 0x7FF = 127.9375 degC 0x7FE = 127.8750 degC :

		0x000 = 0 degC : 0x801 = - 127.9375 degC 0x800 = -128.0000 degC
Get Sensor Temp temperature	0x53 0xE0 0x01 0x6E 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x6F 0x50 0x53 0xE1 0x01 0x50	12 bit number returned in 2 bytes Reg 6E, bits 3..0 = temp bits 11..8 Reg 6F, bits 7..0 = temp bits 7..0 12 bit value to be converted to temperature from ADC calibration values (see " Get manufacturers Data")
Get Micro version	0x56 0x50	Two bytes transmitted from camera when command received. 1st byte Major version 2nd byte Minor version.
Get FPGA version	0x53 0xE0 0x01 0x7E 0x50 0x53 0xE1 0x01 0x50 0x53 0xE0 0x01 0x7F 0x50 0x53 0xE1 0x01 0x50	Set address 7E (Major Version Byte) Read address 7E, 1 byte Set address 7F (Minor Version Byte) Read address 7F, 1 byte
Get Unit Serial Number	0x53 0xAE 0x05 0x01 0x00 0x00 0x02 0x00 0x50 0x53 0xAF 0x02 0x50	2 bytes returned 1st byte is the LSB 2nd is the MSB
Get manufacturers Data	0x53 0xAE 0x05 0x01 0x00 0x00 0x02 0x00 0x50 0x53 0xAF 0x12 0x50	Get 18 bytes from cameras EPROM. For 2 byte values 1st byte returned is the LSB. Starting at address 0x000002 2 bytes Serial number 3 bytes Build Date (DD/MM/YY) 5 bytes Build code (5 ASCII chars) 2 bytes ADC cal 0degC point 2 bytes ADC cal+4 0degC point 2 bytes DAC cal 0degC point 2 bytes DAC cal+4 0degC point

Table 8: Query Commands.

NOTES:

- Command 0x4F writes to the system status register, 0x49 reads from the system status register.

4.5 Serial Command Examples with ACK + Check Sum

NOTE: Assume that Command Ack and Check sum mode are enabled unless otherwise stated

4.5.1 Example Power-up/Initialisation Sequence

Command	TX bytes (to camera)	RX'd bytes (From camera)
Power up camera	----------	----------
Get system status Poll this command until the Rx byte, Bit 2 = 1 to indicate that the FPGA has booted successfully	0x49 0x50 0x19 Note that the check sum byte has been added here but is not required at power up as the camera has not yet been set to check sum mode	0x06 (status = 0x06) At this stage only the status byte is returned. Above byte bit 2 = 1 indicates FPGA booted. A value of 0x02 would indicate not booted
Set System status (=0x53) Enable cmd ack mode Enable check sum mode Enable comms to EPROM	0x4F 0x53 0x50 0x4C	0x50 0x4C (ack + chk_sum)
Get Micro version	0x56 0x50 0x06	0x02 0x05 0x50 0x06 (V2.5)
Get FPGA version 4 separate commands sent with check sum. After each cmd wait for response before sending next	0x53 0xE0 0x01 0x7E 0x50 0x9C	0x50 0x9C
	0x53 0xE1 0x01 0x50 0xE3	0x01 0x50 0xE3 (1st byte = 1)
	0x53 0xE0 0x01 0x7F 0x50 0x9D	0x50 0x9D
	0x53 0xE1 0x01 0x50 0xE3	0x18 0x50 0xE3 (2nd byte = 24) Version = 1.24
Get manufacturers Data 2 separate commands sent with check sum. After each cmd wait for response before sending next	0x53 0xAE 0x05 0x01 0x00 0x00 0x02 0x00 0x50 0xAB	0x50 0xAB
	0x53 0xAF 0x12 0x50 0xBE	0x12 0x27 0x11 0x0A 0x0C 0x4C 0x61 0x72 0x6E 0x65 0xCA 0x04 0x14 0x03 0x8E 0x06 0xE4 0x09 0x50 0xBE Serial no. = 10002 Build date = 17/10/12 Build code = Larne ADC cal 0degC = 1226 ADC cal+40degC = 788 DAC cal 0degC = 1678

		DAC cal+40degC = 2532
Set System status (=0x52) This command is optional. And is included here to help prevent access to the EPROM for corrupt data. For additional EPROM accesses status should be set to 0x53	0x4F 0x52 0x50 0x4D	0x50 0x4D (ack + chk_sum)
Additional commands may now be sent to set camera for the required functionality e.g TEC on, AGC on High gain mode … etc.		

Table 9: Example Power-up/Initialisation Commands.

4.5.2 Set System Status (Enable Command Ack and Check sum mode)

From power up

Command	TX bytes (to camera)	RX'd bytes (From camera)
Set System status (=0x56)	0x4F 0x52 0x50 0x4D	0x50 0x4D (ack + chk_sum)

YY Bit 7= 0 - reserved
YY Bit 6= 1 to enable check sum mode
YY Bit 5= 0 to enable external comms
YY Bit 4 = 1 to enable command ack
YY Bit 3 = 0 - reserved
YY Bit 2 = 0 - reserved (FPGA DONE in read mode)
YY Bit 1 = 1 FPGA NOT in RESET
YY Bit 0 = 0 to disable comms to FPGA EPROM

4.5.3 Get System Status

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get system status	0x49 0x50 0x19	0x56 0x50 0x19 (status = 0x56)

4.5.4 Get Micro Version

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get Micro version	0x56 0x50 0x06	0x02 0x05 0x50 0x06 (V2.5)

4.5.5 Get FPGA Version

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get FPGA version	0x53 0xE0 0x01 0x7E 0x50 0x9C	0x50 0x9C
	0x53 0xE1 0x01 0x50 0xE3	0x01 0x50 0xE3
	0x53 0xE0 0x01 0x7F 0x50 0x9D	0x50 0x9D
	0x53 0xE1 0x01 0x50 0xE3	0x18 0x50 0xE3 (v1.24)

4.5.6 Reset Camera

Command	TX bytes (to camera)	RX'd bytes (From camera)
Micro Reset	0x55 0x99 0x66 0x11 0x50 0xEB	None
Set system State to Hold FPGA in RST -- Poll camera with this command every 500msecs until Rx bytes received	0x4F 0x51 0x50 0x4E	(0x50 0x4E) received when Micro has re-booted successfully
Set system State to boot the FPGA	0x4F 0x52 0x50 0x4D	0x50 0x4D
Get system status -- Poll the camera with this command every 500ms until bit 2 of the received status indicates that the FPGA has booted ok.	0x49 0x50 0x19	(0x52 0x50 0x19) -- FPGA not booted (0x56 0x50 0x19) -- FPGA booted ok.

4.5.7 Read Sensor PCB Temperature

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get PCB temperature	0x53 0xE0 0x02 0x70 0x00 0x50 0x91	0x50 0x91
	0x53 0xE1 0x01 0x50 0xE3	0x01 0x50 0xE3
	0x53 0xE0 0x02 0x71 0x00 0x50 0x90	0x50 0x90
	0x53 0xE1 0x01 0x50 0xE3	0x93 0x50 0xE3 (25.18degC)

4.5.8 Set Camera to External Trigger (-ve edge) and High Gain mode

Command	TX bytes (to camera)	RX'd bytes (From camera)
Set Gain/Trigger mode	0x53 0xE0 0x02 0xF2 0x46 0x50 0x55	0x50 0x55

4.6 Serial Command Error Examples

NOTE: Assume that Command Ack and Check sum mode are enabled unless otherwise stated

4.6.1 Missing or Wrong Checksum

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get system status	0x49 0x50	0x52 0x19

Camera has received a partial command but not received the correct check sum and therefore responds with an error code of 0x52 + sends the check sum byte that it had been expecting. The command is ignored.

4.6.2 Partial Host Command With Missing Data/ETX/Checksum

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get system status	0x49	0x51 0x19

Camera has received a partial command but not received expected data or the ETX character. Camera responds with error code 0x51 + sends the check sum byte that it had been expecting. The command is ignored.

4.6.3 Corrupt/Unknown Host Command

Command	TX bytes (to camera)	RX'd bytes (From camera)
Get system status	0x48 0x50 0x19	0x54 0x48

1st byte is corrupt and the camera has received an unknown command. Camera responds with error code 0x54 + sends the check sum byte that it had been expecting. The command is ignored.

APPENDIX A - **FPGA FIRMWARE UPLOAD**

CAMERA EPROM

The cameraEPROM is divided into15 sectors with address spaces as outlined below. Note that each address points to a 16bit word.

/* Sector Structure...

Sector	Kwords	words	start	end	start	end
1	4	4096	0	4095	000000	000FFF
2	4	4096	4096	8191	001000	001FFF
3	4	4096	8192	12287	002000	002FFF
4	4	4096	12288	16383	003000	003FFF
5	4	4096	16384	20479	004000	004FFF
6	4	4096	20480	24575	005000	005FFF
7	4	4096	24576	28671	006000	006FFF
8	4	4096	28672	32767	007000	007FFF
9	32	32768	32768	65535	008000	00FFFF
10	32	32768	65536	98303	010000	017FFF
11	32	32768	98304	131071	018000	01FFFF
12	32	32768	131072	163839	020000	027FFF
13	32	32768	163840	196607	028000	02FFFF
14	32	32768	196608	229375	030000	037FFF
15	32	32768	229376	262143	038000	03FFFF

SECTOR 1 - is used for Manufacture specific data i.e. serial number etc.

SECTORS 2-15 are used to hold the FPGA configuration information.

To program a new FPGA configuration
1. Sectors 2-15 must be erased
2. a new bit file must be uploaded to Sectors 2-15

Note that SECTOR 1 must not be ERASED as this contains detailed data about the camera.

SECTOR ERASE

The following command is used to erase a sector.

SECTOR xx ERASE - 0x53 0xAE 0x05 0x04 0xAA 0xBB 0xCC 0x00 0x50

Where the Hex Number AABBCC represents an address in the sector to be erased. After the SECTOR erase command has been issued a small delay is required for the ERASE to take place. Successful erase can be determined by polling the sector with the following command.

0x53 0xAF 0x01 0x50

If a value of 0xFF is returned the sector erase is complete.

Example Sector ERASEs

SECTOR 2 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x10 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 3 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x20 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 4 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x30 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 5 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x40 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 6 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x50 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 7 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x60 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 8 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x70 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 9 ERASE - 0x53 0xAE 0x05 0x04 0x00 0x80 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 10 ERASE - 0x53 0xAE 0x05 0x04 0x01 0x00 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 11 ERASE - 0x53 0xAE 0x05 0x04 0x01 0x80 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 12 ERASE - 0x53 0xAE 0x05 0x04 0x02 0x00 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 13 ERASE - 0x53 0xAE 0x05 0x04 0x02 0x80 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 14 ERASE - 0x53 0xAE 0x05 0x04 0x03 0x00 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)
SECTOR 15 ERASE - 0x53 0xAE 0x05 0x04 0x03 0x80 0x00 0x00 0x50
0x53 0xAF 0x01 0x50 (Continue to poll until 0xFF received)

SECTOR PROGRAMMING

Bursts of 32 DATA bytes (sixteen 16bit words) should be sent to the EPROM using a single command, the EPROM will auto increment the addresses.

Burst write command
0x53 0xAE 0x25 0x02 0xAA 0xBB 0xCC 0xN1 0xN2 0xN3 .....0xN32 0x00 0x50

The address of the burst write is given by AABBCC, 32 DATA bytes as read from bit file are sent N1-N32
Address AABBCC should start at the base address of sector 2 i.e. 0x001000 and increment by 16 for every burst command until the end of file.

At the end of file the last burst may not require 32bytes due to the file size, if this is the case the last 32 should be padded out to 32. Data in padding ignored.

Notes :
- It is recommended to operate the camera with Command Ack. Waiting for a command Ack will ensure burst writes have taken place before moving to the next burst write.
- The bit stream contains a check sum that is used by the FPGA during power up. If data is corrupted during upload the FPGA will not boot.
- Verification that FPGA has successfully booted can be done by reading the FPGA version number.

Example command list

Command	**TX bytes (to camera)**	**RX'd bytes (from camera)**	**Comments**
Enable Command Acknowledge + Enable EROM comms + Hold FPGA in reset	0x4F 0x11 0x50	0x50	
Erase EEPROM sector 2	0x53 0xAE 0x05 0x04 0x00 0x10 0x00 0x00 0x50	0x50	
Confirm Sector 2 erase (by reading LSByte)	0x53 0xAF 0x01 0x50	0xFF 0x50	Poll until 0xFF is returned
Erase EEPROM sectors 3-15 and confirm erase after each sector.	As above with relevant sector address	As above	Poll after each sector is erased until 0xFF is returned
Burst write 32 bytes of bit file	0x53 0xAE 0x25 0x02 0x00 0x10 0x00 0xN1 0xN2 0xN3 .....0xN32 0x00 0x50	0x50	1st burst starting at Sector 2 address.
Multiple burst writes of 32 bytes of bit file	0x53 0xAE 0x25 0x02 0xAA 0xBB 0xCC 0xN1 0xN2 0xN3 .....0xN32 0x00 0x50	0x50	Address 0xAABBCC starts at sector 2 base address and needs to be incremented by 16 for each successive burst until end of file.
Set System State	0x4F 0x12 0x50	0x50	FPGA will now boot with new firmware, need to delay approx. 500msec
Get FPGA version	0x53 0xE0 0x01 0x7E 0x50	0x50	Version 2.1
	0x53 0xE1 0x01 0x50	0x02 0x50	
	0x53 0xE0 0x01 0x7F 0x50	0x50	
	0x53 0xE1 0x01 0x50	0x01 0x50	