Effect of Scaling of Interconnections on the Time Delay of VLSI Circuits

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Abstract—**Effect of scaling of dimensions, i.e., increase in chip size and decrease in minimum feature size, on the *RC* time delay associated with interconnections in VLSIC's has been investigated. Analytical expressions have been developed to relate this time delay to various elements of technology, i.e., interconnection material, minimum feature size, chip area, length of the interconnect, etc. Empirical expressions to predict the trends of the technological elements as a function of chronological time have been developed. Calculations of time delay for interconnections made of poly-Si, WSi_2, W, and Al have been done and they indicate that as the chip area is increased and other device-related dimensions are decreased the interconnection time delay becomes significant compared to the device time delay and in extreme cases dominates the chip performance.**

I. Introduction

With the advances in technology, the integrated-circuit (IC) chip size, complexity, and device packing density is continuously increasing. New developments in lithographic and etching techniques have resulted in reduction in the minimum feature size used in the IC's. At the same time, improvements in materials technology have allowed integration of more and more devices on the same chip, resulting in increased area. According to theory of scaling [1], the smaller dimensions of an MOS transistor should enhance its speed. As a first-order approximation, therefore, this should proportionally increase the circuit speed. Indeed, for smaller circuits it does happen. However, for larger circuits, the time delays associated with the interconnections can play a significant role in determining the performance of the circuit. As the minimum feature size is made smaller, the area of cross section of the interconnection also reduces. At the same time, a higher integration level allows the chip area to increase, causing the length of the interconnections to increase. The net effect of this "*scaling of interconnections*" is reflected into an appreciable *RC* time delay. For a very large chip with extremely small geometries, the time delay associated with interconnections could become an appreciable portion of the total time delay, and hence the circuit performance could no longer be decided by the device performance.

The time delay associated with the interconnections is dependent upon two factors; the resistance of the interconnections, and the capacitance controlled by the dielectric media. Generally, silicon dioxide is used as the dielectric. The success of silicon in microelectronics can be largely attributed to excellent properties of Si/SiO_2 interface and ease of thermal oxidation of silicon to produce a passivating layer of SiO_2. Therefore, as far as the dielectric material is concerned, our choice is somewhat limited to SiO_2. Fortunately for interconnections, a variety of materials have been used which can be broadly classified into three categories; metals, polycrystalline silicon (polysilicon), and metal silicides. A big variation of resistivity is available in this case, e.g., the resistivities of heavily doped polysilicon and aluminum are 5×10^{-4} and 2.25×10^{-6} $\Omega \cdot$ cm, respectively. Obviously, the proper choice of the material within the constraints placed by the fabrication technology can result in minimization of the *RC* delay time. The materials which have been used or proposed to form interconnections can be broadly classified into four categories, heavily doped polysilicon, low-temperature metals, high-temperature refractory metals, and metal silicides. Here, we will consider N^+ polysilicon, Al, W, and WSi_2 as the representatives of each group.

In this work, the effect of increase in chip area and decrease in the minimum feature size on the performance of the circuit has been investigated. A theory of *scaling of interconnections* has been developed. From the information available in the literature, empirical equations have been developed to predict the various elements of the technology, i.e., minimum feature size, maximum chip area, maximum interconnection length, etc., at a given point in time. Time delays associated with interconnections made of different materials have been calculated. Utilizing the theory of scaling of interconnections and scaling of MOS transistors [1] the time delay associated with interconnections and devices have been compared.

II. Modeling of Distributed *RC* Time Delay

The time delay associated with the interconnection is dependent upon two parameters; the resistance and the capacitance associated with the interconnections. Fig. 1 shows a schematic diagram of closely packed interconnections in an IC. The resistance of an interconnection line of length L, width W, thickness H, and resistivity ρ is given by

$$R = \rho \frac{L}{WH}. \tag{1}$$

Assuming a parallel-plate capacitance model, the capacitance between the interconnection and the silicon substrate is given by

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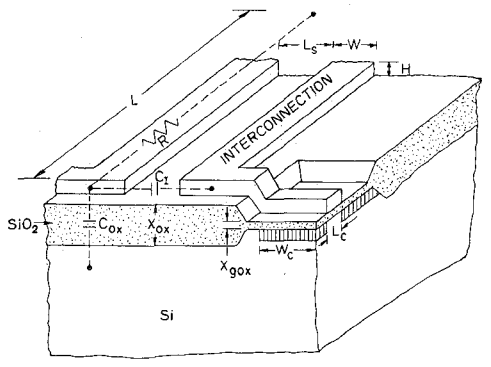

Fig. 1. Cross section of MOS transistors and parasitics associated with the interconnections.

$$C_{ox} = K_{ox}\,\epsilon_0\,\frac{WL}{X_{ox}} \tag{2}$$

where X_{ox} and K_{ox} are the SiO_2 thickness and dielectric constant, respectively, and ϵ_0 is the permittivity of free space. The capacitance between the two adjacent interconnections separated by a distance of L_s is

$$C_I = K_{ox}\,\epsilon_0\,\frac{HL}{L_s} \tag{3}$$

where it has been assumed that the dielectric between them is SiO_2. The total line capacitance is given by

$$C = C_{ox} + C_I$$

$$= K_{ox}\,\epsilon_0 L\left\{\frac{W}{X_{ox}} + \frac{H}{L_s}\right\}. \tag{4}$$

In the calculation of C_{ox} and C_I, a simple model of parallel-plate capacitance has been assumed and the effect of fringing field and finite electrode thickness [2], [3] has been ignored to maintain simplicity. By doing elaborate numerical analysis, it is possible to take these factors into account, however, the analytical nature of the calculations to follow will be lost. Dang and Shigyo have shown [2] that the above assumption is more erroneous only for small ratio of W to X_{ox}. For W/X_{ox} higher than 3, the error caused by this simple model is within a factor of two. In general, the line capacitance could be approximated by the relationship [2]

$$C = K_1(C_{ox} + C_I) \tag{5}$$

where K_1 is the factor which takes into account the fringing fields and its value can be calculated using the two-dimensional analysis of Dang and Shigyo [2].

An interconnection should be treated as a distributed-parameter transmission line in order to calculate the accurate value of time delay. Fig. 2 shows a lumped value form of the RC distributed line which can be used to derive approximate pulse-response time [4], [5]. The transient response to a step input to the distributed RC network of Fig. 2 has been shown by Kaufman and Garrett [4] to be

$$V_0(t) = 1 - \frac{4}{n}\sum_{n=0}^{\infty}\frac{(-1)^n}{2n+1}\exp\left[-\left(\frac{2n+1}{2}n\right)^2\frac{t}{RC}\right]. \tag{6}$$

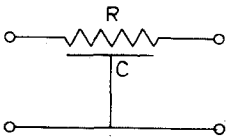

Fig. 2. Schematic of a distributed RC network representing an interconnection.

TABLE I
MOS DEVICE SCALING FOR A CONSTANT FIELD

Device/Circuit Parameter	Scaling Factor* (S)
Device dimensions L_c, W_c, X_{gox}	1/S
Doping concentration	S
Voltage	1/S
Field	1
Current	1/S
Gate Delay	1/S
Power dissipation/device	$1/S^2$
Power density	1
Speed power product/device	$1/S^3$

*Scaling factor S > 1.

The time it takes the output to reach from 10 to 90 percent of its final value, defined as rise time τ, is 0.89 RC according to (6). Compared to that, rise time of a corresponding one-lump RC circuit is 2.2 RC. Similar analysis of distributed RC line has been done by Wilnai [5] with identical results. Therefore, in the analysis to follow, $\tau_L = 0.89\ RC$ will be used as a figure of merit of the interconnection line. From (1) and (5) we obtain

$$\tau_L = 0.89\,K_1 K_{ox}\,\epsilon_0\,\rho\,\frac{L^2}{WH}\left(\frac{W}{X_{ox}} + \frac{H}{L_s}\right). \tag{7}$$

It is obvious that the figure of merit or rise time τ_L is heavily dependent upon various dimensions involved in a chip, i.e., L, W, H, X_{ox}, and L_s. Therefore, in order to obtain more information about τ_L, first we have to relate the above dimensions to various elements of the VLSI technology. In the next section, a theory of "*scaling of interconnections*" will be developed analogous to the theory of MOS device scaling [1], where various dimensions involved with devices and interconnections will be related to various elements of the technology and the time frame.

III. Scaling of Device and Interconnection Lines

The area occupied by an MOS transistor can be made smaller by shortening its channel width and length leading to a faster device. Substrate doping plus the junction built-in potential determine the minimum depletion-region thickness of an operable device which, in turn, establishes the minimum device size. Based on the above observations, the linear transformation (device scaling) in Table I has been suggested [1]. According

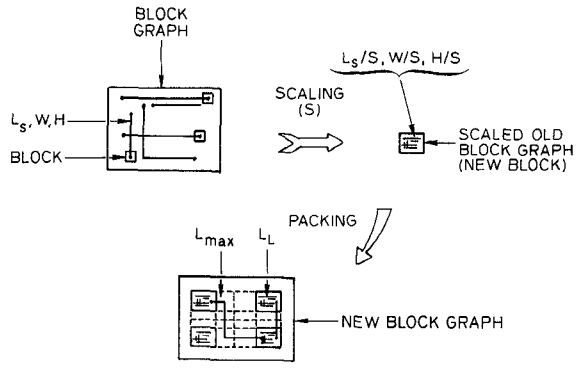

Fig. 3. Integration of scaled circuits.

to Table I, as the average feature size drops by a scaling factor of $1/S$, device performance is enhanced; as gate delay is reduced by a factor of $1/S$, and power dissipation/device by a factor of $1/S^2$, more devices can be packed on a chip.

Smaller dimensions, larger chip size, and circuit innovations all contribute to the progress of integration and the generation of a larger number of components on a single chip. Increasing these components raises the number of connections required for signal transmission. To clarify the problem of interconnections, the following terms are defined [6]:

A "block graph" is a structure consisting of interconnected blocks; a logic design is an example.

A "block" is an undefined primitive. In a logic design, for example, it can be a NOR circuit, a storage element, register, or an IC chip.

In the following discussion, only planar transistors with a silicon substrate and silicon-dioxide dielectric are considered, and the interconnections are assumed to be in a single plane isolated by a silicon-dioxide layer. It is assumed that a specific block graph can be scaled down and miniaturized so that it can be packed with the others on the same chip, thereby generating a super-block graph containing the old scaled-down block graphs as illustrated in Fig. 3. The interconnections within a block are defined as local interconnections and between blocks are termed as long-distance interconnections.

The concept of scaling the local interconnection lines can be understood by examining Figs. 1, 3, and Table II. It can be seen in Table II that, after scaling, the line response time remains constant and the line voltage drop stays the same; however, current density increases which can introduce severe device-performance problems, such as electromigration. A comparison between Tables I and II reveals that the total delay time of a scaled block graph is a function of gate delay only because the scaling rule dictates the gate-delay reduction (by a factor of $1/S$) with a constant line response time. Because of the short lines in a scaled block graph, gate delay is typically one order of magnitude higher than the local line response. The effect of long-distance interconnection lines on total delay time for the transmission of signals from block to block is discussed in the following sections.

The communication between blocks in a super-block graph is accomplished via long-distance interconnections. In the design of a complex system with a large number of functions on a chip, optimization of length of the interconnections is of major importance. The average wire length can be estimated

TABLE II
SCALING OF LOCAL INTERCONNECTION LINES FOR CONSTANT RESPONSE TIME AND CONSTANT FIELD

Interconnection Parameter	Scaling Factor* (S)
Interconnection dimensions L_L, H, W, L_s, X_{ox}	1/S
Line resistance $R = \rho L_L/WH$	S
Line capacitance $C_{ox} = K_{ox}\,\varepsilon_o\,L_s W/X_F$	1/S
Interelectrode capacitance $C_I' = K_{ox}\,\varepsilon_o\,L\,H/L_s$	1/S
Line response time 0.89 RC	1
Line voltage drop IR	1
Line current density	S

*Scaling factor S > 1.

by a very useful statistical formula [7]

$$L_{max} = KA^g \tag{8}$$

where

L_{max} maximum wire length
A chip area
K, g constants.

A good rule of thumb is $K = g = 1/2$ [7]. With these values, the average length of the long-distance interconnections is given by

$$L_{max} = \frac{\sqrt{\text{chip area}}}{2}. \tag{9}$$

Assuming that chip area will increase with the continuing development of IC processing, the effect of scaling of transistors and local interconnections on the scaling of long-distance interconnection lines can be determined. The results are summarized in Table III where it is assumed that the maximum long-distance or block-to-block interconnection line increases by a factor of $S_c > 1$. It can be concluded, therefore, that the long-distance line voltage drop will increase with scaling. Because the long-distance line response time rises drastically as a result of scaling, a substantial amount of delay and energy is dissipated during communication across the interconnection lines, and therefore, the performance of the circuits can suffer from technological advancement.

IV. Estimation of Average Interconnection Length

The systematic approach taken to anticipate the problems that will arise in future VLSI can be optimized by introducing realistic data. Fig. 4 is an extrapolation of the basic capabilities of semiconductor technology as measured by chip size and minimum dimension resulting from the lithographic process. The data for this plot were obtained by many investigators of bipolar and MOS technologies. The prediction of a 0.5-μm feature size and 200-mm^2 chip size by the late 1980's appears to be reasonable. Applying (9) and the data in Fig. 4, the

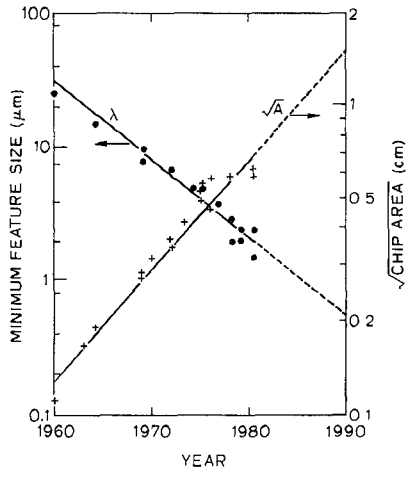

Fig. 4. Variation of minimum feature size and chip size versus year of fabrication for the state-of-the-art chip fabricated that year.

TABLE III
SCALING OF LONG-DISTANCE INTERCONNECTION LINES FOR CONSTANT LOCAL RESPONSE TIME AND CONSTANT FIELD

Interconnection Parameter	Scaling Factor* (S)
Long-distance interconnection dimensions H, W, L_S, X_F	1/S
Long-distance interconnection dimension L_{max}†	S_c
Line resistance $R = \rho L_{max}/WH$	$S^2 S_c$
Line capacitance $C_{ox} = K_{ox}\ \epsilon_o\ L_{max}\ W/X_{ox}$	S_c
Interelectrode capacitance $C_I = K_{ox}\ \epsilon_o\ L_{max}\ H/L_S$	S_c
Line response time 0.89 RC	$S^2 S_c^2$
Line voltage drop IR	SS_c
Line current density	S

*$S, S_c > 1$.

†$L_{max} = \frac{\sqrt{\text{chip area}}}{2} \rightarrow$ scaling factor S_c.

maximum average long-distance wire length is estimated to be one-half the size of the chip edge. An exponential fitting to these data reveals the following relationships:

$$\lambda = 10^{-5} \exp\,[-0.135\,(t - 1900)] \tag{10}$$

where λ is the minimum feature size (μm), t = year (1968, 1975, 1990), and, for long-distance interconnection length (block to block)

$$L_{\max} = \frac{\sqrt{A}}{2} = 2.5 \times 10^{-5} \exp\,[0.089\,(t - 1900)] \quad \text{cm}. \tag{11}$$

V. Estimation of Average Delay Time for Signal Transmission

In this section, the long-distance interconnection line delay has been addressed as an unavoidable limit on a system performance. A model for interconnection delay time was developed in Section III. Equation (7) relates the delay time to various technological elements. We will further develop this equation in this section.

According to the theory of scaling [1], vertical as well as horizontal dimensions should be scaled down to reduce the device size and thus improve the device performance. Therefore, most of the device dimensions are controlled by the minimum feature size λ, allowed by the technology. For a large chip, the major fraction of the area is occupied by the interconnections and not by the device [7]. Therefore, to minimize the chip area, the width and spacing between the interconnections should be kept at the minimum feature size, i.e.,

$$L_s = W = \lambda. \tag{12}$$

We can also assume that the thickness of the oxide and the interconnection scale with the minimum feature size. A good assumption is

$$X_{ox} = 0.35\,\lambda$$
$$H = 0.25\,\lambda. \tag{13}$$

For the relationships predicted by (12) and (13), the value of K_1 from the model of Dang and Shigyo [2] is approximately 2. By combining (7), (9), (12), and (13), a simple relationship is obtained to calculate τ_L

$$\tau_L = 5.53\,\epsilon_0 K_{ox} \rho \frac{A}{\lambda^2}. \tag{14}$$

The above equation relates τ_L to some key technological parameters. The product $K_{ox}\rho$ is a purely physical measure determined by the electrode material and the property of its surrounding ambient (SiO_2); on the other hand, A/λ^2 is a measure of the technology and number of components on the chip (bits of memory, logic gates). Because the objective for improving IC fabrication technology is to pack more components on a single chip, the target is to increase the value of A/λ^2; however, $K_{ox}\rho$ must be reduced to minimize τ_L. This can be achieved by lowering electrode resistivity by the selection of low-resistance materials as the interconnection electrode.

By substituting the values of λ and A from (10) and (11), respectively, in (14), τ_L can be predicted as a function of time

$$\tau_L = 1.3 \times 10^8\ \epsilon_0 K_{ox} \rho \exp\,[0.448\,(t - 1900)]. \tag{15}$$

The above equation predicts the interconnection delay time as a function of time for the largest chip fabricated that year using the state-of-the-art technology as predicted by Fig. 4. The estimated values of τ_L as a function of time are plotted in Fig. 5 for polysilicon, tungsten silicide, tungsten, and aluminum with thin-film resistivities of 500, 30, 10, and 3 $\mu\Omega \cdot$ cm, respectively. Also plotted are the values of gate delay obtained from the literature.[1] It is evident that as time is progressing, the delay is decreasing, however, the interconnection delay is increasing. Depending upon the interconnection materials, at certain times the speed of the state-of-the-art chip will be

[1]The data shown here were collected from various publications, conference proceedings, and product announcements by various manufacturers. The gate delay does not scale here by the scaling factor S mainly because not all of the scaling rules were followed in manufacturing these IC's.

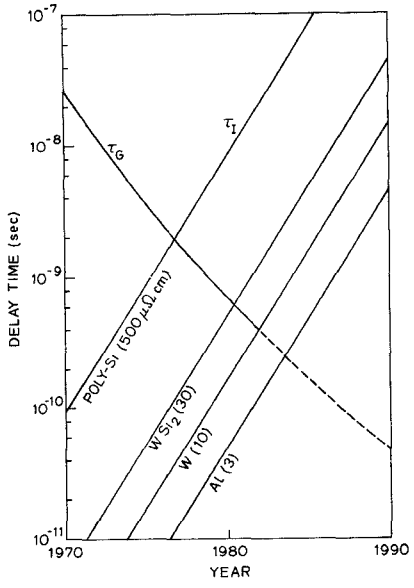

Fig. 5. Interconnection time delay and average gate delay versus year of fabrication for the state-of-the-art chip fabricated that year.

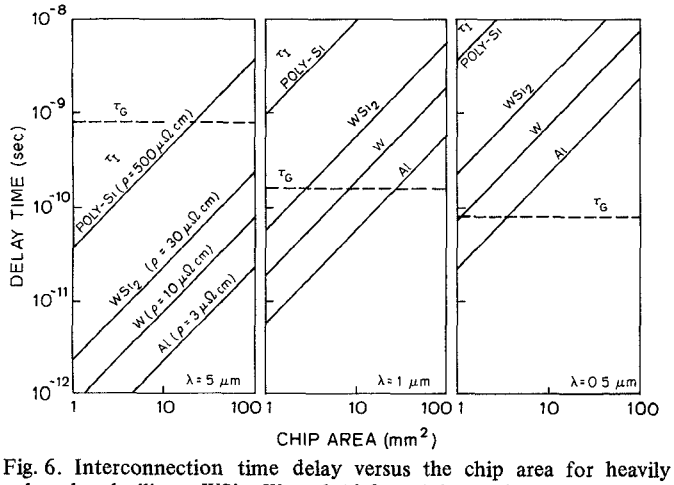

Fig. 6. Interconnection time delay versus the chip area for heavily doped polysilicon, WSi_2, W, and Al for minimum feature sizes of 5, 1, and 0.5 μm.

limited by the interconnections and not by the devices. This is a serious implication and could become a major factor in the evolution of integrated electronics.

The preceding analysis was done only for the state-of-the-art chip with biggest area and smallest feature size, to show the technological trends. In general, one would like to know the values of τ_g and τ_L for all values of λ and A, because most of the chips manufactured at a certain time do not necessarily follow the state-of-the-art technology. Using (14), τ_L has been calculated as a function of A and λ and the results are plotted in Fig. 6. It is seen that τ_L increases as A is increased and λ is decreased, which are trends for future technology. Also shown are values of τ_g which are dependent only upon λ and not upon A. Ideal scaling rules [1] have been assumed to estimate these values of τ_g. It is seen clearly that for 5-μm technology, except for very-large-area chips, the performance is mainly device controlled. For 1-μm technology, the higher resistivity materials combined with large chip area make the performance interconnection controlled. For the lower resistivity material like W and Al, the chip performance is still controlled by the

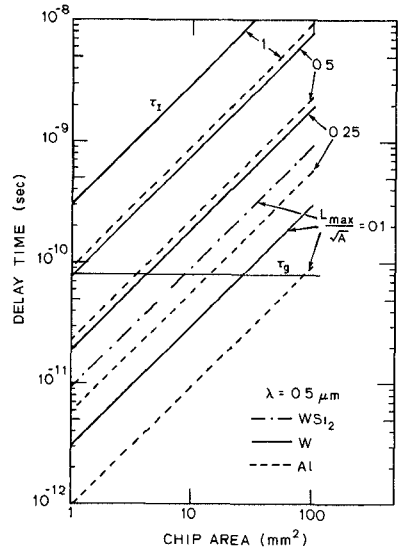

Fig. 7. Interconnection time delays versus chip area for $L_{max} = \sqrt{A}$ = 1.0, 0.5, 0.25, and 0.1.

devices. For 0.5-μm technology, the chip performance is largely controlled by the interconnections.

In the analysis leading to Figs. 5 and 6 it was assumed that $L_{max} = 0.5\sqrt{A}$. This might not always be correct. In many circuits, L_{max} might be either larger or smaller than $0.5\sqrt{A}$. Fig. 7 shows the effect of this variation. It is evident that for the same chip area substantial reduction in τ_L can be obtained by keeping the length of interconnections smaller.

VI. Materials for Multilayer Interconnections

It has been demonstrated in this work that, as device dimensions are becoming increasingly smaller, severe requirements are being imposed on the electrode material. The basic demand is conductivity because it can substantially improve the resistances and delay times of the electrical interconnection lines used for VLSI structures. In general, several other requirements are imposed on interconnection materials by the fabrication technology. In a multilayer interconnection structure, the layers incorporated early in the process sequence might be subjected to several fabrication steps, yet other layers incorporated much later might not be subjected to that many steps. The most rigorous set of requirements can be summarized as

low resistivity,
ability to withstand the chemicals and high temperatures required in the fabrication process,
ability to be thermally oxidized,
stability of contacts to other layers,
good MOS properties,
resistance to electromigration,
capability to be defined into fine patterns.

Not all of the requirements will be applicable to all of the layers, however, the selection of a material becomes easier if it meets more requirements.

Historically, metals like aluminum and gold have been used in bipolar and MOS IC's. With the advent of silicon-gate MOS technology, polysilicon has been extensively used to form gate electrodes and interconnections. Refractory metals such as tungsten (W), molybdenum (Mo), titanium (Ti), and tantalum

(Ta) and their silicides are receiving increased attention as a replacement/compliment of polysilicon. Table IV gives a comparison of the properties of polysilicon, metals, and silicides. Polysilicon meets all of the requirements addressed above, however, its high resistivity is beginning to limit the performance of the larger area circuits. Its use is, therefore, limited to the interconnections in those parts of the circuit where *RC* delay times are not critical and where cleanliness and other good properties of polysilicon are badly needed; for example, to form gate electrodes in MOS transistors and the local interconnections of relatively small length. Aluminum does not meet all of the requirements. Because of its poor high-temperature capabilities, it can be incorporated in the process only after all of the high-temperature steps have been finished. Very fine lines of Al are questionable because of its poor electromigration properties [8]. Since the oxides of W and Mo are volatile at high temperatures, these metals can be used only when all of the steps where exposure to high-temperature oxidizing ambient might occur are over but high-temperature steps in inert ambient are still remaining. Silicides of W, Mo, and Ta have reasonably good compatibility with the IC fabrication technology [9]-[12]. They have fairly high conductivity; they can withstand all of the chemicals normally encountered during the fabrication process. Therefore, they can be used in all of the applications where polysilicon has been used so far. $TiSi_2$ is also very attractive for this application, except its etch rate in hydrofluoric acid (HF) is very large. If the use of HF can be avoided during the fabrication by employing dry-etching techniques, $TiSi_2$ can also be used successfully [13]. A combination of silicides and polysilicon (usually known as polycide) can also be used in such situations [11]. Since the conductivity of such a sandwich layer is dominated by the silicide, in this study we have not tried to differentiate between polycides and silicides.

One factor which has not been discussed in this work is the use of a dielectric material with lower dielectric constant than SiO_2. This will result in lower capacitance as predicted by (4). Not much work has been done in this area, however, this could become an important area of future research.

VII. Conclusion

From the results presented here it is evident that *RC* time delay associated with interconnections can be a significant portion of the total circuit time delay, especially for VLSIC. If the device dimensions are scaled down following the laws of ideal scaling [1] and the circuit size and complexity keeps growing as it has been in the past, this problem becomes even more serious, as is evident from Figs. 4 and 5. If the design rules are not altered drastically, e.g., the length of the interconnections bears the relationship governed by (9), the overall performance of the future VLSI circuits will be totally controlled by the properties of interconnection material, as shown in Figs. 5 and 6. Eventually for very large circuits, even Al may not prove to be a low-resistivity material. By changing the design rules, e.g., by making the length of the interconnection smaller, the circuit performance could be significantly improved as shown in Fig. 7. A combination of several materials will have to be used to optimize the circuit performance. The selection of the materials will be dictated by the requirements of the circuits and conditions imposed by fabrication technology.

TABLE IV
Properties of Interconnection Materials

Materials	Bulk Resistivity ($\mu\Omega$ cm)	Thin-Film Resistivity ($\mu\Omega$ cm)	Melting Point (°C)	Chemical Compatibility	Thermal Oxidation
Poly-Si	250	500	1410	YES	YES
Al	2.26	3	660	?	NO
W	5.5	10	3410	?	NO
Mo	5.0	10	2610	?	NO
WSi_2	12.5	30	2165	YES	YES
$MoSi_2$	21.6	40	2050	YES	YES
$TaSi_2$	8.5	35	2170	YES	YES
$TiSi_2$	13	15	1540	?*	YES

* $TiSi_2$ is etched severely in HF

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